TEXAS INSTRUMENTS

Data Transmission Circuits

Line Circuits

Data Book

Volume 1

1995/1996

Mixed-Signal Products

Data Transmission Circuits Data Book

Volume 1

Line Circuits

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INTRODUCTION

In the 1995/1996 ***Data Transmission Circuits Data Book, Volume 1***, the Mixed-Signal Products Division of Texas Instruments (TI) presents technical information on various products for electronic media and electronic devices.

The TI data transmission circuits represent technologies from classic bipolar through Advanced Low-Power Schottky (ALS), IMPACT™, LinBiCMOS™, CMOS, and BiMOS processes. The ALS and IMPACT oxide-isolated technologies provide the data transmission family with improved speed-power characteristics. LinBiCMOS technology has the best features of CMOS and bipolar processes of fast switching speeds, low quiescent power, high voltage breakdowns, voltage or current precision, and stability.

This data book provides information on the following types of products:

- Data line drivers
- Data line receivers
- Data line transceivers

The data transmission line drivers, receivers, and transceivers, which support many popular data transmission standards, can connect electronic devices and systems at high data rates over significant cable lengths.

Among new products offered by TI in the 1995/1996 *Data Transmission Circuits Data Book, Volume 1* are LinBiCMOS circuits for the standard footprints of EIA RS-485, including military temperature range offerings; differential drivers and receivers that operate from a 3-V supply; new circuits for EIA/TIA-423-B; a single-ended Small Computer System Interface (SCSI) transceiver with integrated termination; and low-cost EIA/TIA-232-E driver and receiver combinations.

The data book is organized for quick location of a specific data sheet. The sequence is in base part number order (i.e., SN75ALS176 is located next to the SN75176B). The alphanumeric index provides a quick method of locating the data sheet for a known part number and indicates new products in this edition. A preview of new products that are near release to production are included for the first time in this data book.

The selection guide is grouped by industry standard and includes key features and the standard device footprint of the products in each category. The cross-reference guide lists other manufacturers devices with the suggested TI replacement. Applications, ordering, and package mechanical information are the last sections of the data book.

While this data book offers design and specification data only for data transmission products, complete technical data for any TI semiconductor product is available from your nearest TI Field Sales Office, local authorized TI distributor, or by writing directly to:

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or telephone the TI Literature Response number: 1-800-477-8924.

We sincerely believe the new 1995/1996 *Data Transmission Circuits Data Book, Volume 1* will be a valuable addition to your collection of technical literature.

1 General Information

Devices in **bold type** are new to this data book.

ALPHANUMERIC INDEX

Devices in **bold type** are new to this data book.

EIA RS-485

DRIVERS/RECEIVERS PER PACKAGE	DRIVER/RECEIVER t_{pd} (ns)	I_{CC} (mA)	FOOTPRINT	DEVICE TYPE	PAGE NUMBER
0/4	27	27	AM26LS32	SN75ALS173	2–473
	35	70		SN55173	2–465
				SN65173	2–465
				SN75173	2–465
	30	11		SN55LBC173	2–479
				SN65LBC173	2–487
				SN75LBC173	2–487
	27	27	MC3486	SN75ALS175	2–535
	35	70		SN65175	2–525
				SN75175	2–525
	30	11		SN55LBC175	2–541
				SN65LBC175	2–549
				SN75LBC175	2–549
1/1	25/45	5.4	SN75176	SN55LBC176	2–605
				SN65LBC176	2–605
				SN75LBC176	2–605
	13/19	30		SN65ALS176	2–591
				SN75ALS176	2–591
	11.5/18			SN75ALS176A	2–591
	10/16.5			SN75ALS176B	2–591
	22/37	50		TL3695	2–1011
	60/35			SN75176A	2–557
	22/35	55		SN65176B	2–567
				SN75176B	2–567
		70		SN95176B	2–579
	22/40		SN75179	SN75179B	2–615
	18/30	4.2		SN65LBC179	2–623
				SN75LBC179	2–623
	13/19	55	SN75ALS180	SN65ALS180	2–633
				SN75ALS180	2–633
	18/30	4	SN75ALS180	SN65LBC180	2–645
				SN75LBC180	2–645
2/2	22/37	50	MC34050	SN75ALS1177	2–959
	35/35	110		SN751177	2–949
	22/37	50	MC34051	SN75ALS1178	2–959
	35/35	110		SN751178	2–949
3/3	13/19	90	SN75ALS170	SN75ALS170	2–405
			SN75ALS171	SN75ALS171	2–419
	22/37	72		SN75ALS1711	2–977

EIA RS-485 (continued)

DRIVERS/RECEIVERS PER PACKAGE	DRIVER/RECEIVER t_{pd} (ns)	I_{CC} (mA)	FOOTPRINT	DEVICE TYPE	PAGE NUMBER
4/0	22	55	AM26LS31	SN65ALS172A	2–443
				SN75ALS172A	2–443
	65	60		SN75172	2–435
	20	7	AM26LS31	SN55LBC172	2–449
				SN65LBC172	2–457
				SN75LBC172	2–457
	22	55	MC3487	SN75ALS174A	2–503
	65	60		SN75174	2–495
	20	7		SN55LBC174	2–509
				SN65LBC174	2–517
				SN75LBC174	2–517
9/9	19.6/33	45	SN75LBC976	SN75LBC976	2–897
	10/10	60		SN75976A	2–875
	26.4/30.7	45	SN75LBC978	SN75LBC978	2–919

EIA RS-422-A, CCITT v.11

DRIVERS/RECEIVERS PER PACKAGE	DRIVER/RECEIVER t_{pd} (ns)	I_{CC} (mA)	FOOTPRINT	DEVICE TYPE	PAGE NUMBER
0/2	25	50	SN75157	SN75157	2–321
	300		uA9637	SN75146	2–279
	25			uA9637A	2–1039
	85	50	uA9639	uA9639	2–1049
0/4	30	14	AM26LS32	AM26C32	2–35
				AM26LS32A	2–41
	27	27		SN75ALS173	2–473
	22	35		SN75ALS193	2–757
				SN75ALS197	2–801
	35	70		AM26LS32A	2–41
				AM26LS33A	2–41
				SN55173	2–465
				SN65173	2–465
				SN75173	2–465
	27	27	MC3486	SN75ALS175	2–535
	22	35		SN55ALS195	2–779
				SN75ALS195	2–779
				SN75ALS199	2–823
	35	70		SN65175	2–525
				SN75175	2–525
		70		MC3486	2–69
1/1	13/19	30	SN75176	SN65ALS176	2–591
				SN75ALS176	2–591
	11.5/18			SN75ALS176A	2–591
	10/16.5			SN75ALS176B	2–591
	60/35	50		SN75176A	2–557
	22/37	50		TL3695	2–1011
	22/35	55		SN65176B	2–567
				SN75176B	2–567
		70		SN95176B	2–579
	22/40		SN75179	SN75179B	2–615
	13/19	30	SN75ALS180	SN65ALS180	2–633
				SN75ALS180	2–633
2/0	25	50	SN75158	SN75158	2–327
		65	SN75159	SN75159	2–335
	7	40	uA9638	SN75ALS191	2–743
	15	65		uA9638	2–1045

EIA RS-422-A, CCITT v.11 (continued)

DRIVERS/RECEIVERS PER PACKAGE	DRIVER/RECEIVER t_{pd} (ns)	I_{CC} (mA)	FOOTPRINT	DEVICE TYPE	PAGE NUMBER
2/2	12/27	9	MC34050	SN65C1167	2-941
				SN75C1167	2-941
	22/37	50		SN75ALS1177	2-959
	35/35	110		SN751177	2-949
	12/27	9	MC34051	SN65C1168	2-941
				SN75C1168	2-941
	22/37	50		SN75ALS1178	2-959
	35/35	110		SN751178	2-949
3/3	13/19	90	SN75ALS170	SN75ALS170	2-405
	22/37	72	SN75ALS171	SN75ALS1711	2-977
	13/19	90		SN75ALS171	2-419
4/0	12	3	AM26LS31	AM26C31	2-11
	14	45		SN55ALS192	2-747
				SN75ALS192	2-747
	22	55		SN65ALS172A	2-443
				SN75ALS172A	2-443
	65	60		SN75172	2-435
	20	80		AM26LS31	2-19
	14	45	MC3487	SN55ALS194	2-769
				SN75ALS194	2-769
	22	55		SN65ALS174A	2-503
				SN75ALS174A	2-503
	65	60		SN75174	2-495
	20	80		MC3487	2-75
	30		SN75151	SN75151	2-291

EIA/TIA-423-B, CCITT V.10†

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4/4	SN75LBC784	SN75LBC784	2-849
4/4	SN75LBC876	SN75LBC786	2-855
2/0	uA9636A	uA9636A	2-1033

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EIA/TIA-232, CCITT V.28

DRIVERS/RECEIVERS PER PACKAGE	SUPPLY VOLTAGE(S)	FOOTPRINT	DEVICE TYPE	PAGE NUMBER
0/4	5 V	MC1489	MC1489	2–725
			SN55189	2–725
			SN75189	2–725
			MC1489A	2–725
			SN55189A	2–725
			SN75189A	2–725
			SN65C189	2–733
			SN75C189	2–733
			SN65C189A	2–733
			SN75C189A	2–733
	5 V or 12 V	SN75154	SN75154	2–303
1/1	±5 V	SN75155	SN75155	2–311
2/0	±12 V	SN75150	SN75150	2–285
		uA9636	uA9636A	2–1033
2/2	5 V	MAX232	MAX232	2–63
3/3	±5 V	MC145406	SN65C1406	2–969
			SN75C1406	2–969
	±12 V, 5 V		TL145406	2–1023
			SN75185	2–675
3/5	±5 V	SN75C185	SN65C185	2–685
	±5 V	SN75C185	SN75C185	2–685
	5 V	SN75LBC187	SN75LBC187	2–703
	3 V	SN75LV4735	SN75LV4735	2–991
	3 V or 5 V	SN75LV4737A	SN75LV4737A	2–1001
4/0	±9 V	MC1488	MC1488	2–709
4/0	±9 V	MC1488	SN55188	2–709
			SN75188	2–709
	±5 V		SN65C188	2–717
			SN75C188	2–717
		LT1030	LT1030C	2–57
		SN75C198	SN65C198	2–813
			SN75C198	2–813
4/4	±12 V, 5 V	SN75186	SN75186	2–693
	±5 V	SN75C1154	SN65C1154	2–933
			SN75C1154	2–933
4/5	5 V	MAX241	SN75LBC241	2–843

miscellaneous standards

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	17/10	SN75LBC088	SN75LBC088	2–145
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		DS3897	SN55ALS057	2–89
			SN75ALS057	2–89
	8/8	DS3896	SN55ALS056	2–89
			SN75ALS056	2–89
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		SN75161	SN55ALS161	2–383
			SN75161B	2–369
			SN75ALS161	2–383
		SN75162	SN75162B	2–369
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	0/8	SN75128	SN75128	2–247
		SN75129	SN75129	2–247
	2/0	N8T23	SN75123	2–231
			N8T23	2–231
	3/3	SN751730	SN751730	2–985
	4/0	MC3481	SN75126	2–241
		MC3485	SN75130	2–253

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general purpose

DRIVERS/RECEIVERS PER PACKAGE	TYPE OF LINE CIRCUIT	DRVR (R_L)/ RVR (V_{th})	FOOTPRINT	DEVICE TYPE	PAGE NUMBER
0/2	Differential, $-15 < V_{ICM} < 15$ V	1000 mV	DS8820	DS8820A	2–657
				SN55182	2–657
	Differential, $-3 < V_{ICM} < 3$ V	10 mV	SN75107	SN75207	2–835
	Differential, $-15 < V_{ICM} < 15$ V	1000 mV	DS8820	SN75182	2–657
0/2	Differential, $-3 < V_{ICM} < 3$ V	10 mV	SN75107	SN75207B	2–835
	Differential, $-6 < V_{ICM} < 6$ V	25 mV		SN55107A	2–159
				SN55107B	2–159
				SN75107A	2–159
				SN75107B	2–159
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				SN55108A	2–159
				SN55108B	2–159
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	Differential, $-15 < V_{ICM} < 15$ V	1000 mV	SN75115	SN55115	2–207
				SN75115	2–207
	Single Ended	Adjustable	SN75140	SN75140	2–271
			SN75141	SN75141	2–271
0/4	Differential, $-15 < V_{ICM} < 15$ V	0.5 V	AM26LS32	AM26LS33A	2–41
1/1	Differential, $-15 < V_{ICM} < 15$ V	100 Ω/1000 mV	SN75116	SN55116	2–217
				SN75116	2–217
	Differential, $0 < V_{ICM} < 6$ V		SN75117	SN75117	2–217
	Differential, $-15 < V_{ICM} < 15$ V		SN75118	SN75118	2–217
	Differential, $0 < V_{ICM} < 6$ V		SN75119	SN75119	2–217
2/0	Differential, Voltage Mode	100 Ω	DS8830	DS8830	2–667
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				SN75183	2–667
2/0	Differential, Current Mode	NA	SN75109	SN55109A	2–177
				SN75109A	2–177
			SN75110	SN55110A	2–177
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				SN75114	2–199
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			AM26S11	AM26S11C	2–3
	Single Ended, Open Collector	50 Ω	SN75138	SN55138	2–259
				SN75138	2–259

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Manufacturers are arranged in alphabetical order.

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ADM232L1	MAX232I	2–63
ADM241L	SN75LBC241	2–843
ADM485	SN75LBC176	2–605

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LT1081	MAX232C	2–63
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MOTOROLA	SUGGESTED TI REPLACEMENT	PAGE NO.
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MC1489A	SN75189A	2–725
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MC14C89A	SN75C189A	2–733
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MC34051	SN751178	2–949
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MC3485	SN75130	2–253
MC3486	MC3486	2–69
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MC75107	SN75107A	2–159
MC75108	SN75108A	2–159
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NATIONAL SEMICONDUCTOR	SUGGESTED TI REPLACEMENT	PAGE NO.
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NATIONAL SEMICONDUCTOR	SUGGESTED TI REPLACEMENT	PAGE NO.
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DS55110A	SN55110A	2–177
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DS55173	SN55173	2–465
DS75107	SN75107A	2–159
DS75107A	SN75107B	2–159
DS75108	SN75108A	2–159
DS75108A	SN75108B	2–159
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DS75113	SN75113	2–187
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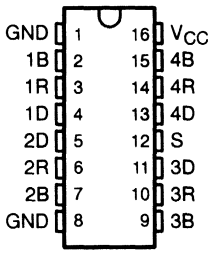
2 Line Circuits

SLLS116B – JANUARY 1977 – REVISED MAY 1995

- **Schottky Circuitry for High Speed, Typical Propagation Delay Time . . . 12 ns**
- **Drivers Feature Open-Collector Outputs for Party-Line (Data Bus) Operation**
- **Driver Outputs Can Sink 100 mA at 0.8 V Maximum**
- **PNP Inputs for Minimal Input Loading**
- **Designed to Be Interchangeable With Advanced Micro Devices AM26S10 and AM26S11**

D OR N PACKAGE
(TOP VIEW)



THE AM26S11 IS NOT RECOMMENDED FOR NEW DESIGNS

description

The AM26S10C and AM26S11C are quadruple bus transceivers utilizing Schottky-diode-clamped transistors for high speed. The drivers feature open-collector outputs capable of sinking 100 mA at 0.8 V maximum. The driver and strobe inputs use pnp transistors to reduce the input loading.

The driver of the AM26S10C is inverting; the driver of the AM26S11C is noninverting. Each device has two ground connections for improved ground current-handling capability. For proper operation, the ground pins should be tied together.

The AM26S10C and AM26S11C are characterized for operation over the temperature range of 0°C to 70°C.

Function Tables

AM26S10C
(transmitting)

INPUTS		OUTPUTS	
S	D	B	R
L	H	L	H
L	L	H	L

AM26S11C
(transmitting)

INPUTS		OUTPUTS	
S	D	B	R
L	H	H	L
L	L	L	H

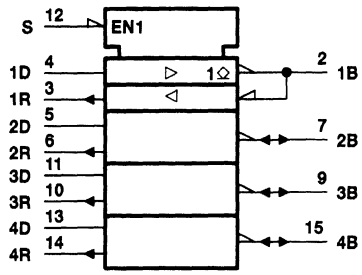
AM26S10C AND AM26S11C
(receiving)

INPUTS			OUTPUT
S	B	D	R
H	H	X	L
H	L	X	H

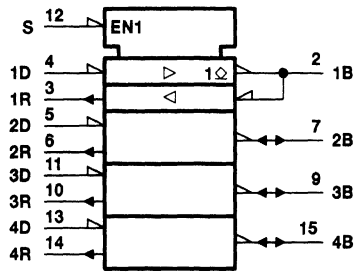
H = high level, L = low level, X = irrelevant

logic symbols†

AM26S10C



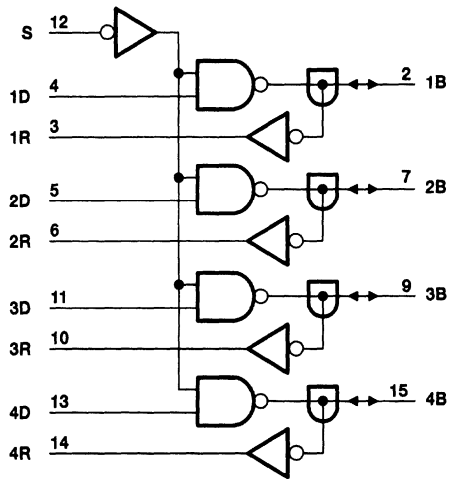
AM26S11C



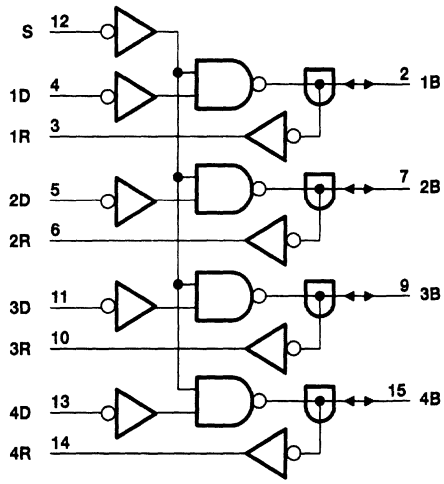
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

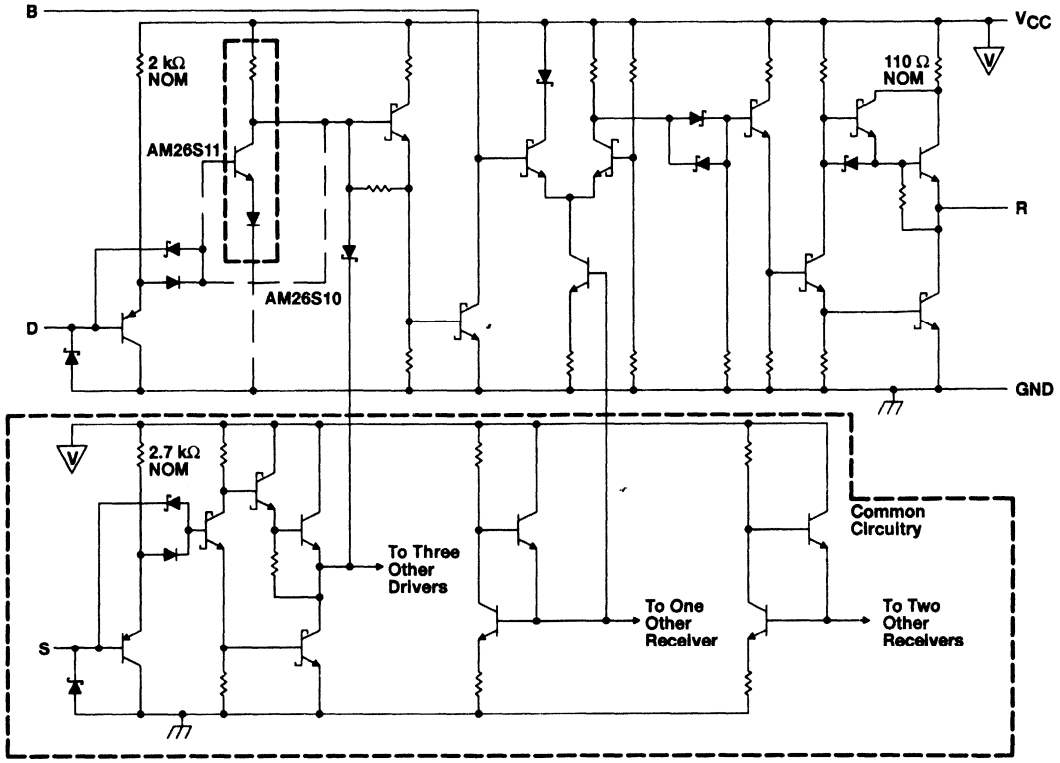
AM26S10C



AM26S11C



schematic (each transceiver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Driver or strobe input voltage range, V_I ..... −0.5 V to 5.5 V
Bus voltage range, driver output off, V_O ..... −0.5 V to 5.25 V
Driver or strobe input current range, I_I ..... −30 mA to 5 mA
Driver output current, I_O ..... 200 mA
Receiver output current, I_O ..... 30 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminals connected together.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-levael input voltage, V_{IH}	D or S	2			V
	B	2.25			
Low-level input voltage, V_{IL}	D or S			0.8	V
	B			1.75	
Receiver high-level output current, I_{OH}				−1	mA
Low-level output current, I_{OL}	Driver			100	mA
	Receiver			20	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating free-air temperature range

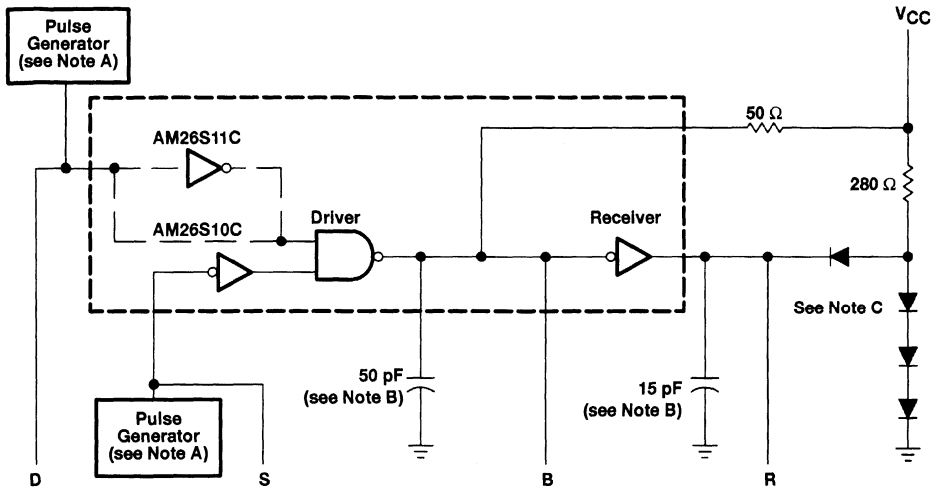
PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	D or S	V_{CC} = 4.75 V, I_I = −18 mA					−1.2	V
V_{OH}	High-level output voltage	R	V_{CC} = 4.75 V, I_{OH} = −1 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,	2.7	3.4		V
V_{OH}	Low-level output voltage	R	V_{CC} = 4.75 V, V_{IL} = 0.8 V	V_{IH} = 2 V,	I_{OL} = 20 mA			0.5	V
		B			I_{OL} = 40 mA		0.33	0.5	
					I_{OL} = 70 mA		0.42	0.7	
					I_{OL} = 100 mA		0.51	0.8	
$I_{O(off)}$	Off-stage output current	B	V_{IH} = 2 V, V_{IL} = 0.8 V	V_{CC} = 5.25 V,	V_O = 0.8 V			−50	μA
				V_{CC} = 5.25 V,	V_O = 4.5 V			100	
				V_{CC} = 0,	V_O = 4.5 V			100	
I_{IH}	High-level input current	D	V_{CC} = 5.25 V, V_I = 2.7 V					30	μA
		S						20	
I_I	Input current at maximum input voltage	D or S	V_{CC} = 5.25 V, V_I = 5.5 V					100	μA
I_{IL}	Low-level input current	D	V_{CC} = 5.25 V, V_I = 0.4 V					−0.54	mA
		S						−0.36	
I_{OS}	Short-circuit output current‡	R	V_{CC} = 5.25 V			−18		−60	mA
I_{CC}	Supply current		V_{CC} = 5.25 V, All driver outputs low	Strobe at 0 V,	No load,		45	70	mA
								80	

† All typical values are at T_A = 25°C and V_{CC} = 5 V.
‡ Not more than one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.

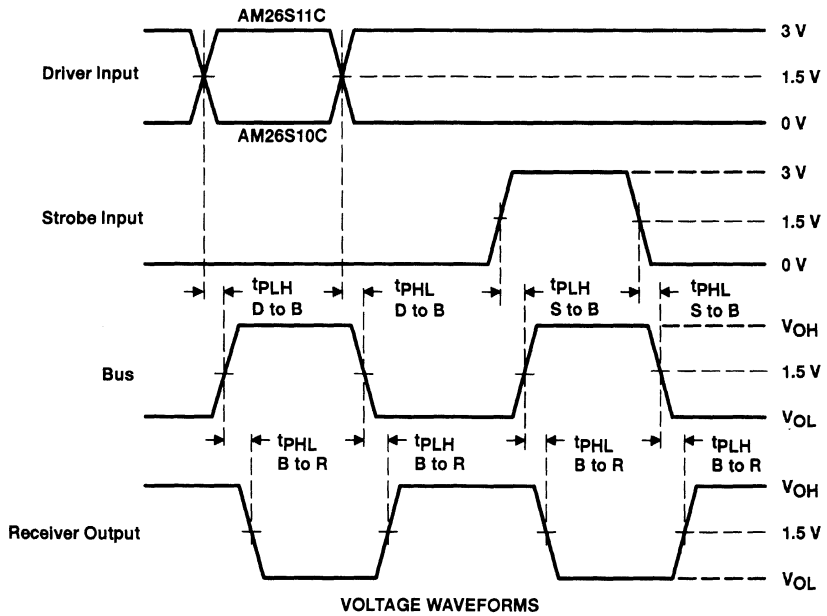
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	AM26S10C			AM26S11C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	D	B	See Figure 1		10	15		12	19	ns
t_{PHL}	Propagation delay time, high-to-low-level output					10	15		12	19	
t_{PLH}	Propagation delay time, low-to-high-level output	S	B			14	18		15	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					13	18		14	20	
t_{PLH}	Propagation delay time, low-to-high-level output	B	R			10	15		10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output					10	15		10	15	
t_{TLH}	Transition time, low-to-high-level output		B		4	10		4	10		ns
t_{THL}	Transition time, high-to-low-level output				2	4		2	4		

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_O = 50 Ω, t_r = 10 ± 5 ns.
B. Includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

Figure 1. Test Circuit and Voltage Waveforms

APPLICATION INFORMATION

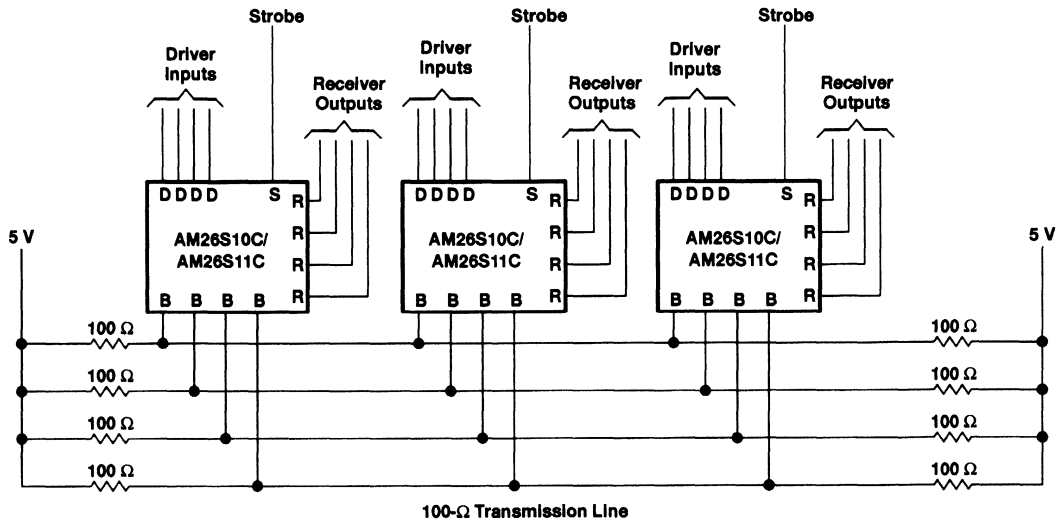


Figure 2. Party-Line System

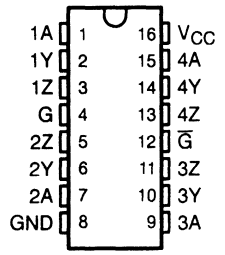
- **Meet or Exceed the Requirements of ANSI EIA/TIA-422-B and ITU Recommendation V.11**
- **Low Power, I_{CC} = 100 μA Typ**
- **Operate From a Single 5-V Supply**
- **High Speed, $t_{PLH} = t_{PHL}$ = 7 ns Typ**
- **Low Pulse Distortion, $t_{sk(p)}$ = 0.5 ns Typ**
- **High Output Impedance in Power-Off Conditions**
- **Improved Replacement for AM26LS31**

description

The AM26C31C, AM26C31I, and AM26C31M are four complementary-output line drivers designed to meet the requirements of ANSI EIA/TIA-422-B and ITU (formerly CCITT). The 3-state outputs have high-current capability for driving balanced lines such as twisted-pair or parallel-wire transmission lines, and they provide the high-impedance state in the power-off condition. The enable function is common to all four drivers and offers the choice of an active-high or active-low enable input. BiCMOS circuitry reduces power consumption without sacrificing speed.

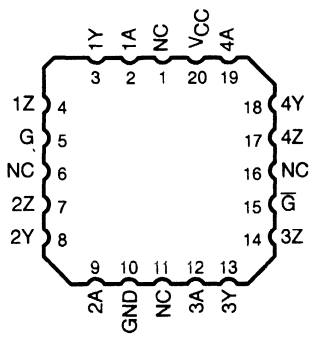
The AM26C31C is characterized for operation from 0°C to 70°C, the AM26C31I is characterized for operation from −40°C to 85°C, and the AM26C31M is characterized for operation from −55°C to 125°C

AM26C31C, AM26C31I . . . D OR DB† OR N PACKAGE
AM26C31M . . . J OR W PACKAGE
(TOP VIEW)



† The DB package is only available left-ended taped (order AM26C31IDBLE or AM26C31CDBLE).

AM26C31M . . . FK PACKAGE
(TOP VIEW)



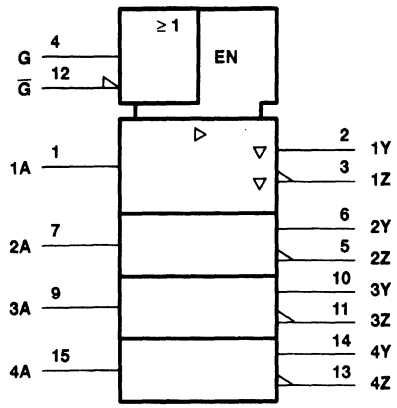
NC – No internal connection

FUNCTION TABLE
(each driver)

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

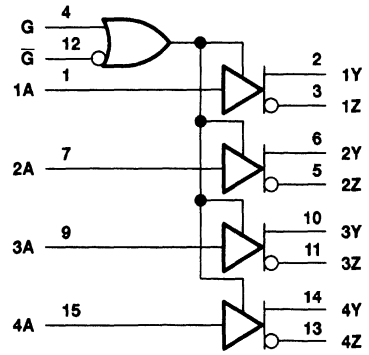
H = high level X = irrelevant
L = low level Z = high impedance (off)

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Input voltage range, V_I ..... −0.5 V to V_{CC} + 0.5 V
Differetial input voltage range, V_{ID} ..... −14 V to 14 V
Output voltage range, V_O ..... −0.5 V to 7 V
Input or output clamp current, I_{IK} or I_{OK} ..... ±20 mA
Output current, I_O ..... ±150 mA
V_{CC} current ..... 200 mA
GND current ..... −200 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: AM26C31C ..... 0°C to 70°C
AM26C31I ..... −40°C to 85°C
AM26C31M ..... −55°C to 125°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential output voltage (V_{OD}), are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	—
DW	781 mW	6.2 mW/°C	502 mW	409 mW	—
N	1150 mW	9.2 mW/°C	736 mW	598 mW	—
FK	1375 mW	11 mW/°C	—	—	275 mW
J	1375 mW	11 mW/°C	—	—	275 mW
W	1000 mW	8.0 mW/°C	—	—	200 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
Differential input voltage, V_{ID}			±7		
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}				−20	mA
Low-level output current, I_{OL}				20	mA
Operating free-air temperature, T_A	AM26C31C	0		70	°C
	AM26C31I	−40		85	
	AM26C31M	−55		125	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	AM26C31C AM26C31I			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_O = −20 mA	3.8	4.5		V
V_{OL}	Low-level output voltage	I_O = 20 mA		0.2	0.4	V
$\lvert V_{OD}\rvert$	Differential output voltage magnitude	R_L = 100 Ω, See Figure 1	2	3.1		V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage‡				±0.4	V
V_{OC}	Common-mode output voltage				3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage‡				±0.4	V
I_I	Input current	V_I = V_{CC} or GND			±1	µA
$I_{O(off)}$	Driver output current with power off	V_{CC} = 0, V_O = 6 V			100	µA
		V_{CC} = 0, V_O = −0.25 V			−100	
I_{OS}	Driver output short-circuit current	V_O = 0	−30		−150	mA
I_{OZ}	Off-state (high-impedance-state) output current	V_O = 2.5 V			20	µA
		V_O = 0.5 V			−20	µA
I_{CC}	Quiescent supply current	I_O = 0, V_I = 0 V or 5 V			100	µA
		I_O = 0, V_I = 2.4 V or 0.5 V, See Note 2		1.5	3	mA
c_I	Input capacitance			6		pF
R_I	Input resistance	V_{IC} = −7 V to 7 V	4	17		kΩ

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

‡ $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

NOTE 2: Measured per input. All other inputs are at 0 or 5 V.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			AM26C31M			UNIT
					MIN	TYP†	MAX	
V_{OH}	High-level output voltage	$I_O = -20$ mA	$T_A = 25°C$		3.8	4.5		V
			$T_A = -55°C$ to $125°C$		2.2			
V_{OL}	Low-level output voltage	$I_O = 20$ mA				0.2	0.4	V
$\lvert V_{OD}\rvert$	Differential output voltage magnitude	$R_L = 100\ \Omega$, See Figure 1			2	3.1		V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage‡						±0.4	V
V_{OC}	Common-mode output voltage						3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage‡						±0.4	V
I_I	Input current	$V_I = V_{CC}$ or GND					±1	µA
$I_{O(off)}$	Driver output current with power off	$V_{CC} = 0$,	$V_O = 6$ V				100	µA
		$V_{CC} = 0$,	$V_O = -0.25$ V				−100	
I_{OS}	Driver output short-circuit current	$V_O = 0$	$T_A = 25°C$		−30		−150	mA
			$T_A = -55°C$ to $125°C$				−170	
I_{OZ}	Off-state (high-impedance-state) output current	$V_O = 2.5$ V					20	µA
		$V_O = 0.5$ V					−20	µA
I_{CC}	Quiescent supply current	$I_O = 0$,	$V_I = 0$ V or 5 V				100	µA
		$I_O = 0$, See Note 2	$V_I = 2.4$ V or 0.5 V,	$T_A = 25°C$		1.5	3	mA
				$T_A = -55°C$ to $125°C$			3.2	
c_i	Input capacitance					6		pF
R_I	Input resistance	$V_{IC} = -7$ V to 7 V			4	17		kΩ

† All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.

‡ $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

NOTE 2: Measured per input. All other inputs are at 0 V or 5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		AM26C31C AM26C31I			UNIT
				MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low- to high-level output	S1 is open,	See Figure 2	9	17	27	ns
t_{PHL}	Propagation delay time, high- to low-level output			9	17	27	ns
$t_{sk(p)}$	Pulse skew time ($\|t_{PLH} - t_{PHL}\|$)				0.5	4	ns
$t_{r(OD)}$, $t_{f(OD)}$	Differential output rise and fall times	S1 is open,	See Figure 3		5	10	ns
t_{PZH}	Output enable time to high level	S1 is closed,	See Figure 4		10	19	ns
t_{PZL}	Output enable time to low level				10	19	ns
t_{PHZ}	Output disable time from high level				7	16	ns
t_{PLZ}	Output disable time from low level				7	16	ns
C_{pd}	Power dissipation capacitance (see Note 3)	No load			100		pF

switching characteristics, V_{CC} = 5 V, T_A = –55°C to 125°C

PARAMETER		TEST CONDITIONS		AM26C31M			UNIT
				MIN	TYP†	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	S1 is open,	See Figure 2	9	17	27	ns
t_{PHL}	Propagation delay time, high-to-low-level output			9	17	27	ns
$t_{sk(p)}$	Pulse skew time ($\|t_{PLH} - t_{PHL}\|$)				0.5	4	ns
$t_{r(OD)}$, $t_{f(OD)}$	Differential output rise and fall times	S1 is open,	See Figure 3		5	12	ns
t_{PZH}	Output enable time to high level	S1 is closed,	See Figure 4		10	19	ns
t_{PZL}	Output enable time to low level				10	19	ns
t_{PHZ}	Output disable time from high level				7	16	ns
t_{PLZ}	Output disable time from low level				7	16	ns
C_{pd}	Power dissipation capacitance (see Note 3)	No load			100		pF

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

NOTE 3: C_{pd} is used to estimate the switching losses according to $P_D = C_{pd} V_{CC}^2 f$, where P_D is in watts, C_{pd} is in farads, V_{CC} is in volts, and f is in hertz.

PARAMETER MEASUREMENT INFORMATION

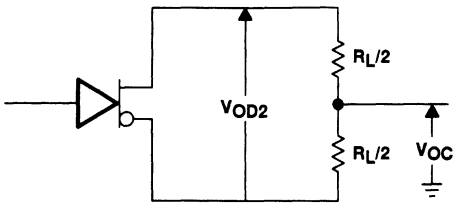
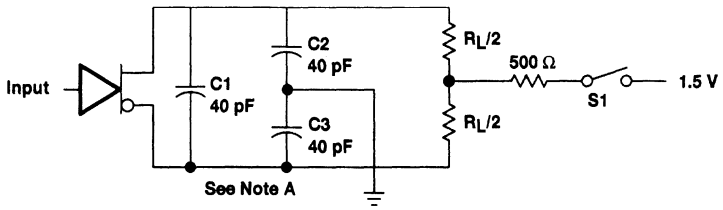


Figure 1. Differential and Common-Mode Output Voltages



TEST CIRCUIT

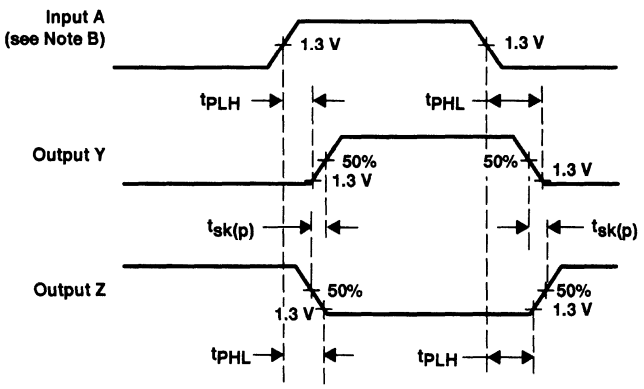


Figure 2. Propagation Delay Time and Skew Waveforms and Test Circuit

NOTES: A. C1 – C3 includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, and t_f ≤ 6 ns.

PARAMETER MEASUREMENT INFORMATION

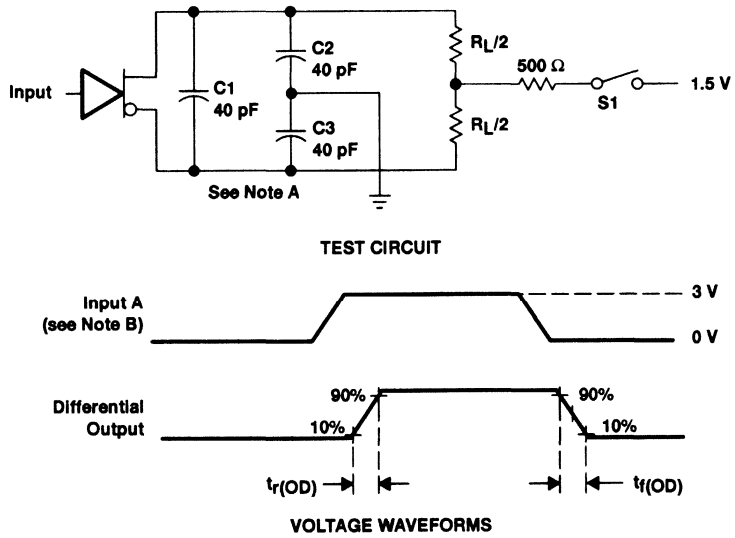


Figure 3. Differential Output Rise and Fall Time Waveforms and Test Circuit

NOTES: A. C1 – C3 includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, and t_f ≤ 6 ns.

PARAMETER MEASUREMENT INFORMATION

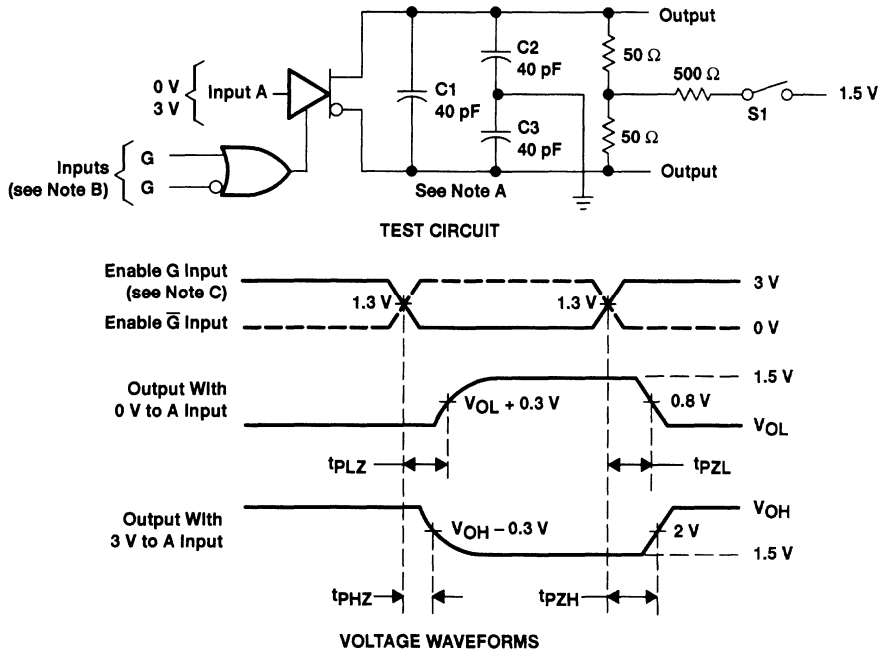
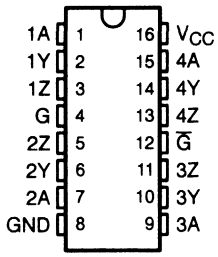


Figure 4. Output Enable and Disable Time Waveforms and Test Circuit

NOTES: A. C1 – C3 includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r < 6 ns, and t_f < 6 ns.
C. Each enable is tested separately.

- **Meets or Exceeds the Requirements of ANSI EIA/TIA-422-B and ITU Recommendation V.11**
- **Operates From a Single 5-V Supply**
- **TTL Compatible**
- **Complementary Outputs**
- **High Output Impedance in Power-Off Conditions**
- **Complementary Output Enable Inputs**

D OR N PACKAGE
(TOP VIEW)



description

The AM26LS31C is a quadruple complementary-output line driver designed to meet the requirements of ANSI EIA/TIA-422-B and ITU (formerly CCITT) V.11. The 3-state outputs have high-current capability for driving balanced lines such as twisted-pair or parallel-wire transmission lines, and they provide a high-impedance state in the power-off condition. The enable function is common to all four drivers and offers the choice of an active-high or active-low enable input. Low-power Schottky circuitry reduces power consumption without sacrificing speed.

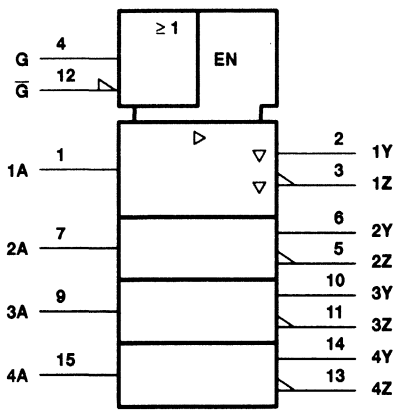
The AM26LS31C is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each driver)

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

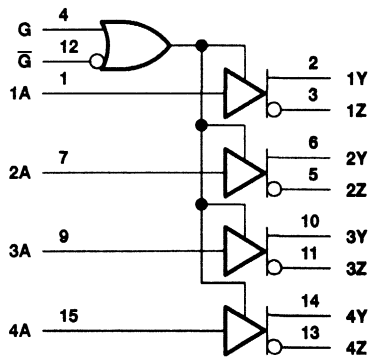
H = high level X = irrelevant
L = low level Z = high impedance (off)

logic symbol†

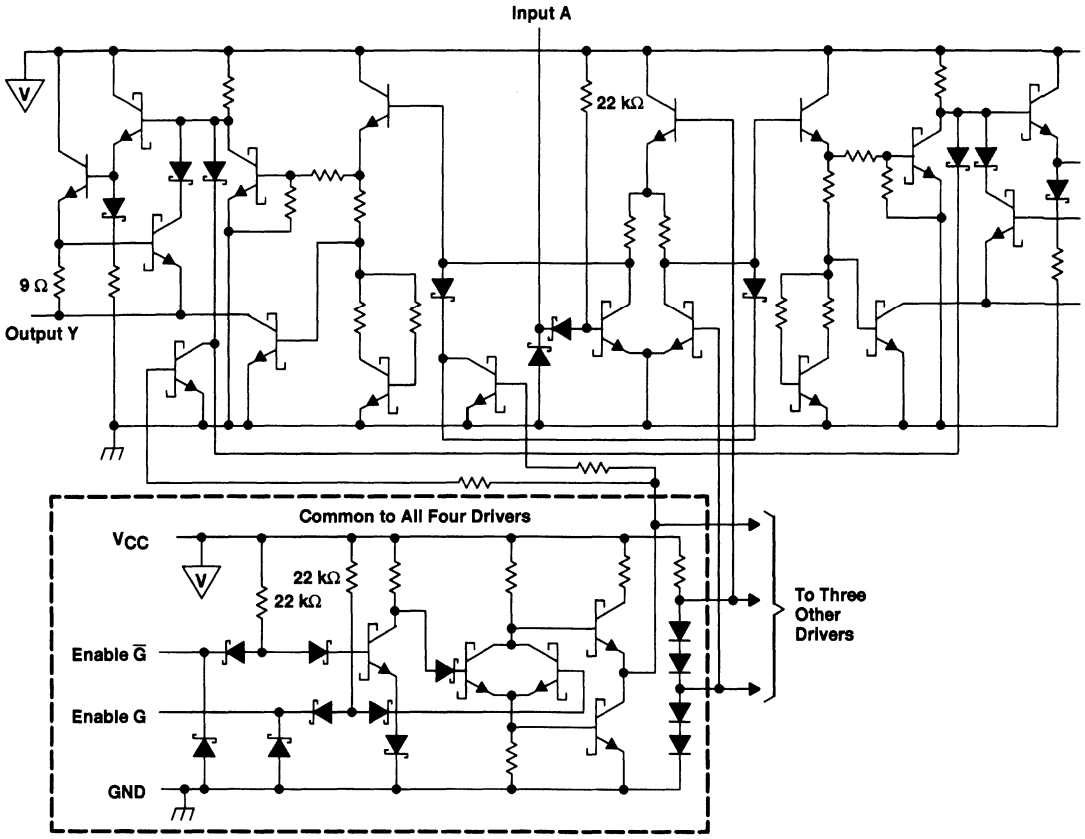


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic (each driver)



All resistor values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I	7 V
Output off-state voltage	5.5 V
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential output voltage V_{OD}, are with respect to network GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

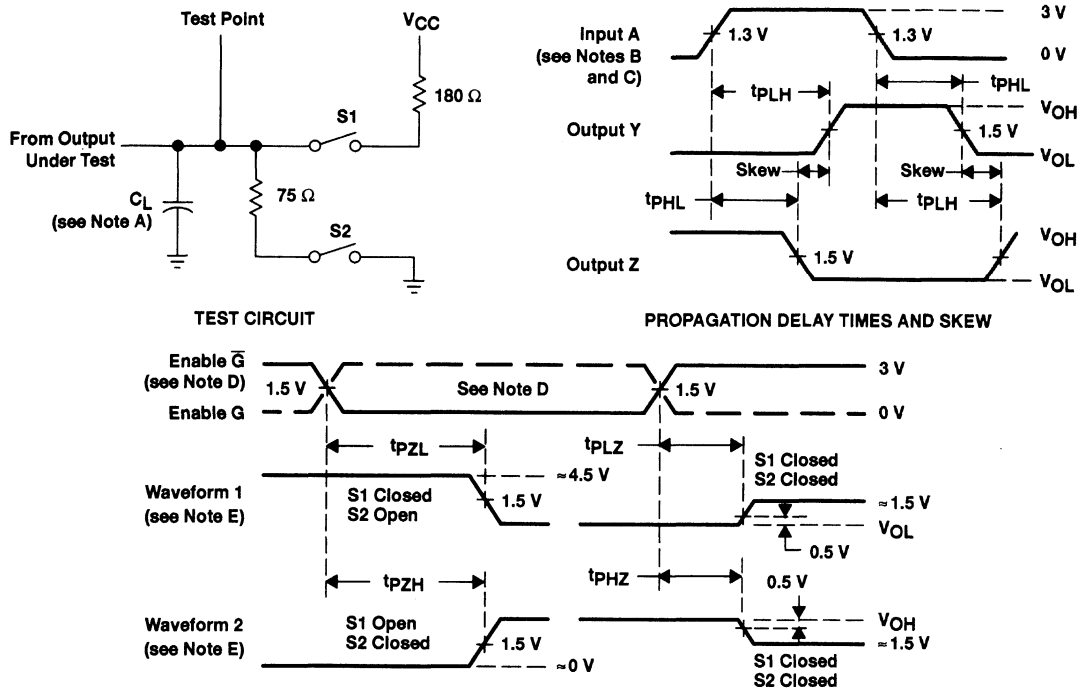
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V, I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, I_{OH} = −20 mA		2.5			V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, I_{OL} = 20 mA				0.5	V
I_{OZ}	Off-state (high-impedance-state) output current	V_{CC} = 4.75 V	V_O = 0.5 V			−20	µA
			V_O = 2.5 V			20	
I_I	Input current at maximum input voltage	V_{CC} = 5.25 V, V_I = 7 V				0.1	mA
I_{IH}	High-level input current	V_{CC} = 5.25 V, V_I = 2.7 V				20	µA
I_{IL}	Low-level input current	V_{CC} = 5.25 V, V_I = 0.4 V				−0.36	mA
I_{OS}	Short-circuit output current‡	V_{CC} = 5.25 V		−30		−150	mA
I_{CC}	Supply current	V_{CC} = 5.25 V,	All outputs disabled		32	80	mA

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, See Figure 1	S1 and S2 open,		14	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output				14	20	ns
	Output-to-output skew				1	6	ns
t_{PZH}	Output enable time to high level	C_L = 30 pF, See Figure 1	R_L = 75 Ω,		25	40	ns
t_{PZL}	Output enable time to low level	C_L = 30 pF, See Figure 1	R_L = 180 Ω,		37	45	ns
t_{PHZ}	Output disable time from high level	C_L = 10 pF, See Figure 1	S1 and S2 closed,		21	30	ns
t_{PLZ}	Output disable time from low level				23	35	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\ \Omega$, $t_r \leq 15$ ns, and $t_f \leq 6$ ns.
C. When measuring propagation delay times and skew, switches S1 and S2 are open.
D. Each enable is tested separately.
E. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

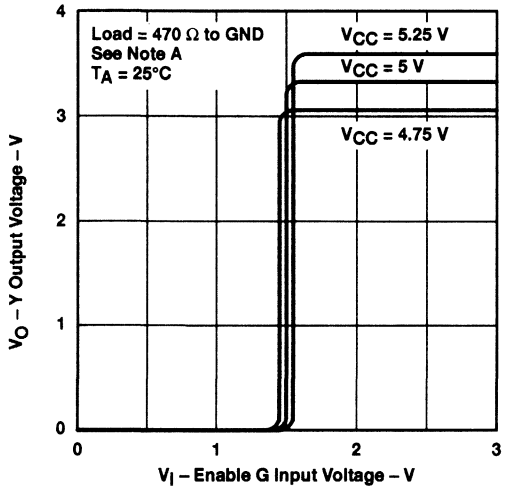


Figure 2

OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

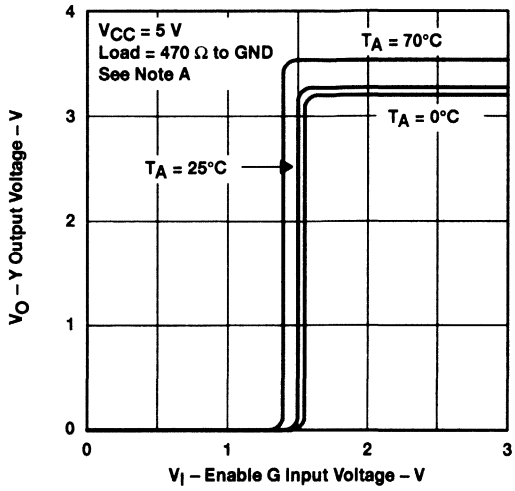


Figure 3

OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

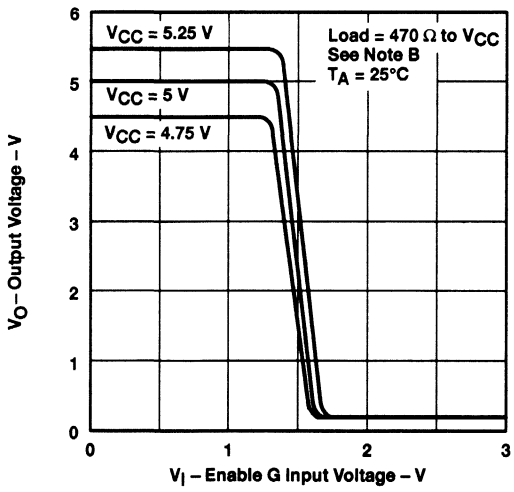


Figure 4

OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

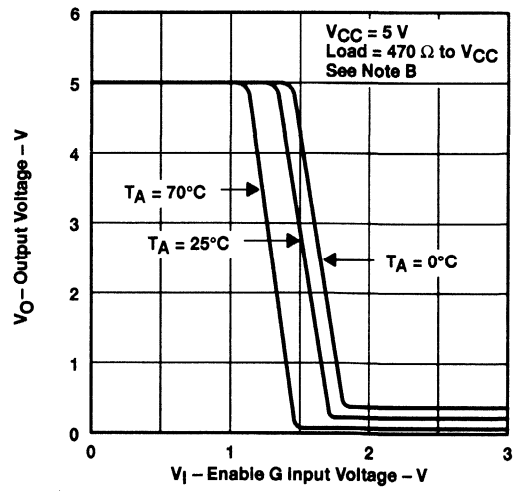


Figure 5

NOTES: A. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during testing of the Z outputs.
B. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

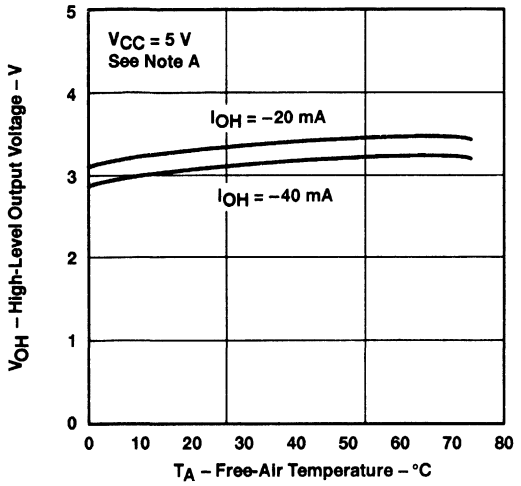


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

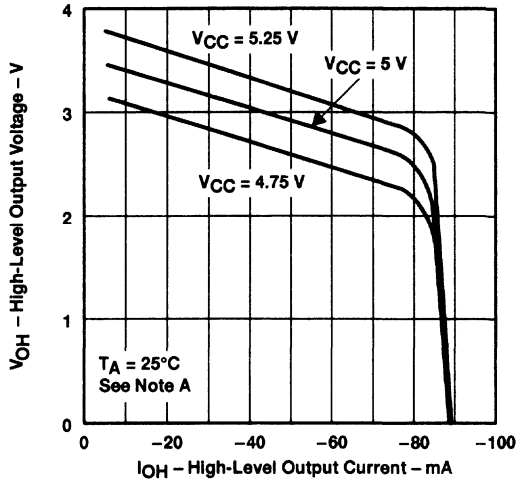


Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

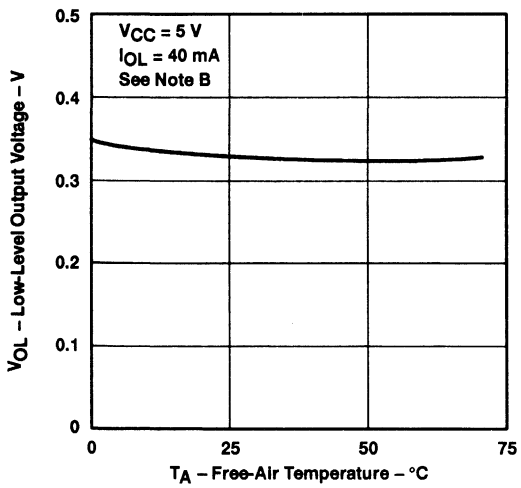


Figure 8

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

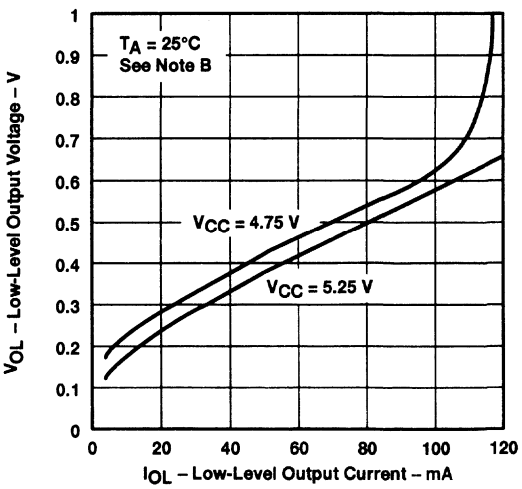


Figure 9

NOTES: A. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during testing of the Z outputs.
B. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z inputs.

TYPICAL CHARACTERISTICS

Y OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

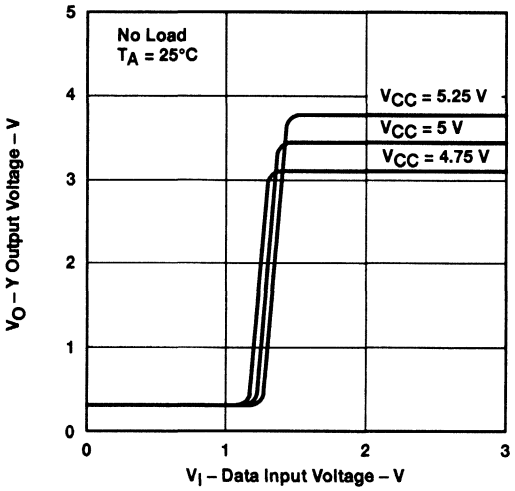


Figure 10

Y OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

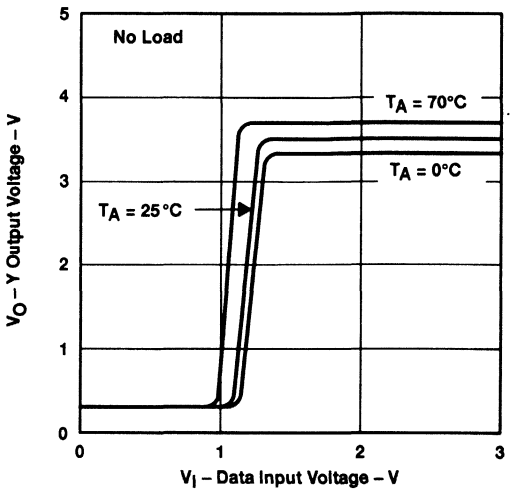


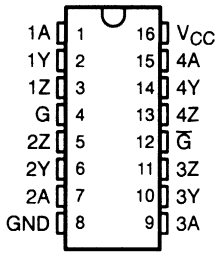
Figure 11

AM26LV31C
LOW-VOLTAGE HIGH-SPEED QUADRUPLE DIFFERENTIAL LINE DRIVER

SLLS201A – MAY 1995 – REVISED SEPTEMBER 1995

- **32-MHz Switching Rate**
- **Operates From a Single 3.3-V Supply**
- **Propagation Delay Times . . . 8 ns TYP**
- **Pulse Skew Time . . . 500 ps TYP**
- **High Output Drive Current . . . ±30 mA**
- **Controlled Rise and Fall Times . . . 3 ns TYP**
- **Differential Output Voltage With 100-Ω Load 1.5 TYP**
- **Ultra-Low Power Dissipation**
  - **dc . . . 0.3 mW MAX**
  - **32 MHz All Channels (No Load) 385 mW TYP**
- **Low Voltage Pin Compatible Replacement For AM26C31, AM26LS31, MB571**
- **High Output Impedance In Power-off Condition**
- **Driver Output Short Protection Circuit**

D OR NS PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each driver)

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H = high level X = irrelevant
L = low level Z = high impedance (off)

description

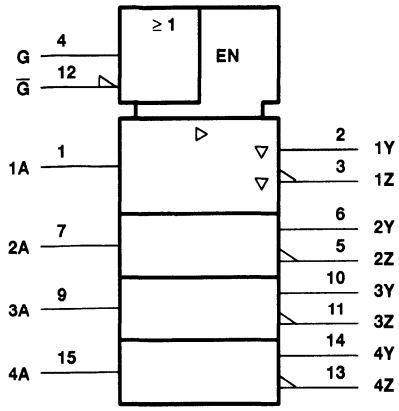
The AM26LV31C is a monolithic BiCMOS quadruple differential line driver with 3-state outputs and is designed to be similar to ANSI Standard EIA/TIA-422-B and ITU Recommendation V.11 drivers with reduced supply voltage range.

The device is optimized for balanced bus transmission at switching rates up to and exceeding 32 MHz. The outputs have very high current capability for driving balanced lines such as twisted-pair transmission lines and provide a high-impedance in the power-off condition. The enable function is common to all four drivers and offers the choice of active-high or active-low enable inputs. The AM26LV31C is designed using TI's proprietary LinIMPACT-C60™ facilitating ultra-low power consumption without sacrificing speed. This device offers optimum performance when used with the AM26LV32 quadruple line receivers.

The AM26LV31C is characterized for operation from 0°C to 70°C.

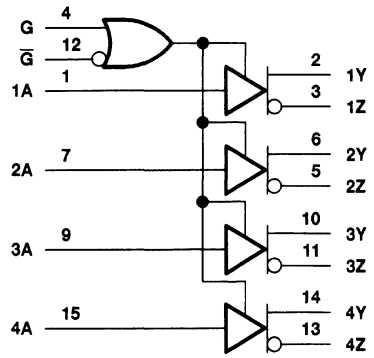
LinIMPACT-C60 is a trademark of Texas Instruments Incorporated.

logic symbol†

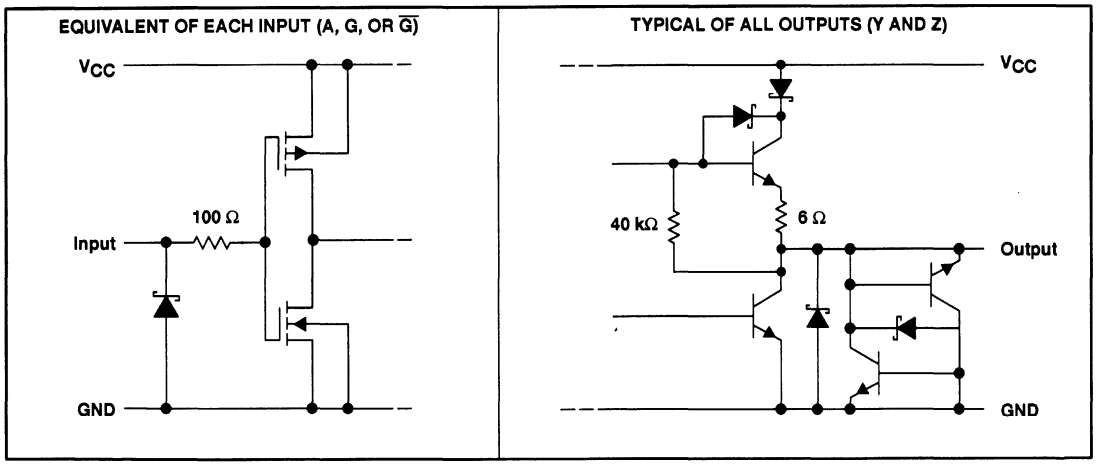


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic (each driver)



All resistor values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.3 V to 6 V
Input voltage range, V_I ..... −0.3 V to 6 V
Output voltage range, V_O ..... −0.3 V to 6 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
NS	992 mW	7.9 mW/°C	637 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−30	mA
Low-level output current, I_{OL}			30	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating supply voltage range and free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V,	$I_{OH} = -12$ mA	1.85	2.3		V
V_{OL}	Low-level output voltage	V_{IL} = 0.8 V,	I_{OH} = 12 mA		0.8	1.05	V
$\lvert V_{OD}\rvert$	Differential output voltage§	RL = 100 Ω		0.95	1.5		V
V_{OC}	Common-mode output voltage			1.3	1.55	1.8	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current with power off	$V_O = -0.25$ V or 6 V,	V_{CC} = 0			±100	μA
I_{OZ}	Off-state (high-impedance-state) output current	$V_O = -0.25$ V or 6 V, G = 0.8V or $\overline{G}$ = 2 V				±100	μA
I_{IH}	High-level input current	V_{CC} = 0 or 3 V,	V_I = 5.5 V			10	μA
I_{IL}	Low-level input current	V_{CC} = 3.6 V,	V_I = 0			−10	μA
I_{OS}	Short-circuit output current	V_{CC} = 3.6 V,	V_O = 0			−200	mA
I_{CC}	Supply current (all drivers)	$V_I = V_{CC}$ or GND,	No load			100	μA
C_{pd}	Power dissipation capacitiance (all drivers)¶	No load			160		pF

‡ All typical values are at V_{CC} = 3.3 V and T_A = 25°C.
§ $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.
¶ C_{pd} determines the no-load dynamic current consumption. $I_S = C_{pd} V_{CC} \times f + I_{CC}$

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 2		4	8	12	ns
t_{PHL}	Propagation delay time, high- to low-level output			4	8	12	ns
t_t	Transition time (t_r or t_f)				3		ns
SR	Slew rate, single-ended output voltage	See Note 2 and Figure 2			0.3	1	V/ns
t_{PZH}	Output enable time to high level	See Figure 3			10	20	ns
t_{PZL}	Output enable time to low level	See Figure 4			10	20	ns
t_{PHZ}	Output disable time from high level	See Figure 3			10	20	ns
t_{PLZ}	Output disable time from low level	See Figure 4			10	20	ns
$t_{sk(p)}$	Pulse skew	f = 32 MHz,	See Note 3		0.5	1.5	ns
$t_{sk(lim)1}$	Skew limit†	f = 32 MHz,	See Note 4			1.5	ns
$t_{sk(lim)2}$	Skew limit (device to device)†	f = 32 MHz,	See Note 5			3	ns

† This specification applies to any five degree band within the operating temperature range at the same V_{CC}.

NOTES: 2. Slew rate is defined by this equation. $SR = \dfrac{90\%\,(V_{OH} - V_{OL}) - 10\%\,(V_{OH} - V_{OL})}{t_r}$, the differential slew rate of V_{OD} is 2 × SR.
3. Pulse skew is defined as the $\lvert t_{PLH} - t_{PHL}\rvert$ of each channel.
4. Skew limit is the maximum difference in propagation delay times between any two channels of one device.
5. Skew limit (device to device) is the maximum difference in propagation delay times between any two channels of any device.

PARAMETER MEASUREMENT INFORMATION

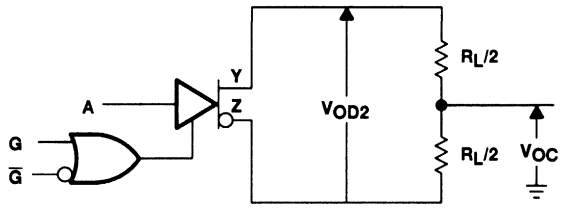
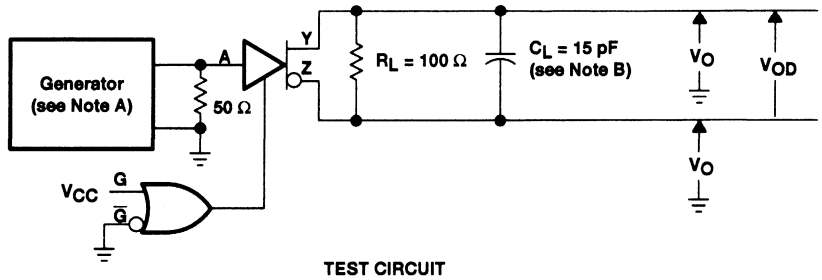
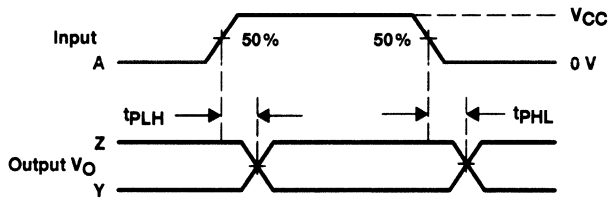


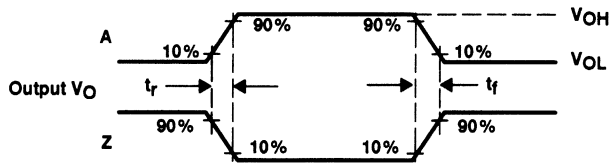
Figure 1. Differential and Common-Mode Output Voltages



TEST CIRCUIT



PROPAGATION DELAY TIMES

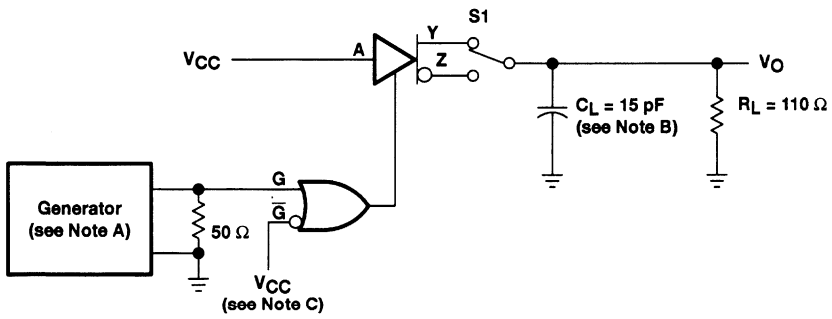


RISE AND FALL TIMES

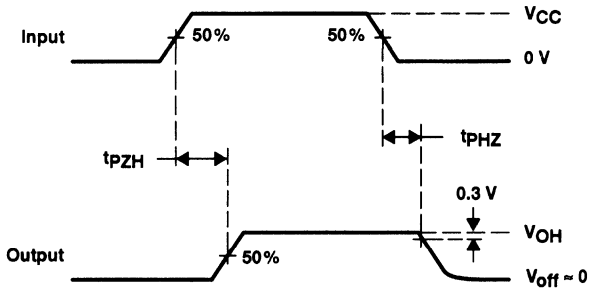
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 32 MHz, Z_O = 50 Ω, 50% duty cycle, t_r and $t_f \leq 2$ ns.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms, t_{PHL} and t_{PLH}

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

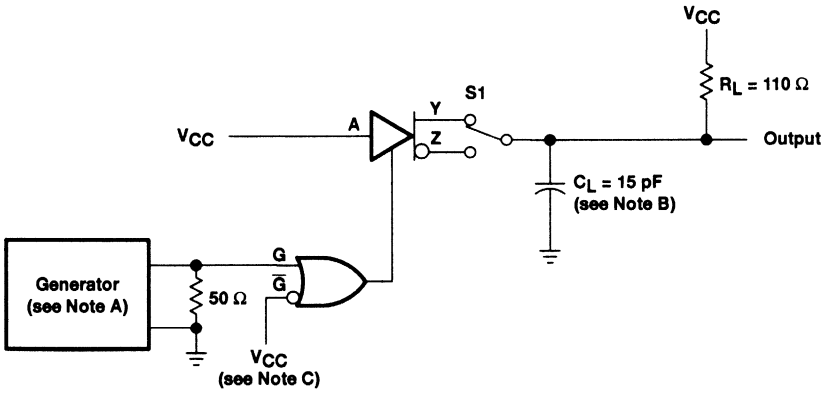


VOLTAGE WAVEFORMS

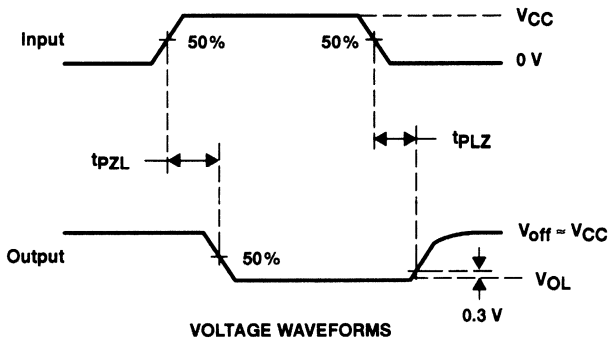
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, 50% duty cycle, t_r and t_f (10% to 90%) ≤ 2 ns.
B. C_L includes probe and jig capacitance.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted wave form to $\overline{G}$.

Figure 3. Test Circuit and Voltage Waveforms, t_{PZH} and t_{PHZ}

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, 50% duty cycle, t_r and t_f (10% to 90%) ≤ 2 ns.
B. C_L includes probe and jig capacitance.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted wave form to $\overline{G}$.

Figure 4. Test Circuit and Voltage Waveforms, t_{PZL} and t_{PLZ}

- **Meets or Exceeds the Requirements of ANSI EIA/TIA-422-B, EIA/TIA-423-B, and ITU Recommendation V.10 and V.11**
- **Low Power, I_{CC} = 10 mA Typ**
- **±7-V Common-Mode Range With ±200-mV Sensitivity**
- **Input Hysteresis . . . 60 mV Typ**
- **t_{pd} = 17 ns Typ**
- **Operate From a Single 5-V Supply**
- **3-State Outputs**
- **Input Fail-Safe Circuitry**
- **Improved Replacements for AM26LS32**

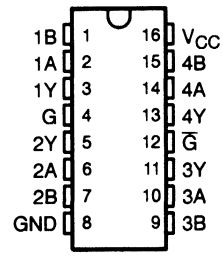
description

The AM26C32C, AM26C32I, and AM26C32M are quadruple differential line receivers for balanced or unbalanced digital data transmission. The enable function is common to all four receivers and offers a choice of active-high or active-low input. The 3-state outputs permit connection directly to a bus-organized system. Fail-safe design ensures that if the inputs are open, the outputs are always high.

The AM26C32 is manufactured using a BiCMOS process, which is a combination of bipolar and CMOS transistors. This process provides the high voltage and current of bipolar with the low power of CMOS to reduce the power consumption to about one-fifth that of the standard AM26LS32 while still maintaining ac and dc performance.

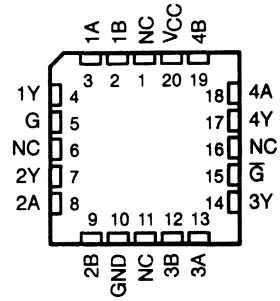
The AM26C32C is characterized for operation from 0°C to 70°C, the AM26C32I is characterized from −40°C to 85°C, and the AM26C32M is characterized from −55°C to 125°C.

AM26C32C, AM26C32I . . . D, DBT, N, OR NST PACKAGE
AM26C32M . . . J OR W PACKAGE
(TOP VIEW)



† The DB and NS packages are available left-ended taped and reeled only (order device AM26C32CDBLE or AM26C32CNSLE).

FK PACKAGE
(TOP VIEW)



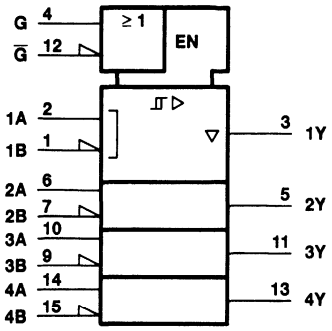
NC – No internal connection

FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUT	ENABLES		OUTPUT
	G	$\overline{G}$	
$V_{ID} \geq V_{IT+}$	H	X	H
	X	L	H
$V_{IT-} < V_{ID} < V_{IT+}$	H	X	?
	X	L	?
$V_{ID} \leq V_{IT-}$	H	X	L
	X	L	L
X	L	H	Z

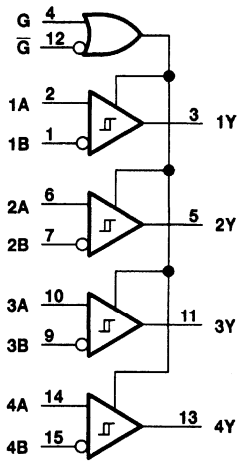
H = high level, L = low level, X = irrelevant
Z = high impedance (off), ? = indeterminate

logic symbol†

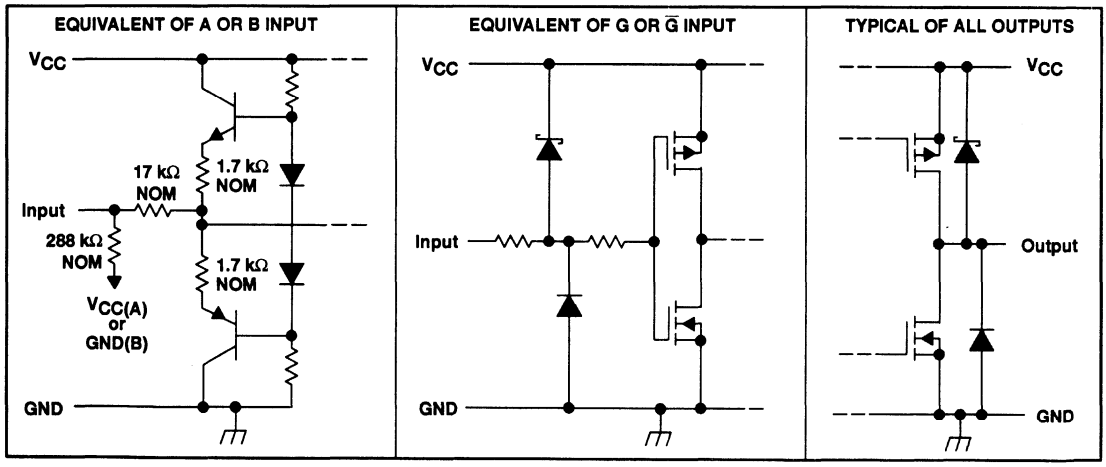


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage range, V_I: A or B inputs ..... −11 V to 14 V
G or $\overline{G}$ inputs ..... −0.5 V to V_{CC} + 0.5 V
Differential input voltage range, V_{ID} ..... −14 V to 14 V
Output voltage range, V_O ..... −0.5 V to V_{CC} + 0.5 V
Output current, I_O ..... ±25 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: AM26C32C ..... 0°C to 70°C
AM26C32I ..... −40°C to 85°C
AM26C32M ..... −55°C to 125°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential output voltage, V_{OD}, are with respect to network GND. Currents into the device are positive and currents out of the device are negative.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	—
DB	781 mW	6.2 mW/°C	502 mW	409 mW	—
N	1150 mW	9.2 mW/°C	736 mW	598 mW	—
NS	625 mW	5.0 mW/°C	400 mW	325 mW	—
J	1375 mW	11 mW/°C	—	—	275 mW
W	1000 mW	8.0 mW/°C	—	—	200 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Common-mode input voltage, V_{IC}				±7	V
High-level output current, I_{OH}				−6	mA
Low-level output current, I_{OL}				6	mA
Operating free-air temperature, T_A	AM26C32C	0		70	°C
	AM26C32I	−40		85	
	AM26C32M	−55		125	

electrical characteristics over recommended ranges of V_{CC}, V_{IC}, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Differential input high-threshold voltage	$V_O = V_{OH}$ min, $I_{OH} = -440\ \mu A$	V_{IC} = full range			0.2	V
			V_{IC} = 0 to 5.5 V			0.1	
V_{IT-}	Differential input low-threshold voltage	V_O = 0.45 V, I_{OL} = 8 mA	V_{IC} = full range	−0.2‡			V
			V_{IC} = 0 to 5.5 V	−0.1‡			
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)				60		mV
V_{IK}	Enable input clamp voltage	V_{CC} = 4.5 V,	$I_I = -18$ mA			−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	$I_{OH} = -6$ mA	3.8			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV,	I_{OL} = 6 mA		0.2	0.3	V
I_{OZ}	Off-state (high-impedance-state) output current	$V_O = V_{CC}$ or GND			±0.5	±5	μA
I_I	Line input current	V_I = 10 V,	Other input at 0 V			1.5	mA
		$V_I = -10$ V,	Other input at 0 V			−2.5	
I_{IH}	High-level enable current	V_I = 2.7 V				20	μA
I_{IL}	Low-level enable current	V_I = 0.4 V				−100	μA
r_i	Input resistance	One input to ground		12	17		kΩ
I_{CC}	Supply current	V_{CC} = 5.5 V			10	15	mA

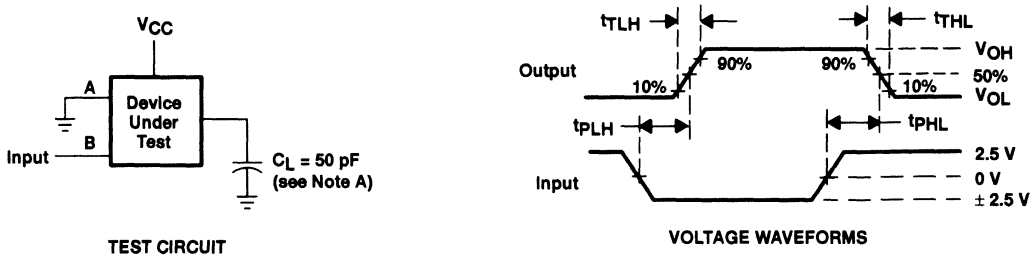
† All typical values are at V_{CC} = 5 V, V_{IC} = 0, and T_A = 25°C.
‡ The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage.

switching characteristics over recommended ranges of operating conditions, C_L = 50 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	AM26C32C AM26C32I			AM26C32M			UNIT
			MIN	TYP§	MAX	MIN	TYP§	MAX	
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 1	9	17	27	9	17	27	ns
t_{PHL}	Propagation delay time, high- to low-level output		9	17	27	9	17	27	ns
t_{TLH}	Output transition time, low- to high-level output	See Figure 1		4	9		4	10	ns
t_{THL}	Output transition time, high- to low-level output			4	9		4	9	ns
t_{PZH}	Output enable time to high level	See Figure 2		13	22		13	22	ns
t_{PZL}	Output enable time to low level			13	22		13	22	ns
t_{PHZ}	Output disable time from high level	See Figure 2		13	22		13	26	ns
t_{PLZ}	Output disable time from low level			13	22		13	25	ns

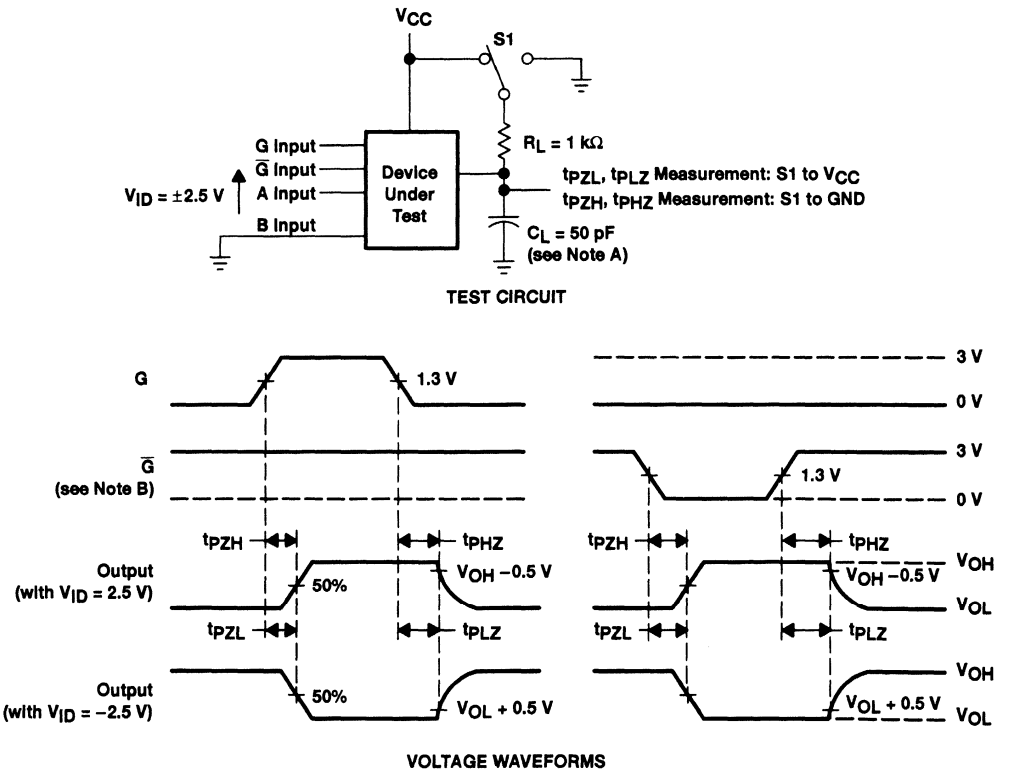
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



NOTE A. C_L includes probe and jig capacitance.

Figure 1. Switching Test Circuit and Voltage Waveforms



NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle ≤ 50%, $t_r = t_f = 6$ ns.

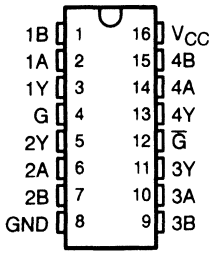
Figure 2. Enable/Disable Time Test Circuit and Output Voltage Waveforms

AM26LS32AC, AM26LS33AC, AM26LS32AM, AM26LS33AM
QUADRUPLE DIFFERENTIAL LINE RECEIVERS

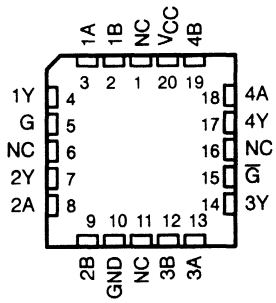
SLLS115B – OCTOBER 1980 – REVISED MAY 1995

- **AM26LS32A Meets or Exceeds the Requirements of ANSI EIA/TIA-422-B, EIA/TIA-423-B, and ITU Recommendations V.10 and V.11**
- **AM26LS32A Has ±7-V Common-Mode Range With ±200-mV Sensitivity**
- **AM26LS32A Has ±15-V Common-Mode Range With ±500-mV Sensitivity**
- **Input Hysteresis . . . 50 mV Typical**
- **Operates From a Single 5-V Supply**
- **Low-Power Schottky Circuitry**
- **3-State Outputs**
- **Complementary Output Enable Inputs**
- **Input Impedance . . . 12 kΩ Min**
- **Designed to Be Interchangeable With Advanced Micro Devices AM26LS32™ and AM26LS33™**

AM26LS32AC, AM26LS33AC . . . D OR N PACKAGE
AM26LS32AM, AM26LS33AM . . . J PACKAGE
(TOP VIEW)



AM26LS32AM, AM26LS33AM . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The AM26LS32A and AM26LS33A are quadruple differential line receivers for balanced and unbalanced digital data transmission. The enable function is common to all four receivers and offers a choice of active-high or active-low input. The 3-state outputs permit connection direct to a bus-organized system. Fail-safe design ensures that if the inputs are open, the outputs will always be high.

Compared to the AM26LS32 and the AM26LS33, the AM26LS32A and AM26LS33A incorporate an additional stage of amplification to improve sensitivity. The input impedance has been increased resulting in less loading of the bus line. The additional stage has increased propagation delay; however, this will not affect interchangeability in most applications.

The AM26LS32AC and AM26LS33AC are characterized for operation from 0°C to 70°C. The AM26LS32AM and AM26LS33AM are characterzed for operation over the full military temperature range of −55°C to 125°C.

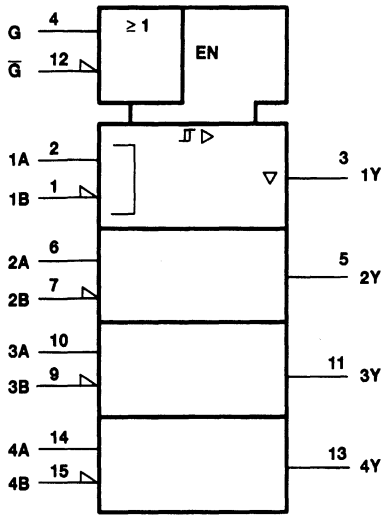
FUNCTION TABLE
(each receiver)

DIFFERENTIAL A – B	ENABLES G	ENABLES $\overline{G}$	OUTPUT Y
$V_{ID} \geq V_{IT+}$	H	X	H
	X	L	H
$V_{IT-} \leq V_{ID} \leq V_{IT+}$	H	X	?
	X	L	?
$V_{ID} \leq V_{IT-}$	H	X	L
	X	L	L
X	L	H	Z
Open	H	X	H
	X	L	H

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

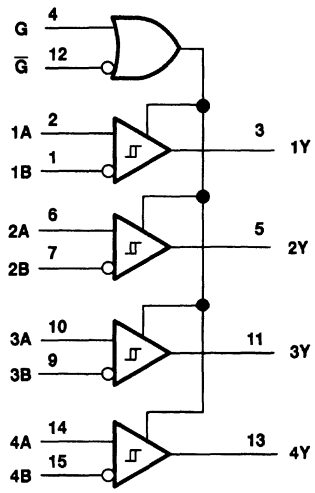
AM26LS32 and AM26LS33 are trademarks of Advanced Mircro Devices, Inc.

logic symbol†

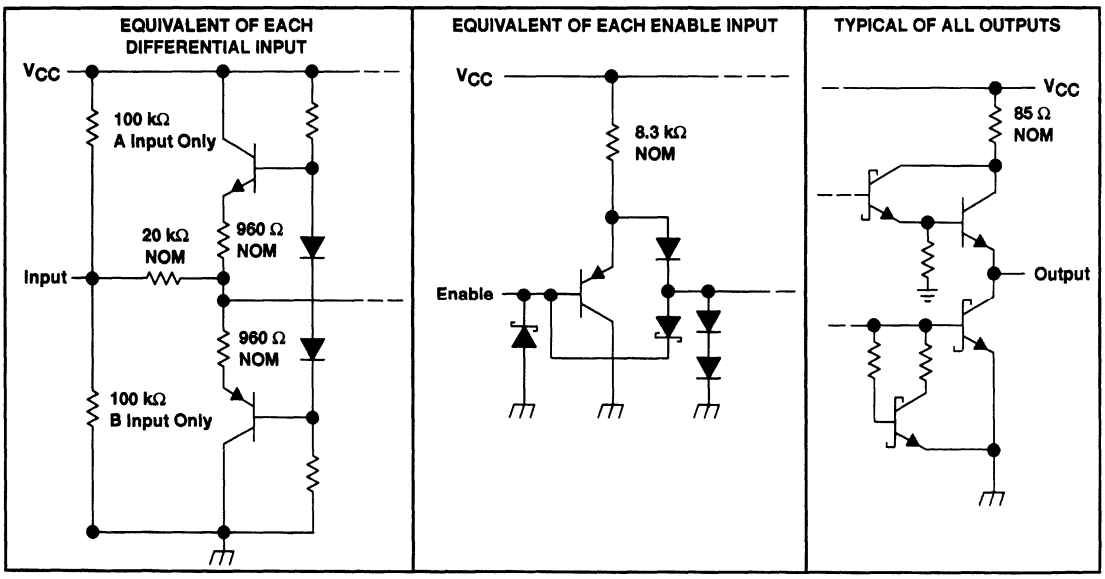


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

		AM26LS32AC AM26LS33AC	AM26LS32AM AM26LS33AM	UNIT
Supply voltage, V_{CC} (see Note 1)		7	7	V
Input voltage, V_I	Any differential input	±25	±25	V
	Other inputs	7	7	
Differential input voltage, V_{ID} (see Note 2)		±25	±25	V
Continuous total power dissipation		See Dissipation Rating Table		
Operating free-air temperature range, T_A		0 to 70	−55 to 125	°C
Storage temperature range, T_{stg}		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package	260		°C
Case temperature for 60 seconds, T_C	FK package		260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J package	300	300	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltage values are at the noninverting (A) input terminals with respect to the inverting (B) input terminals.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—

recommended operating conditions

		AM26LS32AC AM26LS33AC			AM26LS32AM AM26LS33AM			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.75	5	5.25	4.5	5	5.5	V
High-level input voltage, V_{IH}		2			2			V
Low-level input voltage, V_{IL}				0.8			0.8	V
Common-mode input voltage, V_{IC}	AM26LS32AC, AM26LS32AM			±7			±7	V
	AM26LS33AC, AM26LS33AM			±15			±15	
High-level output current, I_{OH}				−440			−440	μA
Low-level output current, I_{OL}				8			8	mA
Operating free-air temperature, T_A		0		70	−55		125	°C

electrical characteristics over recommended ranges of V_{CC}, V_{IC}, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshhold voltage	$V_O = V_{OH}$min, $I_{OH} = -440\ \mu A$		AM26LS32A			0.2	V
				AM26LS33A			0.5	
V_{IT-}	Negative-going input threshhold voltage	$V_O = 0.45$ V, $I_{OL} = 8$ mA		AM26LS32A	−0.2‡			V
				AM26LS33A	−0.5‡			
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)					50		mV
V_{IK}	Enable input clamp voltage	V_{CC} = MIN, $I_I = -18$ mA					−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, $V_{ID} = 1$ V, $V_{I(G)} = 0.8$ V, $I_{OH} = -440\ \mu A$		'32AC, '33AC	2.7			V
				'32AM, '33AM	2.5			
V_{OL}	Low-level output voltage	V_{CC} = MIN, $V_{ID} = -1$ V, $V_{I(G)} = 0.8$ V		$I_{OL} = 4$ mA			0.4	V
				$I_{OL} = 8$ mA			0.45	
I_{OZ}	Off-state (high-impedance-state) output current	V_{CC} = MAX		$V_O = 2.4$ V			20	μA
				$V_O = 0.4$ V			−20	
I_I	Line input current	$V_I = 15$ V,	Other input at −10 V to 15 V				1.2	mA
		$V_I = -15$ V,	Other input at −15 V to 10 V				−1.7	
$I_{I(EN)}$	Enable input current	$V_I = 5.5$ V					100	μA
I_{IH}	High-level enable current	$V_I = 2.7$ V					20	μA
I_{IL}	Low-level enable current	$V_I = 0.4$ V					−0.36	mA
r_I	Input resistance	$V_{IC} = -15$ V to 15 V,	One input to ac ground		12	15		kΩ
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−15		−85	mA
I_{CC}	Supply current	V_{CC} = MAX,	All outputs disabled			52	70	mA

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$, and $V_{IC} = 0$.

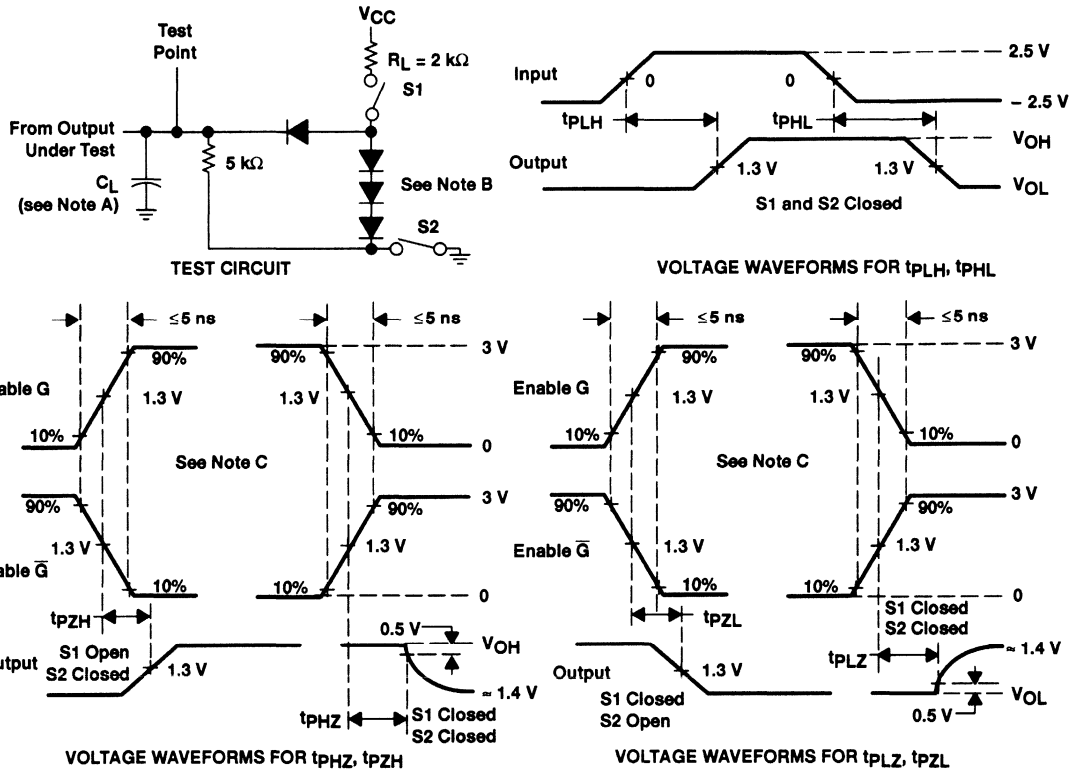
‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.

§ Not more than one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$C_L = 15$ pF, See Figure 1		20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output			22	35	ns
t_{PZH}	Output enable time to high level	$C_L = 15$ pF, See Figure 1		17	22	ns
t_{PZL}	Output enable time to low level			20	25	ns
t_{PHZ}	Output disable time from high level	$C_L = 5$ pF, See Figure 1		21	30	ns
t_{PLZ}	Output disable time from low level			30	40	ns

PARAMETER MEASUREMENT INFORMATION

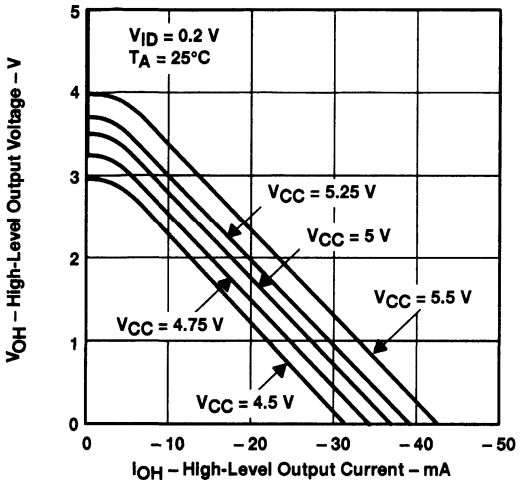


NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Enable G is tested with $\overline{G}$ high; $\overline{G}$ is tested with G low.

Figure 1

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT†



† V_{CC} = 5.5 V and V_{CC} = 4.5 V applies to M-suffix devices only.

Figure 2

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

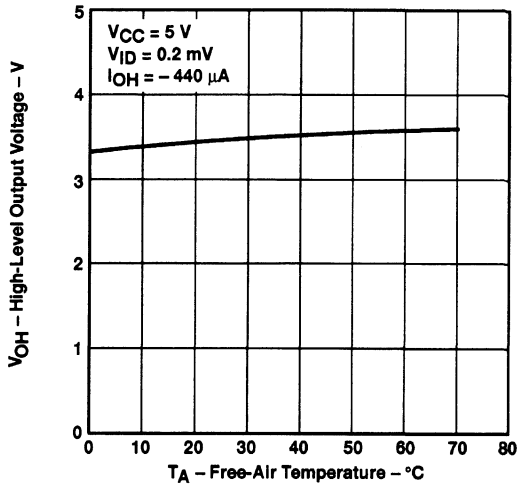


Figure 3

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

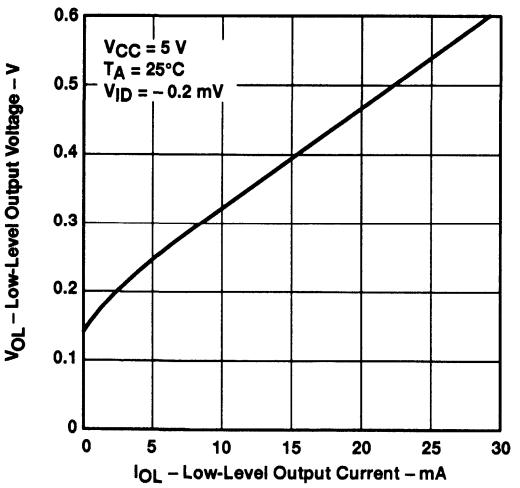


Figure 4

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

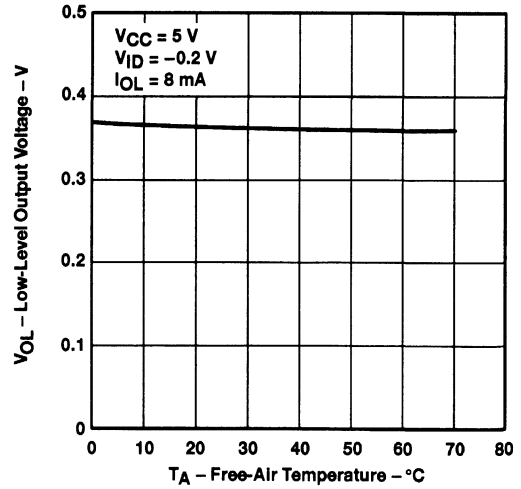


Figure 5

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
ENABLE G VOLTAGE

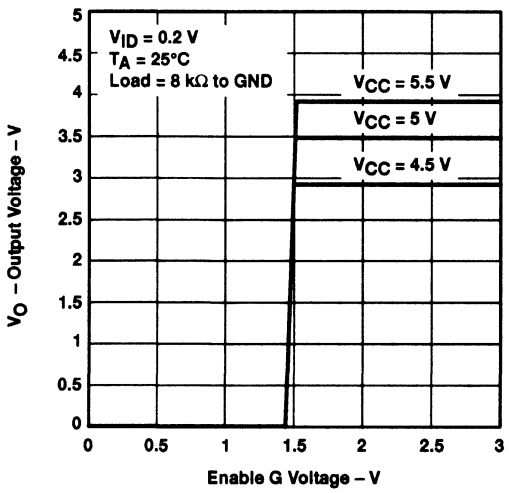


Figure 6

OUTPUT VOLTAGE
vs
ENABLE G VOLTAGE

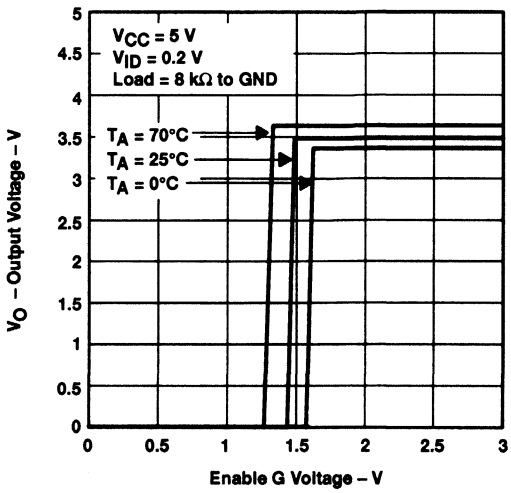


Figure 7

OUTPUT VOLTAGE
vs
ENABLE G VOLTAGE

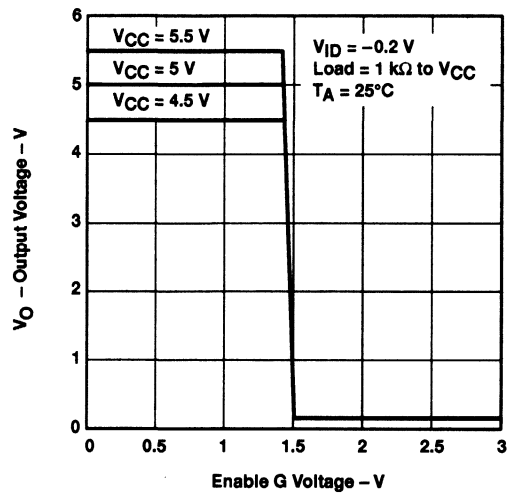


Figure 8

OUTPUT VOLTAGE
vs
ENABLE G VOLTAGE

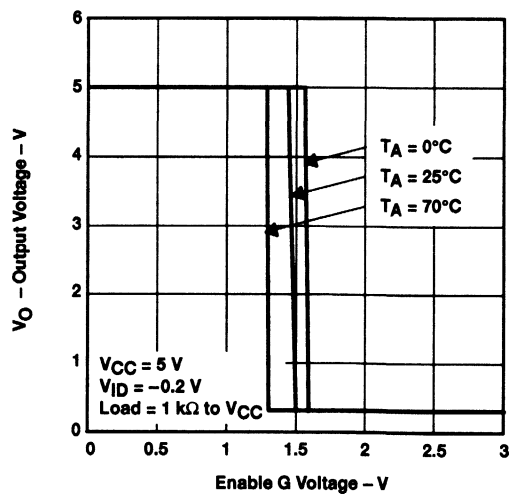


Figure 9

TYPICAL CHARACTERISTICS

AM26LS32A
OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

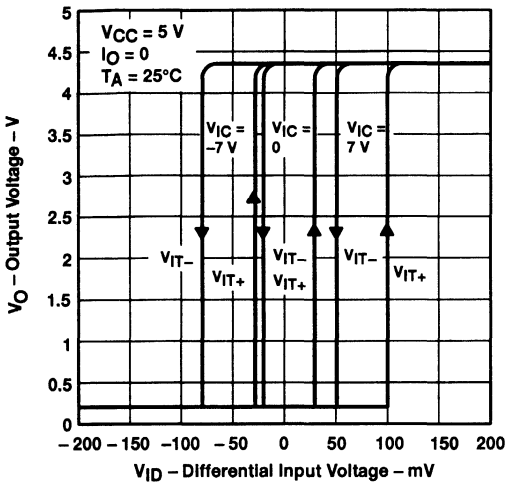


Figure 10

AM26LS33A
OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

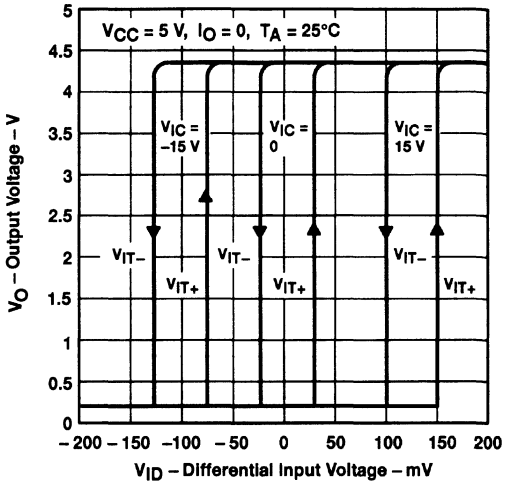
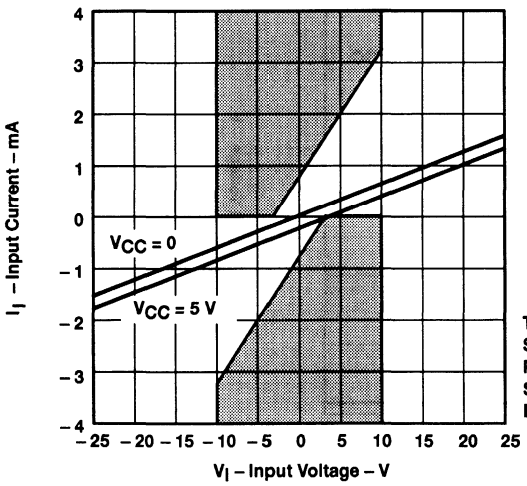


Figure 11

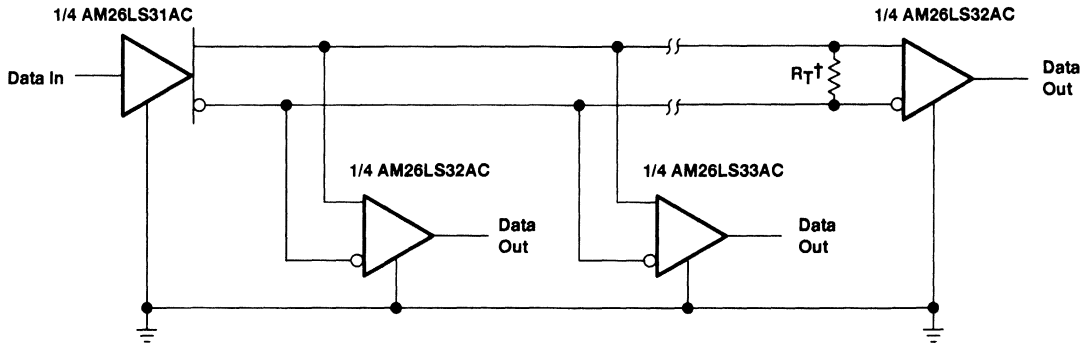
INPUT CURRENT
vs
INPUT VOLTAGE



The Unshaded Area Shows Requirements of Paragraph 4.2.1 of ANSI Standards EIA/TIA-422-B and EIA/TIA-423-B

Figure 12

APPLICATION INFORMATION



† R_T equals the characteristic impedance of the line.

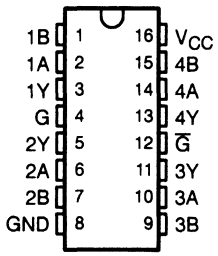
Figure 13. Circuit With Multiple Receivers

AM26LV32C
LOW VOLTAGE HIGH-SPEED QUADRUPLE DIFFERENTIAL LINE RECEIVER

SLLS202A – MAY 1995 – REVISED SEPTEMBER 1995

- **32-MHz Switching Rate**
- **Operates from a Single 3.3-V Supply**
- **Ultra-Low Power Dissipation . . . 27 mW Typ**
- **Open-Circuit Fail Safe**
- **–0.3-V to 5.5-V Common-Mode Range With ±200 mV Sensitivity**
- **Accepts 5-V Logic Inputs With a 3.3-V Supply**
- **Input Hysteresis . . . 50 mV Typ**
- **235 mW With Four Receivers at 32 MHz**
- **Pin-Compatible with the AM26C32, AM26LS32, and MB570**

D OR NST PACKAGE
(TOP VIEW)



† The NS package is only available left-ended taped and reeled. To order use part number AM26LV32CNSLE.

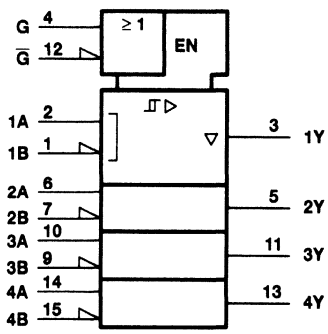
description

The AM26LV32 monolithic, BiCMOS, quadruple, differential line receiver with 3-state output is designed to be similar to ANSI EIA/TIA-422-B and ITU Recommendation V.11 receivers with reduced common-mode voltage range due to reduced supply voltage. The device is optimized for balanced bus transmission at switching rates up to and exceeding 32 MHz. The enable function is common to all four receivers and offers a choice of active-high or active-low inputs. The 3-state outputs permit connection directly to a bus-organized system. Each device features receiver high input impedance and input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of –0.3 V to 5.5 V. Fail-safe design ensures that if the inputs are open circuited, the outputs are always high. This device is designed using the TI proprietary LinIMPACT-C60™ technology facilitating ultra-low power consumption without sacrificing speed.

This device offers optimum performance when used with the AM26LV31 quadruple line drivers.

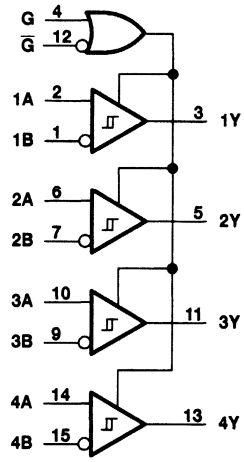
The AM26LV32C is available in the 16-pin D or the EIAJ NS small-outline packages and is characterized for operation over a temperature range of 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



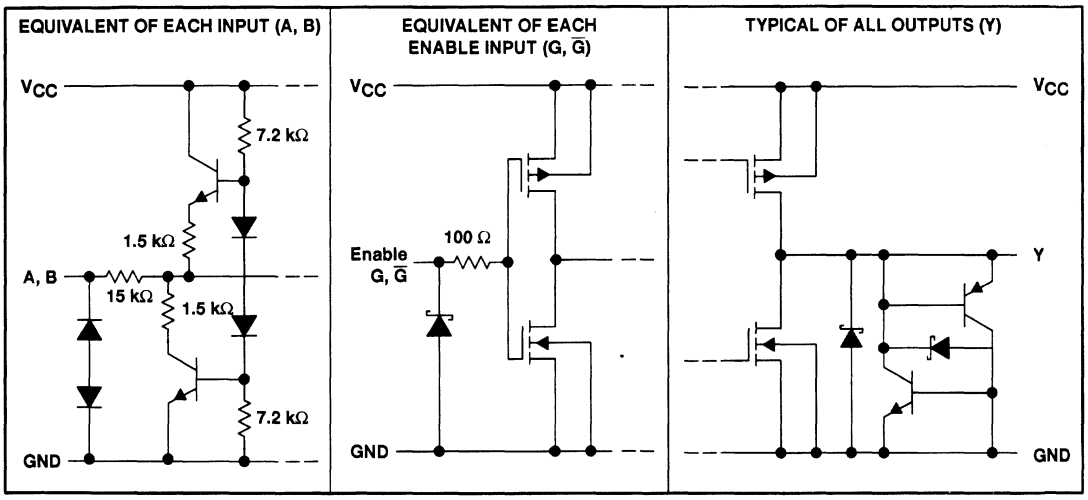
LinIMPACT-C60 is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUT	ENABLES		OUTPUT
	G	$\overline{G}$	
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
-0.2 V $< V_{ID} < 0.2$ V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
Open circuit	H	X	H
	X	L	
X	L	H	Z

H = high level, L = low level, X = irrelevant
Z = high impedance (off), ? = indeterminate

schematics of equivalent inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.3 V to 6 V
Input voltage range, V_I (A or B inputs) ..... −4 V to 8 V
Differential input voltage, V_{ID} (see Note 2) ..... ±12
Enable input voltage range ..... −0.3 V to 6 V
Output voltage range, V_O ..... −0.3 V to 6 V
Maximum output current, I_O ..... ±25 mA
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the GND terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
NS	992 mW	7.9 mW/°C	636 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
High-level input voltage, $V_{IH(EN)}$	2			V
Low-level input voltage, $V_{IL(EN)}$			0.8	V
Common-mode input voltage, V_{IC}	−0.3		5.5	V
Differential input voltage, V_{ID}			±5.8	
High-level output current, I_{OH}			−5	mA
Low-level output current, I_{OL}			5	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Differential input high-threshold voltage					0.2	V
V_{IT-}	Differential input low-threshold voltage			−0.2			V
V_{IK}	Enable input clamp voltage	I_I = −18 mA			−0.8	−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = −5 mA	2.4	3.2		V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV,	I_{OL} = 5 mA		0.17	0.5	V
I_{OZ}	High-impedance-state output current	V_O = 0 to V_{CC}				±50	µA
$I_{IH(E)}$	High-level enable input current	V_{CC} = 0 or 3 V,	V_I = 5.5 V			10	µA
$I_{IL(E)}$	Low-level enable input current	V_{CC} = 3.6 V,	V_I = 0 V			−10	µA
r_I	Input resistance			7	12		kΩ
I_I	Input current	V_I = 5.5 V or −0.3 V,	All other inputs GND			±700	µA
I_{CC}	Supply current	$V_{I(E)}$ = V_{CC} or GND,	No load, line inputs open		8	17	mA
C_{pd}	Power dissipation capacitance‡	One channel			150		pF

† All typical values are at V_{CC} = 3.3 V and T_A = 25°C.
‡ C_{pd} determines the no-load dynamic current consumption, $I_S = C_{pd} \times V_{CC} \times f + I_{CC}$.

switching characteristics over recommended ranges of operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 1	8	16	20	ns
t_{PHL}	Propagation delay time, high- to low-level output		8	16	20	ns
t_t	Transistion time (t_r or t_f)	See Figure 1		5		ns
t_{PZH}	Output enable time to high level	See Figure 2		17	40	ns
t_{PZL}	Output enable time to low level	See Figure 3		10	40	ns
t_{PHZ}	Output disable time from high level	See Figure 2		20	40	ns
t_{PLZ}	Output disable time from low level	See Figure 3		16	40	ns
$t_{sk(p)}$	Pulse skew	See Note 3		4	6	ns
$t_{sk(limc)}$	Skew limit	See Note 4		4	6	ns
$t_{sk(lim)}$	Skew limit (device to device)	See Note 5		6	9	ns

NOTES: 3. $t_{sk(p)}$ is $|t_{PLH} - t_{PHL}|$ of each channel.
4. $t_{sk(limc)}$ is the maximum difference in propagation delay times between any two channels of one device.
5. $t_{sk(lim)}$ is the maximum difference in propagation delay times between any two channels of any two devices. This specification applies to any 5°C band within the operation temperature range at the same V_{CC}.

PARAMETER MEASUREMENT INFORMATION

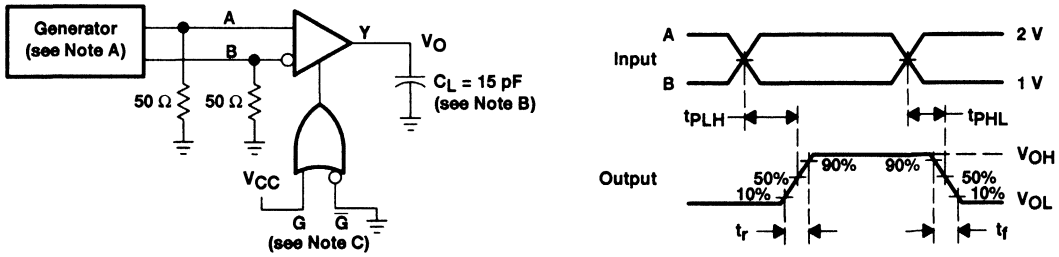


Figure 1. t_{PLH} and t_{PHL} Test Circuit and Voltage Waveforms

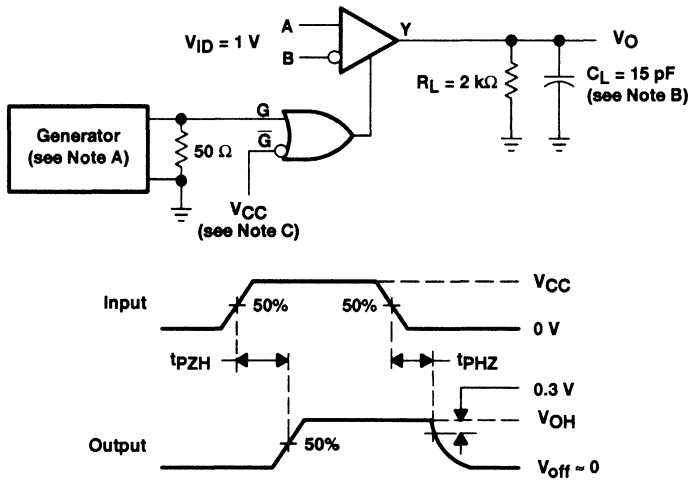


Figure 2. t_{PZH} and t_{PHZ} Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by generator having the following characterstics:
Z_O = 50 Ω, PRR = 10 MHz, t_r and t_f (10% to 90%) ≤ 2 ns, 50% duty cycle.
B. C_L includes probe and jig capacitance.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform $\overline{G}$.

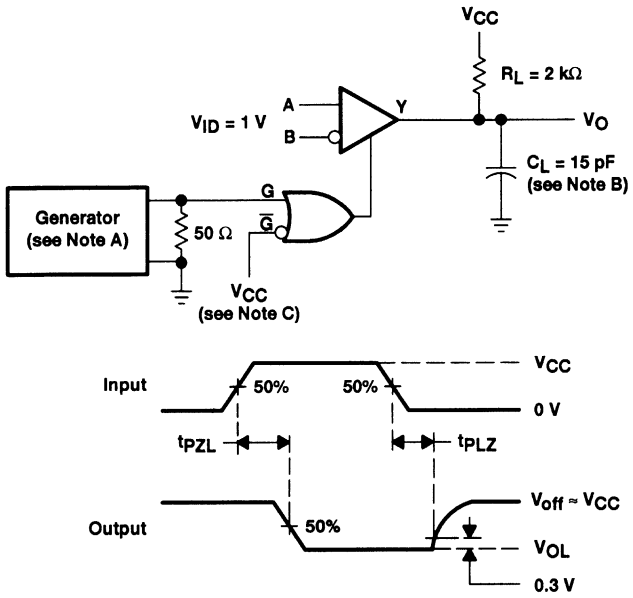


Figure 3. t_{PZL} and t_{PLZ} Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by generator having the following characterstics:
Z_O = 50 Ω, PRR = 10 MHz, t_r and t_f (10% to 90%) ≤ 2ns, 50% duty cycle.
B. C_L includes probe and jig capacitance.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform $\overline{G}$.

- **Low Supply Voltage . . . ±5 V to ±15 V**
- **Supply Current . . . 500 μA Typ**
- **Zero Supply Current When Shut Down**
- **Outputs Can Be Driven ±30 V**
- **Output Open When Off (3-State)**
- **10-mA Output Drive**
- **Outputs of Several Devices Can Be Connected in Parallel**
- **Meets or Exceeds the Requirements of ANSI EIA/TIA-232-E Specifications**
- **Designed to Be Interchangeable With Linear Technology LT1030**

description

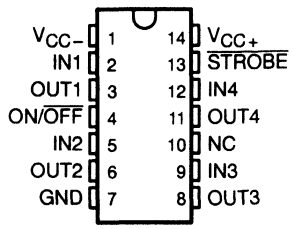
The LT1030C is an EIA/TIA-232-E line driver that operates over a ±5-V to ±15-V supply voltage range on low supply current. The device can be shut down to zero supply current. Current limiting fully protects the outputs from externally-applied voltages of ±30 V. Since the output swings to within 200 mV of the positive supply and to within 1 V of the negative supply, supply voltage requirements are minimized.

A major advantage of the LT1030C is the high-impedance output state when the device is off or powered down. This feature allows several different drivers on the same bus.

The device can be used as an EIA/TIA-232-E driver, micropower interface, or level translator, among others.

The LT1030C is characterized for operation from 0°C to 70°C.

D OR N PACKAGE
(TOP VIEW)



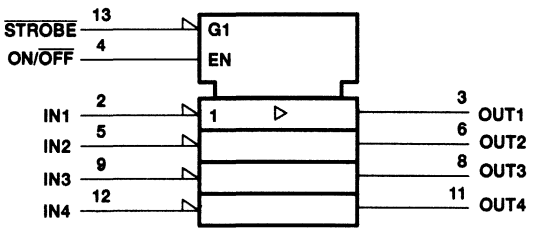
NC – No internal connection

AVAILABLE OPTIONS

T_A	PACKAGE	
	SMALL OUTLINE (D)	PLASTIC DIP (N)
0°C to 70°C	LT1030CD	LT1030CN

The D package is available taped and reeled. Add the suffix R to the device type (i.e., LT1030CDR).

logic symbol†

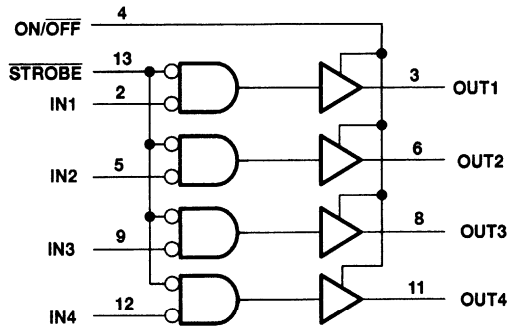


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Terminal Functions

Terminal NAME	Terminal NO.	DESCRIPTION
GND	7	Ground terminal
IN1, IN2, IN3, IN4	2, 5, 9, 12	Logic inputs. INx operate properly on TTL or CMOS levels. Output valid from $V_I = V_{CC-} + 2$ V to 15 V. Connect to 5 V when not used.
ON/$\overline{OFF}$	4	ON/$\overline{OFF}$ shuts down the entire circuit. It cannot be left open. For normally on operation, connect between 5 V and 10 V. If V_{IL} is at or near 0.8 V, significant settling time may be required.
OUT1, OUT2, OUT3, OUT4	3, 6, 8, 11	Line driver outputs
$\overline{STROBE}$	13	$\overline{STROBE}$ forces all outputs low. Drive with 3 V. Strobe terminal input impedance is approximately 2 kΩ to GND. Leave $\overline{STROBE}$ open when not used.
V_{CC+}	14	Positive supply
V_{CC-}	1	Negative supply

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC+} (see Note 1) ..... 0 V to 15 V
Supply voltage range, V_{CC-} ..... 0 V to −15 V
Input voltage range, logic inputs, V_I ..... V_{CC-} to 25 V
Input voltage range at ON/$\overline{OFF}$, V_I ..... 0 V to 12 V
Output voltage range, V_O (any output) ..... V_{CC+} − 30 V to V_{CC-} + 30 V
Duration of output short circuit to ±30 V at (or below) 25°C (see Note 2) ..... unlimited
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to GND.
2. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC+}	5	15	V
Supply voltage, V_{CC-}	−5	−15	V
High-level input voltage, V_{IH} (see Note 3)	2	15	V
Low-level input voltage, V_{IL} (see Note 3)		0.8	V
Operating free-air temperature, T_A	0	70	°C

NOTE 3: These V_{IH} and V_{IL} specifications apply only for inputs IN1 – IN4. For operating levels for ON/$\overline{OFF}$, see Figure 2.

electrical characteristics over operating free-air temperature range, $V_{CC\pm}$ = ±5 V to ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OM+}	Maximum positive peak output voltage swing	I_O = −2 mA, T_A = 25°C	V_{CC+}−0.3	V_{CC+}−0.1		V
V_{OM-}	Maximum negative peak output voltage swing	I_O = 2 mA, T_A = 25°C		V_{CC-}+0.9	V_{CC-}+1.4	V
I_{IH}	High-level input current	$V_I \geq 2$ V, T_A = 25°C		2	20	µA
I_{IL}	Low-level input current	$V_I \leq 0.8$ V, T_A = 25°C		10	20	µA
I_I	Input current, ON/$\overline{OFF}$	V_I = 0		−0.1	−10	µA
		V_I = 5 V		30	65	
I_O	Output current	T_A = 25°C	5	12		mA
I_{OZ}	Off-state output current	V_O = ±15 V, T_A = 25°C, ON/$\overline{OFF}$ at 0.4 V		±2	±100	µA
I_{CC}	Supply current (all outputs low)	$V_I \geq$ at 2.4 V, I_O = 0		500	1000	µA
$I_{CC(off)}$	Off-state supply current	ON/$\overline{OFF}$ at 0.4 V			10	µA
		ON/$\overline{OFF}$ at 0.1 V		10	150	

operating characteristics, $V_{CC\pm}$ = ±5 V to ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
SR	Driver slew rate	R_L = 3 kΩ, C_L = 51 pF	4	15	30	V/µs

† All typical values are at $V_{CC\pm}$ = ±12 V, T_A = 25°C.

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

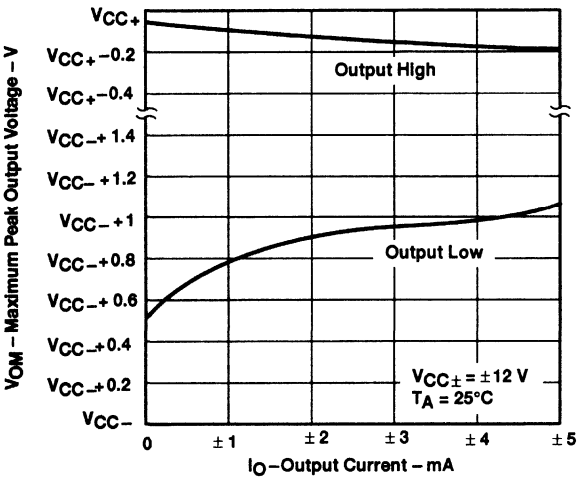


Figure 1

ON/$\overline{\text{OFF}}$ TERMINAL VOLTAGE
vs
FREE-AIR TEMPERATURE

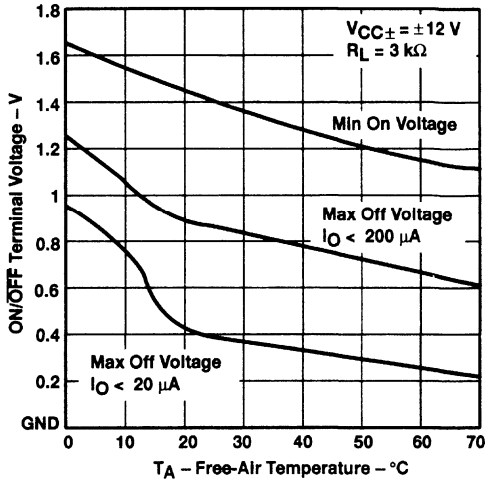


Figure 2

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

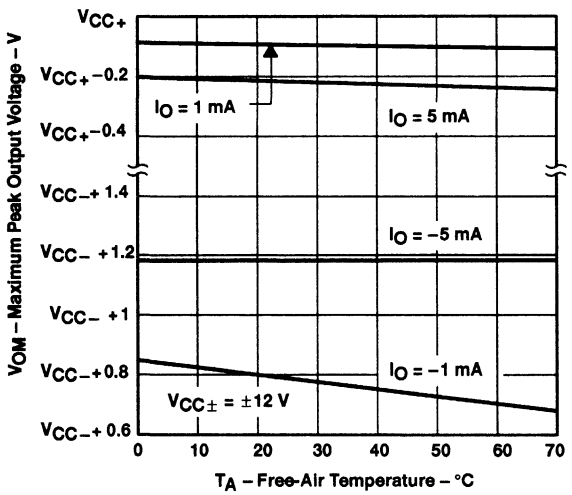


Figure 3

ON/$\overline{\text{OFF}}$ TERMINAL CURRENT
vs
ON/$\overline{\text{OFF}}$ TERMINAL VOLTAGE

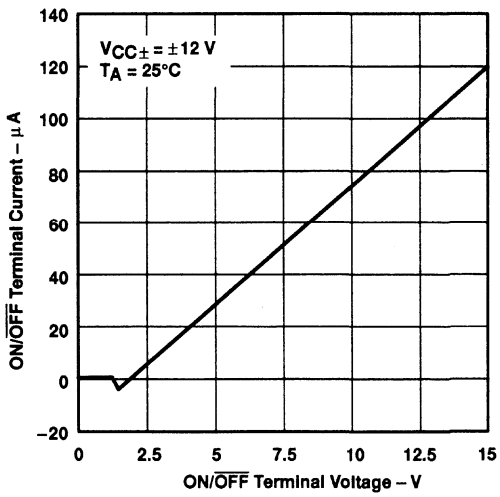


Figure 4

TYPICAL CHARACTERISTICS

OUTPUT CURRENT vs FREE-AIR TEMPERATURE

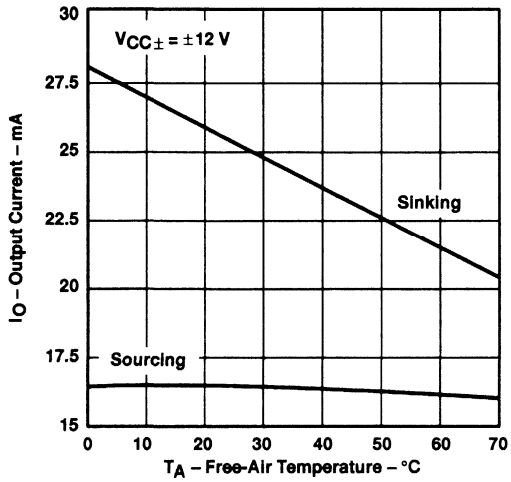


Figure 5

OFF-STATE OUTPUT CURRENT vs FREE-AIR TEMPERATURE

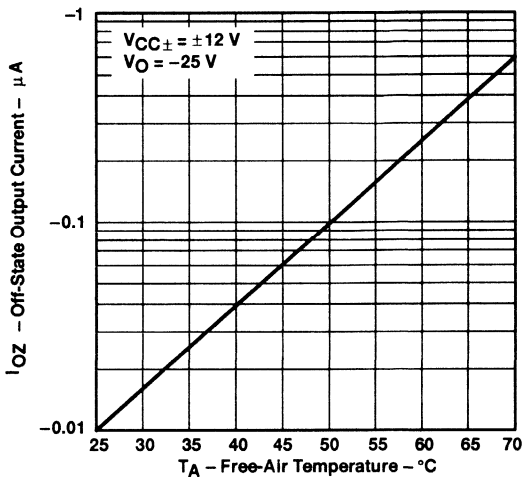


Figure 6

OFF-STATE SUPPLY CURRENT vs FREE-AIR TEMPERATURE

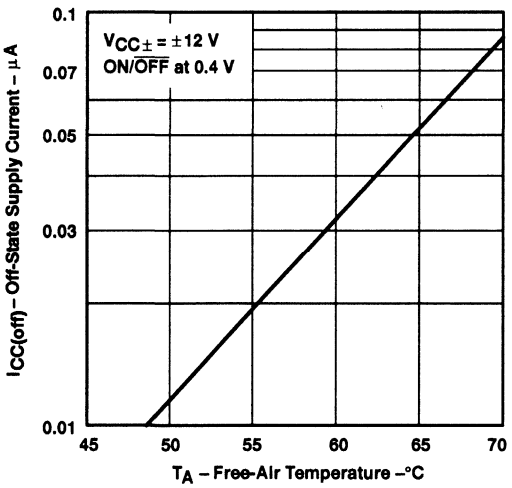


Figure 7

SUPPLY CURRENT vs TOTAL SUPPLY VOLTAGE

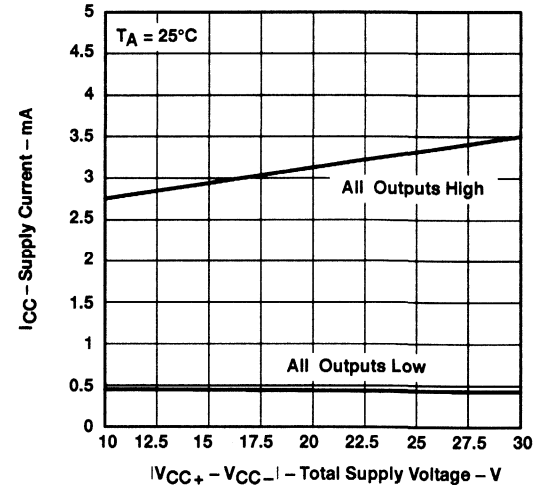


Figure 8

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

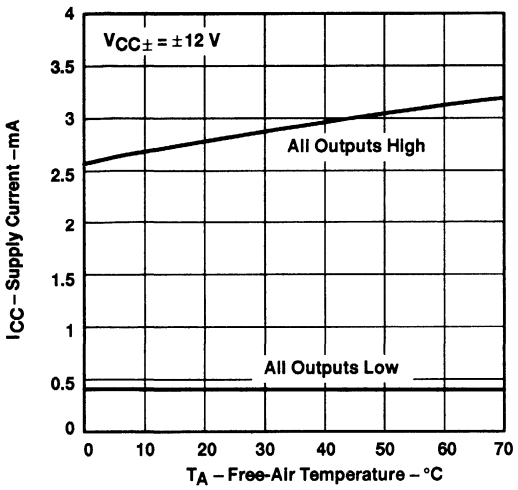


Figure 9

SLEW RATE vs FREE-AIR TEMPERATURE

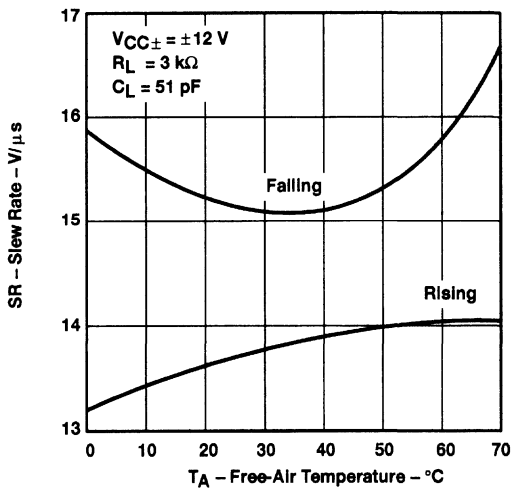


Figure 10

APPLICATION INFORMATION

forward biasing the substrate

As with other bipolar integrated circuits, forward biasing the substrate diode can cause problems. The LT1030C will draw high current from V_{CC+} to GND if V_{CC-} is open-circuited or pulled above ground. Connecting a diode from V_{CC-} to GND (if possible) prevents the high-current state. Any low-cost diode can be used (see Figure 11).

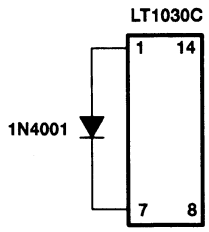
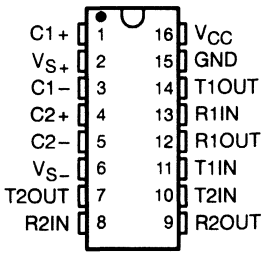


Figure 11. Connecting a Diode From V_{CC-} to GND

- **Operates With Single 5-V Power Supply**
- **LinBiCMOS™ Process Technology**
- **Two Drivers and Two Receivers**
- **±30-V Input Levels**
- **Low Supply Current . . . 8 mA Typ**
- **Meets or Exceeds ANSI EIA/TIA-232-E and ITU Recommendation V.28**
- **Designed to be Interchangeable With Maxim MAX232**
- **Applications**
  - **EIA/TIA-232-E**
  - **Battery-Powered Systems**
  - **Terminals**
  - **Modems**
  - **Computers**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015**

DW OR N PACKAGE
(TOP VIEW)

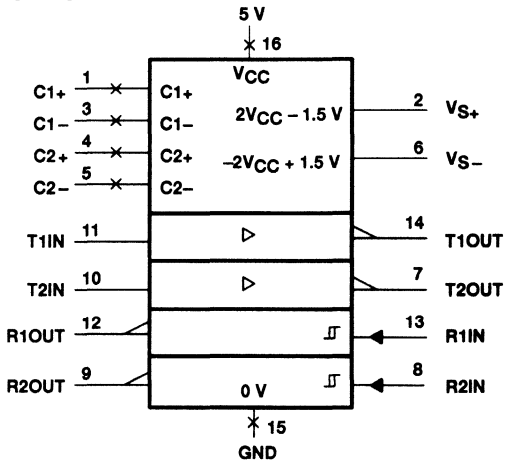


description

The MAX232 is a dual driver/receiver that includes a capacitive voltage generator to supply EIA/TIA-232-E voltage levels from a single 5-V supply. Each receiver converts EIA/TIA-232-E inputs to 5-V TTL/CMOS levels. These receivers have a typical threshold of 1.3 V and a typical hysteresis of 0.5 V, and can accept ±30-V inputs. Each driver converts TTL/CMOS input levels into EIA/TIA-232-E levels. The driver, receiver, and voltage-generator functions are available as cells in the Texas Instruments LinASIC™ library.

The MAX232 is characterized for operation from 0°C to 70°C. The MAX232I is characterized for operation from –40°C to 85°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

LinASIC and LinBiCMOS are trademarks of Texas Instruments Incorporated.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input supply voltage range, V_{CC} (see Note 1) ..... −0.3 V to 6 V
Positive output supply voltage range, V_{S+} ..... V_{CC} −0.3 V to 15 V
Negative output supply voltage range, V_{S-} ..... −0.3 V to −15 V
Input voltage range, V_I: Driver ..... −0.3 V to V_{CC} + 0.3 V
Receiver ..... ±30 V
Output voltage range, V_O: T1OUT, T2OUT ..... V_{S-} −0.3 V to V_{S+} + 0.3 V
R1OUT, R2OUT ..... −0.3 V to V_{CC} + 0.3 V
Short-circuit duration: T1OUT, T2OUT ..... unlimited
Operating free-air temperature range, T_A: MAX232 ..... 0°C to 70°C
MAX232I ..... −40°C to 85°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level input voltage, V_{IH} (T1IN,T2IN)	2			V
Low-level input voltage, V_{IL} (T1IN, T2IN)			0.8	V
Receiver input voltage, R1IN, R2IN			±30	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	T1OUT, T2OUT	R_L = 3 kΩ to GND		5	7		V
		R1OUT, R2OUT	I_{OH} = −1 mA		3.5			
V_{OL}	Low-level output voltage‡	T1OUT, T2OUT	R_L = 3 kΩ to GND			−7	−5	V
		R1OUT, R2OUT	I_{OL} = 3.2 mA				0.4	
V_{IT+}	Receiver positive-going input threshold voltage	R1IN, R2IN	V_{CC} = 5 V,	T_A = 25°C		1.7	2.4	V
V_{IT-}	Receiver negative-going input threshold voltage	R1IN, R2IN	V_{CC} = 5 V,	T_A = 25°C	0.8	1.2		V
V_{hys}	Input hysteresis voltage	R1IN, R2IN	V_{CC} = 5 V		0.2	0.5	1	V
r_i	Receiver input resistance	R1IN, R2IN	V_{CC} = 5,	T_A = 25°C	3	5	7	kΩ
r_o	Output resistance	T1OUT, T2OUT	V_{S+} = V_{S-} = 0,	V_O = ± 2 V	300			Ω
I_{OS}§	Short-circuit output current	T1OUT, T2OUT	V_{CC} = 5.5 V,	V_O = 0		±10		mA
I_{IS}	Short-circuit input current	T1IN, T2IN	V_I = 0				200	µA
I_{CC}	Supply current		V_{CC} = 5.5 V, T_A = 25°C	All outputs open,		8	10	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.

§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH(R)}$	Receiver propagation delay time, low- to high-level output	See Figure 2		500		ns
$t_{PHL(R)}$	Receiver propagation delay time, high- to low-level output	See Figure 2		500		ns
SR	Driver slew rate	R_L = 3 kΩ to 7 kΩ, See Figure 3			30	V/μs
SR(tr)	Driver transition region slew rate	See Figure 4		3		V/μs

APPLICATION INFORMATION

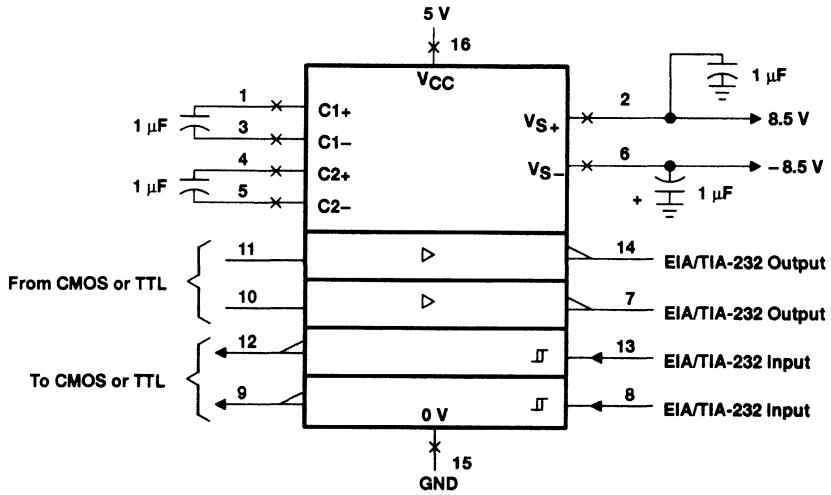
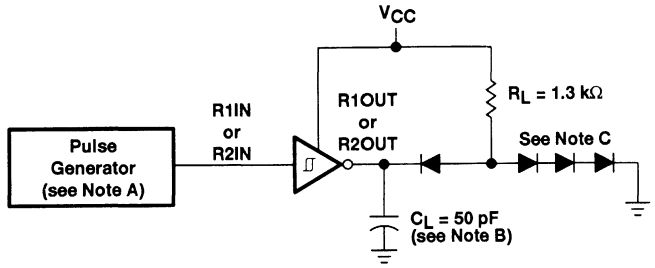
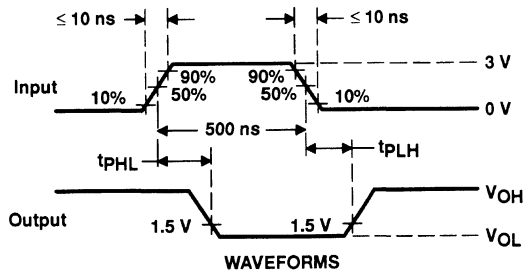


Figure 1. Typical Operating Circuit

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

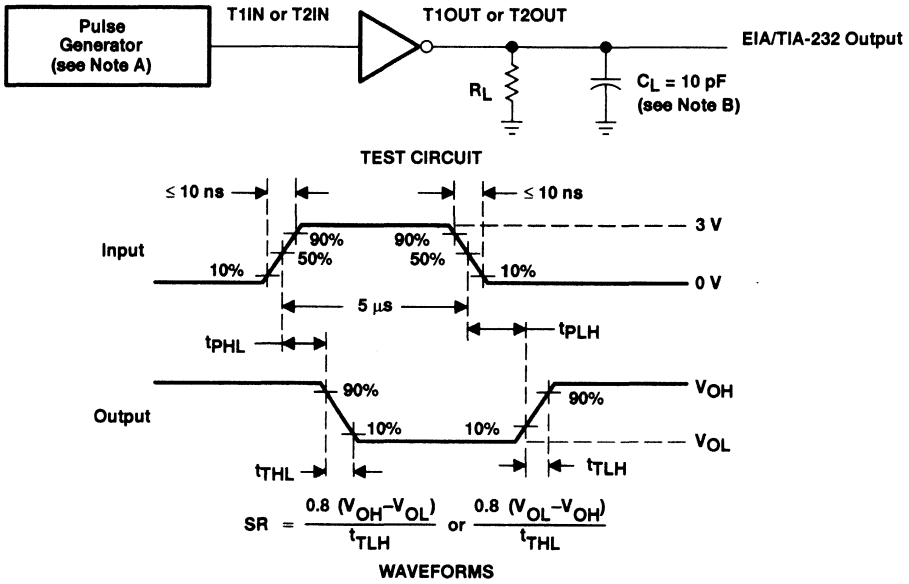


WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

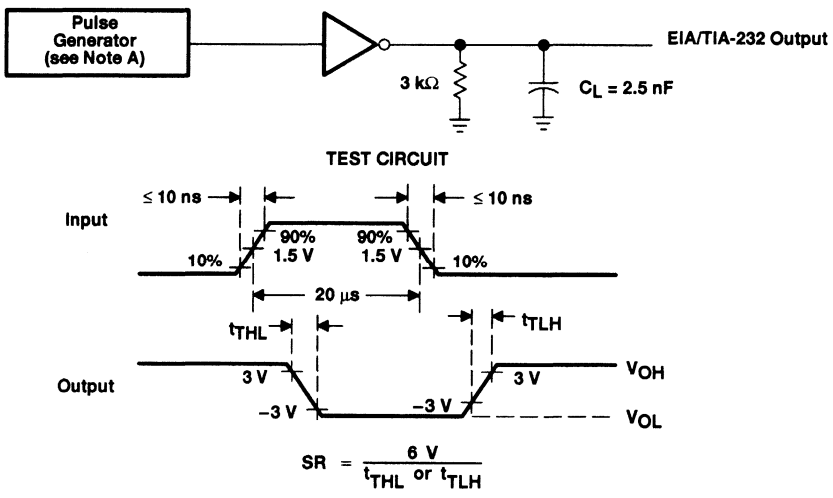
Figure 2. Receiver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurement

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurement (5-µs Input)



NOTE A: The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.

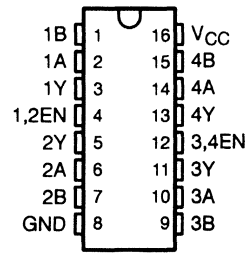
Figure 4. Test Circuit and Waveforms for t_{THL} and t_{TLH} Measurement (20-µs Input)

MC3486
QUADRUPLE DIFFERENTIAL LINE RECEIVER WITH 3-STATE OUTPUTS

SLLS097B – JUNE 1980 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-422-B and EIA/TIA-423-B and ITU Recommendations V.10 and V.11**
- **3-State, TTL-Compatible Outputs**
- **Fast Transition Times**
- **Operates From Single 5-V Supply**
- **Designed to Be Interchangeable With Motorola™ MC3486**

D OR N PACKAGE
(TOP VIEW)



description

The MC3486 is a monolithic quadruple differential line receiver designed to meet the specifications of ANSI Standards EIA/TIA-422-B and EIA/TIA-423-B and ITU Recommendations V.10 and V.11. The MC3486 offers four independent differential-input line receivers that have TTL-compatible outputs. The outputs utilize 3-state circuitry to provide a high-impedance state at any output when the appropriate output enable is at a low logic level.

The MC3486 is designed for optimum performance when used with the MC3487 quadruple differential line driver. It is supplied in a 16-pin package and operates from a single 5-V supply.

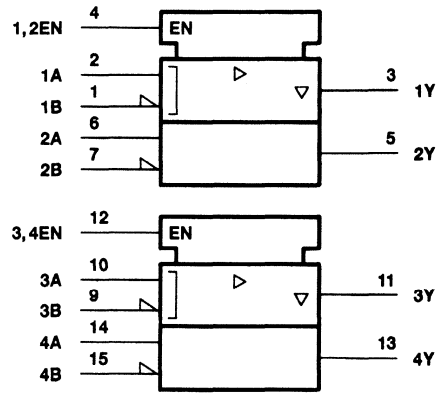
The MC3486 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A-B	ENABLE	OUTPUT Y
$V_{ID} \leq 0.2$ V	H	H
-0.2 V $< V_{ID} < 0.2$ V	H	?
$V_{ID} \leq -0.2$ V	H	L
Irrelevant	L	Z
Open	H	?

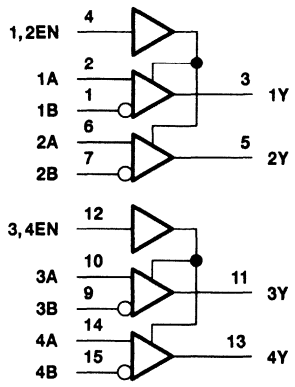
H = high level, L = low level, Z = high impedance (off), ? = indeterminate

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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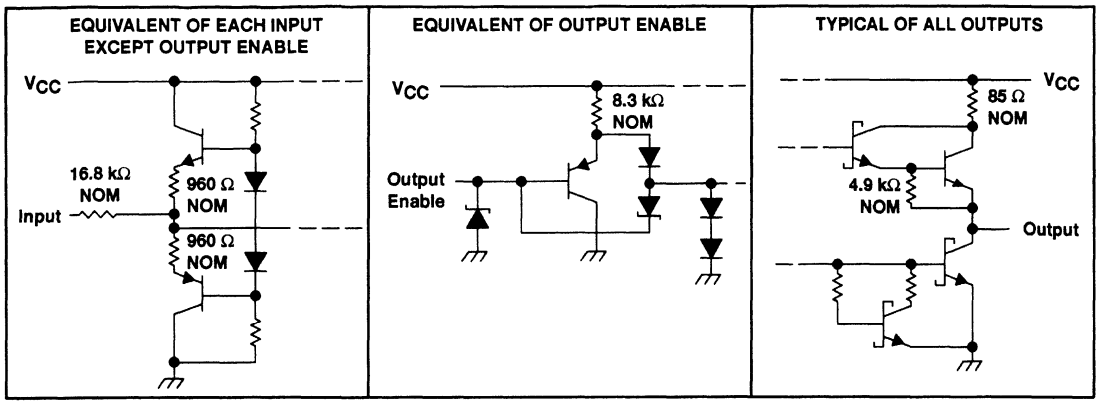
schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 8 V
Input voltage, V_I (A or B inputs) ..... ±15 V
Differential input voltage, V_{ID} (see Note 2) ..... ±25 V
Enable input voltage ..... 8 V
Low-level output current, I_{OL} ..... 50 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential-input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Differential input voltage, V_{ID}			±6	V
High-level enable input voltage, V_{IH}	2			V
Low-level enable input voltage, V_{IL}			0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{IT+}	Differential input high-threshold voltage	V_O = 2.7 V, I_O = −0.4 mA				0.2	V
V_{IT-}	Differential input low-threshold voltage	V_O = 0.5 V, I_O = −8 mA			−0.2†		V
V_{IK}	Enable-input clamp voltage	I_I = −10 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 0.4 V, I_O = −0.4 mA, See Note 3 and Figure 1			2.7		V
V_{OL}	Low-level output voltage	V_{ID} = −0.4 V, I_O = 8 mA, See Note 3 and Figure 1				0.5	V
I_{OZ}	High-impedance-state output current	V_{IL} = 0.8 V,	V_{ID} = −3 V,	V_O = 2.7 V		40	μA
		V_{IL} = 0.8 V,	V_{ID} = 3 V,	V_O = 0.5 V		−40	
I_{IB}	Differential-input bias current	V_{CC} = 0 V or 5.25 V, Other inputs at 0 V		V_I = −10 V		−3.25	mA
				V_I = −3 V		−1.5	
				V_I = 3 V		1.5	
				V_I = 10 V		3.25	
I_{IH}	High-level enable input current	V_I = 5.25 V				100	μA
		V_I = 2.7 V				20	
I_{IL}	Low-level enable input current	V_I = −0.5 V				−100	μA
I_{OS}	Short-circuit output current	V_{ID} = 3 V,	V_O = 0,	See Note 4	−15	−100	mA
I_{CC}	Supply current	V_{IL} = 0				85	mA

† The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet for threshold voltages only.

NOTES: 3. Refer to ANSI Standards EIA/TIA-422-B and EIA/TIA-423-B for exact conditions.
4. Only one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	See Figure 2		28	35	ns
t_{PLH}	Propagation delay time, low- to high-level output			27	30	ns
t_{PZH}	Output enable time to high level	See Figure 3		13	30	ns
t_{PZL}	Output enable time to low level			20	30	ns
t_{PHZ}	Output disable time from high level			26	35	ns
t_{PLZ}	Output disable time from low level			27	35	ns

PARAMETER MEASUREMENT INFORMATION

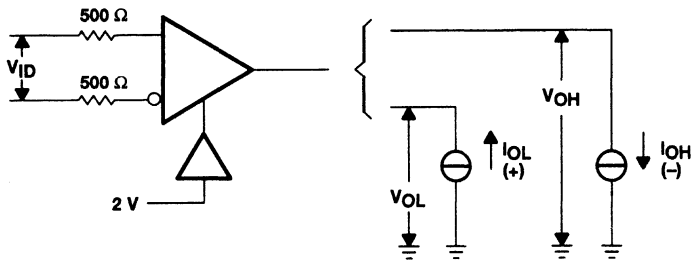


Figure 1. V_{OH}, V_{OL}

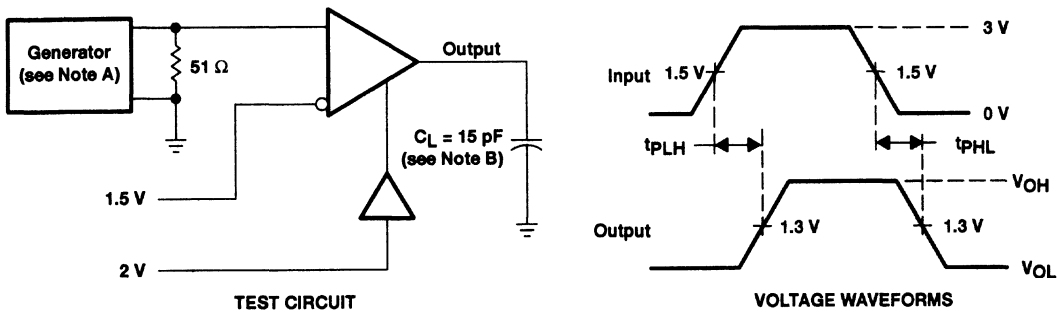


Figure 2. Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and stray capacitance.

PARAMETER MEASUREMENT INFORMATION

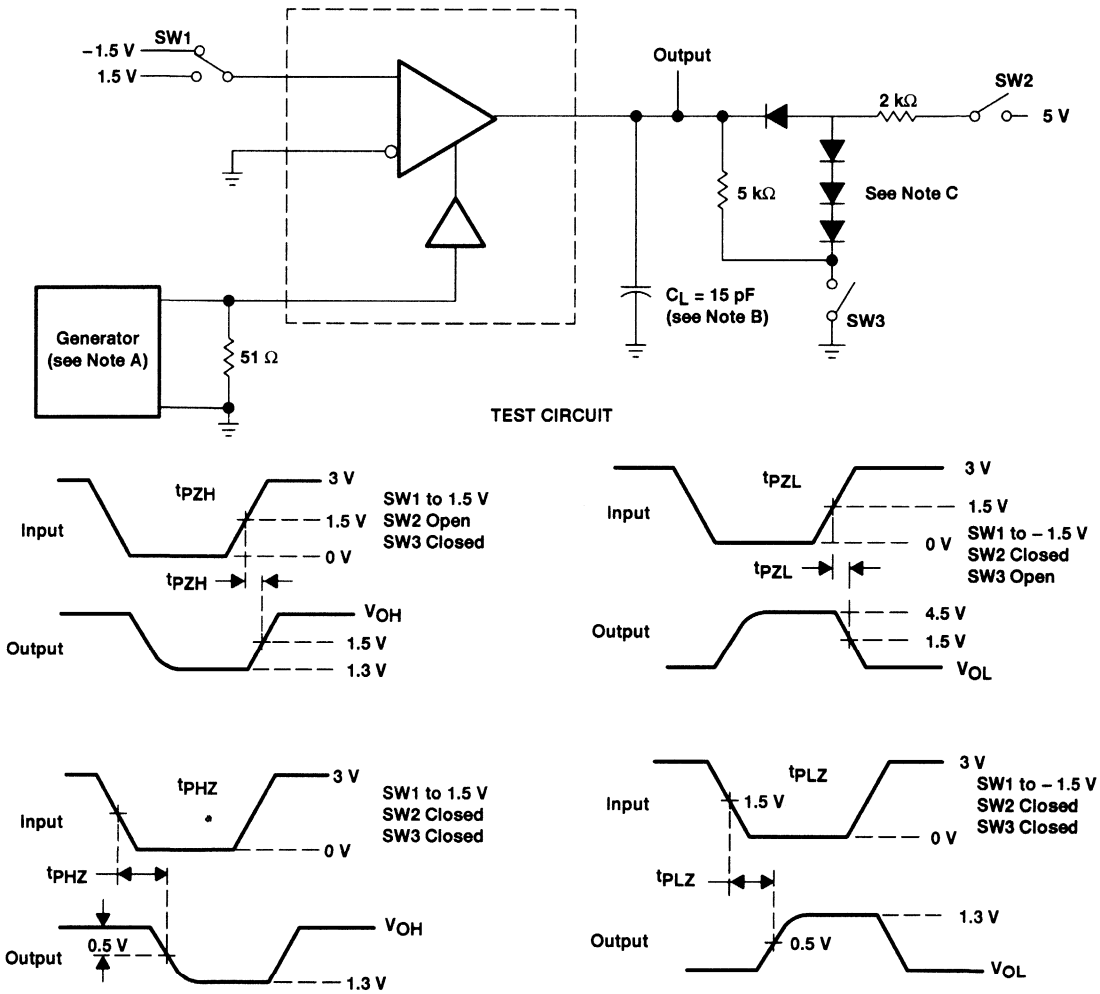
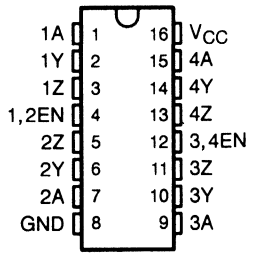


Figure 3. Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns.
B. C_L includes probe and stray capacitance.
C. All diodes are 1N916 or equivalent.

- **Meets or Exceeds Requirements of ANSI EIA/TIA-422-B and ITU Recommendation V.11**
- **3-State, TTL-Compatible Outputs**
- **Fast Transition Times**
- **High-Impedance Inputs**
- **Single 5-V Supply**
- **Power-Up and Power-Down Protection**
- **Designed to Be Interchangeable With Motorola MC3487**

D OR N PACKAGE
(TOP VIEW)



description

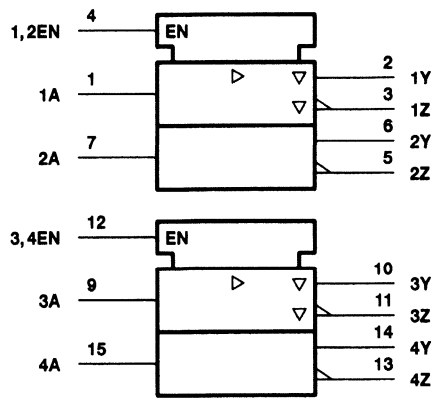
The MC3487 offers four independent differential line drivers designed to meet the specifications of ANSI EIA/TIA-422-B and ITU Recommendation V.11. Each driver has a TTL-compatible input buffered to reduce current and minimize loading.

The driver outputs utilize 3-state circuitry to provide high-impedance states at any pair of differential outputs when the appropriate output enable is at a low logic level. Internal circuitry is provided to ensure a high-impedance state at the differential outputs during power-up and power-down transition times provided the output enable is low. The outputs are capable of source or sink currents of 48 mA.

The MC3487 is designed for optimum performance when used with the MC3486 quadruple line receiver. It is supplied in a 16-pin dual-in-line package and operates from a single 5-V supply.

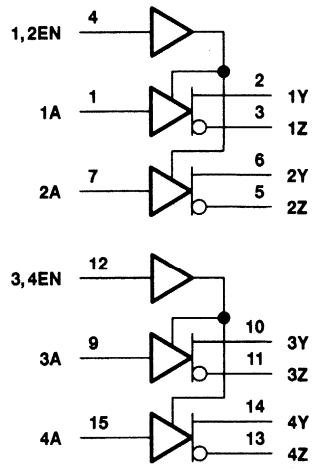
The MC3487 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

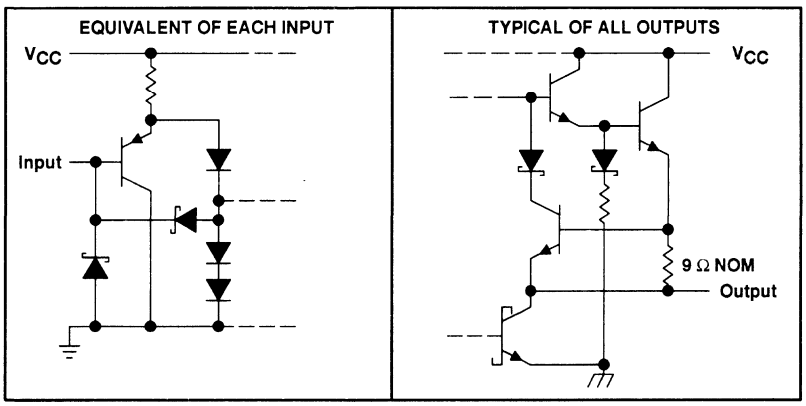


FUNCTION TABLE
(each driver)

INPUT	OUTPUT ENABLE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = TTL high level, L = TTL low level, X = irrelevant, Z = High impedance

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 8 V
Input voltage, V_I ..... 5.5 V
Output voltage, V_O ..... 7 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential output voltage, V_{OD}, are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{IL} = 0.8 V,	V_{IH} = 2 V,	I_{OH} = −20 mA	2.5		V
V_{OL}	Low-level output voltage	V_{IL} = 0.8 V,	V_{IH} = 2 V,	I_{OL} = 48 mA		0.5	V
$\lvert V_{OD}\rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 1		2		
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage†	R_L = 100 Ω,	See Figure 1			±0.4	V
V_{OC}	Common-mode output voltage‡	R_L = 100 Ω,	See Figure 1			3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage†	R_L = 100 Ω,	See Figure 1			±0.4	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V			100	µA
			V_O = −0.25 V			−100	
I_{OZ}	High-impedance-state output current	Output enables at 0.8 V	V_O = 2.7 V			100	µA
			V_O = 0.5 V			−100	
I_I	Input current at maximum input voltage	V_I = 5.5 V				100	µA
I_{IH}	High-level input current	V_I = 2.7 V				50	µA
I_{IL}	Low-level input current	V_I = 0.5 V				−400	µA
I_{OS}	Short-circuit output current§	V_I = 2 V			−40	−140	mA
I_{CC}	Supply current (all drivers)	Outputs disabled				105	mA
		Outputs enabled,	No load			85	

† $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

‡ In ANSI Standard EIA/TIA-422-B, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

§ Only one output at a time should be shorted, and duration of the short circuit should not exceed one second.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 15 pF,	See Figure 2		20	ns
t_{PHL}	Propagation delay time, high- to low-level output				20	ns
	Skew time				6	ns
$t_{t(OD)}$	Differential-output transition time	C_L = 15 pF,	See Figure 3		20	ns
t_{PZH}	Output enable time to high level	C_L = 50 pF,	See Figure 4		30	ns
t_{PZL}	Output enable time to low level				30	ns
t_{PHZ}	Output disable time from high level				25	ns
t_{PLZ}	Output disable time from low level				30	ns

PARAMETER MEASUREMENT INFORMATION

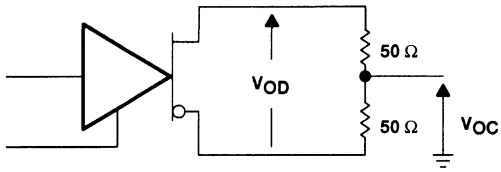


Figure 1. Differential and Common-Mode Output Voltages

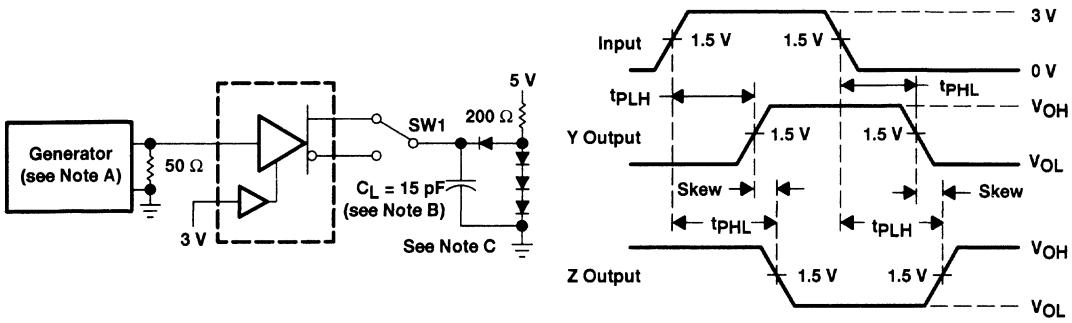


Figure 2. Test Circuit and Voltage Waveforms

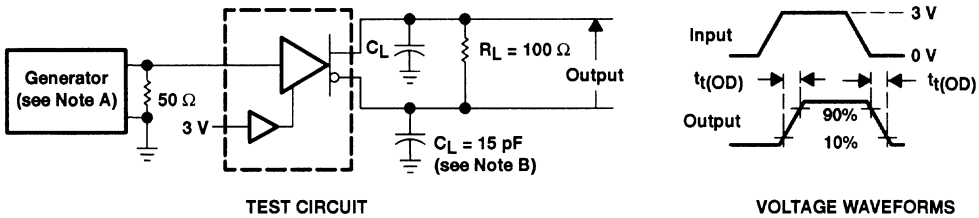
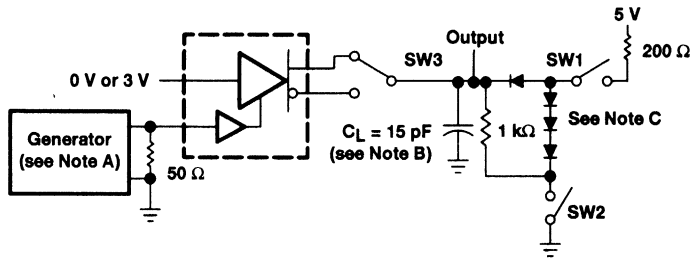


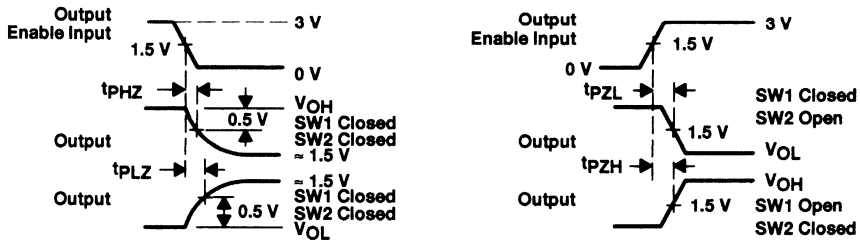
Figure 3. Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \le 5$ ns, $t_f \le 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50\ \Omega$.
B. C_L includes probe and stray capacitance.
C. All diodes are 1N916 or 1N3064.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

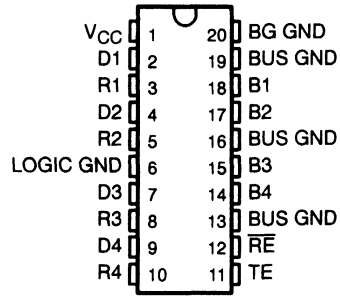
Figure 4. Driver Test Circuit and Voltage Waveforms

NOTES: D. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50\ \Omega$.
E. C_L includes probe and stray capacitance.
F. All diodes are 1N916 or 1N3064.

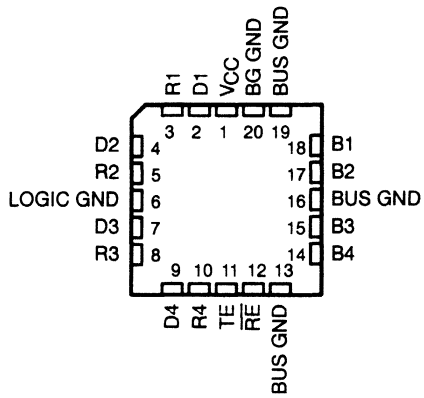
SLLS034B – JANUARY 1988 – REVISED MAY 1995

- **High-Speed Quadruple Transceiver**
- **Meets or Exceeds Requirements of IEEE Std. 896.1 – 1987**
- **Drives Load Impedances as Low as 10 Ω**
- **High-Speed Advanced Low-Power Schottky Circuits**
- **Low Power Dissipation . . . 81 mW Max per Channel**
- **High-Impedance PNP Inputs**
- **BTL™ Logic Level 1-V Bus Swing Reduces Power Consumption**
- **Low Bus-Port Capacitance**
- **Power-Up/Power-Down Protection (Glitch Free)**
- **Open-Collector Driver Outputs Allows Wired-OR Connections**
- **Multiple Bus Channel Ground Returns to Reduce Channel Noise Interference**
- **Designed to be a Faster, Lower Power Functional Equivalent of the National Semiconductor DS3893**

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The SN75ALS053 is a four-channel, monolithic, high-speed, advanced low-power Schottky device designed for two-way data communication in a densely populated backplane. The SN75ALS053 has independent driver input (Dn) and receiver output (Rn) pins and separate driver and receiver disables. This transceiver is designed for use in high-speed bus systems and is similar to the SN75ALS057 transceiver except that the trapezoidal feature has been eliminated to speed up the propagation delays.

These transceivers feature open-collector driver outputs, each with a series Schottky diode to reduce capacitive loading to the bus. By using a 2-V pullup on the bus, the output signal swing will be approximately 1 V, which reduces the power necessary to drive the bus load capacitance. The driver outputs are capable of driving an equivalent dc load of as low as 10 Ω.

The receivers have a precision threshold set by an internal bandgap reference to give accurate input thresholds over V_{CC} and temperature variations.

These transceivers are compatible with Backplane Transceiver Logic (BTL™) technology at significantly reduced power dissipation per channel.

The SN75ALS053 is characterized for operation from 0° to 70°C.

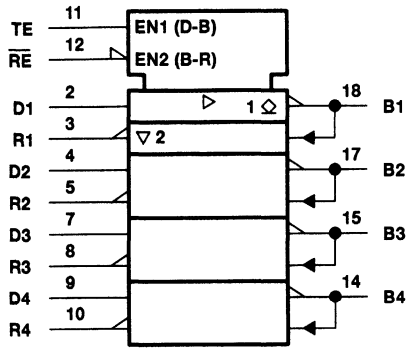
BTL and DS3893 are trademarks of National Semiconductor Corporation.

FUNCTION TABLE
TRANSMIT/RECEIVE

CONTROLS		CHANNELS	
TE	$\overline{RE}$	D→B	B→R
L	L	D	R
L	H	D	D
H	L	T	R
H	H	T	D

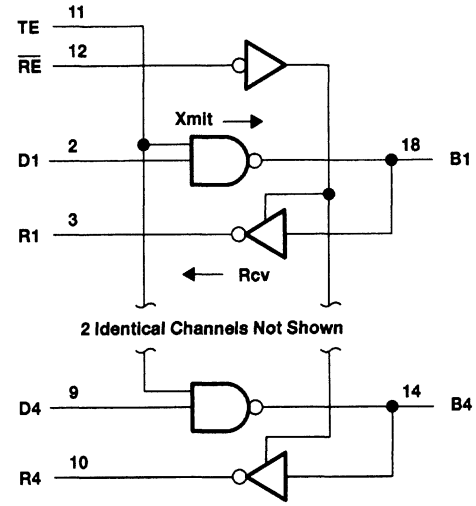
H = high level, L = low level, R = receive,
T = transmit, D = disable
Direction of data transmission is from Dn to Bn, direction of data reception is from Bn to Rn.

logic symbol†

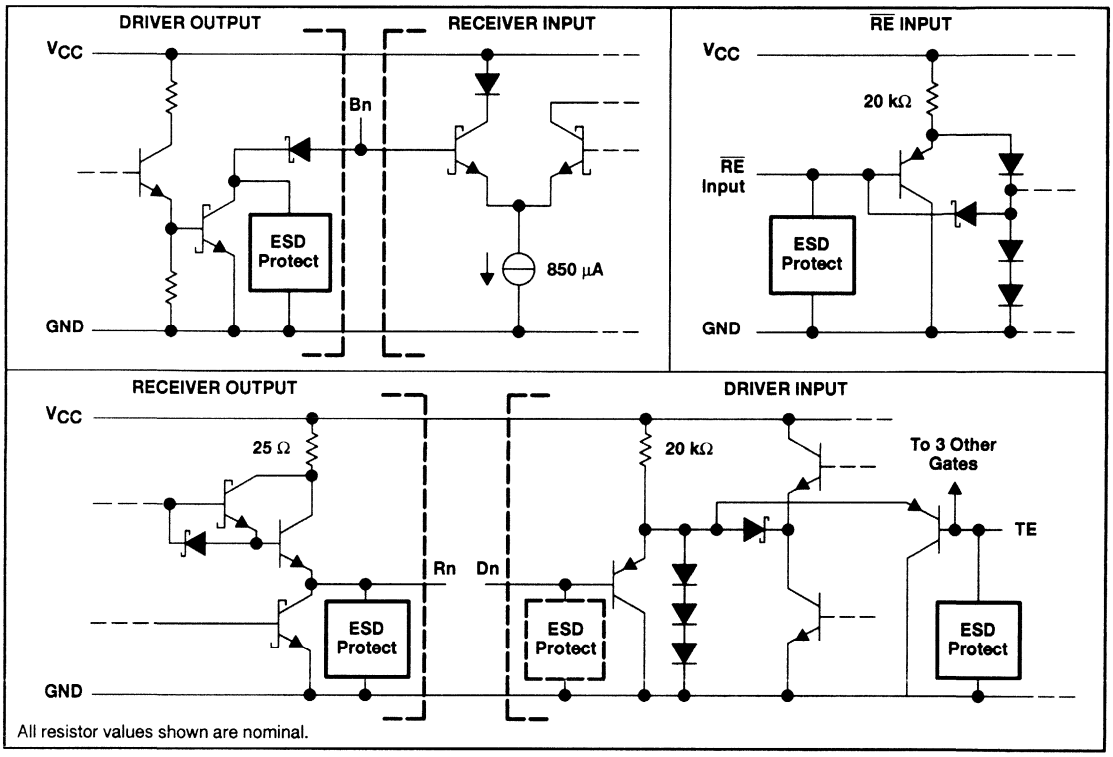


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	6 V
Control input voltage, V_I	5.5 V
Driver input voltage, V_I	5.5 V
Driver output voltage, V_O	2.5 V
Receiver input voltage, V_I	2.5 V
Receiver output voltage, V_O	5.5 V
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	– 65°C to 150°C
Case temperature for 10 seconds, T_C: FN package	260°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds: N package	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
FN	1400 MW	11.2 MW/°C	896 MW
N	1150 MW	9.2 MW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level driver and control input voltage, V_{IH}	2			V
Low-level driver and control input voltage, V_{IL}			0.8	V
Bus termination voltage	1.9		2.1	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage at Dn, DE, or $\overline{RE}$		$I_I = -18$ mA			−1.5	V
V_{IT}	Receiver input threshold voltage at Bn			1.426		1.674	V
V_{OH}	High-level output voltage at Rn		Bn at 1.2 V, $\overline{RE}$ at 0.8 V, $I_{OH} = -1$ mA	2.5			V
V_{OL}	Low-level output voltage	Rn	Bn at 2 V, $\overline{RE}$ at 0.8 V, $I_{OL} = 20$ mA			0.5	V
		Bn	Dn at 2.4 V, TE at 2.4 V, See Figure 1, $V_L = 2$ V, $R_L = 10\ \Omega$	0.75		1.2	
I_{IH}	High-level input current	Dn, TE or $\overline{RE}$	$V_I = V_{CC}$			40	µA
		Bn	$V_I = 2$ V, $V_{CC} = 0$ or 5.25 V, Dn at 0.8 V, TE at 0.8 V			100	
I_{IL}	Low-level input current at Dn, TE or $\overline{RE}$		$V_I = 0.4$ V			−400	µA
I_{OS}	Short-circuit output at Rn		Rn at 0 V, Bn at 1.2 V, $\overline{RE}$ at 0.8 V	−70		−200	mA
I_{CC}	Supply current					65	mA
$C_{o(B)}$	Driver output capacitance		$V_{CC} = 5$ V, $T_A = 25°C$		6.5		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

driver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time low-to-high-level output	Dn	Bn	TE at 3 V, V_L = 2 V, See Figure 2	2	7	ns
t_{PHL}	Propagation delay time high-to-low-level output				2	7	
t_{PLH}	Propagation delay time low-to-high-level output	Dn	Bn	Dn at 3 V, V_L = 2 V, See Figure 2	2	7	ns
t_{PHL}	Propagation delay time high-to-low-level output				2	7	
t_{TLH}	Transition time, low-to-high-level output	Dn	Bn	TE at 3 V, V_L = 2 V, See Figure 2	0.5	5	ns
t_{THL}	Transition time, high-to-low-level output				0.5	5	
	Skew between driver channels†	Dn	Bn	TE at 3 V, V_L = 2 V		1	ns

receiver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Bn	Rn	$\overline{RE}$ at 0.3 V, TE at 0.3 V	2	8	ns
t_{PHL}	Propagation delay time, high-to-low-level output				2	8	
t_{PLZ}	Output disable time from low level	$\overline{RE}$	Rn	Bn at 2 V, TE at 0.3 V, V_L = 5 V, C_L = 5 pF, R_L1 = 500 Ω, See Figure 4		6	ns
t_{PZL}	Output enable time to low level	$\overline{RE}$	Rn	Bn at 2 V, TE at 0.3 V, V_L = 5 V, C_L = 5 pF, R_L1 = 500 Ω, See Figure 4		12	ns
t_{PHZ}	Output disable time from high level	$\overline{RE}$	Rn	Bn at 1 V, TE at 0.3 V, V_L = 0, C_L = 5 pF, R_L1 = 500 Ω, See Figure 4		6	ns
t_{PZH}	Output enable time to high level	$\overline{RE}$	Rn	Bn at 1 V, TE at 0.3 V, V_L = 0, C_L = 5 pF, R_L1 = 500 Ω, See Figure 4		12	ns
	Skew between receiver channels†	Bn	Rn	$\overline{RE}$ at 0.3 V, TE at 0.3 V		1	ns

† Skew is the difference between the propagation delay time (t_{PLH} or t_{PHL}) of one receiver channel and that same propagation delay time of any other receiver channel. It applies for both t_{PLH} and t_{PHL}.

PARAMETER MEASUREMENT INFORMATION

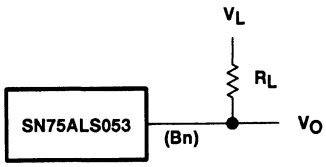
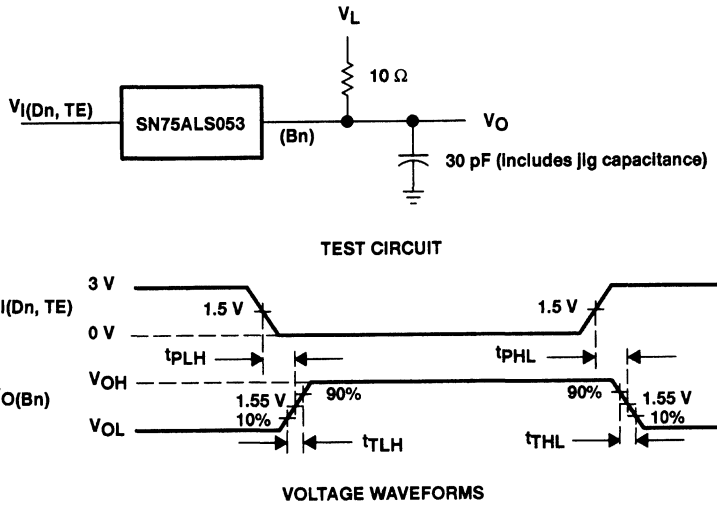


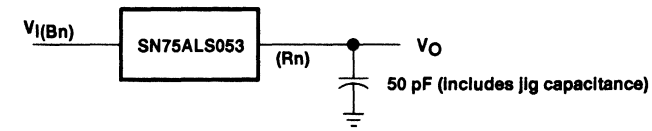
Figure 1. Driver Low-Level-Output-Voltage Test Circuit



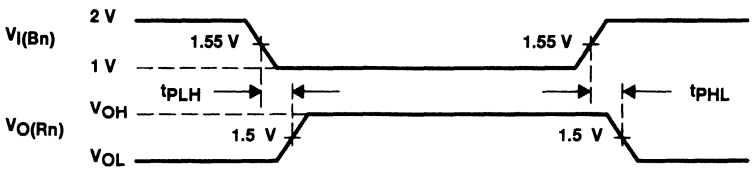
NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%

Figure 2. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



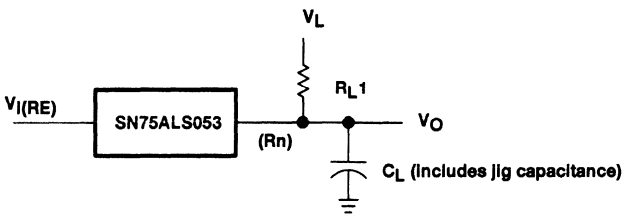
TEST CIRCUIT



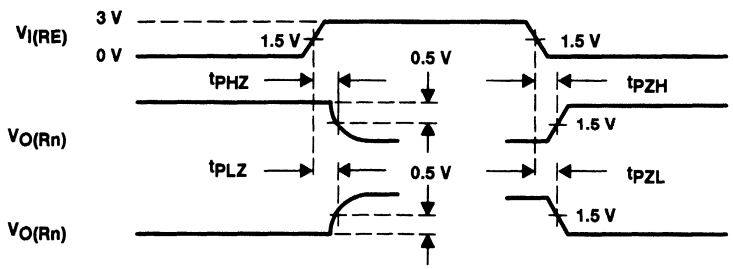
VOLTAGE WAVEFORMS

NOTE: $t_r = t_f \leq 10$ ns from 10% to 90%

Figure 3. Receiver Test Circuit and Voltage Waveforms



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%

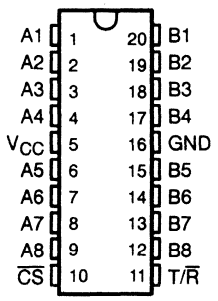
Figure 4. Test Circuit and Voltage Waveforms From $\overline{RE}$ to Rn

SLLS028E – AUGUST 1987 – REVISED MAY 1995

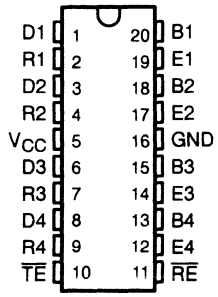
SUITABLE FOR IEEE STANDARD 896 APPLICATIONS†

- SN55ALS056 and SN75ALS056 are Octal Transceivers
- SN55ALS057 and SN75ALS057 are Quad Transceivers
- High-Speed Advanced Low-Power Schottky (ALS) Circuitry
- Low Power Dissipation:
  SN55' Devices . . . 60 mW/Channel Max
  SN75' Devices . . . 52.5 mW/Channel Max
- High-Impedance pnp Inputs
- Logic-Level 1-V Bus Swing Reduces Power Consumption
- Trapezoidal Bus Output Waveform Reduces Noise Coupling to Adjacent Lines
- Power-Up/Power-Down Protection (Glitch Free)
- Open-Collector Driver Outputs Allow Wired-OR Connections
- Designed to Be a Faster, Lower-Power Functional Equivalent of National DS3896, DS3897

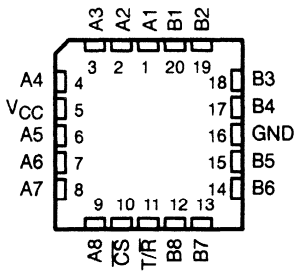
SN55ALS056 . . . J OR W PACKAGE
SN75ALS056 . . . DW OR N PACKAGE
(TOP VIEW)



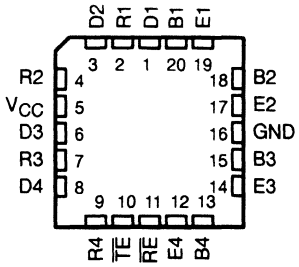
SN55ALS057 . . . J OR W PACKAGE
SN75ALS057 . . . DW OR N PACKAGE
(TOP VIEW)



SN55ALS056 . . . FK PACKAGE
(TOP VIEW)



SM55ALS057 . . . FK PACKAGE
(TOP VIEW)



† The transceivers are suitable for IEEE Standard 896 applications to the extent of the operating conditions and characteristics specified in this data sheet. Certain limits contained in the IEEE specification are not met or cannot be tested over the entire military temperature range.

SLLS028E – AUGUST 1987 – REVISED MAY 1995

description

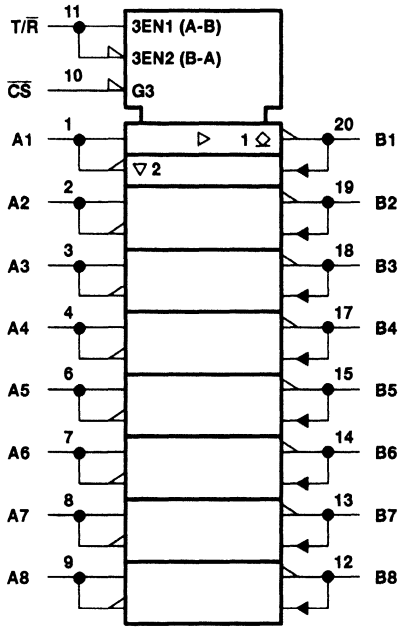
The SN55ALS056 and SN75ALS056 are 8-channel, monolithic, high-speed, advanced low-power Schottky (ALS) devices designed for 2-way data communication in a densely populated backplane. The SN55ALS057 and SN75ALS057 are 4-channel versions with independent driver-input (Dn) and receiver-output (Rn) pins and a separate driver disable for each driver (En).

These transceivers feature open-collector driver outputs with series Schottky diodes to reduce capacitive loading to the bus. By using a 2-V pullup termination on the bus, the output signal swing is approximately 1 V, which reduces the power necessary to drive the bus load capacitance. The driver outputs generate trapezoidal waveforms that reduce crosstalk between channels. The drivers are capable of driving an equivalent dc load as low as 18.5 Ω. The receivers have internal low-pass filters to further improve noise immunity.

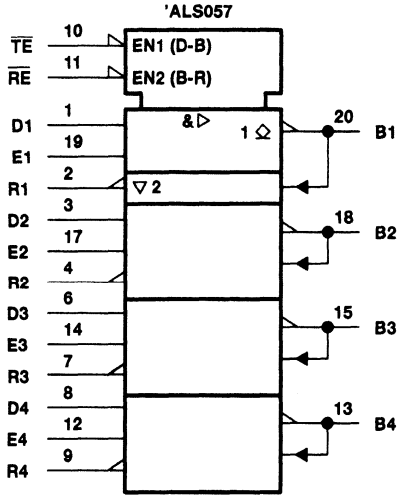
The SN55ALS056 and SN55ALS057 are characterized over the full military operating range of –55°C to 125°C. The SN75ALS056 and SN75ALS057 are characterized for operation from 0°C to 70°C.

logic symbols†

'ALS056

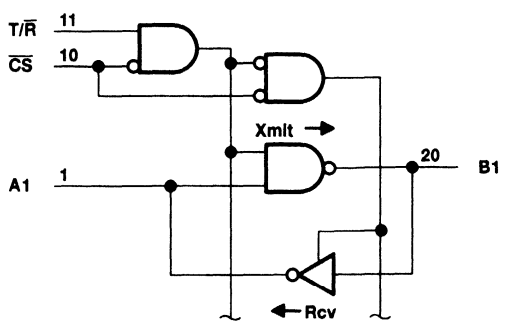


'ALS057

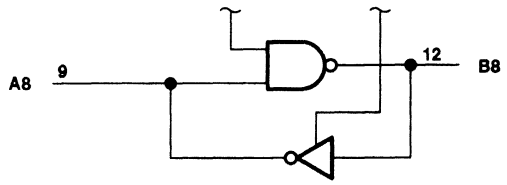


logic diagrams (positive logic)

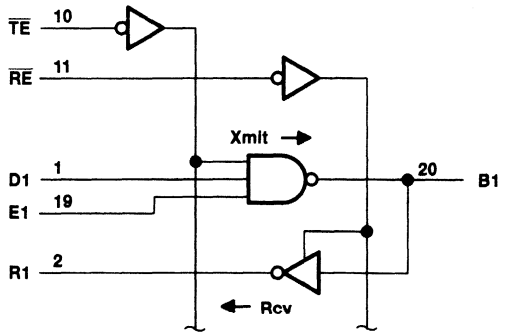
'ALS056



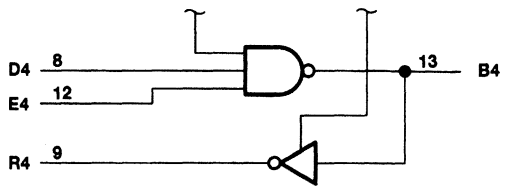
6 Identical Channels Not Shown



'ALS057



2 Identical Channels Not Shown



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Function Tables

'ALS056 TRANSMIT/RECEIVE

CONTROLS		CHANNELS
$\overline{CS}$	T/$\overline{R}$	A ↔ B
L	H	T (A → B)
L	L	R (B → A)
H	X	D

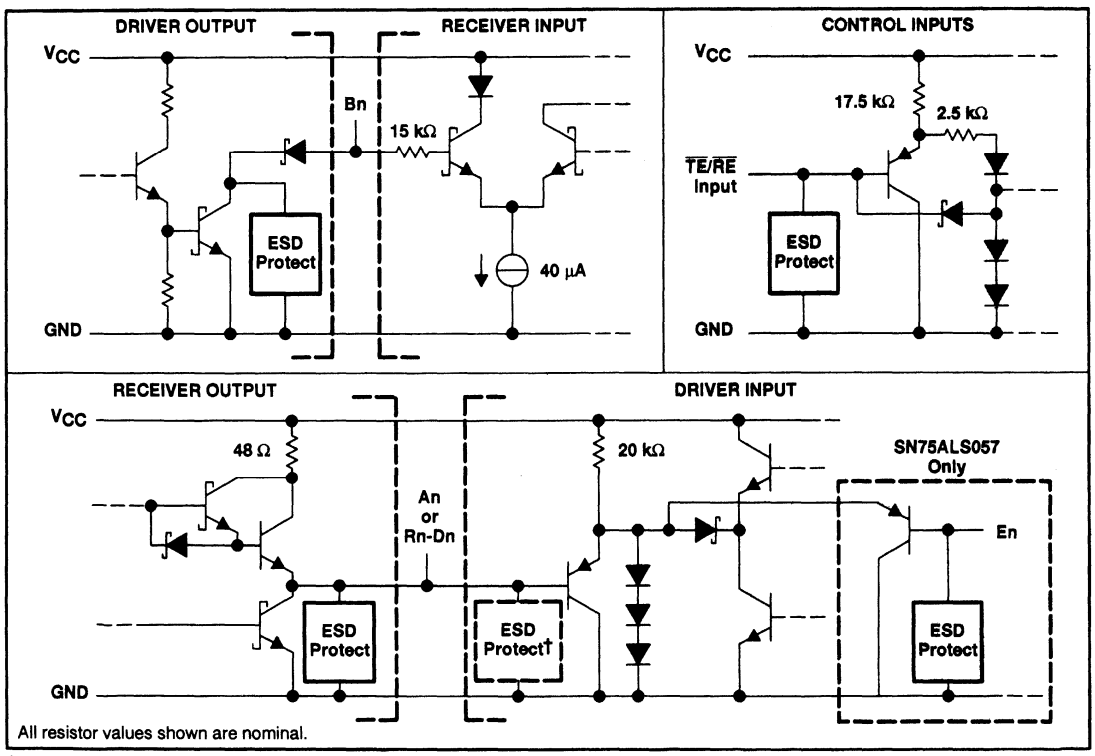
'ALS057 TRANSMIT/RECEIVE

CONTROLS			CHANNELS	
$\overline{TE}$	$\overline{RE}$	En	D → B	B → R
L	L	L	D	R
L	L	H	T	R
L	H	L	D	D
L	H	H	T	D
H	L	X	D	R
H	H	X	D	D

H = high level, L = low level, R = receive, T = transmit, D = disable, X = irrelevant

Direction of data transmission is from An to Bn for the 'ALS056 and from Dn to Bn for the 'ALS057. Direction of data reception is from Bn to An for the 'ALS056 and from Bn to Rn for the 'ALS057. Data transfer is inverting in both directions.

schematics of inputs and outputs



† Additional ESD protection is on the 'ALS057, which has separate receiver-output and driver-input pins.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 6 V
Control input voltage, V_I ..... 5.5 V
Driver input voltage, V_I ..... 5.5 V
Driver output voltage, V_O ..... 2.5 V
Receiver input voltage, V_I ..... 2.5 V
Receiver output voltage, V_O ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN55ALS05_ ..... −55°C to 125°C
SN75ALS05_ ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Case temperature for 60 seconds, T_C: FK package ..... 300 °C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package ..... 260 °C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package ..... 300 °C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—
J	1375 mW	11.0 mW/°C	880 mW	275 mW
W	1000 mW	8.0 mW/°C	640 mW	200 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	SN55ALS05_	4.5	5	5.5	V
	SN75ALS05_	4.75	5	5.25	
High-level driver and control input voltage, V_{IH}		2			V
Low-level driver and control input voltage, V_{IL}				0.8	V
Bus termination voltage		1.9		2.1	V
Operating free-air temperature, T_A	SN55ALS05_	−55		125	°C
	SN75ALS05_	0		70	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

SN55ALS056

PARAMETER			TEST CONDITIONS†		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage at An, T/$\overline{R}$, or $\overline{CS}$		V_{CC} = 4.5 V,	I_I = –18 mA			–1.5	V
V_{IT}	Receiver input threshold voltage at Bn		V_{CC} = 5 V,	T_A = 25°C	1.43		1.69	V
			V_{CC} = 5 V,	T_A = –55°C to 125°C	1.4		1.7	
V_{OH}	High-level output voltage at An		V_{CC} = 4.5 V, $\overline{CS}$ at 0.8 V, I_{OH} = – 400 µA	Bn at 1.2 V, T/$\overline{R}$ at 0.8 V,	2.4			V
V_{OL}	Low-level output voltage	An	V_{CC} = 4.5 V, $\overline{CS}$ at 0.8 V, I_{OL} = 16 mA	Bn at 2 V, T/$\overline{R}$ at 0.8 V,			0.5	V
		Bn	V_{CC} = 4.5 V, $\overline{CS}$ at 0.8 V, See Figure 1	An at 2 V, T/$\overline{R}$ at 2 V,	0.75		1.2	
I_{IH}	High-level input current	An, T/$\overline{R}$ or $\overline{CS}$	V_I = V_{CC} = 5.5 V				40	µA
		Bn	V_{CC} = 5.5 V, An at 0.8 V,	V_I = 2 V, T/$\overline{R}$ at 0.8 V			100	
I_{IL}	Low level input current at An, T/$\overline{R}$, or $\overline{CS}$		V_{CC} = 5.5 V,	V_I = 0.4 V			–400	µA
I_{OS}	Short-circuit output current at An		V_{CC} = 5.5 V, Bn at 1.2 V, T/$\overline{R}$ at 0.8 V	An at 0, $\overline{CS}$ at 0.8 V,	–35		–125	mA
I_{CC}	Supply current		V_{CC} = 5.5 V				85	mA
$C_{O(B)}$	Driver output capacitance					4.5		pF

SN75ALS056

PARAMETER			TEST CONDITIONS†		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage at An, T/$\overline{R}$, or $\overline{CS}$		I_I = –18 mA				–1.5	V
V_{IT}	Receiver input threshold voltage at Bn				1.405		1.69	V
V_{OH}	High-level output voltage at An		Bn at 1.2 V, T/$\overline{R}$ at 0.8 V,	$\overline{CS}$ at 0.8 V, I_{OH} = – 400 µA	2.4			V
V_{OL}	Low-level output voltage	An	Bn at 2 V, T/$\overline{R}$ at 0.8 V,	$\overline{CS}$ at 0.8 V, I_{OL} = 16 mA			0.5	V
		Bn	An at 2 V, T/$\overline{R}$ at 2 V, R_L = 18.5 Ω,	$\overline{CS}$ at 0.8 V, V_L = 2 V, See Figure 1	0.75		1.2	
I_{IH}	High-level input current	An, T/$\overline{R}$ or $\overline{CS}$	V_I = V_{CC}				40	µA
		Bn	V_I = 2 V, An at 0.8 V,	V_{CC} = 0 or 5.25 V, T/$\overline{R}$ at 0.8 V			100	
I_{IL}	Low level input current at An, T/$\overline{R}$, or $\overline{CS}$		V_I = 0.4 V				–400	µA
I_{OS}	Short-circuit output current at An		An at 0, $\overline{CS}$ at 0.8 V,	Bn at 1.2 V, T/$\overline{R}$ at 0.8 V	–40		–120	mA
I_{CC}	Supply current						75	mA
$C_{O(B)}$	Driver output capacitance					4.5		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

SN55ALS057

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage at Dn, En, $\overline{TE}$, or $\overline{RE}$		V_{CC} = 4.5 V,	I_I = –18 mA			–1.5	V
V_{IT}	Receiver input threshold voltage at Bn		V_{CC} = 5 V,	T_A = 25°C	1.43		1.69	V
			V_{CC} = 5 V,	T_A = –55°C to 125°C	1.4		1.7	
V_{OH}	High-level output voltage at Rn		V_{CC} = 4.5 V, $\overline{RE}$ at 0.8 V,	Bn at 1.2 V, I_{OH} = – 400 µA	2.4			V
V_{OL}	Low-level output voltage	Rn	V_{CC} = 4.5 V, $\overline{RE}$ at 0.8 V,	Bn at 2 V, I_{OL} = 16 mA			0.5	V
		Bn	V_{CC} = 4.5 V, En at 2 V, See Figure 1	Dn at 2 V, $\overline{TE}$ at 0.8 V,	0.75		1.2	
I_{IH}	High-level input current	Dn, En, $\overline{TE}$, or $\overline{RE}$	V_I = V_{CC} = 5.5 V				40	µA
		Bn	V_{CC} = 5.5 V, Dn at 0.8 V, $\overline{TE}$ at 0.8 V	V_I = 2 V, En at 0.8 V,			100	
I_{IL}	Low-level input current at Dn, En, $\overline{TE}$, or $\overline{RE}$		V_{CC} = 5.5 V,	V_I = 0.4 V			– 400	µA
I_{OS}	Short-circuit output current at Rn		V_{CC} = 5.5 V, Bn at 1.2 V,	Rn at 0, $\overline{RE}$ at 0.8 V	– 435		– 125	mA
I_{CC}	Supply current		V_{CC} = 5.5 V				45	mA
$C_{O(B)}$	Driver output capacitance					4.5		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

SN75ALS057

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage at Dn, En, $\overline{TE}$, or $\overline{RE}$		I_I = –18 mA				–1.5	V
V_{IT}	Receiver input threshold voltage at Bn				1.41		1.69	V
V_{OH}	High-level output voltage at Rn		Bn at 1.2 V, I_{OH} = – 400 µA	$\overline{RE}$ at 0.8 V,	2.4			V
V_{OL}	Low-level output voltage	Rn	Bn at 2 V, I_{OL} = 16 mA	$\overline{RE}$ at 0.8 V,			0.5	V
		Bn	Dn at 2 V, $\overline{TE}$ at 0.8 V, R_L = 18.5 Ω,	En at 2 V, V_L = 2 V, See Figure 1	0.75		1.2	
I_{IH}	High-level input current	Dn, En, $\overline{TE}$, or $\overline{RE}$	V_I = V_{CC}				40	µA
		Bn	V_I = 2 V, Dn at 0.8 V, $\overline{TE}$ at 0.8 V	V_{CC} = 0 or 5.25 V, En at 0.8 V,			100	
I_{IL}	Low-level input current at Dn, En, $\overline{TE}$, or $\overline{RE}$		V_I = 0.4 V				– 400	µA
I_{OS}	Short-circuit output current at Rn		Rn at 0, $\overline{RE}$ at 0.8 V	Bn at 1.2 V,	– 40		– 120	mA
I_{CC}	Supply current						40	mA
$C_{O(B)}$	Driver output capacitance					4.5		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

SN55ALS056 driver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		T_A†	MIN	TYP‡	MAX	UNIT
t_{PLH1}	Propagation delay time, low-to-high-level input	$\overline{CS}$	Bn	An and T/$\overline{R}$ at 2 V, R_L1 = 18 Ω, C_L = 50 pF,	V_L = 2 V, R_L2 = 500 Ω, See Figure 2	25°C			18	ns
						Full range			30	
t_{PHL1}	Propagation delay time, high-to-low-level input					25°C			20	
						Full range			22	
t_{PLH2}	Propagation delay time, low-to-high-level input	An	Bn	$\overline{CS}$ at 0.8 V, V_L = 2 V, R_L2 = 500 Ω, See Figure 2	T/$\overline{R}$ at 2 V, R_L1 = 18 Ω, C_L = 50 pF,	25°C			10	ns
						Full range			40	
t_{PHL2}	Propagation delay time high-to-low-level input					25°C			12	
						Full range			15	
t_{PLH2}	Propagation delay time, high-to-low-level input	An	Bn	$\overline{CS}$ at 0.8 V, R_L1 = 18 Ω, C_L = 50 pF, See Figure 2	T/$\overline{R}$ at 2 V, R_L2 = 500 Ω, V_L = 2 V,	25°C	1	3	10	ns
						Full range	1		13	
t_{PHL2}	Propagation delay time, low-to-high-level input					25°C	1	3	8	ns
						Full range	1		33	ns
t_{PLH3}	Propagation delay time, low-to-high-level input	T/$\overline{R}$	Bn	$\overline{CS}$ at 0.8 V, R_L1 = 18 Ω, C_L = 50 pF,	V_L = 2 V, R_L2 = 500 Ω, See Figure 3	25°C			18	ns
						Full range			37	
t_{PHL3}	Propagation delay time, high-to-low-level input					25°C			18	
						Full range			21	

SN75ALS056 driver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP§	MAX	UNIT
t_{PLH1}	Propagation delay time, low-to-high-level output	$\overline{CS}$	Bn	An and T/$\overline{R}$ at 2 V, R_L1 = 18 Ω, R_L2 not connected,	V_L = 2 V, C_L = 30 pF, See Figure 2			24	ns
t_{PHL1}	Propagation delay time, high-to-low-level output							20	
t_{PLH2}	Propagation delay time, low-to-high-level output	An	Bn	$\overline{CS}$ at 0.8 V, V_L = 2 V, R_L2 not connected, See Figure 2	T/$\overline{R}$ at 2 V, R_L1 = 18 Ω, C_L = 30 pF,			19	ns
t_{PHL2}	Propagation delay time high-to-low-level output							18	
t_{PLH3}	Propagation delay time, low-to-high-level output	T/$\overline{R}$	Bn	$V_{I(An)}$ = 5 V, R_L1 = 18 Ω, R_L2 not connected, See Figure 3	$\overline{CS}$ at 0.8 V, C_L = 30 pF, V_L = 2 V,			25	ns
t_{PHL3}	Propagation delay time, high-to-low-level output							35	
t_{TLH}	Transition time, low-to-high-level output	An	Bn	$\overline{CS}$ at 0.8 V, V_L = 2 V, R_L1 = 18 Ω, See Figure 2	T/$\overline{R}$ at 2 V, C_L = 30 pF, R_L2 not connected,	1	3	11	ns
t_{THL}	Transition time, high-to-low-level output					1	3	6	

† Full range is −55°C to 125°C.
‡ Typical values are at V_{CC} = 5 V.
§ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

SN55ALS056 receiver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		T_A†	MIN	MAX	UNIT
t_{PLH4}	Propagation delay time, low-to-high-level output	Bn	An	$\overline{CS}$ at 0.8 V, R_L1 = 500 Ω, C_L = 50 pF,	T/$\overline{R}$ at 0.8 V, R_L2 = 500 Ω, See Figure 4	25°C		20	ns
						Full range		22	
t_{PHL4}	Propagation delay time, high-to-low-level output					25°C		18	
						Full range		20	
t_{PLZ1}	Output disable time from low level	T/$\overline{R}$	An	Bn at 2 V, V_L = 5 V, R_L2 = 500 Ω, See Figure 3	$\overline{CS}$ at 0.8 V, R_L1 = 500 Ω, C_L = 50 pF,	25°C		17	ns
						Full range		20	
t_{PZL1}	Output enable time to low level					25°C		25	
						Full range		40	
t_{PHZ1}	Output disable time from high level	T/$\overline{R}$	An	Bn at 0.8 V, V_L = 0, R_L2 = 500 Ω, See Figure 3	$\overline{CS}$ at 0.8 V, R_L1 = 500 Ω, C_L = 50 pF,	25°C		12	ns
						Full range		13	
t_{PZH1}	Output enable time to high level	T/$\overline{R}$	An	Bn at 0.8 V, R_L1 open, C_L = 50 pF,	$\overline{CS}$ at 0.8 V, R_L2 = 500 Ω, See Figure 3	25°C		15	ns
						Full range		22	
t_{PLZ2}	Output disable time from low level	$\overline{CS}$	An	Bn at 2 V, R_L1 = 500 Ω, C_L = 50 pF, See Figure 5	T/$\overline{R}$ at 0.8 V, R_L2 = 500 Ω, V_L = 5 V,	25°C		20	ns
						Full range		22	
t_{PZL2}	Output enable time to low level					25°C		13	
						Full range		14	
t_{PHZ2}	Output disable time from high level	$\overline{CS}$	An	Bn at 0.8 V, V_L = 0, R_L1 = R_L2 = 500 Ω,	T/$\overline{R}$ at 0.8 V, C_L = 50 pF, See Figure 5	25°C		12	ns
						Full range		13	
t_{PZH2}	Output enable time to high level			Bn at 0.8 V, R_L1 not connected, C_L = 50 pF,	T/$\overline{R}$ at 0.8 V, R_L2 = 500 Ω, See Figure 5	25°C		14	
						Full range		22	
$t_{w(NR)}$	Receiver noise rejection pulse duration	Bn	An	V_L = 5 V, R_L2 = 500 Ω, See Figure 6	R_L1 = 500 Ω, C_L = 50 pF,	25°C	4		ns
						Full range	2		

† Full range is −55°C to 125°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

SN75ALS056 receiver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH4}	Propagation delay time, low-to-high-level output	Bn	An	$\overline{CS}$ at 0.8 V, $T/\overline{R}$ at 0.8 V, R_L1 = 390 Ω, R_L2 = 1.6 kΩ, C_L = 30 pF, See Figure 4		18	ns
t_{PHL4}	Propagation delay time, high-to-low-level output					18	
t_{PLZ1}	Output disable time from low level	$T/\overline{R}$	An	$\overline{CS}$ at 0.8 V, $V_{I(Bn)}$ = 2 V, V_L = 5 V, R_L1 = 390 Ω, R_L2 not connected, C_L = 15 pF, See Figure 3		20	ns
t_{PZL1}	Output enable time to low level	$T/\overline{R}$	An	$\overline{CS}$ at 0.8 V, $V_{I(Bn)}$ = 2 V, V_L = 5 V, R_L1 = 390 Ω, R_L2 = 1.6 kΩ, C_L = 30 pF, See Figure 3		40	ns
t_{PHZ1}	Output disable time from high level	$T/\overline{R}$	An	$\overline{CS}$ at 0.8 V, $V_{I(Bn)}$ = 0, V_L = 0, R_L1 = 390 Ω, R_L2 not connected, C_L = 15 pF, See Figure 3		17	ns
t_{PZH1}	Output enable time to high level	$T/\overline{R}$	An	$\overline{CS}$ at 0.8 V, $V_{I(Bn)}$ = 0, V_L = 0, R_L1 not connected, R_L2 = 1.6 kΩ, C_L = 30 pF, See Figure 3		15	ns
t_{PLZ2}	Output disable time from low level	$\overline{CS}$	An	Bn at 2 V, $T/\overline{R}$ at 0.8 V, C_L = 5 pF, V_L = 5 V, R_L1 = 390 Ω, R_L2 not connected, See Figure 5		18	ns
t_{PZL2}	Output enable time to low level	$\overline{CS}$	An	Bn at 2 V, $T/\overline{R}$ at 0.8 V, C_L = 30 pF, V_L = 5 V, R_L1 = 390 Ω, R_L2 = 1.6 kΩ, See Figure 5		15	ns
t_{PHZ2}	Output disable time from high level	$\overline{CS}$	An	Bn at 0.8 V, $T/\overline{R}$ at 0.8 V, C_L = 5 pF, V_L = 0, R_L1 = 390 Ω, R_L2 not connected, See Figure 5		8	ns
t_{PZH2}	Output enable time to high level	$\overline{CS}$	An	Bn at 0.8 V, $T/\overline{R}$ at 0.8 V, C_L = 30 pF, V_L = 0, R_L1 not connected, R_L2 = 1.6 kΩ See Figure 5		17	ns
$t_{w(NR)}$	Receiver noise rejection pulse duration	Bn	An	$\overline{CS}$ at 0.8 V, $T/\overline{R}$ at 0.8 V, R_L1 = 390 Ω, R_L2 = 1.6 kΩ, C_L = 30 pF, V_L = 5 V, See Figure 6	3		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

SN55ALS057 driver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A†	MIN	TYP‡	MAX	UNIT
t_{PLH1}	Propagation delay time, low-to-high-level output	$\overline{TE}$	Bn	Dn, En, $\overline{RE}$ at 2 V, V_L = 2 V, R_{L1} = 18 Ω, R_{L2} = 500 Ω, C_L = 50 pF, See Figure 2	25°C			10	ns
					Full range			27	
t_{PHL1}	Propagation delay time, high-to-low-level output				25°C			17	
					Full range			19	
t_{PLH2}	Propagation delay time, low-to-high-level output	Dn or En	Bn	$\overline{TE}$ at 0.8 V, $\overline{RE}$ at 2 V, V_L = 2 V, R_{L1} = 18 Ω, R_{L2} = 500 Ω, C_L = 50 pF, See Figure 2	25°C			10	ns
					Full range			27	
t_{PHL2}	Propagation delay time, high-to-low-level output				25°C			12	
					Full range			15	
t_{TLH}	Transition time, low-to-high-level output	Dn or En	Bn	$\overline{RE}$ at 2 V, V_L = 2 V, R_{L1} = 18 Ω, R_{L2} = 500 Ω, C_L = 50 pF, See Figure 2	25°C	1	3	8	ns
					Full range	1		33	
t_{THL}	Transition time, high-to-low-level output				25°C	1	3	10	ns
					Full range	1		13	

† Full range is –55°C to 125°C.
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

SN75ALS057 driver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
t_{PLH1}	Propagation delay time, low-to-high-level output	$\overline{TE}$	Bn	Dn, En, $\overline{RE}$ at 2 V, V_L = 2 V, R_{L1} = 18 Ω, R_{L2} not connected, C_L = 30 pF, See Figure 2			24	ns
t_{PHL1}	Propagation delay time, high-to-low-level output						20	
t_{PLH2}	Propagation delay time, low-to-high-level output	Dn or En	Bn	$\overline{TE}$ at 0.8 V, $\overline{RE}$ at 2 V, V_L = 2 V, R_{L1} = 18 Ω, R_{L2} not connected, C_L = 30 pF, See Figure 2			19	ns
t_{PHL2}	Propagation delay time, high-to-low-level output						18	
t_{TLH}	Transition time, low-to-high-level output	Dn or En	Bn	$\overline{RE}$ at 2 V, $\overline{TE}$ at 0.8 V, V_L = 2 V, R_{L1} = 18 Ω, R_{L2} not connected, C_L = 30 pF, See Figure 2	1	3	11	ns
t_{THL}	Transition time, high-to-low-level output				1	3	6	

‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

SN55ALS057 receiver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A†	MIN	MAX	UNIT
t_{PLH4}	Propagation delay time, low-to-high-level output	Bn	Rn	$\overline{RE}$ at 0.8 V, $\overline{TE}$ at 2 V, V_L = 5 V, R_L1 = 500 Ω, R_L2 = 500 Ω, C_L = 50 pF, See Figure 4	25°C		20	ns
					Full range		22	
t_{PHL4}	Propagation delay time, high-to-low-level output				25°C		18	
					Full range		20	
t_{PLZ2}	Output disable time from low level	$\overline{RE}$	Rn	Bn at 2 V, $\overline{TE}$ at 2 V, V_L = 5 V, R_L1 = 500 Ω, R_L2 = 500 Ω, C_L = 50 pF, See Figure 5	25°C		15	ns
					Full range		17	
t_{PZL2}	Output enable time to low level				25°C		13	
					Full range		14	
t_{PHZ2}	Output disable time from high level	$\overline{RE}$	Rn	Bn at 0.8 V, $\overline{TE}$ at 2 V, V_L = 0, R_L1 = 500 Ω, R_L2 = 500 Ω, C_L = 50 pF, See Figure 5	25°C		12	ns
					Full range		13	
t_{PZH2}	Output enable time to high level			Bn at 0.8 V, $\overline{TE}$ at 2 V, R_L1 not connected, R_L2 = 500 Ω, C_L = 50 pF, See Figure 5	25°C		14	
					Full range		15	
$t_{w(NR)}$	Receiver noise rejection pulse duration	Bn	Rn	V_L = 5 V, R_L1 = 500 Ω, R_L2 = 500 Ω, C_L = 50 pF, See Figure 6	25°C	4		ns
					Full range	2		

† Full range is –55°C to 125°C.

SN75ALS057 receiver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH4}	Propagation delay time, low-to-high-level output	Bn	Rn	$\overline{RE}$ at 0.8 V, $\overline{TE}$ at 2 V, V_L = 5 V, R_L1 = 390 Ω, R_L2 = 1.6 kΩ, C_L = 30 pF, See Figure 4		18	ns
t_{PHL4}	Propagation delay time, high-to-low-level output					18	
t_{PLZ2}	Output disable time from low level	$\overline{RE}$	Rn	Bn at 2 V, $\overline{TE}$ at 2 V, V_L = 5 V, C_L = 5 pF, R_L1 = 390 Ω, R_L2 not connected, See Figure 5		18	ns
t_{PZL2}	Output enable time to low level	$\overline{RE}$	Rn	Bn at 2 V, $\overline{TE}$ at 2 V, V_L = 5 V, C_L = 30 pF, R_L1 = 390 Ω, R_L2 = 1.6 kΩ, See Figure 5		15	ns
t_{PHZ2}	Output disable time from high level	$\overline{RE}$	Rn	Bn at 0.8 V, $\overline{TE}$ at 2 V, V_L = 0, C_L = 5 pF, R_L1 = 390 Ω, R_L2 not connected, See Figure 5		17	ns
t_{PZH2}	Output enable time to high level	$\overline{RE}$	Rn	Bn at 0.8 V, $\overline{TE}$ at 2 V, V_L = 0, C_L = 30 pF, R_L1 not connected, R_L2 = 1.6 kΩ, See Figure 5		17	ns
$t_{w(NR)}$	Receiver noise rejection pulse duration	Bn	Rn	$\overline{TE}$ at 2 V, $\overline{RE}$ at 0.8 V, V_L = 0, R_L1 = 390 Ω, R_L2 = 1.6 kΩ, C_L = 30 pF, See Figure 6	3		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

SN55ALS057 driver plus receiver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A†	MIN	MAX	UNIT
t_{PLH5}	Propagation delay time, low-to-high-level output	Dn	Rn	$\overline{RE}$ at 0.8 V, $\overline{TE}$ at 0.8 V, V_L = 2 V, R_L1 = 500 Ω, R_L2 = 500 Ω, C_L = 50 pF, See Figure 7	25°C		25	ns
					Full range		35	
t_{PHL5}	Propagation delay time, high-to-low-level output				25°C		25	
					Full range		44	

† Full range is −55°C to 125°C.

SN75ALS057 driver plus receiver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH6}	Propagation delay time, low-to-high-level output	Dn	Rn	$\overline{RE}$ at 0.8 V, $\overline{TE}$ at 0.8 V, R_L1 = 390 Ω, R_L2 = 1.6 kΩ, C_L = 30 pF, See Figure 8		40	ns
t_{PHL6}	Propagation delay time, high-to-low-level output					40	

PARAMETER MEASUREMENT INFORMATION

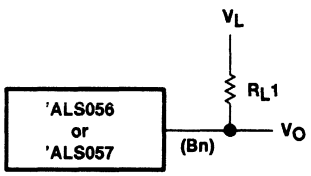
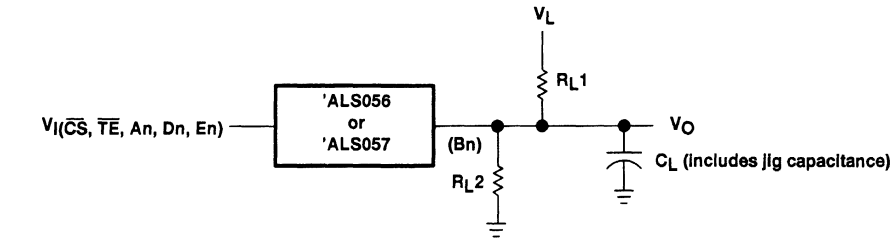
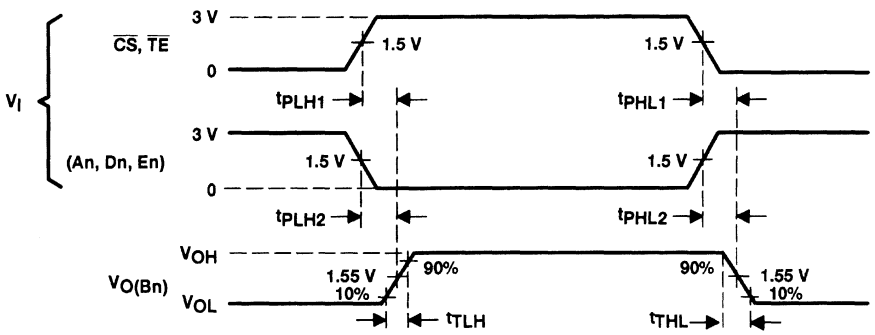


Figure 1. Driver Low-Level-Output-Voltage Test Circuit

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

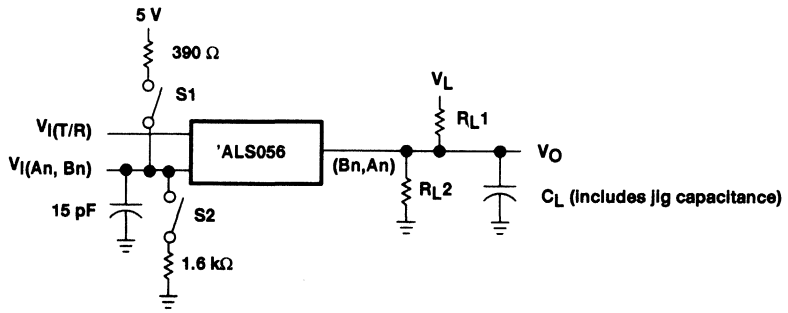


VOLTAGE WAVEFORMS

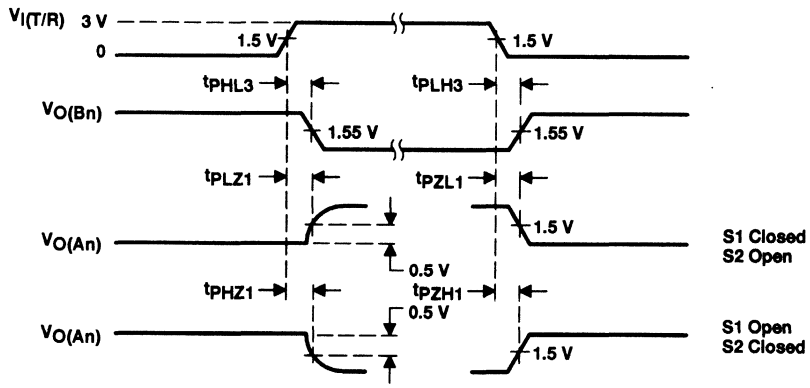
NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%

Figure 2. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



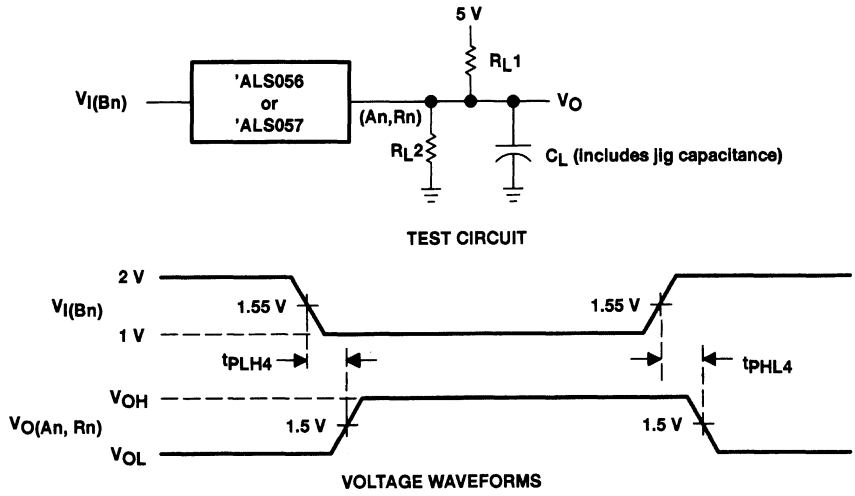
TEST CIRCUIT



VOLTAGE WAVEFORMS

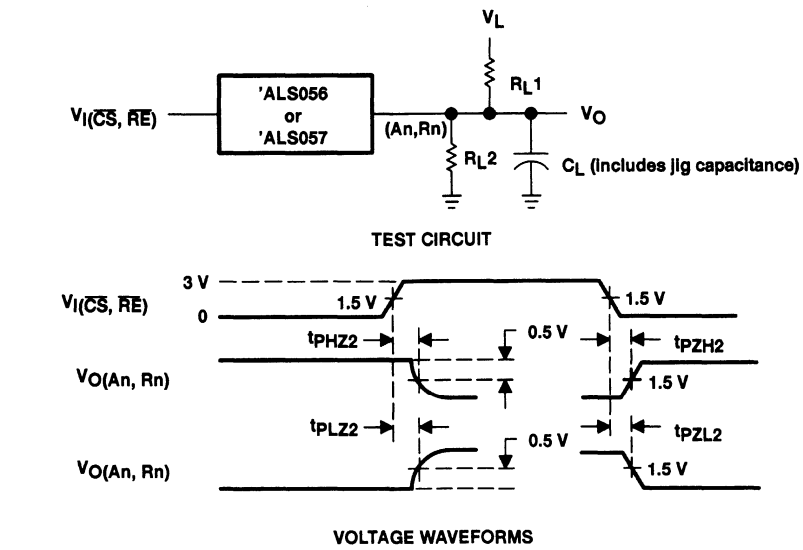
NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%

Figure 3. Propagation Delay From T/$\overline{R}$ to An or Bn Test Circuit and Voltage Waveforms



NOTE: $t_r = t_f \leq 10$ ns from 10% to 90%

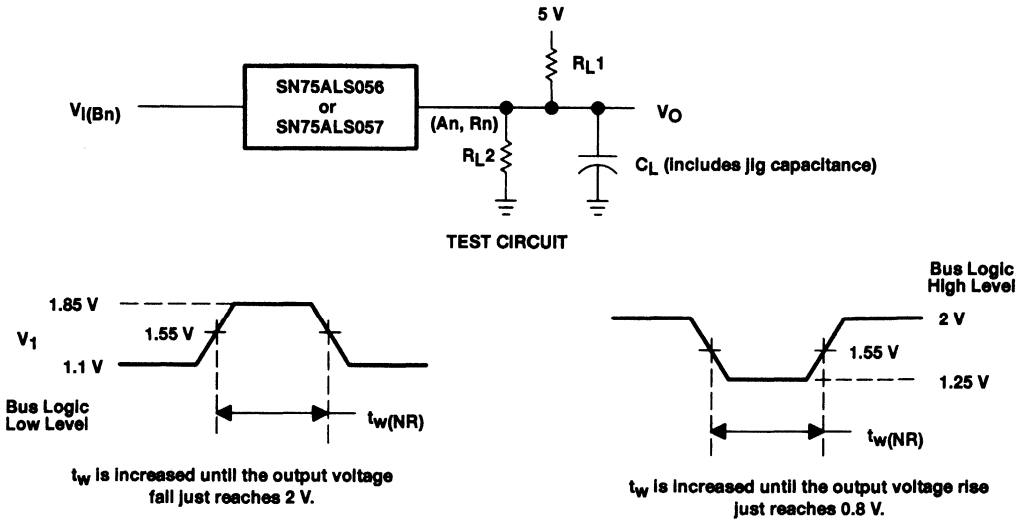
Figure 4. Receiver Test Circuit and Voltage Waveforms



NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%

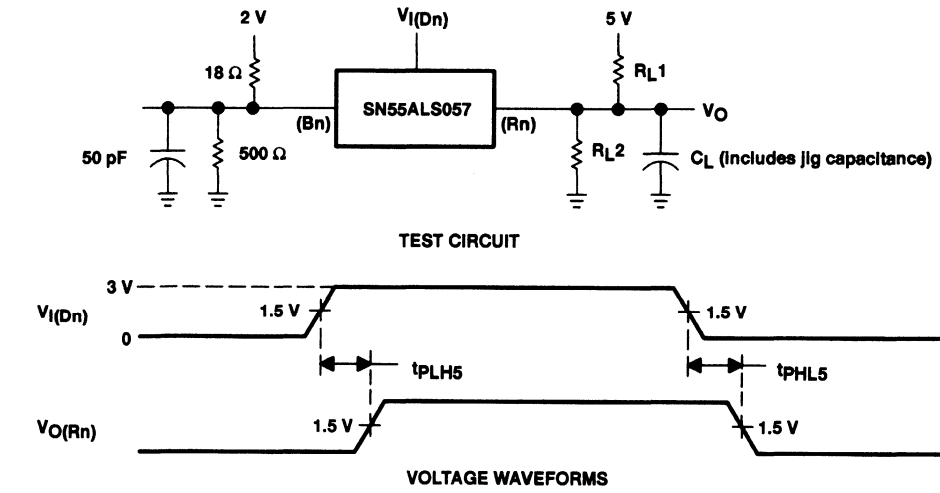
Figure 5. Propagation Delay From $\overline{CS}$ to An or $\overline{RE}$ to Rn Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE: $t_r = t_f \leq 2$ ns from 10% to 90%

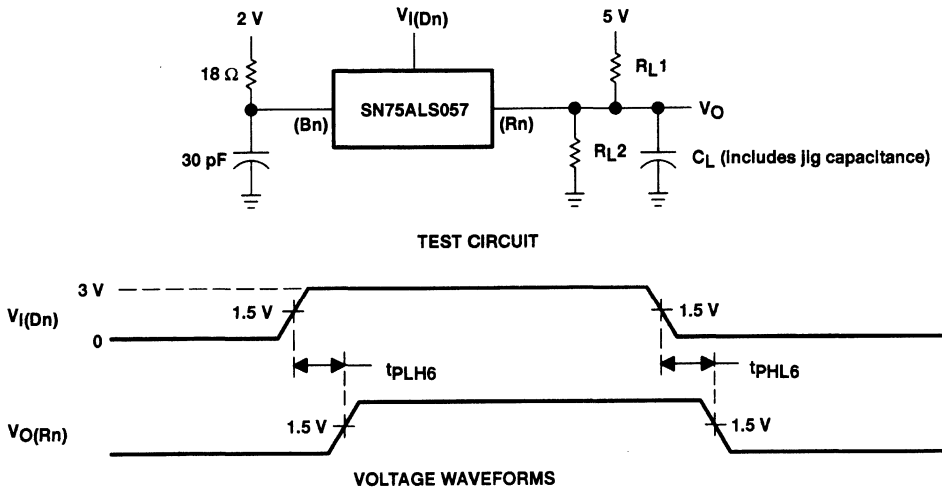
Figure 6. Receiver Noise Immunity Test Circuit and Voltage Waveforms



NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%

Figure 7. Driver Plus Receiver Delay Times Test Circuits and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



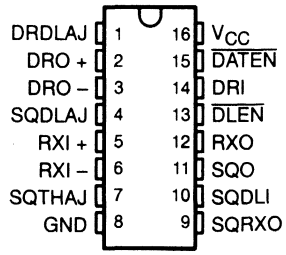
NOTE: $t_r = t_f \leq 5$ ns from 10% to 90%

Figure 8. Driver Plus Receiver Delay Times Test Circuits and Voltage Waveforms

SLLS026C – JANUARY 1987 – REVISED JULY 1990

- IEEE 802.3 1BASE5 Driver and Receiver
- On-Chip Receiver Squelch With Adjustable Threshold
- Adjustable Squelch Delay
- Direct TTL-Level Squelch Output
- Squelch Circuit Allows for External Noise Filtering
- Two Driver-Enable Options
- On-Chip Start-of-Idle Detection and Disable
- Driver Provides 2-V Minimum into a 50-Ω Differential Load Allowing for Use With Doubly-Terminated Lines and Multipoint Architectures
- On-Chip Driver Slew-Rate Control for Very Closely Matched Output Rise and Fall Times

N PACKAGE
(TOP VIEW)



Function Tables

DRIVER

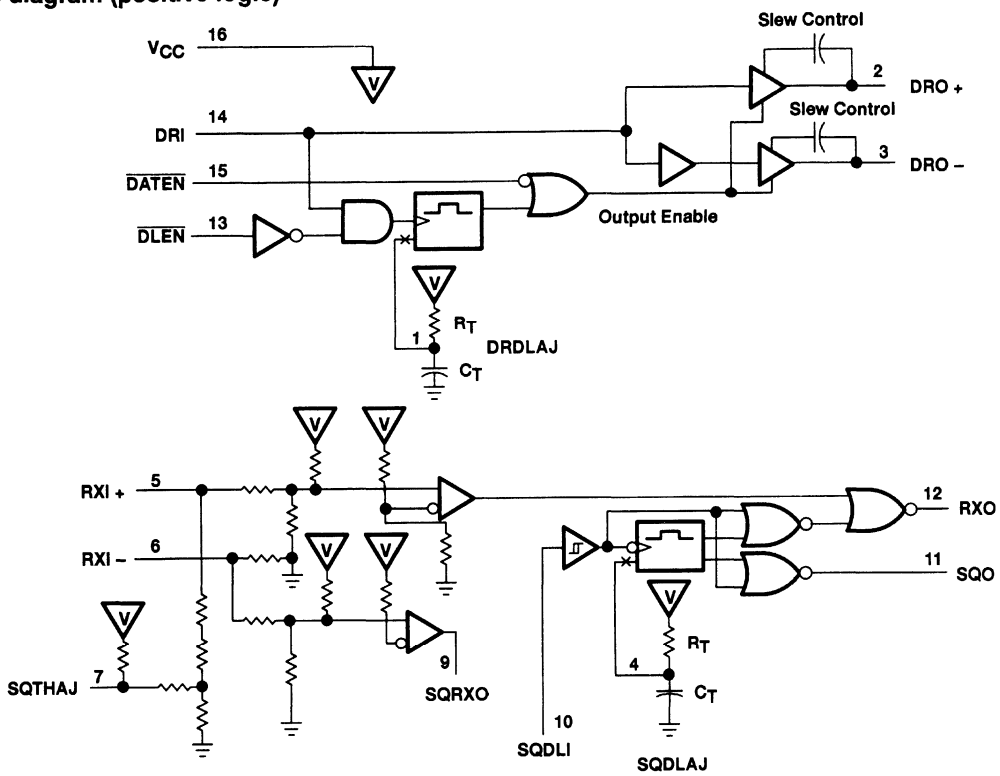
INPUTS			OUTPUTS	
DRI	$\overline{\text{DATEN}}$	$\overline{\text{DLEN}}$	DRO +	DRO –
L	L	X	L	H
H	L	X	H	L
X	H	H	Z	Z
H	H	L	H†	L†
L	H	L	L‡	H‡

RECEIVER§

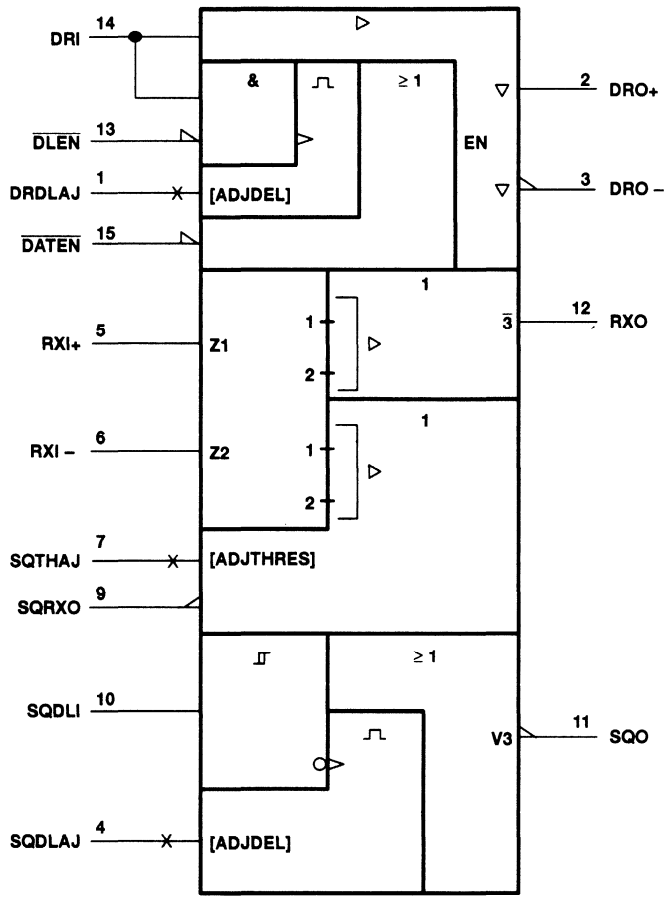
CONDITION	INPUTS		OUTPUTS	
	RXI +	RXI –	RXO	SQO
No active signal ¶	X	X	H	H
Active signal ¶	L	H	L	L
	H	L	H	L

† This condition is valid during the time period set by DRDLAJ following a rising transition on DRI. Following this, when a subsequent positive transition does not occur on DRI, the outputs go to the high-impedance state.
‡ This condition is valid when it occurs within the enable time set by DRDLAJ after a rising transition on DRI. Otherwise, the outputs are in the high-impedance state.
§ Pins 9 and 10 are tied together.
¶ An active signal is one that has an amplitude greater than the threshold level set by SQTHAJ.

logic diagram (positive logic)



logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN75061 is a single-channel driver/receiver pair designed for use in IEEE 802.3, 1BASE5 applications as well as other general data communications circuits. The SN75061 offers both a driver and a receiver that are easily configured for use with a variety of controllers and data encoder/decoders.

The receiver features a full analog squelch circuit with an adjustable threshold and a programmable squelch delay. Internal nodes of the squelch circuitry are brought out to external connections to allow for the insertion of noise-filtering circuitry of the designer's choice.

As with the receiver, the driver offers a variety of implementation options. Driver enabling may be directly controlled by an external logic input or by use of an on-chip one-shot that is retriggered as long as data is being sent to the driver. The driver then automatically goes to the high-impedance state when end-of-packet common phrase occurs. The driver features internal slew-rate control for optimal matching of rise and fall times allowing for reduction of driver-induced jitter.

receiver

The SN75061 receiver implements full analog squelch functions by integrating both a separate, parallel squelch receiver with an externally programmable threshold, and a programmable one-shot. The output of the squelch receiver and the input to the high-level, dc-triggered one-shot are brought out to external connections. These pins can be shorted for direct implementation or used for the insertion of noise-filtering circuitry of the implementer's design. The receiver one-shot can be effectively bypassed by applying a high logic level to SQDLI. The squelch threshold may be set externally by applying an external voltage set to a level that is –2 times the desired threshold voltage. When SQTHAJ is left open, the squelch receiver defaults to its internal preset value of –600 mV. The receiver also outputs a high logic squelch signal when there is not any active data present at the receiver inputs. When data is not present on the transmission line, the receiver output assumes a high level. The unsquelch duration is set externally with an R-C combination at SQDLAJ.

driver

The driver offers a variety of implementation options. Driver enabling may be controlled directly by an active-low, external logic input on $\overline{\text{DATEN}}$ or by use of another on-chip one-shot that retriggers with positive-going transitions on the driver input line. When positive transition does not occur within the pulse duration set by an external R-C combination, the one-shot times out and the driver is automatically put into a high-impedance state. When operating in the delay-enable mode, the 2-bit-time, high-level, start-of-idle pulse prescribed by IEEE 802.3 1BASE5 causes the one-shot to time out and automatically place the driver outputs in the high-impedance state. This delay time is also adjustable for use in other applications. The driver implements an output slew-rate control that is internally set for nominally 40 mV/ns. (This is roughly a 100-ns peak-to-peak differential transition time.) The driver outputs are capable of driving a 50-Ω differential load with a minimum output level of 2 V. Short-circuit output current is greater than 100 mA.

Terminal Functions

PIN NAME	PIN NO.	DESCRIPTION
$\overline{\text{DATEN}}$	15	Driver data enable. When this sign is low, driver outputs are in an active state. When the signal is high, the driver outputs are in a high-impedance state when $\overline{\text{DLEN}}$ is also high.
$\overline{\text{DLEN}}$	13	Driver delay enable. When this signal is low and $\overline{\text{DATEN}}$ is high, the driver outputs are active for a period of time set by DRDLAJ after a positive-going transition on DRI. When there is not any active data on DRI, the outputs are in a high-impedance state.
DRDLAJ	1	Driver delay adjust is a connection for the external R-C combination that determines the duration of the driver output active state after a positive transition on DRI when $\overline{\text{DLEN}}$ is low and $\overline{\text{DATEN}}$ is high.
DRI	14	Driver data input
DRO+	2	Noninverting driver output
DRO–	3	Inverting driver output
GND	8	Ground. Common for all voltages
RXI+	5	Noninverting receiver input
RXI–	6	Inverting receiver input
RXO	12	Main receiver input
SQDLAJ	4	Squelch delay adjust is a connection for an external R-C combination that determines the duration of the receiver unsquelch after a negative-going transition on SQDLI.
SQDLI	10	Squelch delay input is the input to the one-shot that controls the duration of the receiver unsquelch period. The main receiver output remains unsquelched as long as SQDLI is held high. Timing of the unsquelch period begins on the high-to-low transition of SQDLI.
SQO	11	Squelch output is high while the receiver is squelched.
SQRXO	9	Squelch receiver output is high only when the differential receiver input exceeds the threshold set by SQTHAJ.
SQTHAJ	7	Squelch receiver threshold adjust. The voltage at this input determines the threshold of the squelch receiver in a ratio of –2, SQTHAJ to threshold. When the receiver is left open, the squelch receiver threshold defaults to –600 mV.
V_{CC}	16	Supply-voltage input

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} ..... 7 V
Input voltage, V_I (any logic input) ..... 7 V
Receiver differential input voltage ..... ±25 V
Receiver input voltage ..... ±15 V
Driver output voltage ..... –0.5 V to 15 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 1) ..... 1150 mW
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: For operation above 25°C free-air temperature, derate to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Driver high-level input voltage, V_{IH}	2			V
Driver low-level input voltage, V_{IL}			0.8	V
Receiver common-mode input voltage, V_{IC} (see Note 2)	−2.5		5	V
Driver high-level output current, I_{OH}			−150	mA
Driver low-level output current, I_{OL}			150	mA
External timing resistance, R_{ext}	5		260	kΩ
External timing capacitance, C_{ext}	No restriction			
Operating free-air temperature, T_A	0		70	°C

NOTE 2: The algebraic convention, in which the less-positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode input voltage V_{IC} and threshold levels V_{IT+} and V_{IT-}.

electrical characteristics over recommended operating free-air temperature and supply voltage ranges (unless otherwise noted)

driver

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_{OD}	Differential output voltage	R_L = 50 Ω		2	2.4	3.3	V
		R_L = 115 Ω				3.65	
ΔV_{OD}	Change in differential output voltage for a change in logic input state					50	mV
I_{IH}	High-level input current	V_I = 2 4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.5 V		±100		−35	μA
I_{OS}	Short-circuit output current	V_O = 0 or 6 V,	V_I = 0.8 V or 2.5 V			±300	mA
I_{OZ}	High-impedance output current	V_{CC} = 5.25 V	V_{OC} = 10 V			100	μA
			V_{OC} = 0			−100	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

electrical characteristics over recommended operating free-air temperature and supply voltage ranges (unless otherwise noted) (continued)

receiver

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage, squelch delay		I_I = −18 mA				−1.5	V
V_{IT+}	Positive-going input threshold voltage		V_O = 2.7 V,	I_O = −0.4 mA			50	mV
V_{IT-}	Negative-going input threshold voltage		V_O = 0.5 V,	I_O = 16 mA	−50‡			mV
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)					50		mV
V_{IC}	Common-mode input voltage						5	V
V_{OH}	High-level output voltage	RXO	V_{CC} = 4.75 V, SQDLAJ at 0.8 V	I_{OH} = −400 μA,	2.7			V
		SQO			2.7	3.5		
		SQRXO	V_{CC} = 4.75 V, $V_{ID(RXI)}$ = −0.7 V,	I_{OH} = −20 μA, SQDLAJ open	2.7	4.65		
V_{OL}	Low-level output voltage	RXO	V_{CC} = 4.75 V, SQDLAJ at 2 V	I_{OL} = 8 mA			0.45	V
		SQO		I_{OL} = 16 mA			0.5	
				I_{OL} = 8 mA		0.35	0.5	
		SQRXO	V_{CC} = 4.75 V, $V_{ID(RXI)}$ = 50 mV	I_{OL} = 8 mA			0.45	
				I_{OL} = 16 mA			0.5	
I_{IH}	High-level input current	SQDLI	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current		V_I = 0.5 V				−35	μA
I_{OS}	Short-circuit output current	RXO	V_{CC} = 5.25 V,	V_O = 0	−15		−85	mA
		SQO			−15		−100	
		SQRXO	V_{CC} = 5 V,	V_O = 0	−0.8	−1	−1.2	
r_i	Input resistance					10		kΩ
$V_{IT-(sq)}$	Squelch preset input threshold voltage		V_{CC} = 5 V, SQTHAJ open	V_{IC} = 1.5 V to 3.5 V	−525	−600	−675	mV
				V_{IC} = −2.5 V to 1.5 V or 3.5 V to 5 V	−500		−700	mV
	Ratio of SQTHAJ input voltage to actual squelch threshold voltage		SQTHAJ at 200 mV to 4 V		−1.9		−2.1	

driver and receiver

I_{CC}	Supply current	V_{CC} = 5.25 V, No load	Driver outputs disabled,		70	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode input voltage V_{IC} and threshold levels V_{IT+} and V_{IT-}.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

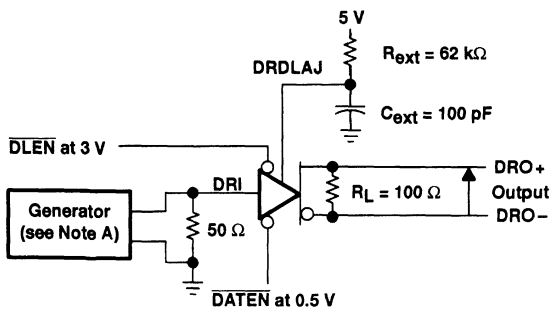
driver

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Differential-output slew rate	V_O = −2 V to 2 V, R_L = 100 Ω (differential),	See Figure 1	28	40	52	mV/ns
$t_{d(OD)}$	Differential-output delay time ($t_{d(OD)+}$ and $t_{d(OD)-}$)	C_L = 15 pF, R_L = 100 Ω (differential),	See Figure 2			160	ns
	Differential-output delay time difference ($t_{d(OD)+} - t_{d(OD)-}$)	R_L = 100 Ω (differential),	See Figure 2			5	ns
t_{PHZ}	Disable time from $\overline{DATEN}$	See Figure 3, 4, and 5				220	ns
t_{PLZ}						300	ns
t_{PZH}	Enable time from $\overline{DATEN}$					220	ns
t_{PZL}						290	ns
t_{PZH}	Enable time from $\overline{DLEN}$					250	ns
$t_{w(en)}$	Enable pulse duration time (with DLEN low)	C_{ext} = 100 pF, See Figure 6	R_{ext} = 62 kΩ,	2	2.5	3	µs

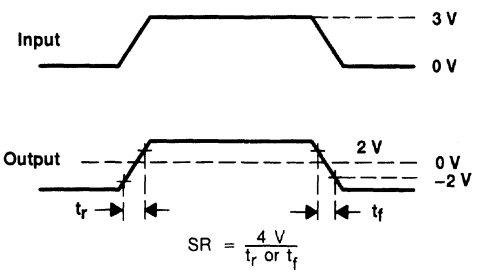
receiver

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{en(RX)}$	Receiver enable time	Squelch off,	See Figure 7		117		ns
t_{PLH}	Propagation delay time, low- to high level output	Squelch off,	See Figure 8		20	35	ns
t_{PHL}	Propagation delay time, high- to low level output	Squelch off,	See Figure 8		22	35	ns
$t_{d(unsq)}$	Unsquelch delay time	C_{ext} = 50 pF, See Figure 9	R_{ext} = 51 kΩ,	1	1.2	1.45	µs
		C_{ext} = 15 pF, See Figure 9	R_{ext} = 6.8 kΩ,			180	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

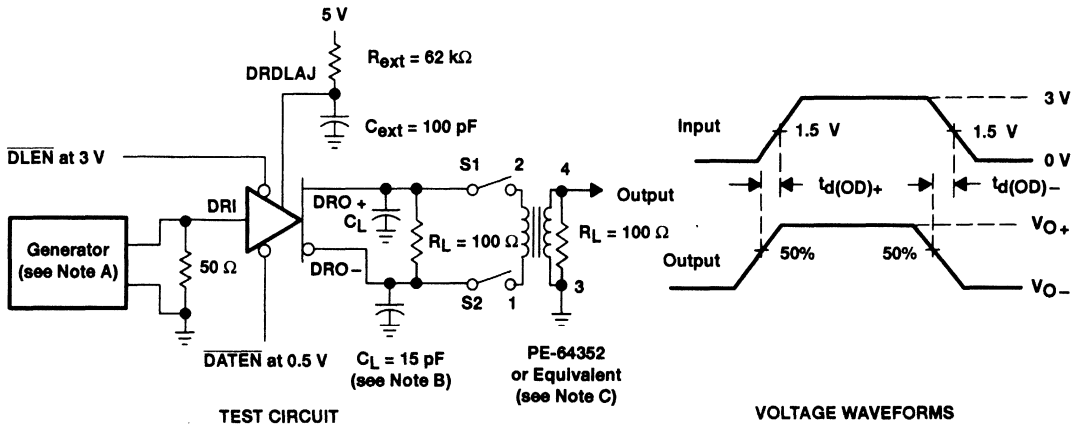


VOLTAGE WAVEFORMS

NOTE A: The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

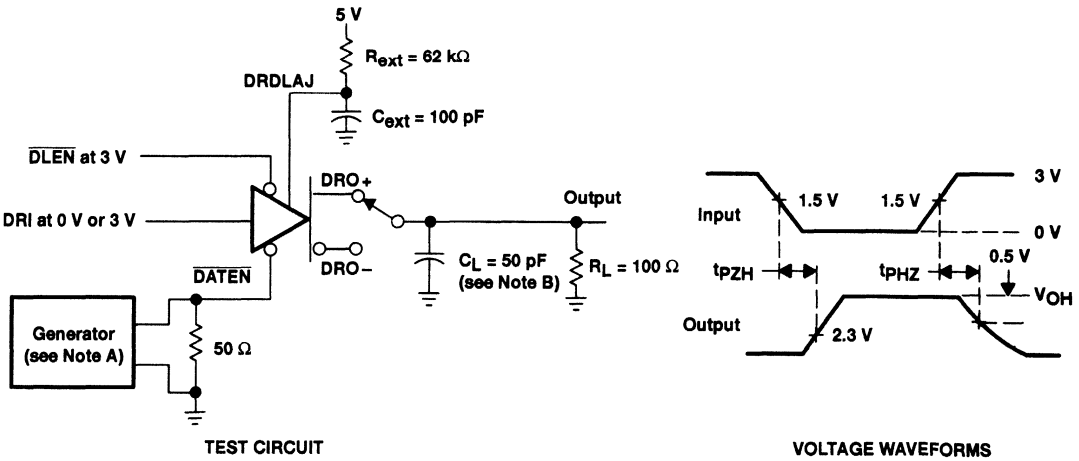
Figure 1. Test Circuit and Voltage Waveforms for Driver Slew Rate

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. When measuring differential-output delay time difference, switches S1 and S2 are closed (Isolation transformer from Pulse Engineering P/N PE-64352).

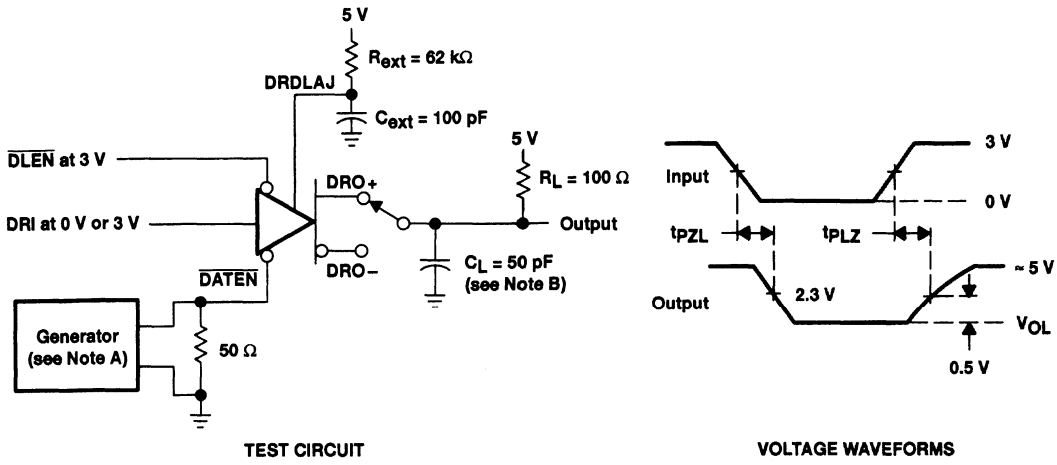
Figure 2. Test Circuit and Voltage Waveforms for Driver Differential Delay Time



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 500 kHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 3. Test Circuit and Voltage Waveforms for Driver Enable and Disable Time

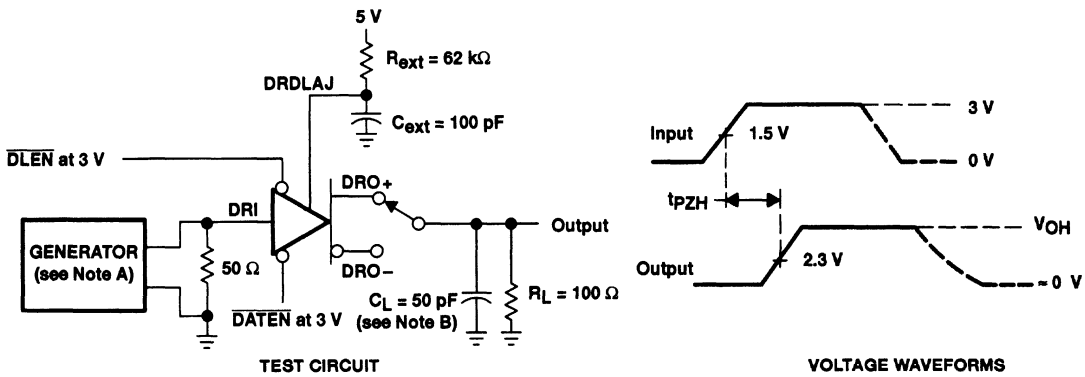
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 200 kHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 4. Test Circuit and Voltage Waveforms for Driver Enable and Disable Time

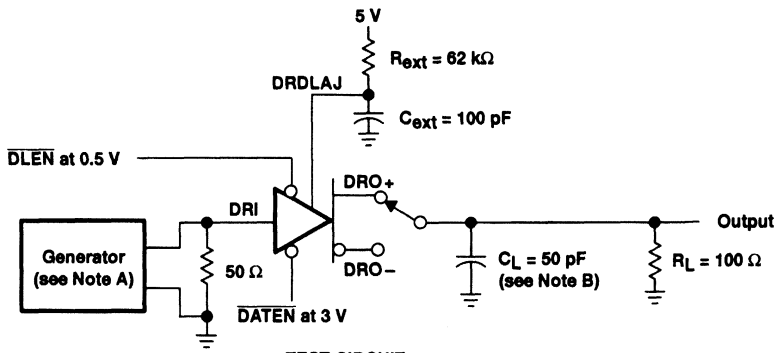


TEST CIRCUIT VOLTAGE WAVEFORMS

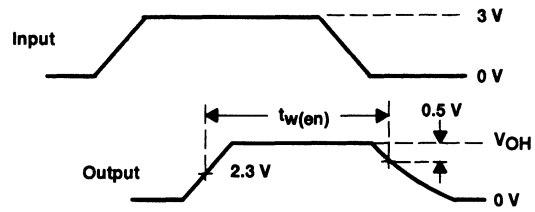
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 5. Test Circuit and Voltage Waveforms for Enable Time From Delay Enable

PARAMETER MEASUREMENT INFORMATION



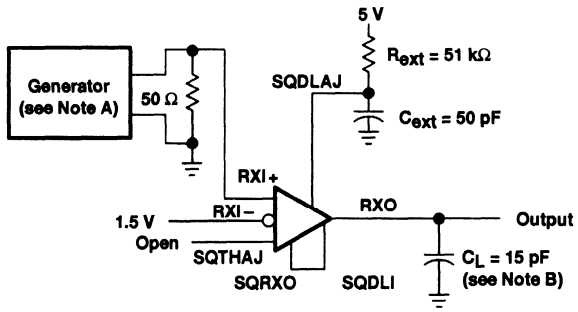
TEST CIRCUIT



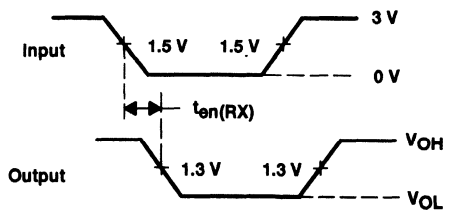
VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 200 kHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 6. Test Circuit and Voltage Waveforms for Enable Pulse Duration With Delay Enable Low



TEST CIRCUIT

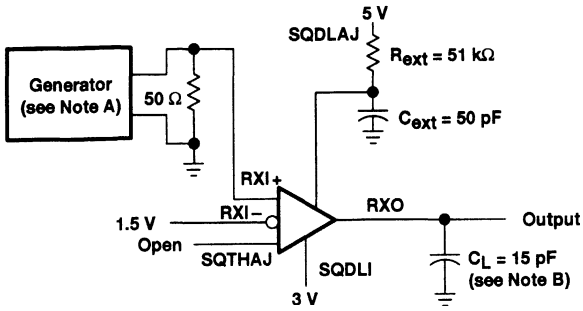


VOLTAGE WAVEFORMS

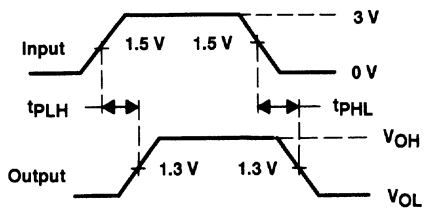
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 500 kHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 7. Test Circuit and Voltage Waveforms for Receiver Enable (Unsquelch) Time

PARAMETER MEASUREMENT INFORMATION



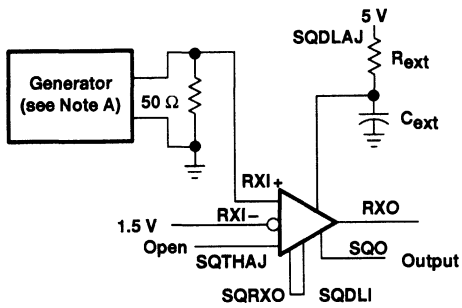
TEST CIRCUIT



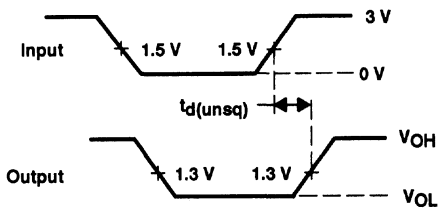
VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 8. Test Circuit and Voltage Waveforms for Receiver Propagation Delay Time



TEST CIRCUIT



VOLTAGE WAVEFORMS

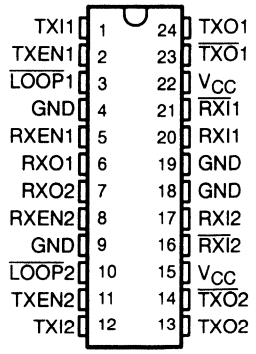
Figure 9. Test Circuit and Voltage Waveforms for Unsquelch Duration Time

NOTE A: The input pulse is supplied by a generator having the following characteristics: PRR ≤ 100 kHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

SLLS054B – APRIL 1989 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of IOS 8802.3:1989 and ANSI/IEEE Std 802.3-1988**
- **Interdevice Loop-Back Paths for System Testing**
- **Squelch Function Implemented on the Receiver Inputs**
- **Drivers Will Drive a Balanced 78-Ω Load**
- **Transformer Coupling Not Required in System**
- **Power-Up/Power-Down Protection (Glitch Free)**
- **Isolated Ground Pins for Reduced Noise Coupling**
- **Fault-Condition Protection Built into the Device**
- **Driver Inputs Are Level-Shifted ECL Compatible**

DW OR NT PACKAGE
(TOP VIEW)



description

The SN75ALS085 is a monolithic, high-speed, advanced low-power Schottky, dual-channel driver/receiver device designed for use in the AUI of ANSI/IEEE Std 802.3-1988. The two drivers on the device drive a 78-Ω balanced, terminated twisted-pair transmission line up to a maximum length of 50 meters. In the off (idle) state, the drivers maintain minimal differential output voltage on the twisted-pair line and, at the same time, remain within the required output common-mode range.

With the driver enable (TXEN) high, upon receiving the first falling edge into the driver input, the differential outputs will rise to full-amplitude output levels within 25 ns. The output amplitude is maintained for the remainder of the packet. After the last positive packet edge is transmitted into the driver, the driver will maintain a minimum of 70% full differential output for a minimum of 200 ns, then decay to a minimum level for the reset (idle) condition within 8 μs. Disabling the driver by taking the driver enable low will also force the output into the idle condition after the normal 8-μs timeout. While operating, the drivers are able to withstand a set of fault conditions and not suffer damage due to the faults being applied. The drivers power up in the idle state to ensure that no activity is placed on the twisted-pair cable that could be interpreted as network traffic.

The line receiver squelch function interfaces to a differential twisted-pair line terminated external to the device. The receiver squelch circuit allows differential receive signals to pass through as long as the input amplitude and pulse duration are greater than the minimum squelch threshold. This ensures a good signal-to-noise ratio while the data path is active and prevents system noise from causing false data transitions during line shutdown and line-idle conditions. The RXO outputs default to a high level and the RXEN outputs default to a low level while the squelch function is blocking the data path through the receiver (idle). The line receiver squelch will become active within 50 ns when the input squelch threshold is exceeded. RXEN will be driven high when the squelch circuit is allowing data to pass through the receiver. The receiver squelch circuit can also withstand a set of fault conditions while operating without causing permanent damage to the device.

description (continued)

The purpose of the loop functions is to provide a means by which system data path verification can be done to isolate faulty interfaces and assist in network diagnosis. The LOOP pins are TTL compatible and must be held high for normal operation. When $\overline{\text{LOOP1}}$ is taken low, the output of driver 1 (TXO1) immediately goes into the idle state. Also, the input to receiver 1 is ignored and a path from TXI1 to RXO1 is established. When $\overline{\text{LOOP1}}$ is taken back high, driver 1 and receiver 1 revert back to their normal operation. When $\overline{\text{LOOP2}}$ is taken low, a similar data path is established between TXI1 and RXO2. TXEN1 must be high for the loop functions to operate and TXEN1 can be used to gate the loop function if desired. During loop operation, the respective receiver enable output (RXEN) will reflect the status of TXEN1.

Function Tables

RECEIVER – $\overline{\text{LOOP}}$ = H

RXI		PREVIOUS RXEN	OUTPUTS	
			RXEN	RXO
V_{ID} = 1315 mV to –175 mV,	t_w < 25 ns	L	L	H
V_{ID} = –275 mV to –1315 mV,	t_w > 50 ns	X	H	L
V_{ID} = 318 mV to 1315 mV,	t_w < 142 ns	H	H	H
V_{ID} = 318 mV to 1315 mV,	t_w > 187 ns	X	L	H

DRIVER – $\overline{\text{LOOP}}$ = H

TXI	TXEN	PREVIOUS TXO	OUTPUT TXO
L	L	Idle	Idle
H	L	Idle	Idle
↓	H	Idle	L
L	H	Active	L
H < 260 µs	H	Active	H
H > 8 µs	H	Active	Idle
L	L > 8 µs	Active	Idle
H < 260 ns	L > 8 µs	Active	Idle
H < 260 ns	L < 260 ns	Active	H
H > 8 µs	L < 260 ns	Active	Idle
L	L < 260 ns	Active	L

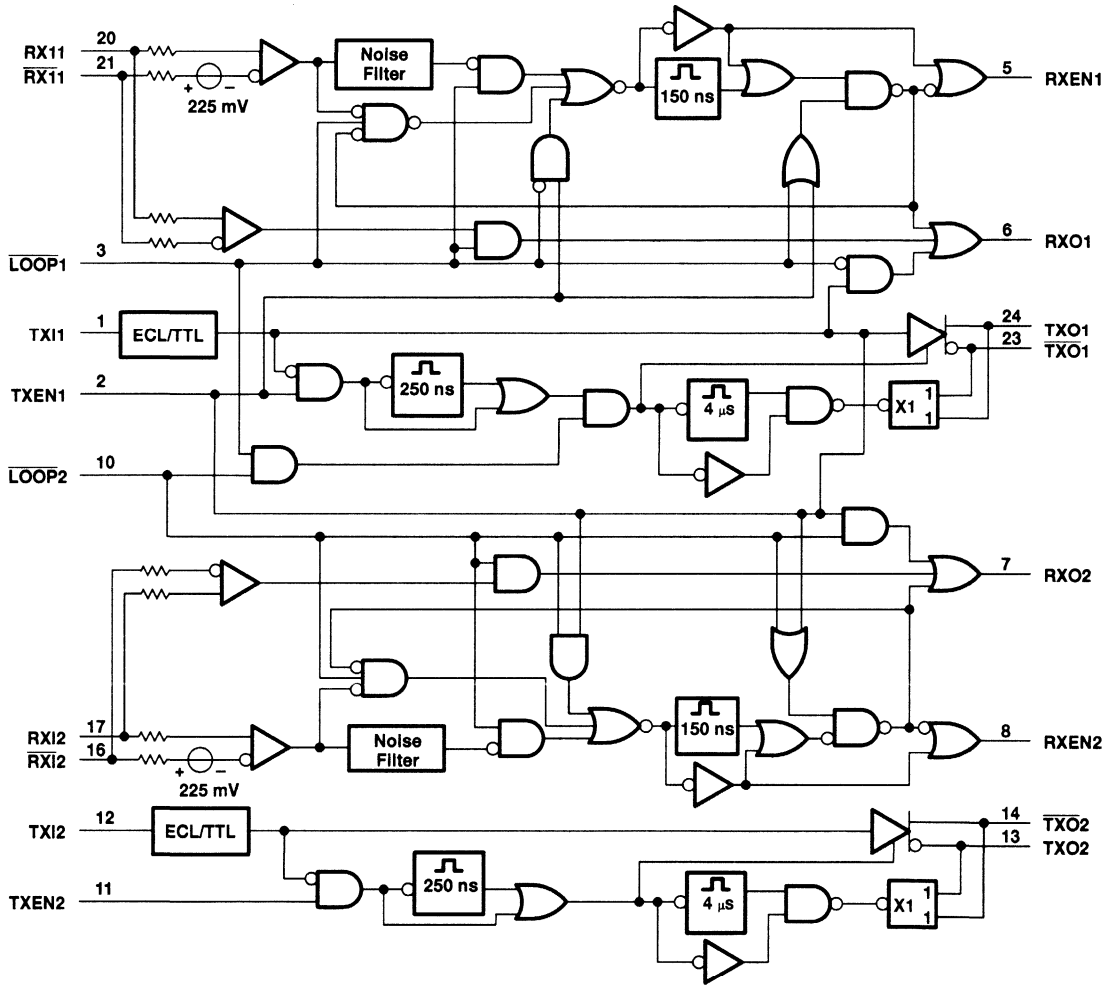
H = $V_I \geq V_T$ max, L = $V_I \leq V_T$ min

LOOP

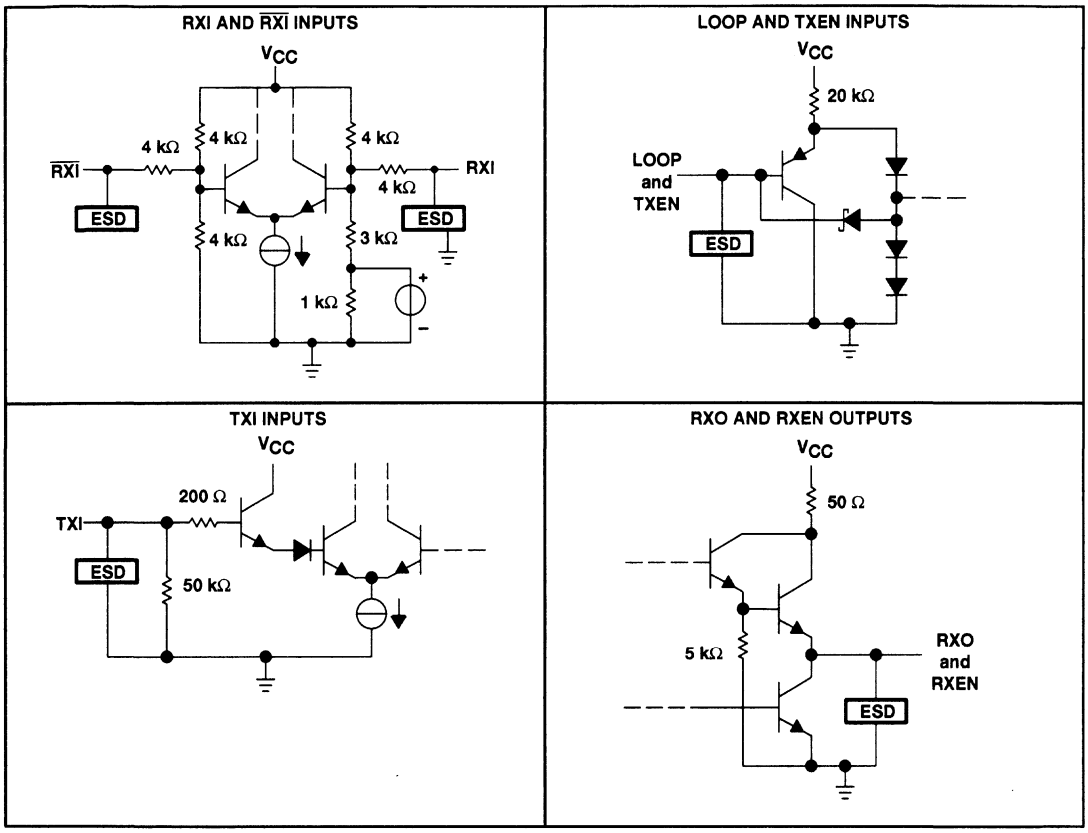
INPUTS						OUTPUTS				
$\overline{\text{LOOP1}}$	$\overline{\text{LOOP2}}$	TXI1	TXEN1	RXI1	RXI2	RXO1	RXO2	RXEN1	RXEN2	TXO1
L	L	L	H	X	X	L	L	H	H	Idle
L	L	H	H	X	X	H	H	H	H	Idle
L	L	X	L	X	X	H	H	L	L	Idle
L	H	L	H	X	Normal	L	Normal	H	Normal	Idle
L	H	H	H	X	Normal	H	Normal	H	Normal	Idle
L	H	X	L	X	Normal	H	Normal	L	Normal	Idle
H	L	L	H	Normal	X	Normal	L	Normal	H	Idle
H	L	H	H	Normal	X	Normal	H	Normal	H	Idle
H	L	X	L	Normal	X	Normal	H	Normal	L	Idle
H	H	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal

H = high level, L = low level, X = don't care

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 6 V
TXI and $\overline{LOOP}$ input voltage, V_I ..... 5.5 V
TXO and $\overline{TXO}$ output voltage, V_O ..... 16 V
RXI and $\overline{RXI}$ input voltage, V_I ..... 16 V
RXO and RXEN output voltage, V_O ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... – 65 °C to 150 °C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1350 mW	10.8 mW/°C	864 mW
NT	1250 mW	10.0 mW/°C	800 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode voltage at RXI inputs, V_{IC}	1		4.2	V
Differential voltage between RXI inputs, V_{ID}	± 318		± 1315	mV
High-level input voltage, $\overline{LOOP}$ and TXEN, V_{IH}	2			V
Low-level input voltage, $\overline{LOOP}$ and TXEN, V_{IL}			0.8	V
High-level output current, RXO and RXEN, I_{OH}			– 0.4	mA
Low-level output voltage, RXO and RXEN, I_{OL}			16	mA
Setup time, driver mode, TXEN high before TXI↓, t_{su1} (see Figure 7)	10			ns
Setup time, loop mode, $\overline{LOOP}$ low before TXEN↑, t_{su2} (see Figure 9)	15			ns
Setup time, loop mode, TXEN high before TXI↓, t_{su3} (see Figure 9)	10			ns
Hold time, loop mode, TXEN high after TXI↑, t_{h1} (see Figure 8)	10			ns
Hold time, loop mode, $\overline{LOOP}$ low after TXEN↓, t_{h2} (see Figure 8)	15			ns
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
V_{IK}	Clamp voltage at all inputs		$I_I = -18$ mA			−1.5	V
$V_{(TO)}$	Driver input (TXI) threshold voltage		$T_A = 0°C$	$V_{CC} = 4.75$ V	3.202	3.752	V
				$V_{CC} = 5$ V	3.389	3.998	
				$V_{CC} = 5.25$ V	3.577	4.244	
			$T_A = 25°C$	$V_{CC} = 4.75$ V	3.213	3.797	V
				$V_{CC} = 5$ V	3.400	4.043	
				$V_{CC} = 5.25$ V	3.588	4.289	
			$T_A = 70°C$	$V_{CC} = 4.75$ V	3.239	3.849	V
				$V_{CC} = 5$ V	3.426	4.095	
				$V_{CC} = 5.25$ V	3.614	4.341	
	Receiver differential input threshold voltage					−275	mV
V_{OC}	Driver output (TXO) common-mode voltage	Idle	TXEN at 0.8 V, $\overline{LOOP}$2 at 2 V,	$\overline{LOOP}$1 at 2 V, See Figure 1	1	4.2	V
		Active	TXEN at 2 V, $\overline{LOOP}$2 at 2 V, See Figure 1	$\overline{LOOP}$1 at 2 V, TXI at 3.2 V,	1	4.2	
		Active	TXEN at 2 V, $\overline{LOOP}$2 at 2 V, See Figure 1	$\overline{LOOP}$1 at 2 V, TXI at 4.4 V,	1	4.2	
V_{OD}	Driver output (TXO) differential voltage	Idle	TXEN at 0.8 V, $\overline{LOOP}$2 at 2 V,	$\overline{LOOP}$1 at 2 V, See Figure 1		±40	mV
		Active	TXEN at 2 V, $\overline{LOOP}$2 at 2 V, See Figure 1	$\overline{LOOP}$1 at 2 V, TXI at 3.2 V,	−600	1315	
		Active	TXEN at 2 V, $\overline{LOOP}$2 at 2 V, See Figure 1	$\overline{LOOP}$1 at 2 V, TXI at 4.4 V,	600	1315	
V_{OH}	High-level output voltage	RXO, RXEN	$I_{OH} = -0.4$ mA		2.4		V
V_{OL}	Low-level output voltage	RXO, RXEN	$I_{OL} = 16$ mA			0.5	V
I_{IH}	High-level input current	TXEN, $\overline{LOOP}$	$V_I = 2$ V			20	µA
		TXI	$V_I = 4.5$ V			400	
		$\overline{RXI}$, RXI	$V_{ID} = -0.5$ V,	$V_{IC} = 1$ V to 4.2 V		1000	
I_{IL}	Low-level input current	TXEN, $\overline{LOOP}$	$V_I = 0.8$ V			−200	mA
		TXI	$V_I = 3.1$ V			100	
			$V_I = 0.3$ V		4	10	
		$\overline{RXI}$, RXI	$V_{ID} = 0.5$ V,	$V_{IC} = 1$ V to 4.2 V		1000	
I_{OD}	Driver differential output current	Idle	TXEN at 0.8 V, $\overline{LOOP}$2 at 2 V,	$\overline{LOOP}$1 at 2 V, See Figure 2		±4	mA
I_{OS}	Short-circuit output current†	RXO, RXEN	V_O at 0 V, RXI at 2 V	$\overline{RXI}$ at 3 V,	−40	−150	mA
I_{CC}	Supply current		$\overline{LOOP}$2 at 2 V, TXI at 4.5 V,	TXEN at 2 V, Outputs open		225	mA

† Not more than one output should be shorted at a time, and the duration of the test should not exceed 1 second.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS†			MIN	MAX	UNIT
Driver fault condition current	TXO shorted to $\overline{\text{TXO}}$,	Current measured in short			150	mA
	TXO at 0 V,	$\overline{\text{TXO}}$ is open,	Current measured at TXO		150	
	TXO is open,	$\overline{\text{TXO}}$ at 0,	Current measured at $\overline{\text{TXO}}$		150	
	TXO at 0 V,	$\overline{\text{TXO}}$ at 0 V,	Current measured at TXO and $\overline{\text{TXO}}$		150	
	TXO at 16 V,	$\overline{\text{TXO}}$ is open,	Current measured at TXO		150	
	TXO is open,	$\overline{\text{TXO}}$ at 16 V,	Current measured at TXO		150	
	TXO at 16 V,	$\overline{\text{TXO}}$ at 16 V,	Current measured at TXO and $\overline{\text{TXO}}$		150	
Receiver fault condition current	RXI shorted to $\overline{\text{RXI}}$,	Current measured in short			10	mA
	RXI at 0 V,	$\overline{\text{RXI}}$ is open,	Current measured at RXI		3	
	RXI is open,	$\overline{\text{RXI}}$ at 0 V,	Current measured at RXI		3	
	RXI at 0 V,	$\overline{\text{RXI}}$ at 0 V,	Current measured at RXI and $\overline{\text{RXI}}$		3	
	RXI at 16 V,	$\overline{\text{RXI}}$ at open,	Current measured at RXI		10	
	RXI at open,	$\overline{\text{RXI}}$ at 16 V,	Current measured at $\overline{\text{RXI}}$		10	
	RXI at 16 V,	$\overline{\text{RXI}}$ at 16 V,	Current measured at RXI and $\overline{\text{RXI}}$		10	

† Fault conditions should be measured on only one channel at a time.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

driver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	TXI	TXO, $\overline{TXO}$	TXEN at 2 V, See Figure 3		15	ns
t_{PHL}	Propagation delay time, high-to-low level output	TXI	TXO, $\overline{TXO}$	TXEN at 2 V, See Figure 3		15	ns
t_{PIL}	Propagation delay time, idle-to-low level output	TXI	TXO, $\overline{TXO}$	TXEN at 2 V, See Figure 4		25	ns
t_{PIL}	Propagation delay time, idle-to-low level output	TXEN	TXO, $\overline{TXO}$	TXI at 3.2 V, See Figure 5		25	ns
t_w	Output pulse duration from low-to-high level to 70% output level		TXO, $\overline{TXO}$	TXEN at 2 V, See Figure 6	260	8000	ns
$V_{OD(U)}$	Driver output differential undershoot voltage	TXI	TXO, $\overline{TXO}$	TXEN at 2 V, See Figure 6		−100	mV
t_{sk}	Driver caused signal skew $t_{PLH} - t_{PHL}$	TXI	TXO, $\overline{TXO}$	TXEN at 2 V, See Figure 3		±3	ns
t_r	Rise time, TXO, $\overline{TXO}$			TXEN at 2 V, See Figure 3	1	5	ns
t_f	Fall time, TXO, $\overline{TXO}$			TXEN at 2 V, See Figure 3	1	5	ns

receiver

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	$\overline{RXI}$, RXI	RXO	V_{IC} = 1 V to 4.2 V, See Figure 10		15	ns
t_{PHL}	Propagation delay time, high-to-low level output	$\overline{RXI}$, RXI	RXO	V_{IC} = 1 V to 4.2 V, See Figure 10		15	ns
t_{PLH}	Start-up delay time, low-to-high level output	$\overline{RXI}$, RXI	RXEN	V_{IC} = 1 V to 4.2 V, V_{ID} = −500 mV, See Figure 12		55	ns
t_{PHL}	Shutdown delay time, high-to-low level output	$\overline{RXI}$, RXI	RXEN	V_{IC} = 1 V to 4.2 V, V_{ID} = 500 mV, See Figure 12	142	181	ns
t_{sk}	Receiver caused signal skew ($t_{PLH} - t_{PHL}$)	$\overline{RXI}$, RXI	RXO	V_{IC} = 1 V to 4.2 V, V_{ID} = 500 mV, See Figure 10		±3	ns
t_w	Pulse duration at $\overline{RXI}$ and RXI (to not activate squelch)			V_{IC} = 1 V to 4.2 V, V_{ID} = −175 mV, See Figure 11	25		ns
t_w	Pulse duration at $\overline{RXI}$ and RXI (to activate squelch)			V_{IC} = 1 V to 4.2 V, V_{ID} = −275 mV, See Figure 11		50	ns
t_{r1}	Rise time, RXO			V_{IC} = 1 V to 4.2 V, V_{ID} = ±500 mV, See Figure 10	1	8	ns
t_{r2}	Rise time, RXEN			V_{IC} = 1 V to 4.2 V, V_{ID} = ±500 mV, See Figure 12	1	8	ns
t_{f1}	Fall time, RXO			V_{IC} = 1 V to 4.2 V, V_{ID} = ±500 mV, See Figure 10	1	8	ns
t_{f2}	Fall time, RXEN			V_{IC} = 2.5 V, V_{ID} = ±500 V, See Figure 12	1	8	ns
t_v	RXO valid after RXEN high			See Figure 10	−10	15	ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

loop

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	TXI	RXO	LOOP at 0.8 V, TXEN at 2 V, See Figure 13		30	ns
t_{PHL}	Propagation delay time, high-to-low level output	TXI	RXO	LOOP at 0.8 V, TXEN at 2 V, See Figure 13		30	ns
t_{PLH}	Propagation delay time, low-to-high level output	TXEN	RXEN	LOOP at 0.8 V, See Figure 14		50	ns
t_{PHL}	Propagation delay time, high-to-low level output	TXEN	RXEN	LOOP at 0.8 V, See Figure 14		50	ns

PARAMETER MEASUREMENT INFORMATION

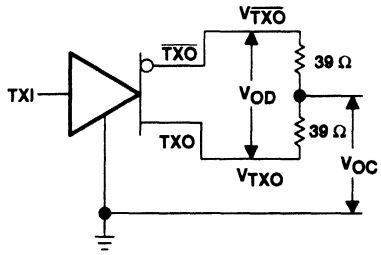


Figure 1. Driver Test Circuit

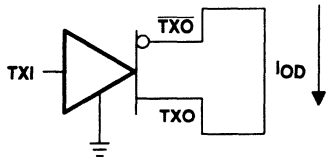
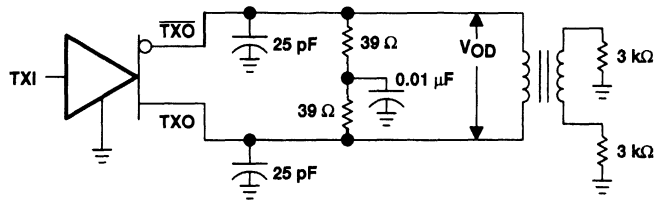
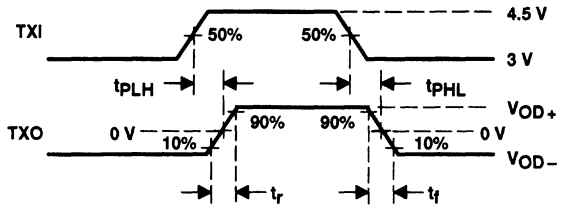


Figure 2. Driver Test Circuit

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



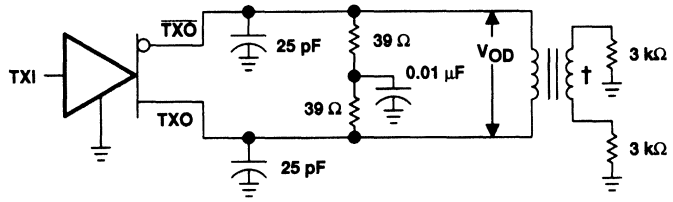
VOLTAGE WAVEFORMS

TRANSFORMER SPECIFICATIONS

Turns Ratio	1:1
Magnetizing Inductance	26 to 30 μH
Winding Resistance	0.6 Ω Max
Rise Time 10% to 90%	5 ns Max
Interwinding Capacitance	25 pF
Leakage Inductance	0.25 μH Max
Inductive Q	1250 Min

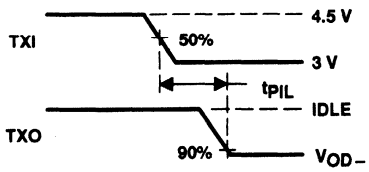
Figure 3. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



† See Figure 3

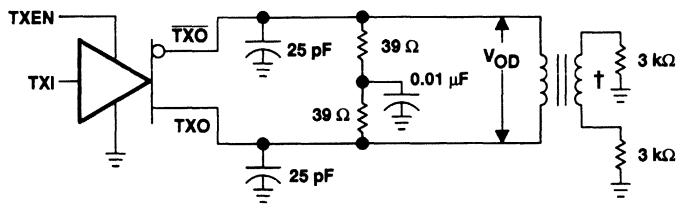
TEST CIRCUIT



VOLTAGE WAVEFORMS

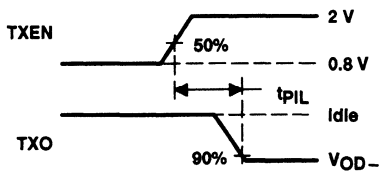
NOTE: Input $t_r \leq 5$ ns; $t_f \leq 5$ ns

Figure 4. Test Circuit and Voltage Waveforms



† See Figure 3

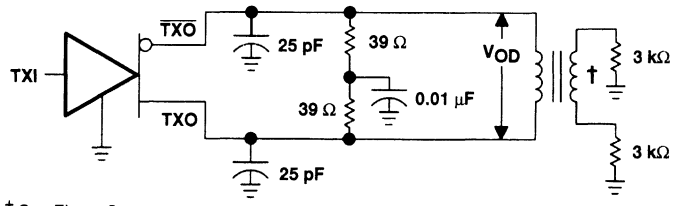
TEST CIRCUIT



VOLTAGE WAVEFORMS

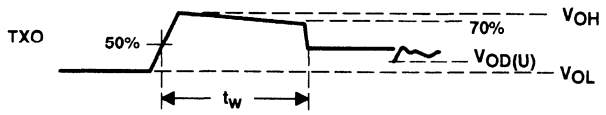
Figure 5. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



† See Figure 3

TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 6. Test Circuit and Voltage Waveforms

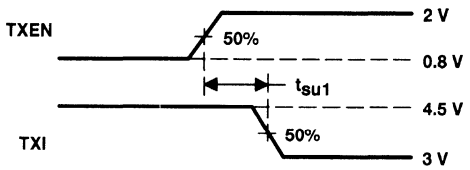


Figure 7

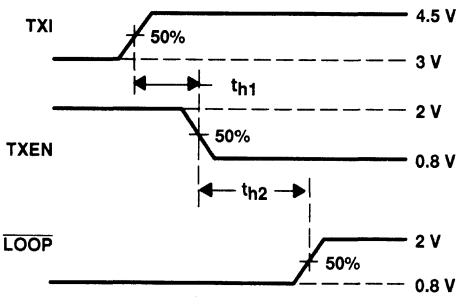


Figure 8

NOTE: Input $t_r \leq 5$ ns; $t_f \leq 5$ ns

PARAMETER MEASUREMENT INFORMATION

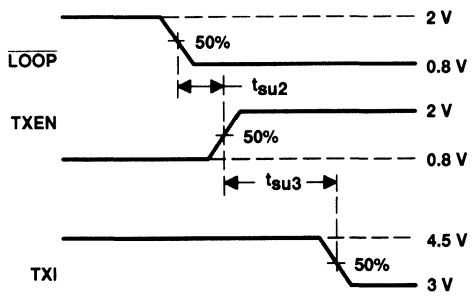
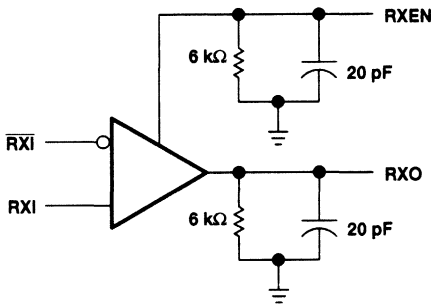
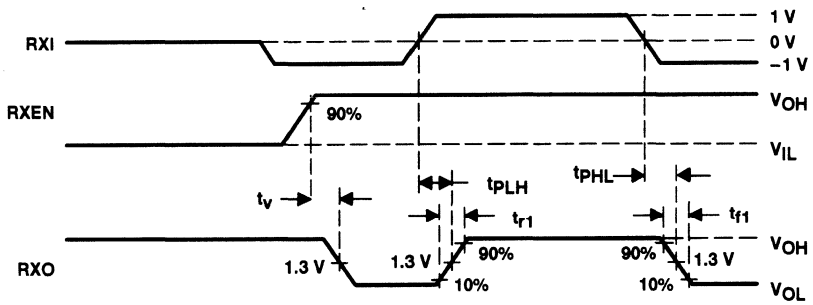


Figure 9



TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 10. Test Circuit and Voltage Waveforms

NOTE: Input $t_r \leq 5$ ns; $t_f \leq 5$ ns

PARAMETER MEASUREMENT INFORMATION

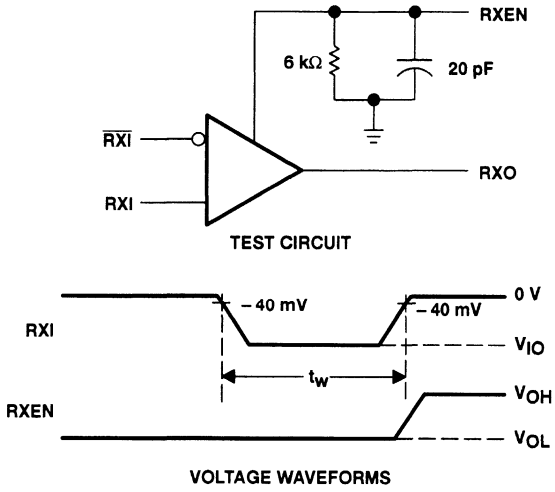


Figure 11. Test Circuit and Voltage Waveforms

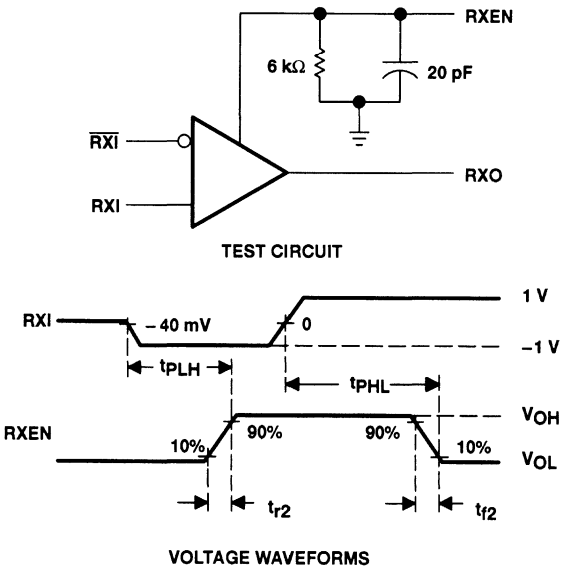


Figure 12. Test Circuit and Voltage Waveforms

NOTE: Input $t_r \leq 5$ ns; $t_f \leq 5$ ns

PARAMETER MEASUREMENT INFORMATION

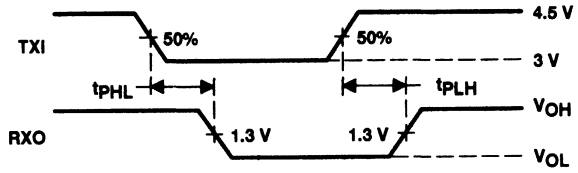


Figure 13

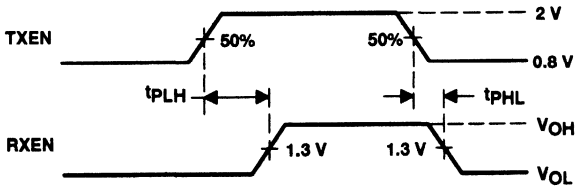


Figure 14

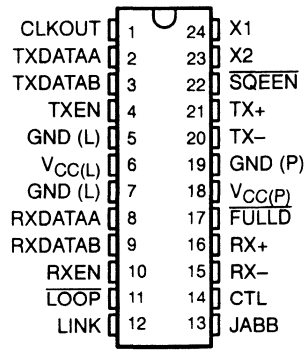
NOTE: Input $t_r \leq 5$ ns; $t_f \leq 5$ ns

SN75LBC086
DIFFERENTIAL I/O DRIVER/RECEIVER PAIR WITH SQUELCH, JABBER CONTROL, AND COLLISION DETECTION

SLLS120A – JUNE 1991 – REVISED SEPTEMBER 1991

- **Meets or Exceeds the IEEE STD 802.3I, Type 10BASE-T**
- **Differential (Twisted-Pair) I/O Driver/Receiver**
- **High-Speed Receiver . . . t_{pd} = 50 ns Max**
- **Receiver Squelch Circuit Integrity Improved With Noise Filter**
- **Jabber Control Prevents Network Lockup**
- **Collision Detection for Multiple-User Networks**
- **Data Link Integrity Monitored With Link Test Pulse**
- **Externally Addressable Test Register Controls Signal Quality Error Testing**
- **CMOS and Raised ECL Compatible**
- **24-Terminal, 300-mil Dual-In-Line Package**

DW PACKAGE
(TOP VIEW)



description

The SN75LBC086 is a single-channel differential driver/receiver interface device for the medium attachment unit (MAU) used in 10-MHz twisted-pair Ethernet applications. The device uses a 5-V supply and is designed to interface with two pairs of telephone-grade twisted-pair cables coupled through isolation transformers. The functional components of the device include a differential receiver and driver, receiver squelch with noise filter, jabber controls, collision detection, data link monitor, and signal quality error (SQE) testing. The LinBiCMOS™ process technology is used in the device design to ensure analog precision, low power, and high-speed operation.

The device contains an elaborate receiver-squelch circuit† that provides an improved level of noise rejection by qualifying the incoming signal stream with three different criteria. First, the signal is compared to a set threshold voltage level. Then, the pulse duration is compared to a set time window. Last, the signal must follow a set pattern of positive and negative pulses before the circuit finally opens the receiver channel to the incoming data packet.

The jabber control is designed to prevent a defective controller from locking up the network by limiting the data packet transmission time to 20 to 30 ms. When a packet length exceeds 20 to 30 ms, the driver is turned off for about 600 ms. The driver-enable input must be made inactive by the controller during this period before the jabber control will release the driver. The JABB output is active (high) when a jabber condition exists.

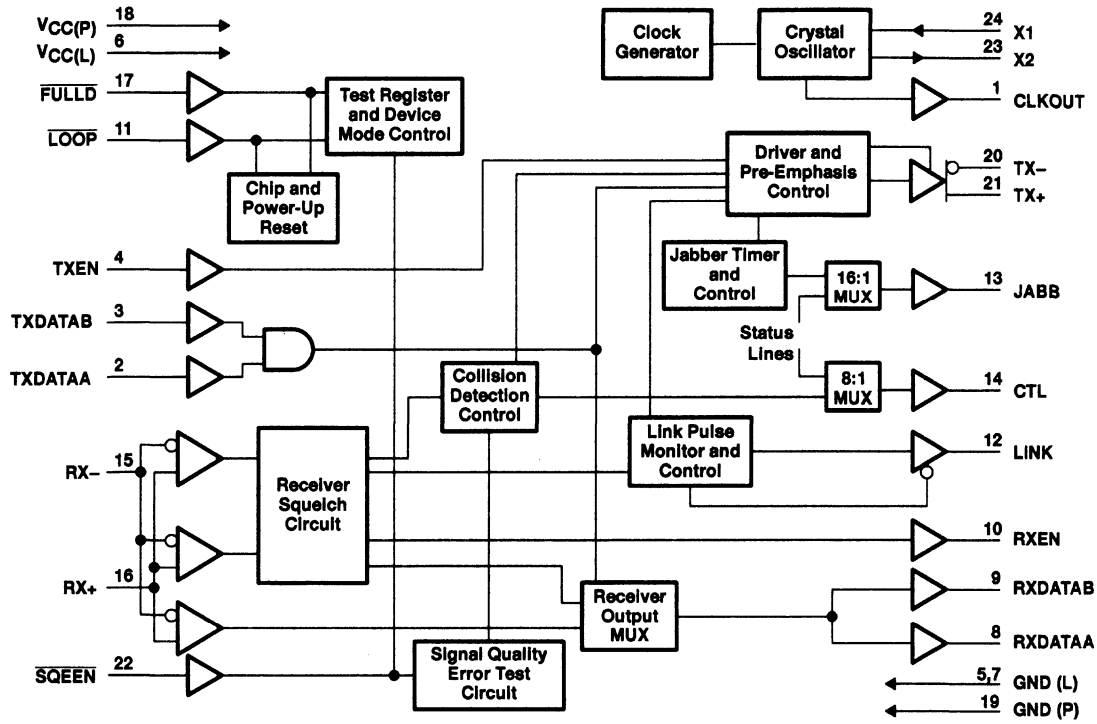
Collision detection is used to arbitrate access to the multiuser network. This detection is done logically by monitoring the receive line for a valid signal during a driver transmission. When a collision is detected, this device informs the controller with an active-high CTL output. After a valid packet transmission, the device also performs a signal quality error test causing the CTL output to go active (high). This test is disabled when the $\overline{\text{SQEEN}}$ input goes inactive (high).

The device tests data-link integrity during the idle state by periodically driving the driver line with a unipolar pulse called a link-test pulse. The receiver looks for this link-test pulse on the receive line. A failed line link is indicated by a high-impedance state at the LINK output. This output drives an LED for monitoring if needed.

An internal test register is externally controlled with inputs $\overline{\text{FULLD}}$ and $\overline{\text{LOOP}}$ to select the device testing mode. When in the test mode, serial test-mode control patterns are clocked into the test register through input $\overline{\text{SQEEN}}$. These control patterns select various modes to test the internal circuits.

† Embodies technology covered by one or more Digital Equipment Corporation Patents.
LinBiCMOS is a trademark of Texas Instruments Incorporated.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL LEVEL	TERMINAL NO.	I/O	DESCRIPTION
CLKOUT	CMOS	1	O	Clock output. This 10-MHz buffered clock drives other interface devices.
CTL	CMOS	14	O	Control. In normal mode, CTL high indicates a collision. In test mode, status lines are muxed out.
$\overline{\text{FULLD}}$	TTL	17	I	Full-duplex mode. When active (low), the device is placed in the full-duplex operating mode for simple point-to-point communication applications. In the full-duplex mode, the receiver and driver are both active with collision detection disabled. After $\overline{\text{LOOP}}$ and $\overline{\text{FULLD}}$ go active (low), in that order, a device reset is initiated and while both are active (low), test select data clocks into the test register using a 100-ns clock at the X1 input. This terminal is held inactive (high) due to an internal pullup resistor.
GND (L)	GROUND	5 7		Logic grounds. These terminals provide a ground return for the CMOS core logic.
GND (P)	GROUND	19		Power ground. This provides a ground return for the input and output buffers, driver (transmitter), and receiver circuits.
JABB	CMOS	13	O	Jabber control. When a jabber condition exists during normal mode operation, this signal goes active (high) to report jabber-control status to the controller. In the test mode, this provides a multiplexed signal for internal timer and counter functions.
LINK	CMOS	12	O	Link status. This 3-state output indicates the status of the receiver and interface link. When driving an LED (with anode to resistor to V_{CC}), a high-impedance level indicates a failed link and the LED is off. A momentary high level indicates the device is receiving valid data and the LED is blinking on and off. A continuous low level indicates the device is receiving valid link pulses but no data, and the LED is on.
$\overline{\text{LOOP}}$	TTL	11	I	Loop-back mode. When the device is in the normal operating mode (not test mode) and $\overline{\text{LOOP}}$ is active (low), the driver (transmit) data is directed to the receive data path to put the device in the loop-back mode and the driver is turned off. After $\overline{\text{LOOP}}$ and $\overline{\text{FULLD}}$ go active (low), in that order, a device reset is initiated and while both are active (low), test select data clocks into the test register using a 100-ns clock at the X1 input. This terminal is held inactive (high) due to an internal pullup resistor.
RX+		16	I	Differential receiver inputs
RX–		15	I	
RXEN	CMOS	10	O	Receiver squelch status. This provides squelch status information to the controller. When active (high), this signal indicates that the data path is valid or open from the receive channel through the device. An inactive (low) indicates that the receive channel is squelched or closed. This signal is capable of driving an LED monitor.
RXDATAA RXDATAB	CMOS ECL	8 9	O O	Received-data serial outputs. These outputs provide a choice of logic levels and serial data either from the differential receiver input (RX+ and RX–) or data from the controller (TXDATAA or TXDATAB) when in the loop-back mode. When the receiver is idle, these output levels are normally high. These terminals are held inactive (high) due to an internal pullup resistor.
$\overline{\text{SQEEN}}$	TTL	22	I	Signal-quality error-test enable. In normal operating mode, this enables the SQE test function performed at the end of a data packet transmission. In the test mode, $\overline{\text{SQEEN}}$ is used (with X1 clock) as a serial data input port to load test patterns or selections into the test register. This terminal is held inactive (high) due to an internal pullup resistor.
TX+		21	O	Differential driver outputs
TX–		20	O	
TXEN	TTL	4	I	Transmitter (driver) enable. When TXEN is active (high), serial data at the TXDATA inputs starts and stops the driver. When TXEN is inactive (low), the driver begins transmitting an idle signal independent of the TXDATA inputs.
TXDATAA TXDATAB	CMOS ECL	2 3	I I	Transmit-data inputs. A choice of logic-level inputs provide Manchester-encoded serial data to the driver. Internal pullup resistors are included.
$V_{CC(L)}$	SUPPLY	6		V_{CC} logic power supply. This provides power to the CMOS core logic.
$V_{CC(P)}$	SUPPLY	18		V_{CC} power supply. This provides power to the input and output buffers, drivers, and receivers.
X1 X2	CMOS	24 23	I O	Crystal input/output. X1 provides an input from an external 10-MHz crystal or another external clock source when the crystal is disconnected. X2 provides an oscillator output.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Input voltage range at any input, V_I ..... −0.5 V to 5.5 V
Output voltage range at any output, V_O ..... −0.5 V to 7 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to device ground pins GND(L) and GND(P) shorted together.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1350 mW	10.8 mW/°C	864 mW

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}			4.75	5	5.25	V
High-level output voltage, V_{IH}	TXDATAA, X1		3.15			V
	TXDATAB (see Figure 1)	T_A = 0°C	$0.984V_{CC}-0.922$		$0.984V_{CC}-0.763$	
		T_A = 25°C	$0.984V_{CC}-0.877$		$0.984V_{CC}-0.727$	
		T_A = 70°C	$0.984V_{CC}-0.825$		$0.984V_{CC}-0.645$	
	TXEN, $\overline{\text{LOOP}}$, $\overline{\text{FULLD}}$, $\overline{\text{SQEEN}}$		2			
Low-level output voltage, V_{IH}	TXDATAA, X1				0.8	V
	TXDATAB (see Figure 1)	T_A = 0°C	$0.75V_{CC}-0.59$		$0.75V_{CC}-0.375$	
		T_A = 25°C	$0.75V_{CC}-0.55$		$0.75V_{CC}-0.35$	
		T_A = 70°C	$0.75V_{CC}-0.531$		$0.75V_{CC}-0.324$	
	TXEN, $\overline{\text{LOOP}}$, $\overline{\text{FULLD}}$, $\overline{\text{SQEEN}}$				0.8	
Differential input voltage, V_{ID}			0.586		2.8	V
Common-mode input voltage, V_{IC}			1.8		3.2	V
Operating free-air temperature, T_A			0		70	°C

electrical characteristics over recommended operating free-air temperature and supply voltage range (unless otherwise noted)

drivers

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	CLKOUT, RXDATAA, RXEN, JABB, CTL	I_{OH} = –12 mA		3.7			V
		RXDATAB	See Figure 1	T_A = 0°C	0.984 V_{CC}–0.922		0.984 V_{CC}–0.763	V
				T_A = 25°C	0.984 V_{CC}–0.877		0.984 V_{CC}–0.727	
				T_A = 70°C	0.984 V_{CC}–0.825		0.984 V_{CC}–0.645	
V_{OL}	Low-level output voltage	CLKOUT, RXDATAA, RXEN, JABB, CTL	I_{OL} = 16 mA				0.5	V
		RXDATAB	See Figure 1	T_A = 0°C	0.75 V_{CC}–0.59		0.75 V_{CC}–0.375	V
				T_A = 25°C	0.75 V_{CC}–0.55		0.75 V_{CC}–0.35	
				T_A = 70°C	0.75 V_{CC}–0.531		0.75 V_{CC}–0.324	
		LINK	I_{OL} = 12 mA				0.5	V
V_{OD}	Differential-output voltage (peak)		See Figure 2		2.2		2.8	V
V_{OD}	Differential-output voltage (step)		See Figure 2		1.53		1.982	V
	Common-mode driver impedance	TX+, TX–			2	5	8	Ω

receivers

PARAMETER			TEST CONDITIONS†	MIN	MAX	UNIT
I_{IH}	High-level input current	TXDATAA, TXEN, $\overline{LOOP}$, $\overline{FULLD}$, $\overline{SQEEN}$	V_I = 5.25 V		20	μA
		X1			100	
		TXDATAB	V_{IH} = MAX		400	
I_{IL}	Low-level input current	TXDATAA, TXEN, $\overline{LOOP}$, $\overline{FULLD}$, $\overline{SQEEN}$	V_I = 0		–20	μA
		X1			–100	
		TXDATAB	V_{IL} = MIN		–400	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

drivers and receivers

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
I_{CC}	Supply current	$V_{CC(L)}$, $V_{CC(P)}$	$V_{CC(L)}$ = 5.25 V, $V_{CC(P)}$ = 5.25 V		180	mA

switching characteristics

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	Propagation delay time	RX+, RX–	RXEN	See Figure 4			5 bit times	
t_{pd2}	Propagation delay time at startup	RX+, RX–	RXDATAA or RXDATAB high	See Figure 4			75	ns
$t_{sk(o)}$	Output skew time	RXEN high	RXDATAA or RXDATAB low	See Figure 4			±10	ns
t_{pd3}	Propagation delay time after startup	RX+, RX–	RXDATAA or RXDATAB high	See Figure 4			50	ns
$t_{sk(p)}$	Pulse skew time ($\|t_{pd3(LH)} - t_{pd3(HL)}\|$)	RX+, RX–	RXDATAA or RXDATAAB	See Figure 4		2		ns
t_{pd4}	Propagation delay time	RX+, RX–	RXEN low	See Figure 5	155		250	ns
t_{pd5}	Propagation delay time	TXDATA or TXDATAB	TX+, TX–	See Figure 6			75	ns
$t_{sk(p)}$	Pulse skew time ($t_{pd5(LH)} - t_{pd5(HL)}$)	TXDATAA or TXDATAB	TX+, TX–	See Figure 6		2		ns
t_{pd6}	Propagation delay time in loop mode	TXDATAA or TXDATAB	RXDATAA, RXDATAB	See Figure 7			50	ns
t_{pd7}	Propagation delay time in loop mode	TXEN high	RXEN high	See Figure 7			50	ns
t_{pd8}	Propagation delay time in loop mode	$\overline{\text{LOOP}}$ low	RXEN low	See Figure 7			30	ns
t_{pd10}	Propagation delay time	TXEN low	RXEN low	See Figure 8			350	ns
t_{pd11}	Propagation delay time	TXEN low	TX+, TX– high	See Figure 8			50	ns
t_{p1}	Precompensation pulse duration		TX+, TX–	See Figure 6	45		55	ns
t_{p2}	Receiver link-beat minimum pulse duration			See Figure 9	80		120	ns
t_{en1}	Enable time	TXDATAA or TXDATAB	TX+, TX–	See Figure 6			75	ns
t_{en2}	Enable time	TXEN	TX+, TX–	See Figure 6			75	ns
t_{dis1}	Disable time, caused by TXDATAA or TXDATAB high or TXEN low	TX+, TX– high	TX+, TX– at 585-mV level	See Figure 8	250			ns
t_{pd12}	Propagation delay time to looped RXEN	TXEN high	RXEN high	See Figure 6			100	ns
t_{pd13}	Propagation delay time for looped back data	TXDATAA or TXDATAB	RXDATAA RXDATAB	See Figure 6			75	ns

timing requirements

	TEST CONDITIONS	MIN	MAX	UNIT
Setup time, test mode, $\overline{\text{SQEEN}}$ before X1↑, t_{su1}	See Figure 10	30		ns
Setup time, test mode, $\overline{\text{LOOP}}$ low before FULLD↓, t_{su2}	See Figure 10	25		ns
Hold time, test mode, $\overline{\text{SQEEN}}$ after X1↑, t_{h1}	See Figure 10	25		ns

PARAMETER MEASUREMENT INFORMATION

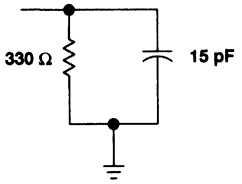


Figure 1. ECL Load Circuit

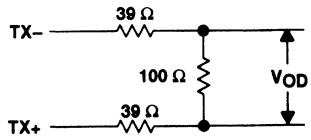


Figure 2. Differential Load Circuit

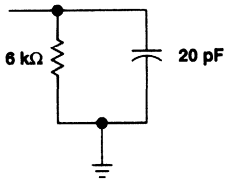


Figure 3. CMOS Load Circuit

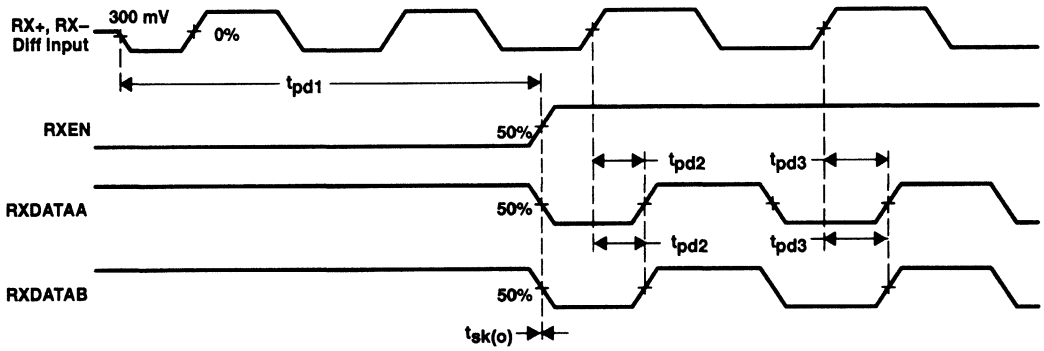


Figure 4. Receiver Startup Waveforms

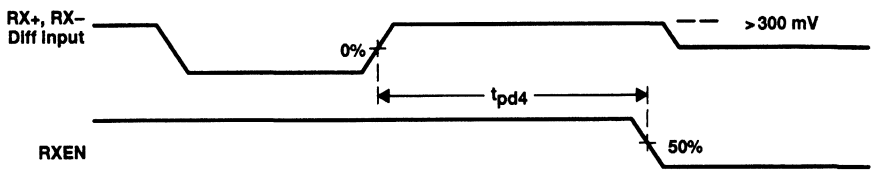


Figure 5. Receiver Shutdown Waveforms

PARAMETER MEASUREMENT INFORMATION

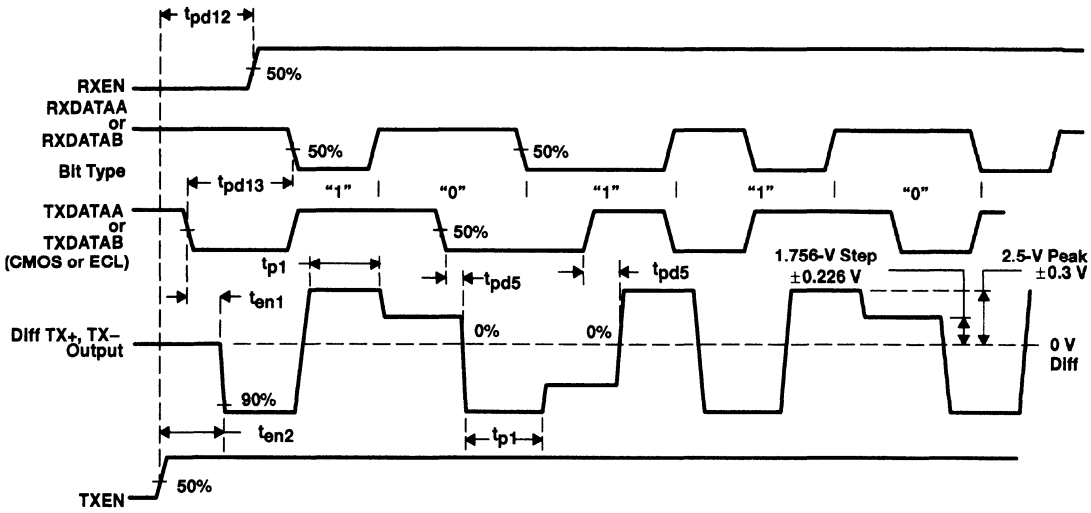


Figure 6. Driver Startup Waveforms

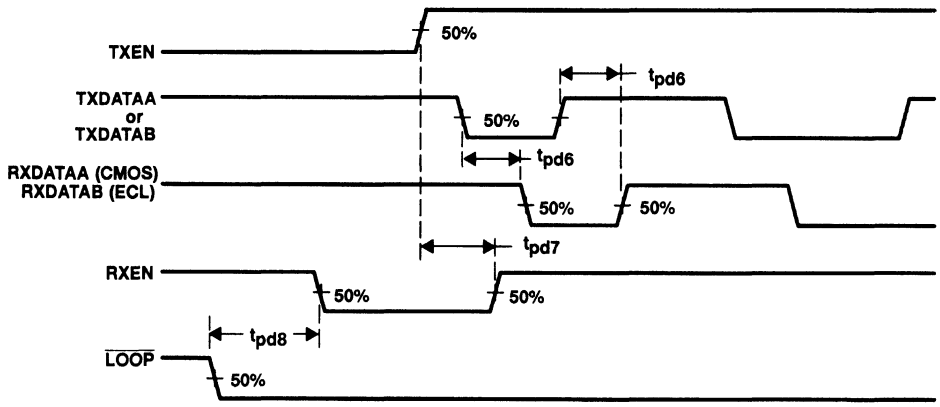


Figure 7. Propagation Delay Waveforms in Loop Mode

PARAMETER MEASUREMENT INFORMATION

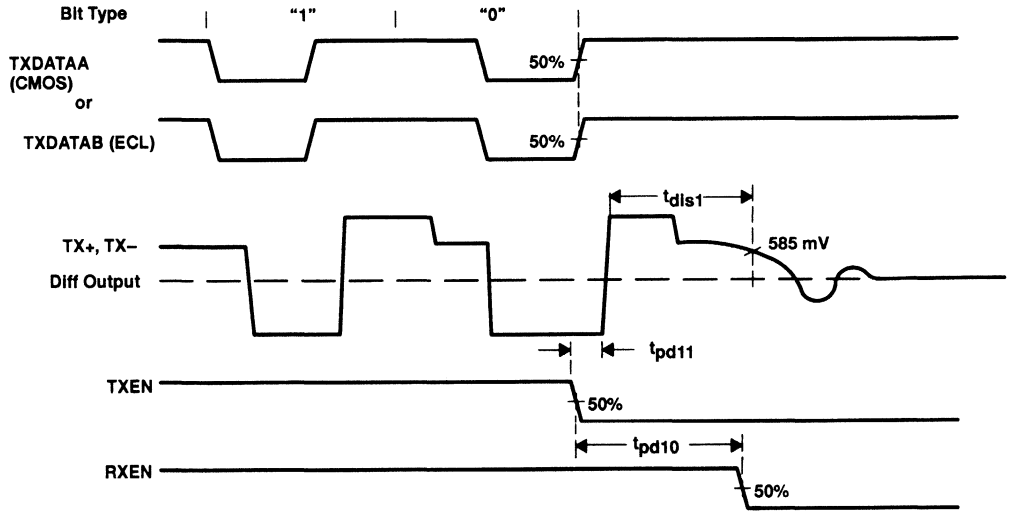


Figure 8. Driver Shutdown Waveforms

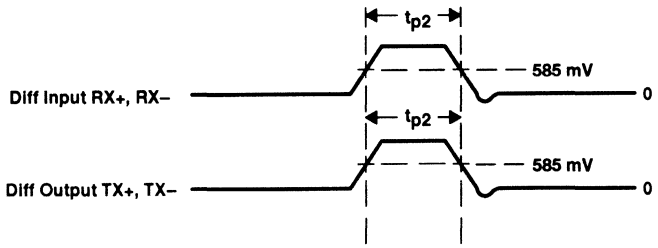


Figure 9. Link Beat Pulse Duration Waveform

PARAMETER MEASUREMENT INFORMATION

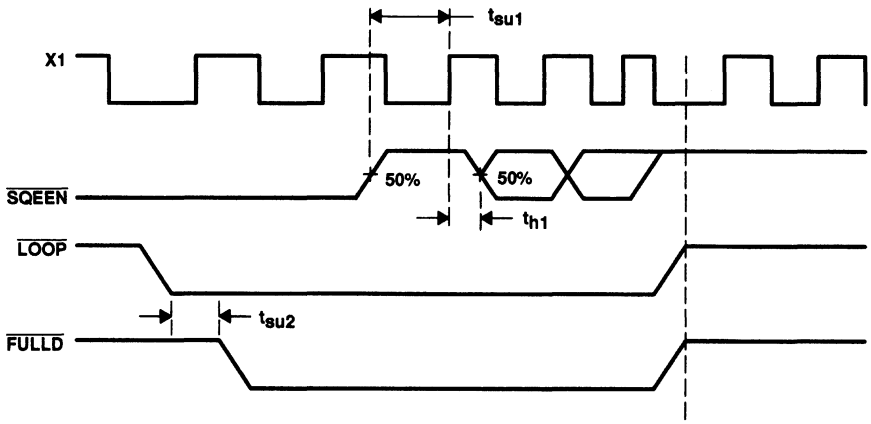
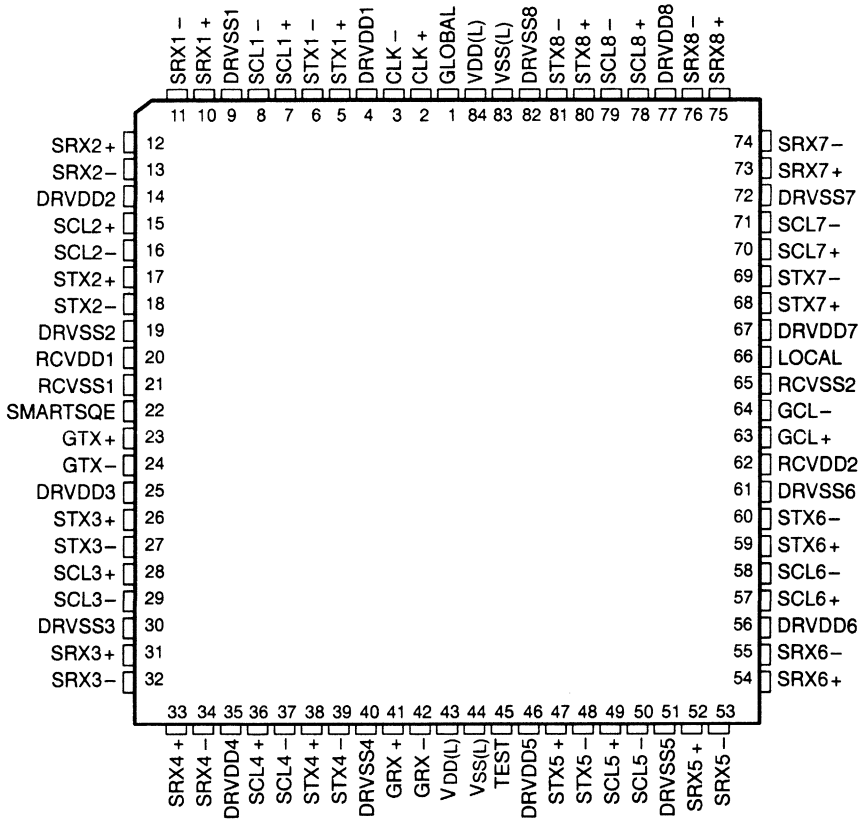


Figure 10. Setup and Hold Time Waveforms

SLLS150A – DECEMBER 1992 – REVISED MAY 1993

- **Meets or Exceeds the Standards Set by ISO 8802.3:1990 and ANSI/IEEE 802.3-1990**
- **Receiver Squelch Circuit Integrity Improved With Noise Filter**
- **Differential (Twisted-Pair) I/O Driver and Receiver**
- **84-Pin, Plastic Leaded Chip Carrier (PLCC) Package**
- **Control Logic Function for Local and Global Modes**
- **Low Port-to-Port Data Propagation Delay**
- **Drives Twisted-Pair Transmission Lines Up to 50 Meters**
- **Collision Detection for Multiple-User Networks**

FN PACKAGE
(TOP VIEW)



description

The SN75LBC088 attachment unit interface (AUI) concentrator chip (ACC) incorporates eight data terminal equipment (DTE) or station ports and one medium attachment unit (MAU) or global port on the same chip for connection to a local area network (LAN). Each station port emulates the driver/receiver functionality, timing, and signal response of a transceiver or MAU designed to meet the IEEE 802.3-1990 standard. The functional components of the ACC are a differential driver, collision detection driver, and a differential line receiver/squelch.

description (continued)

This device also has two operational modes, local and global, and a self-exerciser test mode. The SN75LBC088 uses the LinBiCMOS™ process technology to ensure high-speed operation, analog precision, and low power consumption.

Each of the eight station ports includes two differential drivers (STX1 thru STX8 [STXx] and SCL1 thru SCL8 [SCLx]) and one differential receiver [SRX1 thru SRX8 (SRXx)]. The SRXx (station receive) input pair is for receiving data sent from the station to the network. The STXx (station transmit) output pair is for transmitting network data to the station. The SCLx (station collision) output pair transmits the collision condition to the station.

The global port supports one differential driver (GTX) and two differential receivers (GRX and GCL). The GTX output pair drives data from a station port to the network. The GRX input pair receives network data from the external transceiver and channels it to all eight station ports. The GCL input pair receives network collision status to be forwarded to the individual station ports.

Each station port differential output pair of the SN75LBC088 drives a 78-Ω, balanced, terminated, twisted-pair transmission line up to 50 meters. In the off or idle state, the drivers maintain minimal differential output voltage on the twisted-pair lines and remain within the required output common-mode range. When the driver is internally enabled, the driver goes through what is called a soft start or half-step driver start up due to the first transition out of idle swings only half the normal differential amplitude. The differential outputs then rise to full amplitude output levels within 35 ns. The output amplitude is maintained for the remainder of the packet. After the last transmitted packet positive edge, the driver's enable circuit maintains the differential potential above the output common-mode voltage for at least 210 ns, decay down to a minimum differential voltage, and then return to an idle state. Each driver powers up in the idle state to ensure no activity is placed on the twisted-pair cable that could be interpreted as network traffic.

The line receiver squelch function interfaces to a differential twisted-pair line terminated external to the device. The receiver squelch circuit allows differential receive signals to pass through while the input amplitude and pulse duration are greater than the minimum squelch threshold. This ensures a good signal-to-noise ratio while the data path is active and prevents system noise from causing false data transitions during line shut-down and line-idle conditions.

The SN75LBC088 functional control logic operates in two externally switched modes, local and global. Depending on the selected mode, the internal control logic selects the proper internal data path routing and collision handling. The internal data path is altered prior to enabling external line drivers to prevent data transmissions occurring during data path multiplexing.

Local mode is the simplest of the two modes of operation. While all SRXx input receivers from the stations are inactive, the device is in an idle state. The idle state disables all the STXx and SCLx output drivers to the stations. While in local mode, all control signals to and from the global port are logically disabled by the control logic. When transmit activity is detected on any of the eight SRXx input receivers, the channel's internal squelch goes high. While this condition exists, the single SRXx receiver is routed to all STXx drivers. When the transmission is complete, the channel's internal squelch returns low. This starts an end-of-packet hold on all the STXx output drivers. The driver switches to the idle state after the hold time has elapsed. During the specified squelch (SQE) test interval, the SN75LBC088 internally generates a SQE test burst. When Smart SQE is enabled (SMARTSQE pulled low), the SQE test burst is sent to the SCLX output of the station that transmitted last. If Smart SQE is not enabled, it sends the burst to all the SCLx outputs.The device recognizes a collision when one station is active and any other station(s) becomes active. The device then places a 10-MHz collision signal on all the SCLx output drivers. All STXx data is considered undefined during a collision. The STXx drivers are shut down while the SCLx drivers are active and are not reactivated until all SRXx receiver activity is finished. The device returns to the idle state after all transmit traffic has ceased.

description (continued)

In global mode, the local station users are logically connected to the LAN backbone media. Global mode has two types of signal flow patterns: station to other stations and the LAN, and the LAN to all stations. When a station starts to transmit, its squelch deactivates and is considered active. The control logic then selects the active channel's data for transmission to the LAN. Unlike the local mode, the other stations do not get the data directly from the active port. Data first reaches the transceiver, gets looped back, and then is sent to the eight STXx drivers. This action emulates the operation between a station and a transceiver in a normal point-to-point link.

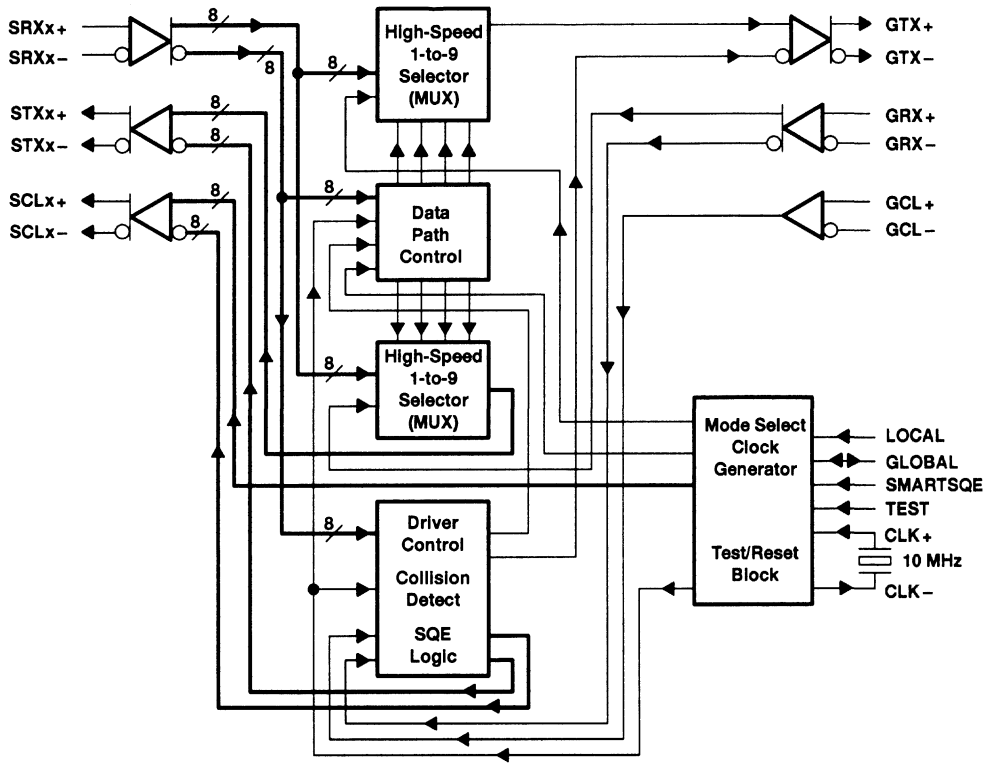
In global mode, local and global collisions are handled differently. For a local collision, the device cannot force a collision on the LAN backbone directly. To create a collision on the LAN, the device transmits a 5-MHz signal onto the GTX drivers to force activity on the LAN segment. Any LAN activity collides with this forced 5-MHz signal and is seen as a collision by the collision receiver. This action keeps the network synchronized. After the global port's data loops back from the LAN, the collision signal is sent to all the local nodes via the SCLx output drivers.

A global collision (collision on the network) is handled normally since station transmit data is routed to the GTX driver. In this instance, data sources are directly in collision. Once a collision is detected on the network, the transceiver asserts a collision signal that is detected on the GCL input receiver. The GCL receiver collision signal is then routed to all the SCLx output drivers tied to the stations.

In global mode, the transceiver generates SQE. When a station finishes a transmission, the transceiver generates the SQE. This is detected on the GCL input. When Smart SQE is enabled (SMARTSQE pulled low), the SQE is sent to the station that originated the transmission. Because of this activity, the ACC has to remember which station transmitted the last signal and only allow collision back to that station during the SQE window. Once the SQE passes, the ACC then allows a collision signal back to all stations to indicate a network collision. When Smart SQE is disabled, the SQE signal is routed to all station collision lines (SCLx).

The SN75LBC088 supports a self-exerciser test mode. The self-exerciser mode tests all the drivers and receivers on the chip. This mode is invoked by pulling both GLOBAL and TEST low. While in the self-exerciser mode, a 6.4-µs packet is generated of consistent preamble on the GTX driver port with a 6.4-µs idle time. The GTX driver, with the help of loop back connectors, routes the preamble to both the GRX and the GCL receivers. The GRX data is then sent internally to all the STXx drivers. External connectors on the STXx drivers individually loop this data back to the local SRXx receiver. When the squelch for a receiver is turned off and the global GCL receiver is unsquelched, the collision driver for that receiver starts sending a collision signal. Each port drives a collision signal based on its own SRXx receiver squelch being held high and the presence of a global collision signal, therefore exercising all the drivers and receivers on the chip.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLK–	3	O	Clock output. Output for an external series-resonant 10-MHz crystal required for internal timing.
CLK+	2	I	Clock input. Input for an external series-resonant 10-MHz crystal required for internal timing. The CLK+ accepts an external TTL level clock also.
DRVDDx	4, 14, 25, 35, 46, 56, 67, 77		V_{DD} power supply. These terminals provide power to the drivers.
DRVSSx	9, 19, 30, 40, 51, 61, 72, 82		V_{SS} power ground. These terminals provide a ground return for the driver circuits.
GCL–	64	I	Global collision. Differential inputs that receive the network collision status for forwarding to the individual station ports.
GCL+	63	I	
GLOBAL	1	I/O	Global. This is a bidirectional terminal. When functioning as an output, the chip is in a test mode and monitors internal nodes that are multiplexed to it. When functioning as an input, the terminal is pulled low (LOCAL held high) and the station ports are connected to the LAN. This terminal is held inactive (high) with an internal pullup resistor.
GRX–	42	I	Global receive. Differential inputs that receive network data from an external transceiver and route it to all eight station ports.
GRX+	41	I	
GTX–	24	O	Global transmit. Differential outputs that transmit data from one of eight station ports to the network.
GTX+	23	O	
LOCAL	66	I	Local. When in local mode, this terminal is pulled low (GLOBAL held high) and the station ports are disconnected from the LAN. This terminal is held inactive (high) with an internal pullup resistor.
RCVDD1	20		V_{DD} power supply. These terminals provide power to the receivers.
RCVDD2	62		
RCVSS1	21		V_{SS} power ground. These terminals provide a ground return for receivers.
RCVSS2	65		
SCLx–	8, 16, 29, 37 50, 58, 71, 79	O	Station port collision. Differential outputs that transmit the collision condition to the station. When during any station transmit activity one or more additional stations become active, the device recognizes this as a collision. The device then places a 10-MHz collision signal on all of the SCLx output drivers.
SCLx+	7, 15, 28, 36, 49, 57, 70, 78	O	
SRX–	11, 13, 32, 34, 53, 55, 74, 76	I	Station port receive. Differential input for receiving data from the station to the network.
SRX+	10, 12, 31, 33, 52, 54, 73, 75	I	
STX–	6, 18, 27, 39, 48, 60, 69, 81	O	Station port transmit. Differential output for transmitting network data to the the station.
STX+	5, 17, 26, 38, 47, 59, 68, 80	O	
SMARTSQE	22	I	This input enables the smart SQE circuitry. In normal operating mode, this enables the SMARTSQE test function performed at the end of a data packet transmission. In the test mode, SMARTSQE works with TEST to place the chip into a special mode. This terminal is held inactive (high) with an internal pullup resistor.
TEST	45	I	Test. To invoke the self-exerciser test mode, this terminal and GLOBAL are enabled.
$V_{DD(L)}$	43, 84		V_{DD} logic power supply. These terminals provide power to the CMOS logic.
$V_{SS(L)}$	44, 83		V_{SS} logic ground. These terminals provide power to a ground return for the CMOS logic.

MODE CONFIGURATION

GLOBAL	LOCAL	SMARTSQE	TEST	CHIP CONFIGURATION
H	L	H	H	Local mode, no SQE
H	L	L	H	Local mode with SQE
L	H	H	H	Global mode, no SQE
L	H	L	H	Global mode with SQE
L	H	H	L	Self exerciser

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} ..... 7 V
Input voltage, V_I ..... 16 V
Output voltage at any output, V_O ..... 16 V
Supply current, I_{CC} ..... 500 mA
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... 0°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
FN	3.0 W	0.024 W/°C	1.92 W

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	DRVDDx, RCVDD1, RCVDD2, $V_{DD(L)}$	4.75	5	5.25	V
Common-mode input voltage, V_{IC}		1		4.2	V
High-level input voltage, V_{IH}	GLOBAL, LOCAL, SMARTSQE, TEST	2.4			V
Low-level input voltage, V_{IL}	GLOBAL, LOCAL, SMARTSQE, TEST			0.8	V
Differential input voltage, V_{ID}	GRX±, GCL±, SRXx±	±318		±1315	mV
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating free-air temperature and supply voltage range (unless otherwise noted)

drivers

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{CM}	Common-mode voltage	See Figure 1	1.0	4.2	V
V_{OD}	Differential-output voltage	See Figure 2	±600	±1315	mV
	Idle differential voltage	See Figure 2		±40	mV
	Idle differential load current			4	mA

receivers

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Differential-input threshold to disable squelch	t > 30 ns†			V_{ID}> –275	mV
	Differential-input threshold to not disable squelch	t < 20 ns†			V_{ID}< –255	mV
V_{ID}	Differential-input voltage		±380		±1315	mV
V_{IC}	Common-mode voltage		1		4.2	V
I_{IC}	Common-mode current				±1	mA
	Hysteresis (threshold)			±40		mV

† t is the duration time that the input signal swings from its common-mode state.

drivers and receivers

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
I_{CC}	Supply current	DRVDDx, RCVDD1, RCVDD2, $V_{DD(L)}$	Steady state		150	mA
			Active		450	

switching characteristics

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	Propagation delay time, internal first stage squelch (see Note 1)	SRXX	Internal 1st stage squelch	See Figure 6	30		65	ns
		GRX						
t_{pd2}	Propagation delay time, internal squelch valid (see Note 2)	SRXx or GRXx	Internal channel squelch	See Figure 6	130		150	ns
t_{pd3}	Propagation delay time, driver startup	SRXx	GTX, STXx	See Figure 6	150		270	ns
		GRX	STXx					
t_{pd4}	Propagation delay time, steady state	SRXx	GTX, STXx	See Figure 6			35	ns
		GRX	STXx					
t_{pd5}	Propagation delay time, steady state	SRXx	GTX, STXx	See Figure 6			35	ns
		GRX	STXx					
t_{sk}	Skew time, signal edge (see Note 3)	SRXx	GTX, STXx	See Figure 6		2		ns
		GRX	STXx					
t_{pd6}	Propagation delay time, last received edge to internal squelch	SRXx or GRX	Internal channel squelch	See Figure 7	144		200	ns
t_{pd7}	Propagation delay time, steady state	SRXx	GTX, STXx	See Figure 7			35	ns
		GRX	STXx					
t_{pd8}	Propagation delay time, last positive edge out to 70% point	GTX, STXx	GTX, STXx	See Figure 7	210		320	ns
t_{pd9}	Propagation delay time, driver idle from last positive edge out (see Note 4)	GTX, STXx	GTX, STXx	See Figure 7	0.21		8	µs
t_{pd10}	Propagation delay time, collision detected to SCLx drivers active	SRXx	Collision signal active	See Figure 8			320	ns
t_{pd11}	Propagation delay time, collision detected to STXx drivers inactive	SRXx	STXx drivers inactive	See Figure 8	350		700	ns
t_{pd12}	Propagation delay time, last SRXx going inactive to collision signal going inactive	Last receiver inactive	Collision drivers inactive	See Figure 8			290	ns
t_{pd13}	Propagation delay time, SCLx drivers active overlap to STXx drivers active	Collision drivers active	STXx drivers active	See Figure 8	200			ns

NOTES: 1. The measurement is referenced to the differential input crossing the −275-mV threshold.
2. The first transmitted bit cell after the squelch deactivates is allowed to have bit cell timing errors. Bit cells beyond this must not be distorted.
3. Skew = $t_{pd4} - t_{pd5} \times t_{pd4}$ must be within ±2 ns of t_{pd5} when measured at the 0% amplitude point.
4. Driver-idle condition exists when the output differential amplitude is less than 40 mV maximum.

PARAMETER MEASUREMENT INFORMATION

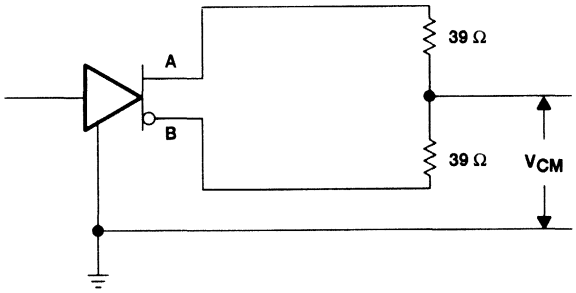


Figure 1. Driver Common-Mode Voltage Test Circuit

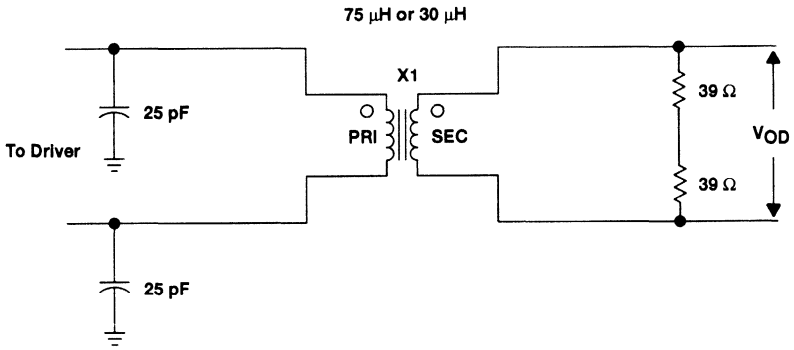


Figure 2. Differential Driver Load Circuit

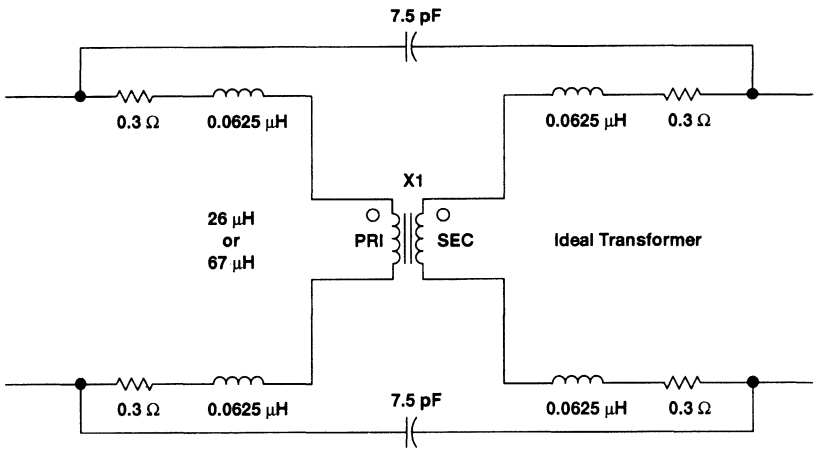
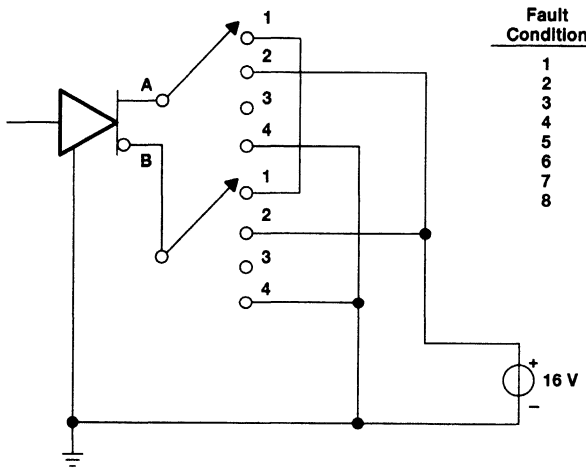


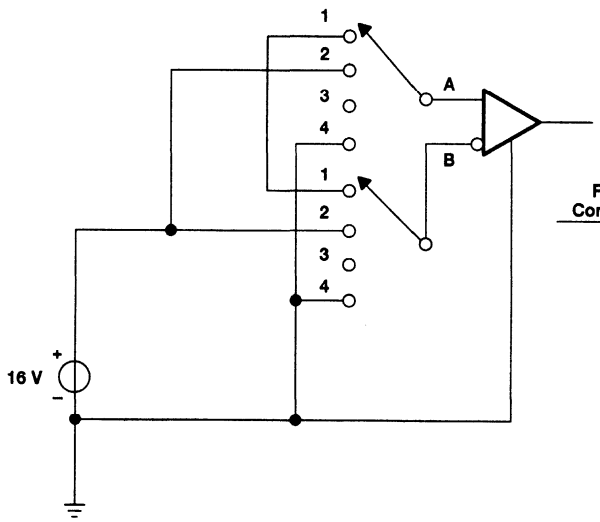
Figure 3. AUI Transformer Model

PARAMETER MEASUREMENT INFORMATION



Fault Condition	Switch Settings Lead A	Lead B
1	1	1
2	4	3
3	3	4
4	4	4
5	2	3
6	3	2
7	2	2
8	3	3

Figure 4. Driver Fault Test Circuit



Fault Condition	Switch Settings Lead A	Lead B
1	1	1
2	4	3
3	3	4
4	4	4
5	2	3
6	3	2
7	2	2
8	3	3

Figure 5. Receiver Fault Test Circuit

PARAMETER MEASUREMENT INFORMATION

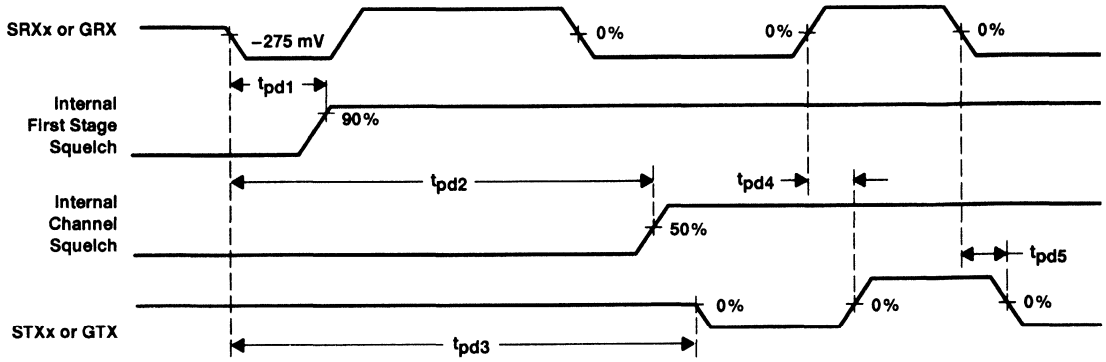


Figure 6. Differential Start-Up Sequence

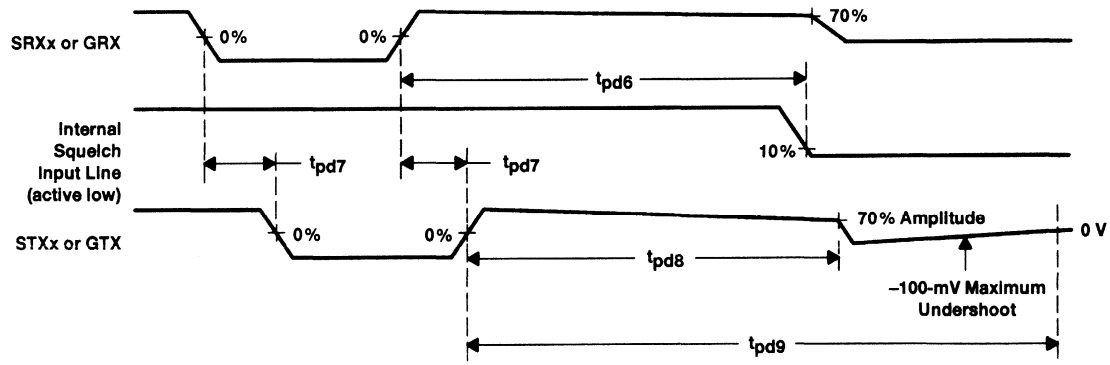


Figure 7. Differential Shut-Down Sequence

PARAMETER MEASUREMENT INFORMATION

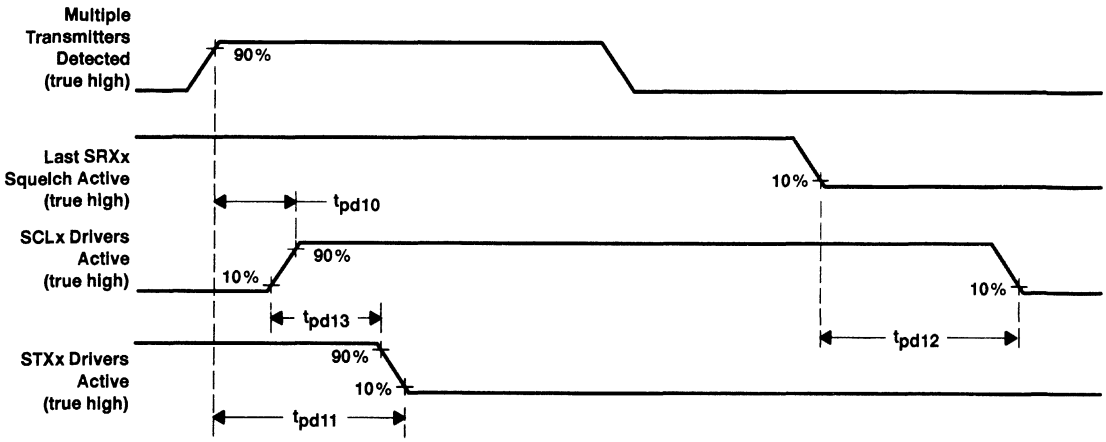


Figure 8. Local Mode Differential STXx Driver Shut-Down Sequence During Collision

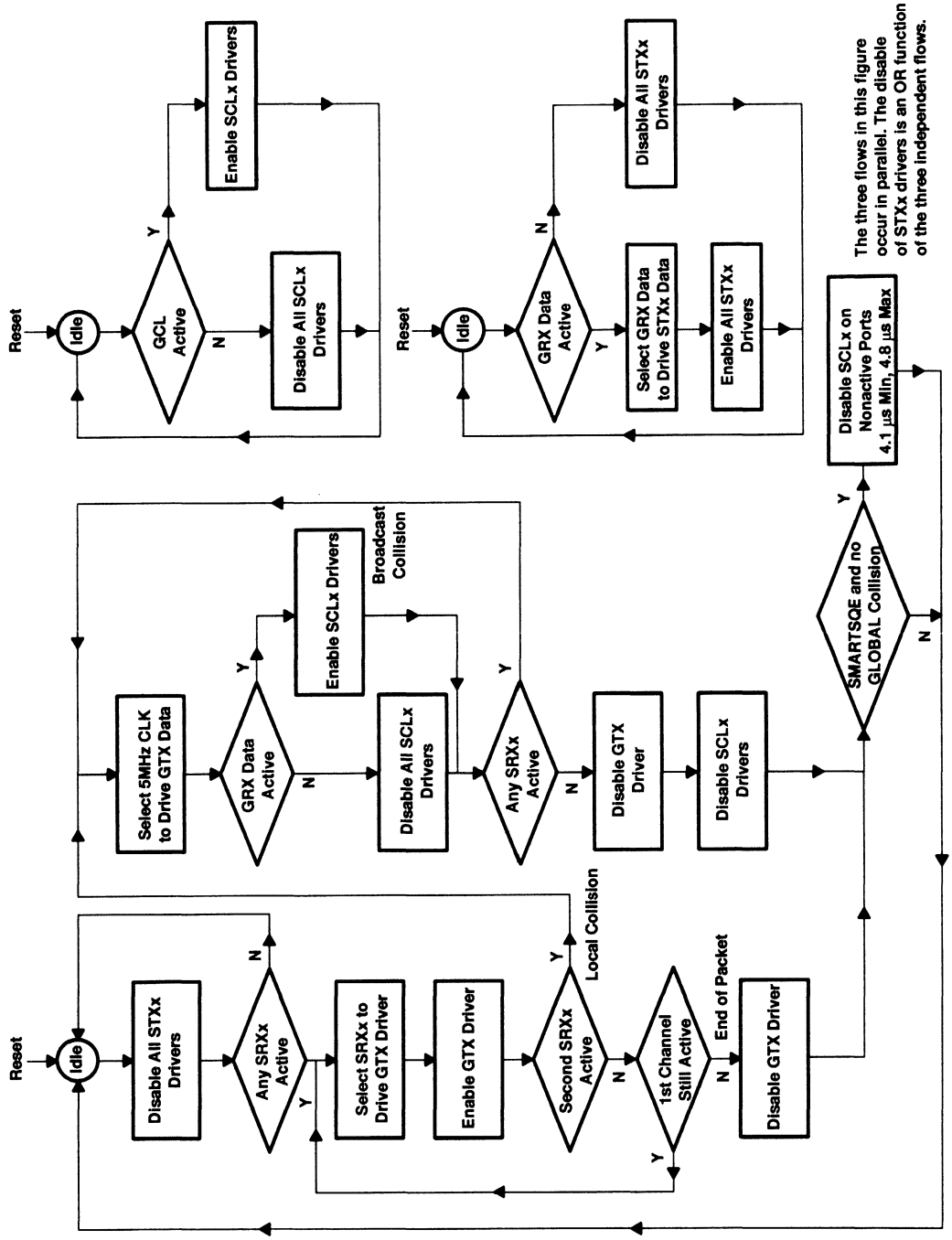


Figure 9. Global Mode Control Flow

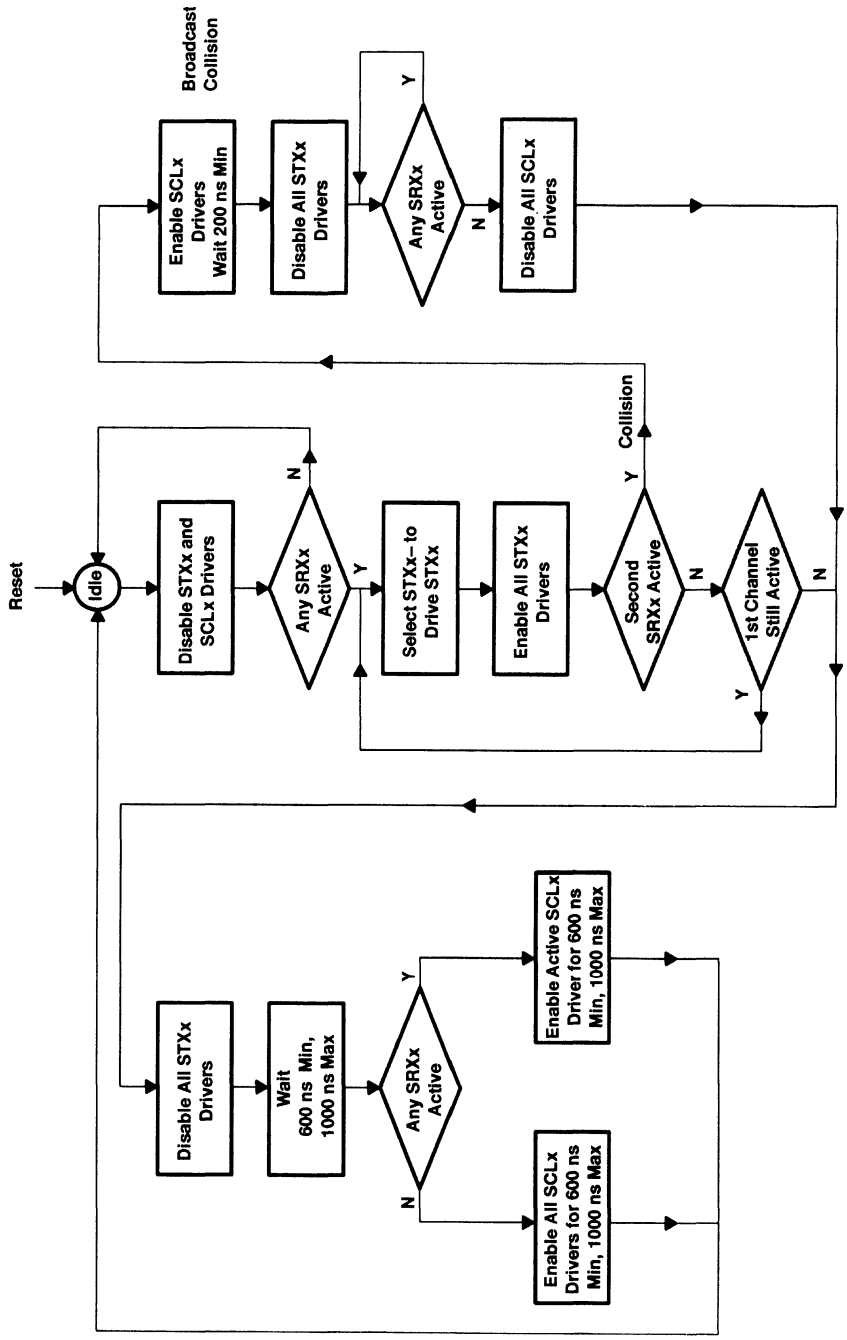
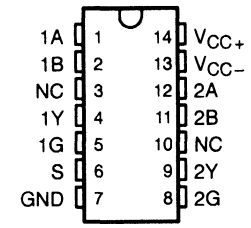


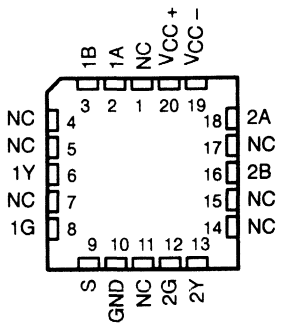
Figure 10. ACC Local Mode Control Flow

- **High Speed**
- **Standard Supply Voltage**
- **Dual Channels**
- **High Common-Mode Rejection Ratio**
- **High Input Impedance**
- **High Input Sensitivity**
- **Differential Common-Mode Input Voltage Range of ±3 V**
- **Strobe Inputs for Receiver Selection**
- **Gate Inputs for Logic Versatility**
- **TTL Drive Capability**
- **High dc Noise Margin**
- **'107A and '107B Have Totem-Pole Outputs**
- **'108A and '108B Have Open-Collector Outputs**
- **B Versions Have Diode-Protected Input for Power-Off Condition**

SN55107A, SN55107B, SN55108A, SN55108B . . . J OR W PACKAGE
SN75107A, SN75107B, SN75108A, SN75108B . . . D, J, OR N PACKAGE
(TOP VIEW)



SN55107A, SN55107B, SN55108A, SN55108B . . . FK PACKAGE
(TOP VIEW)



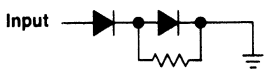
NC – No internal connection

THE SN75108B IS NOT RECOMMENDED FOR NEW DESIGN

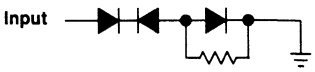
description

These circuits are TTL-compatible, high-speed line receivers. Each is a monolithic dual circuit featuring two independent channels. They are designed for general use as well as such specific applications as data comparators and balanced, unbalanced, and party-line transmission systems. These devices are unilaterally interchangeable with and are replacements for the SN55107, SN55108, SN75107, and SN75108, but offer diode-clamped strobe inputs to simplify circuit design.

The essential difference between the A and B versions can be seen in the schematics. Input-protection diodes are in series with the collectors of the differential-input transistors of the B versions. These diodes are useful in certain party-line systems that may have multiple V_{CC+} power supplies and may be operated with some of the V_{CC+} supplies turned off. In such a system, if a supply is turned off and allowed to go to ground, the equivalent input circuit connected to that supply would be as follows:



A Version

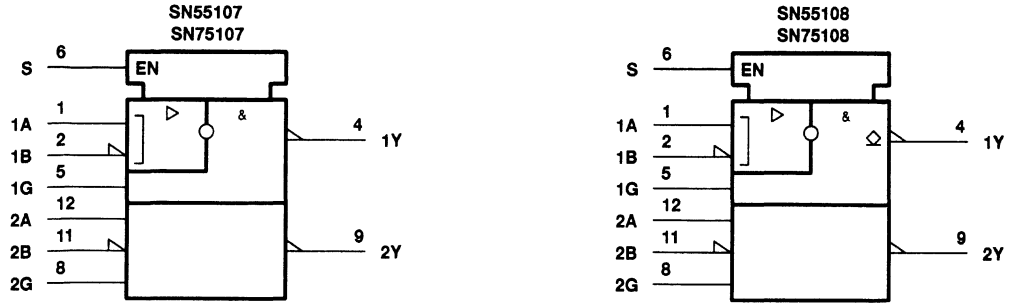


B Version

This would be a problem in specific systems that might possibly have the transmission lines biased to some potential greater than 1.4 V.

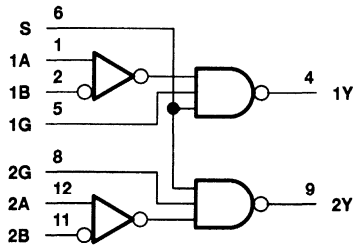
The SN55107A, SN55107B, SN55108A, and SN55108B are characterized for operation over the full military temperature range of −55°C to 125°C. The SN75107A, SN75107B, SN75108A, and SN75108B are characterized for operation from 0°C to 70°C.

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)

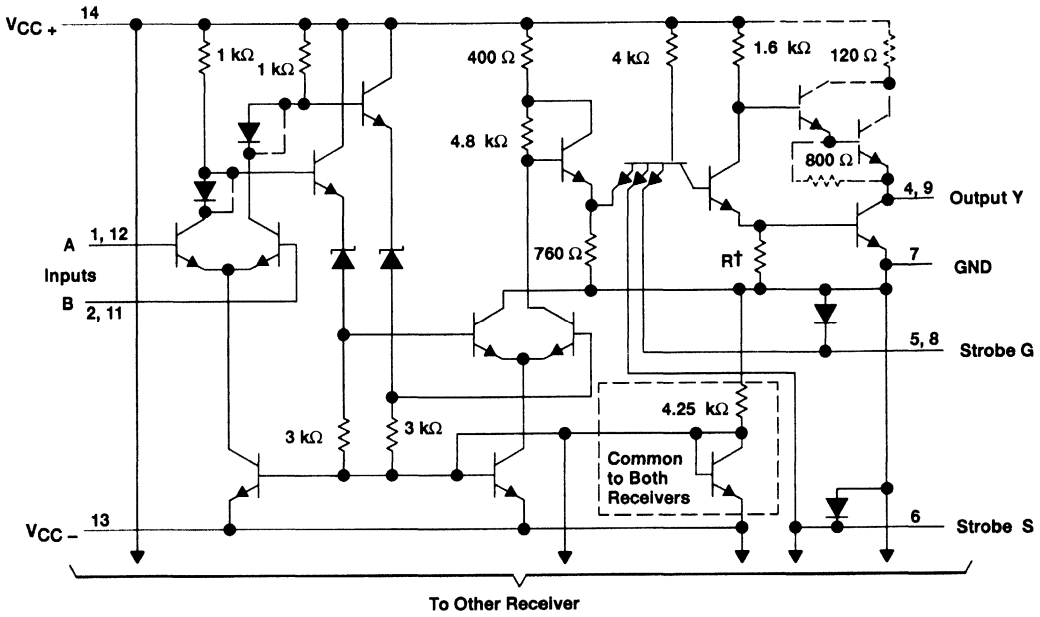


FUNCTION TABLE

DIFFERENTIAL INPUTS A – B	STROBES G	STROBES S	OUTPUT Y
$V_{ID} \geq 25$ mV	X	X	H
−25 mV < V_{ID} < 25 mV	X	L	H
	L	X	H
	H	H	Indeterminate
$V_{ID} \leq -25$ mV	X	L	H
	L	X	H
	H	H	L

H = high level, L = low level, X = irrelevant

schematic (each receiver)



Pin numbers shown are for D, J, N, and W packages.
† R = 1 kΩ for '107A and '107B, 750 Ω for '108A and '108B.
NOTES: 1. Resistor values shown are nominal.
2. Components shown with dashed lines in the output circuitry are applicable to the '107A and '107B only. Diodes in series with the collectors of the differential input transistors are short circuited on '107A and '108A.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC+} (see Note 3) ..... 7 V
Supply voltage, V_{CC-} ..... −7 V
Differential input voltage, V_{ID} (see Note 4) ..... ±6 V
Common-mode input voltage, V_{IC} (see Note 5) ..... ±5 V
Strobe input voltage ..... 5.5 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN55' ..... −55°C to 125°C
SN75' ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Case temperature for 60 seconds, T_C: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or W package ..... 260°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 3. All voltage values, except differential voltages, are with respect to network ground terminal.
4. Differential voltage values are at the noninverting (A) terminal with respect to the inverting (B) terminal.
5. Common-mode input voltage is the average of the voltages at the A and B inputs.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN5510_A,B)	1375 mW	11.0 mW/°C	880 mW	275 mW
J (SN7510_A,B)	1025 mW	8.2 mW/°C	656 mW	—
N	1150 mW	9.2 mW/°C	736 mW	—
W	1000 mW	8.0 mW/°C	640 mW	200 mW

recommended operating conditions (see Note 6)

	SN55107A, SN55107B SN55108A, SN55108B			SN75107A, SN75107B SN75108A, SN75108B			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC+}	4.5	5	5.5	4.75	5	5.25	V
Supply voltage, V_{CC-}	−4.5	−5	−5.5	−4.75	−5	−5.25	V
High-level input voltage between differential inputs, V_{IDH} (see Note 7)	0.025		5	0.025		5	V
Low-level input voltage between differential inputs, V_{IDL} (see Note 7)	−5†		−0.025	−5†		−0.025	V
Common-mode input voltage, V_{IC} (see Notes 7 and 8)	−3†		3	−3†		3	V
Input voltage, any differential input to GND (see Note 8)	−5†		3	−5†		3	V
High-level input voltage at strobe inputs, $V_{IH(S)}$	2		5.5	2		5.5	V
Low-level input voltage at strobe inputs, $V_{IL(S)}$	0		0.8	0		0.8	V
Low-level output current, I_{OL}			−16			−16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

† The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for input voltage levels only.

NOTES: 6. When using only one channel of the line receiver, the strobe G of the unused channel should be grounded and at least one of the differential inputs of the unused receiver should be terminated at some voltage between −3 V and 3 V.
7. The recommended combinations of input voltages fall within the shaded area in Figure 1.
8. The common-mode voltage may be as low as −4 V provided that the more positive of the two inputs is not more negative than −3 V.

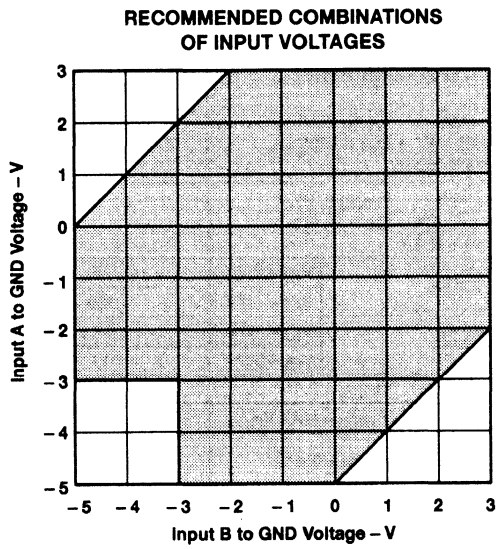


Figure 1. Recommended Combinations of Input Voltages

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

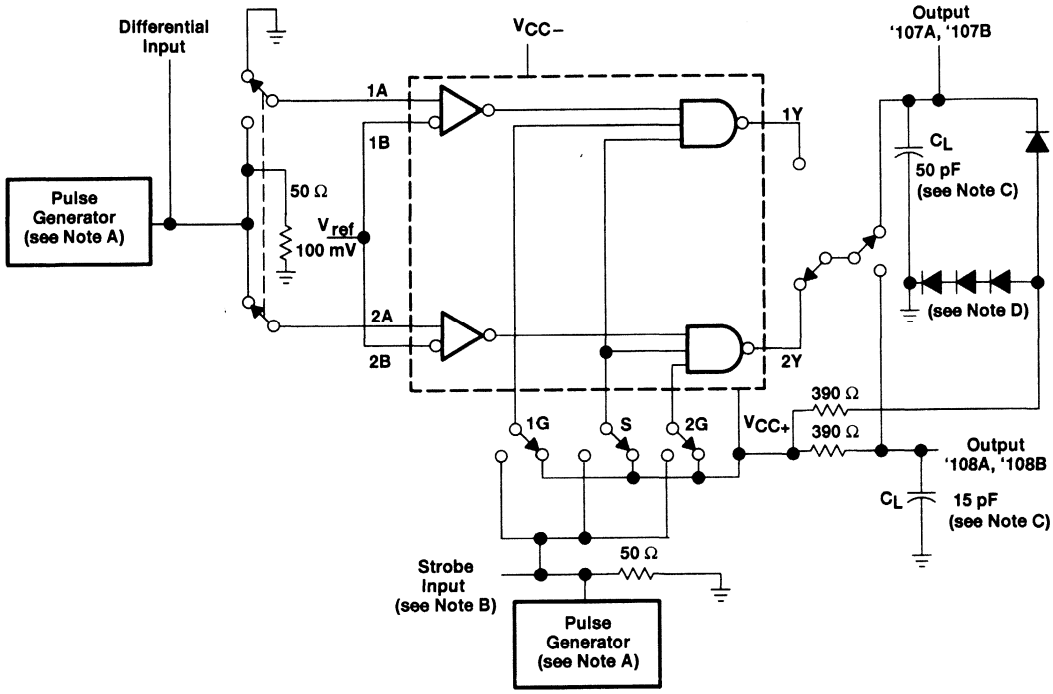
PARAMETER			TEST CONDITIONS†		'107A, '107B MIN	'107A, '107B TYP‡	'107A, '107B MAX	'108A, '108B MIN	'108A, '108B TYP‡	'108A, '108B MAX	UNIT
V_{OH}	High-level output voltage		$V_{CC\pm}$ = MIN, $V_{IL(S)}$ = 0.8 V, V_{IDH} = 25 mV, I_{OH} = −400 µA, V_{IC} = −3 V to 3 V		2.4						V
V_{OL}	Low-level output voltage		$V_{CC\pm}$ = MIN, $V_{IH(S)}$ = 2 V, V_{IDL} = −25 mV, I_{OL} = 16 mA, V_{IC} = −3 V to 3 V				0.4			0.4	V
I_{IH}	High-level input current	A	$V_{CC\pm}$ = MAX	V_{ID} = 5 V		30	75		30	75	µA
		B		V_{ID} = −5 V		30	75		30	75	
I_{IL}	Low-level input current	A	$V_{CC\pm}$ = MAX	V_{ID} = −5 V			−10			−10	µA
		B		V_{ID} = 5 V			−10			−10	
I_{IH}	High-level input current into 1G or 2G		$V_{CC\pm}$ = MAX, $V_{IH(G)}$ = 2.4 V				40			40	µA
			$V_{CC\pm}$ = MAX, $V_{IH(G)}$ = MAX V_{CC+}				1			1	mA
I_{IL}	Low-level input current into 1G or 2G		$V_{CC\pm}$ = MAX, $V_{IL(G)}$ = 0.4 V				−1.6			−1.6	mA
I_{IH}	High-level input current into S		$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = 2.4 V				80			80	µA
			$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = MAX V_{CC+}				2			2	mA
I_{IL}	Low-level input current into S		$V_{CC\pm}$ = MAX, $V_{IL(S)}$= 0.4 V				−3.2			−3.2	mA
I_{OH}	High-level output current		$V_{CC\pm}$ = MIN, V_{OH} = MAX V_{CC+}							250	µA
I_{OS}	Short-circuit output current§		$V_{CC\pm}$ = MAX		−18		−70				mA
I_{CCH+}	Supply current from V_{CC+}, outputs high		$V_{CC\pm}$ = MAX, T_A = 25°C			18	30		18	30	mA
I_{CCH-}	Supply current from V_{CC-}, outputs high		$V_{CC\pm}$ = MAX, T_A = 25°C			−8.4	−15		−8.4	−15	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

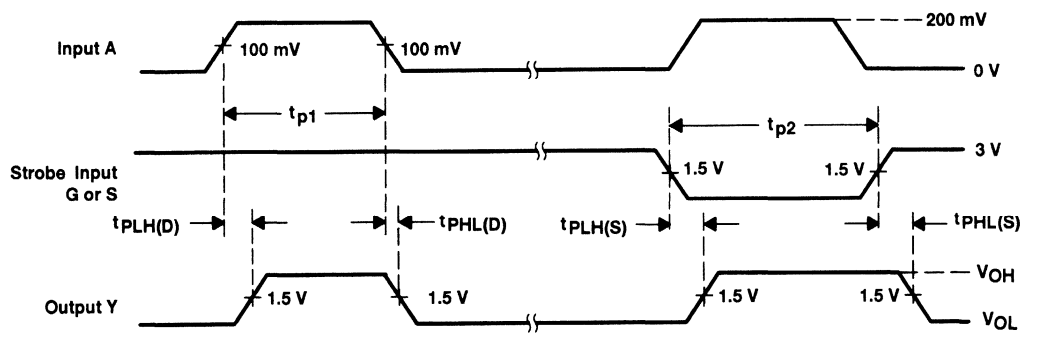
switching characteristics, $V_{CC\pm}$ = ±5 V, T_A = 25°C, R_L = 390 Ω (see Figure 2)

PARAMETER		TEST CONDITIONS	'107A, '107B MIN	'107A, '107B TYP	'107A, '107B MAX	'108A, 108B MIN	'108A, 108B TYP	'108A, 108B MAX	UNIT
$t_{PLH(D)}$	Propagation delay time, low- to high-level output, from differential inputs A and B	C_L = 50 pF		17	25				ns
		C_L = 15 pF					19	25	
$t_{PHL(D)}$	Propagation delay time, high- to low-level output, from differential inputs A and B	C_L = 50 pF		17	25				ns
		C_L = 15 pF					19	25	
$t_{PLH(S)}$	Propagation delay time, low- to high-level output, from strobe input G or S	C_L = 50 pF		10	15				ns
		C_L = 15 pF					13	20	
$t_{PHL(S)}$	Propagation delay time, high- to low-level output, from strobe input G or S	C_L = 50 pF		8	15				ns
		C_L = 15 pF					13	20	

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_O = 50 Ω, t_r = 10 ± 5 ns, t_f = 10 ± 5 ns, t_{pd1} = 500 ns, PRR ≤ 1 MHz, t_{pd2} = 1 μs, PRR ≤ 500 kHz.

B. Strobe input pulse is applied to Strobe 1G when inputs 1A-1B are being tested, to Strobe S when inputs 1A-1B or 2A-2B are being tested, and to Strobe 2G when inputs 2A-2B are being tested.

C. C_L includes probe and jig capacitance.

D. All diodes are 1N916.

Figure 2. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

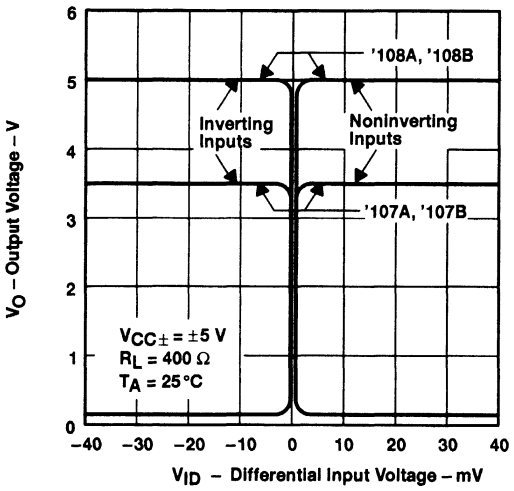


Figure 3

HIGH-LEVEL INPUT CURRENT (1A OR 2A)
vs
FREE-AIR TEMPERATURE

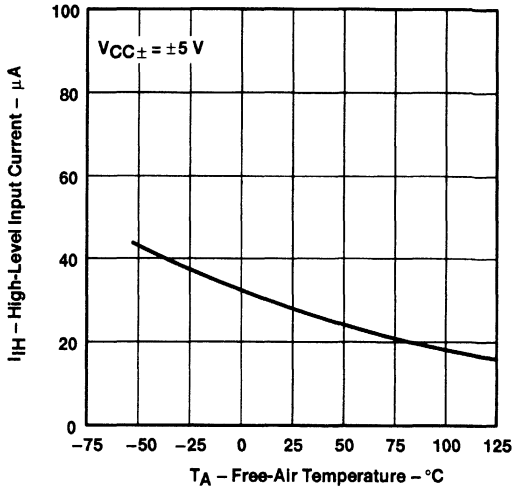


Figure 4

SUPPPLY CURRENT (OUTPUTS HIGH)
vs
FREE-AIR TEMPERATURE

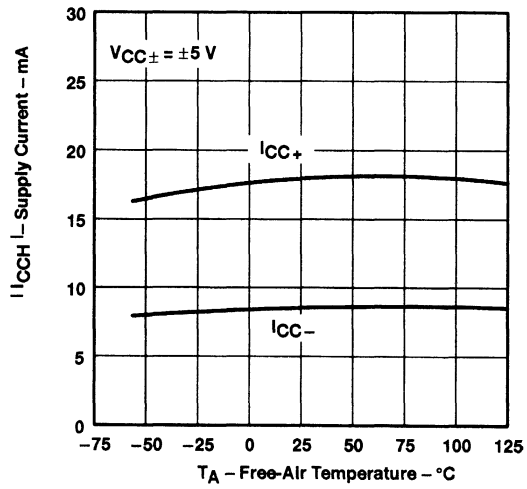


Figure 5

PROPAGATION DELAY TIME
(DIFFERENTIAL INPUTS)
vs
FREE-AIR TEMPERATURE

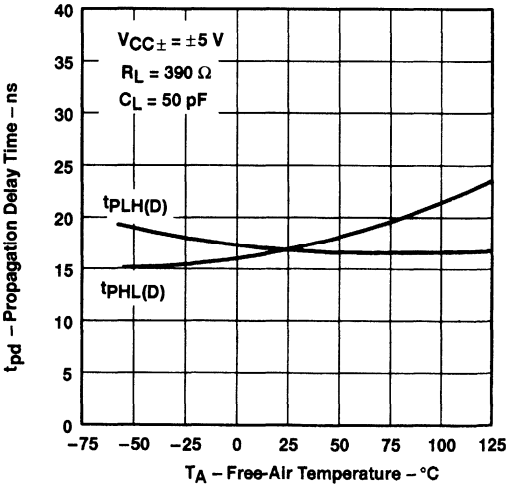


Figure 6

† Values below 0°C and above 70°C apply to SN55' only.

TYPICAL CHARACTERISTICS†

PROPAGATION DELAY TIME (LOW-TO-HIGH LEVEL)
(DIFFERENTIAL INPUTS)
vs
FREE-AIR TEMPERATURE

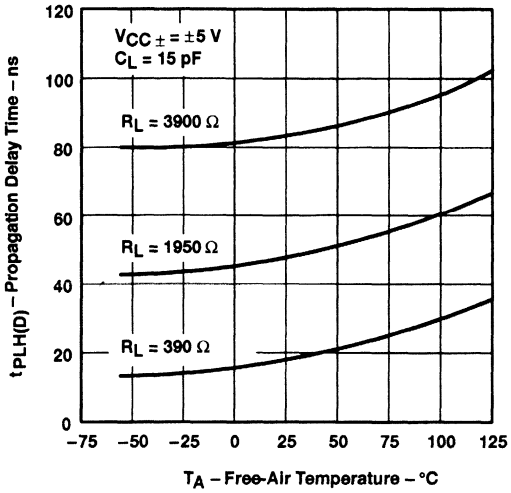


Figure 7

PROPAGATION DELAY TIME (LOW-TO-HIGH LEVEL)
(DIFFERENTIAL INPUTS)
vs
FREE-AIR TEMPERATURE

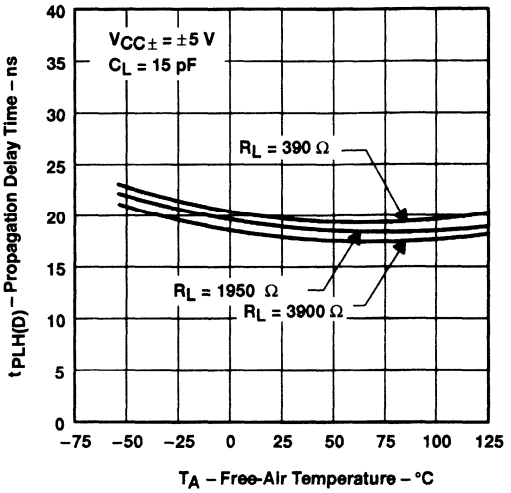


Figure 8

'108A, '108B
PROPAGATION DELAY TIME (STROBE INPUTS)
vs
FREE-AIR TEMPERATURE

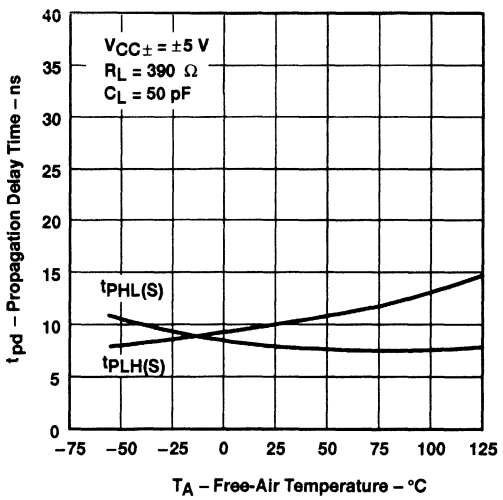


Figure 9

'108A, '108B
PROPAGATION DELAY TIME (STROBE INPUTS)
vs
FREE-AIR TEMPERATURE

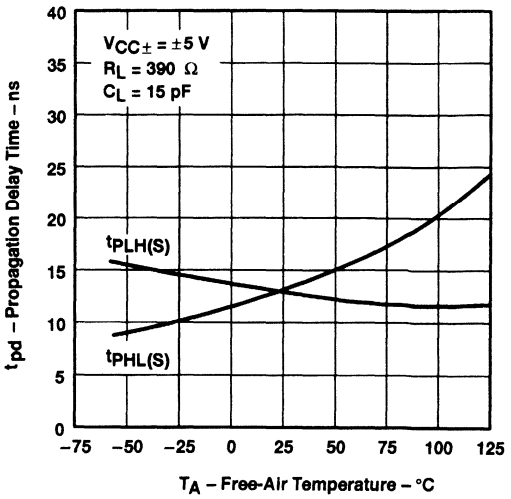


Figure 10

† Values below 0°C and above 70°C apply to SN55' only.

APPLICATION INFORMATION

basic balanced-line transmission system

The '107A, '107B, '108A, and '108B dual line circuits are designed specifically for use in high-speed data transmission systems that utilize balanced terminated transmission lines such as twisted-pair lines. The system operates in the balanced mode, so noise induced on one line is also induced on the other. The noise appears common mode at the receiver input terminals where it is rejected. The ground connection between the line driver and receiver is not part of the signal circuit so that system performance is not affected by circulating ground currents.

The unique driver-output circuit allows terminated transmission lines to be driven at normal line impedances. High-speed system operation is ensured since line reflections are virtually eliminated when terminated lines are used. Crosstalk is minimized by low signal amplitudes and low line impedances.

The typical data delay in a system is approximately 30 + 1.3 L ns, where L is the distance in feet separating the driver and receiver. This delay includes one gate delay in both the driver and receiver.

Data is impressed on the balanced-line system by unbalancing the line voltages with the driver output current. The driven line is selected by appropriate driver-input logic levels. The voltage difference is approximately:

$$V_{DIFF} \approx 1/2 I_{O(on)} \bullet R_T$$

High series line resistance will cause degradation of the signal. The receivers, however, will detect signals as low as 25 mV (or less). For normal line resistances, data may be recovered from lines of several thousand feet in length.

Line-termination resistors (R_T) are required only at the extreme ends of the line. For short lines, termination resistors at the receiver only may prove adequate. The signal amplitude will then be approximately:

$$V_{DIFF} \approx I_{O(on)} \bullet R_T$$

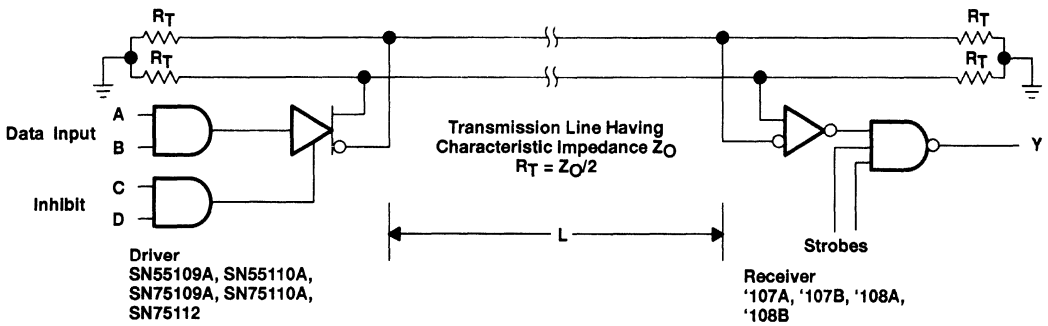


Figure 11. Typical Differential Data Line

data-bus or party-line system

The strobe feature of the receivers and the inhibit feature of the drivers allow these dual line circuits to be used in data-bus or party-line systems. In these applications, several drivers and receivers may share a common transmission line. An enabled driver transmits data to all enabled receivers on the line while other drivers and receivers are disabled. Data is thus time multiplexed on the transmission line. The device specifications allow widely varying thermal and electrical environments at the various driver and receiver locations. The data-bus system offers maximum performance at minimum cost.

APPLICATION INFORMATION

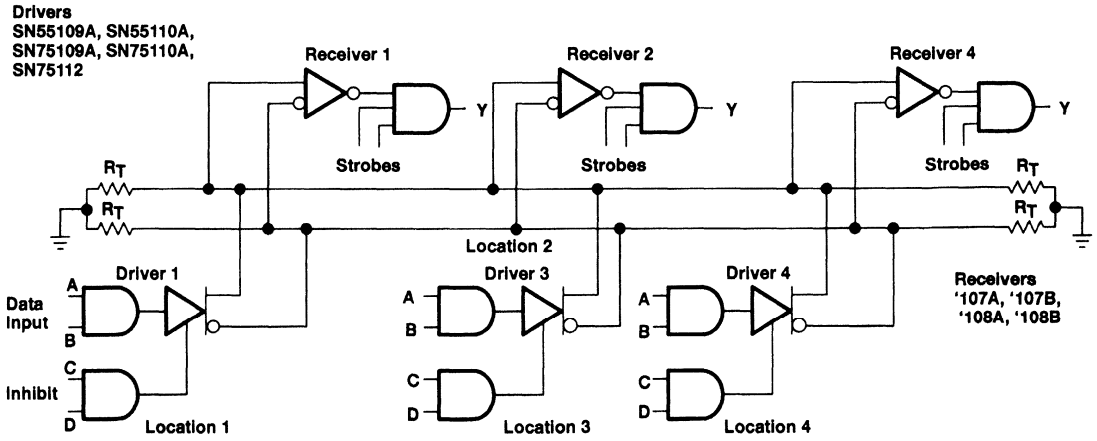


Figure 12. Typical Differential Party Line

unbalanced or single-line systems

These dual-line circuits may also be used in unbalanced or single-line systems. Although these systems do not offer the same performance as balanced systems for long lines, they are adequate for very short lines where environmental noise is not severe.

The receiver threshold level is established by applying a dc reference voltage to one receiver input terminal. The signal from the transmission line is applied to the remaining input. The reference voltage should be optimized so that signal swing is symmetrical about it for maximum noise margin. The reference voltage should be in the range of −3 V to 3 V. It can be provided by a voltage supply or by a voltage divider from an available supply voltage.

A single-ended output from a driver may be used in single-line systems. Coaxial or shielded line is preferred for minimum noise and crosstalk problems. For large signal swings, the high output current (typically 27 mA) of the SN75112 is recommended. Drivers may be paralleled for higher current. When using only one channel of the line drivers, the other channel should be inhibited and/or have its outputs grounded.

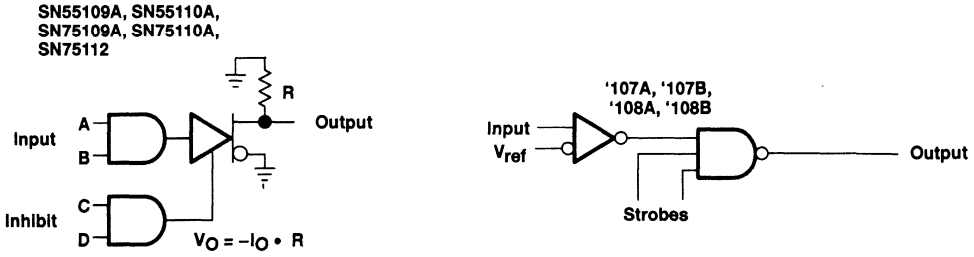


Figure 13. Single-Ended Operation

APPLICATION INFORMATION

'108A, '108B dot-AND output connections

The '108A, '108B line receivers feature an open-collector-output circuit that can be connected in the dot-AND logic configuration with other similar open-collector outputs. This allows a level of logic to be implemented without additional logic delay.

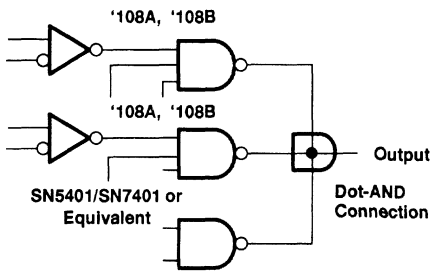


Figure 14. Dot-AND Connection

increasing common-mode input voltage range of receiver

The common-mode voltage range (CMVR) is defined as the range of voltage applied simultaneously to both input terminals that if exceeded does not allow normal operation of the receiver.

The recommended operating CMVR is ±3 V, making it useful in all but the noisiest environments. In extremely noisy environments, common-mode voltage can easily reach ±10 V to ±15 V if some precautions are not taken to reduce ground and power supply noise, as well as crosstalk problems. When the receiver must operate in such conditions, input attenuators should be used to decrease the system common-mode noise to a tolerable level at the receiver inputs. Differential noise is also reduced by the same ratio. These attenuators have been intentionally omitted from the receiver input terminals so the designer may select resistors that will be compatible with his particular application or environment. Furthermore, the use of attenuators adversely affects the input sensitivity, the propagation delay time, the power dissipation, and in some cases (depending on the selected resistor values) the input impedance, therefore, reducing the versatility of the receiver.

The ability of the receiver to operate with approximately ±15 V common-mode voltage at the inputs has been checked using the circuit shown in Figure 15. The resistors R1 and R2 provide a voltage divider network. Dividers with three different values presenting a 5-to-1 attenuation were used so as to operate the differential inputs at approximately ±3 V common-mode voltage. Careful matching of the two attenuators is needed so as to balance the overdrive at the input stage. The resistors used are shown in Table 1.

Table 2 shows some of the typical switching results obtained under such conditions.

Table 1

Attenuator 1:	R1 = 2 kΩ,	R2 = 0.5 kΩ
Attenuator 2:	R1 = 6 kΩ,	R2 = 1.5 kΩ
Attenuator 3:	R1 = 12 kΩ,	R2 = 3 kΩ

Table 2. Typical Propagation Delays for Receiver With Attenuator Test Circuit Shown in Figure 14

DEVICE	PARAMETERS	INPUT ATTENUATOR	TYPICAL (ns)
'107A,'107B	t_{PLH}	1	20
		2	32
		3	42
	t_{PHL}	1	22
		2	31
		3	33
'108A,'108B	t_{PLH}	1	36
		2	47
		3	57
	t_{PHL}	1	29
		2	38
		3	41

APPLICATION INFORMATION

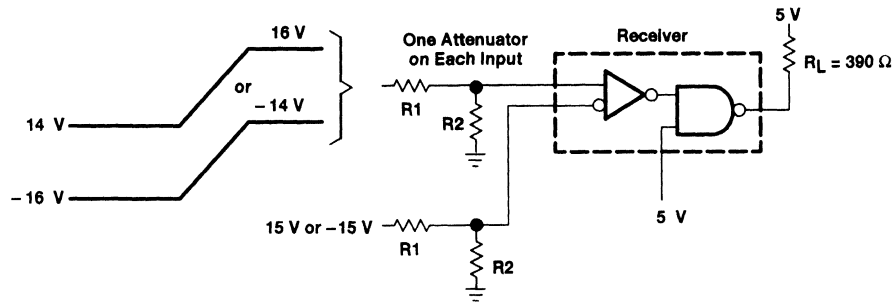


Figure 15. Common-Mode Circuit for Testing Input Attenuators With Results Shown In Table 2

Two methods of terminating a transmission line to reduce reflections are:

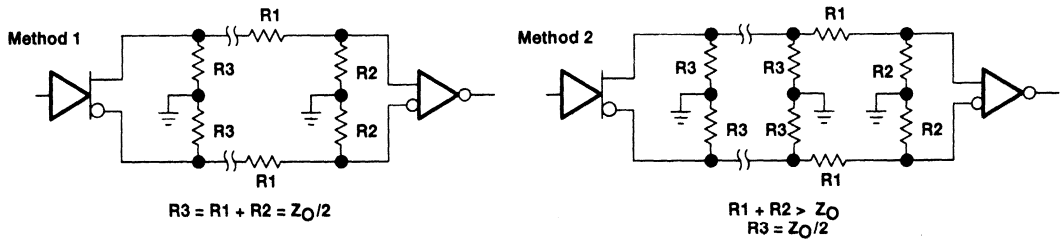


Figure 16. Termination Techniques

The first method uses the resistors as the attenuation network and line termination. The second method uses two additional resistors for the line terminations.

APPLICATION INFORMATION

For party-line operation, method 2 should be used as follows:

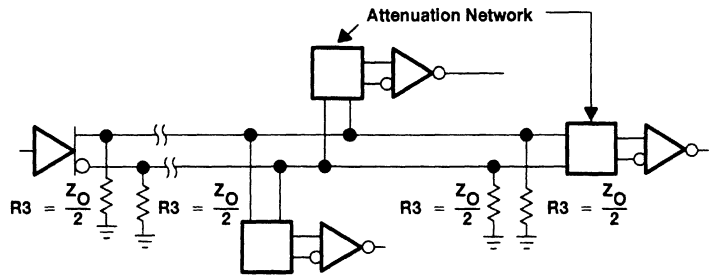


Figure 17. Party-Line Termination Technique

To minimize the loading, the values of R1 and R2 should be fairly large. Examples of possible values are shown in Table 1.

furnace control using the SN75108A

The furnace control circuit in Figure 18 is an example of the possible use of the SN55107A Series in areas other than what would normally be considered electronic systems. Basically, a description of the operation of this control follows. When the room temperature is below the desired level, the resistance of the room temperature sensor is high and channel 1 noninverting input is below (less positive than) the reference level set on the input differential amplifier. This situation causes a low output, operating the heat on relay and turning on the heat. The channel 2 noninverting input is below the reference level when the bonnet temperature of the furnace reaches the desired level. This causes a low output thus operating the blower relay. Normally the furnace is shut down when the room temperature reaches the desired level and the channel 1 output goes high, turning the heat off. The blower remains on as long as the bonnet temperature is high, even after the heat on relay is off. There is also a safety switch in the bonnet that shuts the furnace down if the temperature there exceeds desired limitations. The types of temperature-sensing devices and bias-resistor values used are determined by the particular operating conditions encountered.

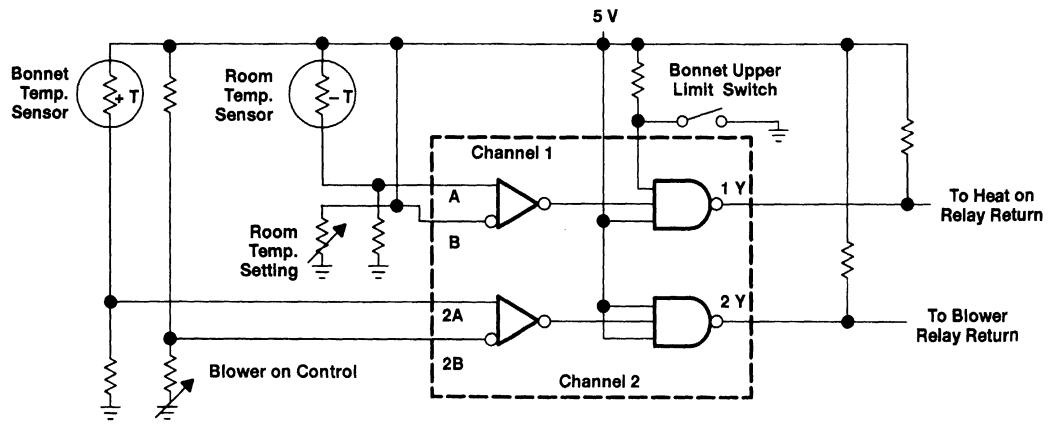


Figure 18. Furnace Control Using SN75108A

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APPLICATION INFORMATION

repeaters for long lines

In some cases, the driven line may be so long that the noise level on the line reaches the common-mode limits or the attenuation becomes too large and results in poor reception. In such a case, a simple application of a receiver and a driver as repeaters [shown in Figure 19(a)] restores the signal level and allows an adequate signal level at the receiving end. If multichannel operation is desired, then proper gating for each channel must be sent through the repeater station using another repeater set as in Figure 19(b).

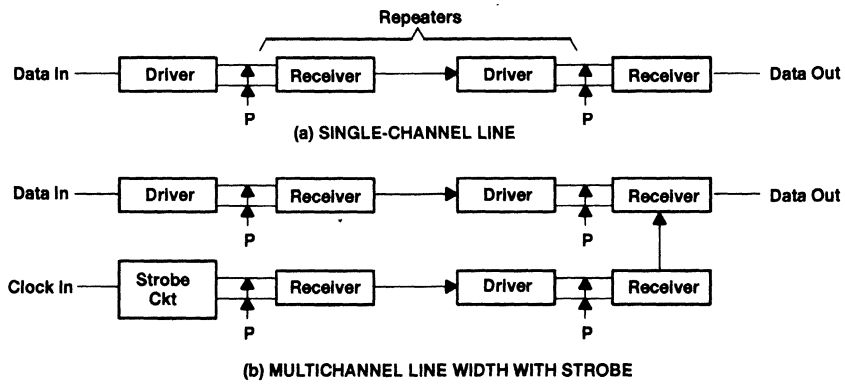


Figure 19. Receiver-Driver Repeaters

receiver as dual differential comparator

There are many applications for differential comparators, such as voltage comparison, threshold detection, controlled Schmitt triggering, and pulse-width control.

As a differential comparator, a '107A or '108A may be connected to compare the noninverting input terminal with the inverting input as shown in Figure 20. Thus the output will be high or low resulting from the A input being greater or less than the reference. The strobe inputs allow additional control over the circuit so that either output or both may be inhibited.

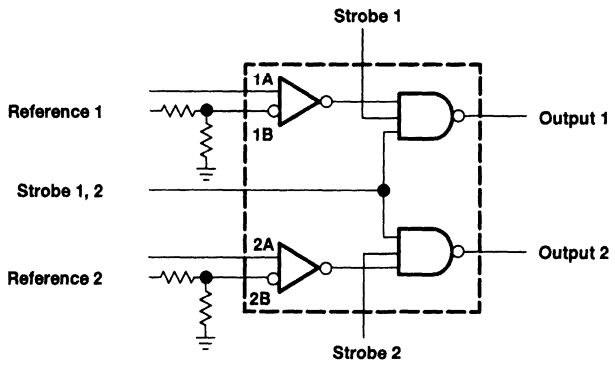
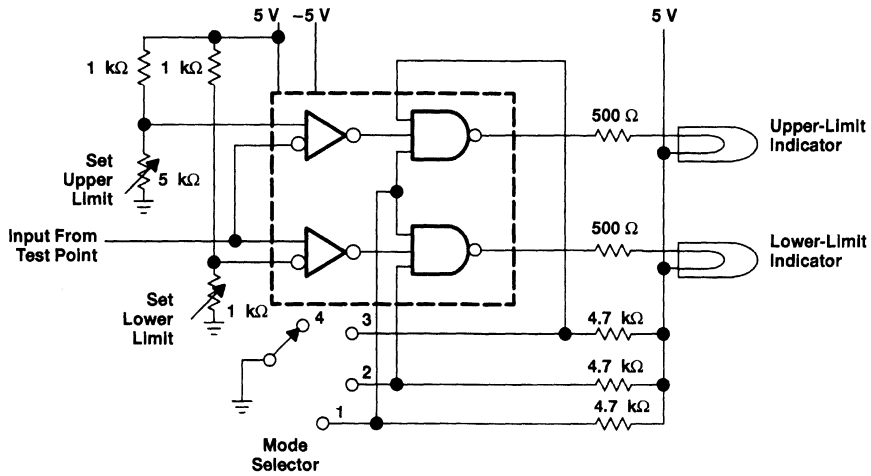


Figure 20. SN55107A Series Receiver as a Dual Differential Comparator

APPLICATION INFORMATION

window detector

The window detector circuit in Figure 21 has a large number of applications in test equipment and in determining upper limits, lower limits, or both at the same time – such as detecting whether a voltage or signal has exceeded its limits or window. Illumination of the upper-limit (lower-limit) indicator shows that the input voltage is above (below) the selected upper (lower) limit. A mode selector is provided for selecting the desired test. For window detecting, the upper and lower limits test position is used.



MODE SELECTOR LEGEND

POSITION	CONDITION
1	Off
2	Test for Upper Limit
3	Test for Lower Limit
4	Test for Upper and Lower Limits

Figure 21. Window Detector Using SN75108A

APPLICATION INFORMATION

temperature controller with zero-voltage switching

The circuit in Figure 22 switches an electric-resistive heater on or off by providing negative-going pulses to the gate of a triac during the time interval when the line voltage is passing through zero. The pulse generator is the 2N5447 and four diodes. This portion of the circuit provides negative-going pulses during the short time (approximately 100 μs) when the line voltage is near zero. These pulses are fed to the inverting input of one channel of the '108A. If the room temperature is below the desired level, the resistance of the thermistor is high and the noninverting input of channel 2 is above the reference level determined by the thermostat setting. This provides a high-level output from channel 2. This output is ANDed with the positive-going pulses from the output of channel 1, which are reinverted in the 2N5449.

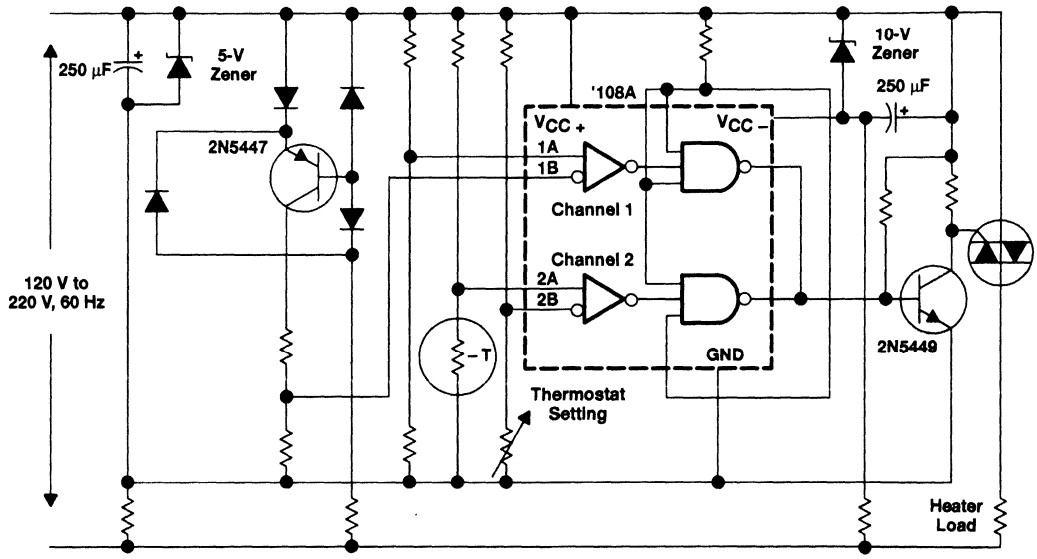
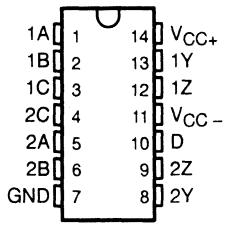


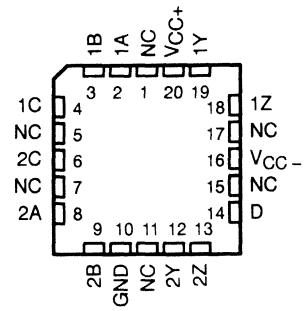
Figure 22. Zero-Voltage Switching Temperature Controller

- **Improved Stability Over Supply Voltage and Temperature Ranges**
- **Constant-Current Outputs**
- **High Speed**
- **Standard Supply Voltages**
- **High Output Impedance**
- **High Common-Mode Output Voltage Range −3 V to 10 V**
- **TTL-Input Compatibility**
- **Inhibitor Available for Driver Selection**
- **Glitch-Free During Power Up/Power Down**
- **SN75112 and External Circuit Meets or Exceeds the Requirements of CCITT Recommendation V.35**

SN55109A, SN55110A . . . J OR W PACKAGE
SN75109A, SN75110A, SN75112 . . . D OR N PACKAGE
(TOP VIEW)



SN55109A, SN55110A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

THE SN75109A IS NOT RECOMMENDED FOR NEW DESIGNS

description

The SN55109A, SN55110A, SN75109A, SN75110A, and SN75112 dual line drivers have improved output current regulation with supply voltage and temperature variations. In addition, the higher current of the SN75112 (27 mA) allows data to be transmitted over longer lines. These drivers offer optimum performance when used with the SN55107A, SN55108A, SN75107A, and SN75108A line receivers.

These drivers feature independent channels with common voltage supply and ground terminals. The significant difference between the three drivers is in the output current specification. The driver circuits feature a constant output current that is switched to either of two output terminals by the appropriate logic levels at the input terminals. The output current can be switched off (inhibited) by low logic levels on the enable inputs. The output current is nominally 6 mA for the '109A, 12 mA for the '110A, and 27 mA for the SN75112.

The enable/inhibit feature is provided so the circuits can be used in party-line or data-bus applications. A strobe or inhibitor (enable D), common to both drivers, is included for increased driver-logic versatility. The output current in the inhibited mode, $I_{O(off)}$, is specified so that minimum line loading is induced when the driver is used in a party-line system with other drivers. The output impedance of the driver in the inhibited mode is very high. The output impedance of a transistor is biased to cutoff.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES				CERAMIC FLATPACK (W)
	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	
0°C to 70°C	SN75109AD SN75110AD SN75112D			SN75109AN SN75110AN SN75112N	
−55°C to 125°C		SN55109AFK SN55110AFK	SN55109AJ SN55110AJ	SN55109AJ SN55110AJ	SN55109AW SN55110AW

The D package is available taped and reeled. Add the suffix R to the device type, (e.g., SN75110ADR).

description (continued)

The driver outputs have a common-mode voltage range of −3 V to 10 V, allowing common-mode voltage on the line without affecting driver performance.

All inputs are diode clamped and are designed to satisfy TTL-system requirements. The inputs are tested at 2 V for high-logic-level input conditions and 0.8 V for low-logic-level input conditions. These tests ensure 400-mV noise margin when interfaced with TTL Series 54/74.

The SN55109A and SN55110A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN75109A, SN75110A, and SN75112 are characterized for operation from 0°C to 70°C.

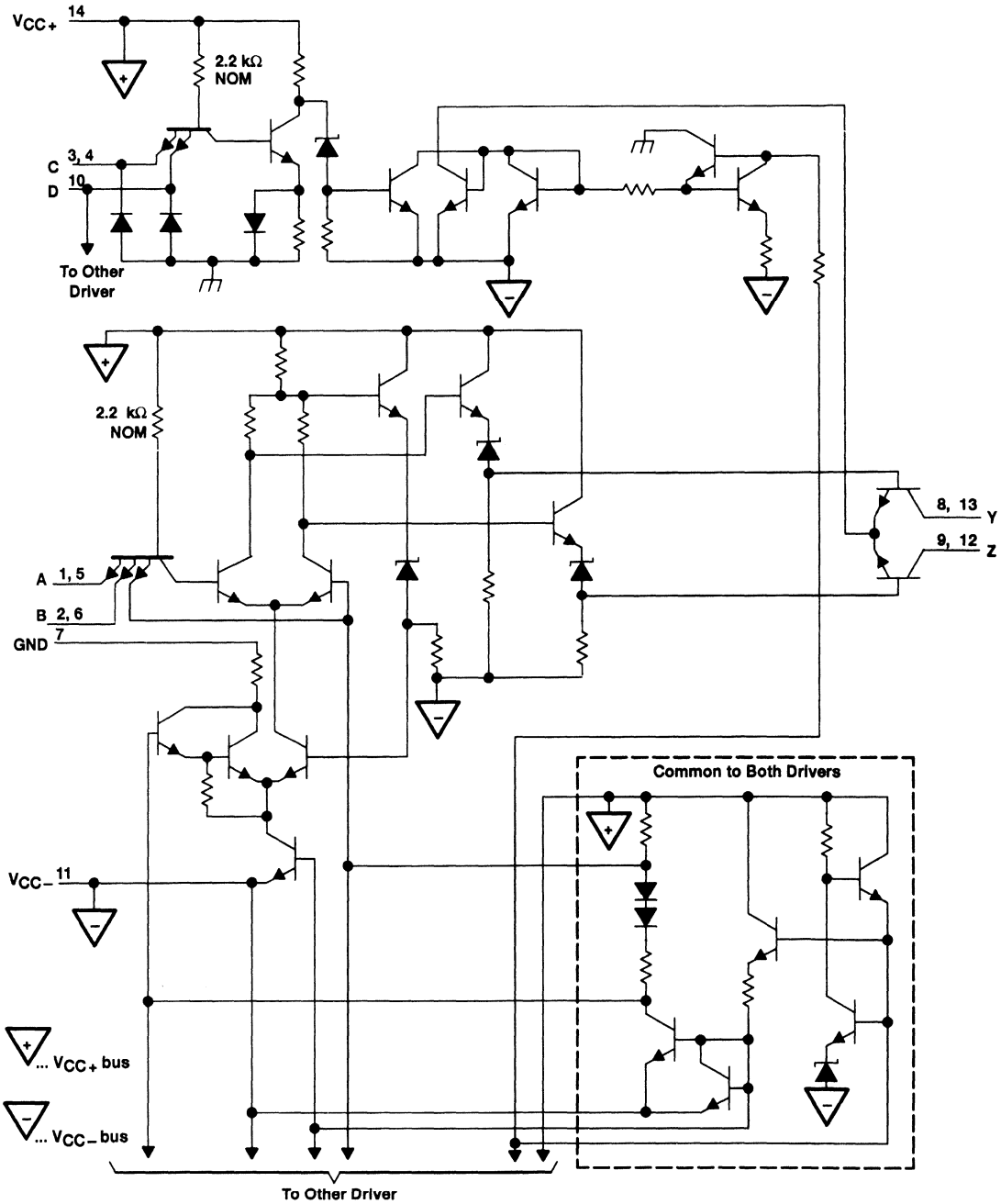
FUNCTION TABLE
(each driver)

LOGIC INPUTS		ENABLE INPUTS		OUTPUTS†	
A	B	C	D	Y	Z
X	X	L	X	Off	Off
X	X	X	L	Off	Off
L	X	H	H	On	Off
X	L	H	H	On	Off
H	H	H	H	Off	On

H = high level, L = low level, X = irrelevant

† When using only one channel of the line drivers, the other channel should be inhibited and/or have its outputs grounded.

schematic (each driver)



Pin numbers shown are for D, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

		SN55109A SN55110A	SN75109A SN75110A	SN75112	UNIT
Supply voltage, V_{CC+} (see Note 1)		7	7	7	V
Supply voltage, V_{CC-}		−7	−7	−7	V
Input voltage, V_I		5.5	5.5	5.5	V
Output voltage range, V_O		−5 to 12	−5 to 12	−5 to 12	V
Continuous total power dissipation (see Note 2)		See Dissipation Rating Table			
Operating free-air temperature range, T_A		−55 to 125	0 to 70	0 to 70	°C
Storage temperature range, T_{stg}		−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds: FK package		260			°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or W package	300			°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package		260	260	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.
2. In the FK, J, or W package, SN55109A and SN55110A chips are either silver glass or alloy mounted, and SN75109A, SN75110A, and SN75112 chips are glass mounted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—
W	1000 mW	8.0 mW/°C	640 mW	200 mW

recommended operating conditions (see Note 3)

	SN55109A SN55110A			SN75109A SN75110A SN75112			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC+}	4.5	5	5.5	4.75	5	5.25	V
Supply voltage, V_{CC-}	−4.5	−5	−5.5	−4.75	−5	−5.25	V
Positive common-mode output voltage	0		10	0		10	V
Negative common-mode output voltage	0		−3	0		−3	V
High-level input voltage, V_{IH}	2			2			V
Low-level output current, V_{IL}			0.8			0.8	V
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 3: When using only one channel of the line drivers, the other channel should be inhibited and/or have its outputs grounded.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN55109A SN75109A			SN55110A SN75110A			SN75112			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage		$V_{CC\pm}$ = MIN, I_L = −12 mA		−0.9	−1.5		−0.9	−1.5		−0.9	−1.5	V
$I_{O(on)}$	On-state output current		$V_{CC\pm}$ = MAX, V_O = 10 V		6	7		12	15		27	36	mA
			V_{CC} = MIN to MAX, V_O = −1 V to 1 V, T_A = 25°C							24	28	32	
			$V_{CC\pm}$ = MIN, V_O = −3 V	3.5	6		6.5	12		18	27		
$I_{O(off)}$	Off-state output current		$V_{CC\pm}$ = MIN, V_O = 10 V			100			100			100	µA
I_I	Input current at maximum input voltage	A, B, or C inputs	$V_{CC\pm}$ = MAX, V_I = 5.5 V			1			1			1	mA
		D input				2			2			2	
I_{IH}	High-level input current	A, B, or C inputs	$V_{CC\pm}$ = MAX, V_I = 2.4 V			40			40			40	µA
		D input				80			80			80	
I_{IL}	Low-level input current	A, B, or C inputs	$V_{CC\pm}$ = MAX, V_I = 0.4 V			−3			−3			−3	mA
		D input				−6			−6			−6	
$I_{CC+(on)}$	Supply current from V_{CC+} with driver enabled		$V_{CC\pm}$ = MAX, A and B inputs at 0.4 V, C and D inputs at 2 V		18	30		23	35		25	40	mA
$I_{CC-(on)}$	Supply current from V_{CC-} with driver enabled				−18	−30		−34	−50		−65	−100	
$I_{CC+(off)}$	Supply current from V_{CC-} with driver inhibited		$V_{CC\pm}$ = MAX, A, B, C, and D inputs at 0.4 V		18			21			30		mA
$I_{CC-(off)}$	Supply current from $V_{CC\pm}$ with driver inhibited				−10			−17			−32		

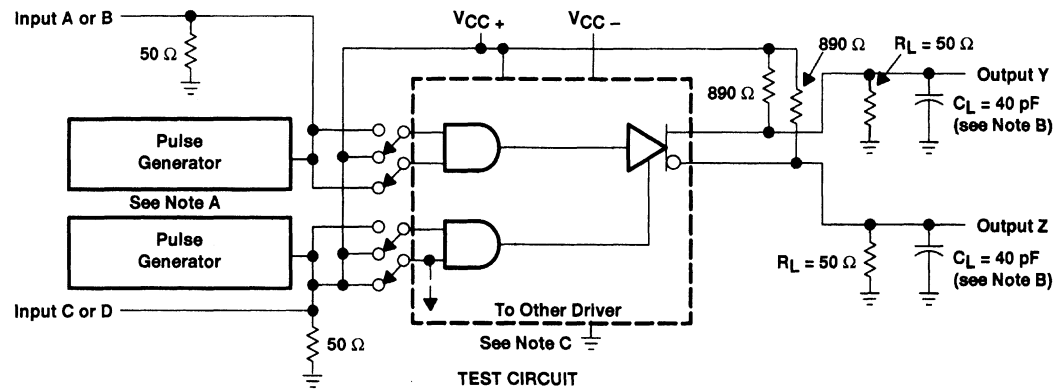
† For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

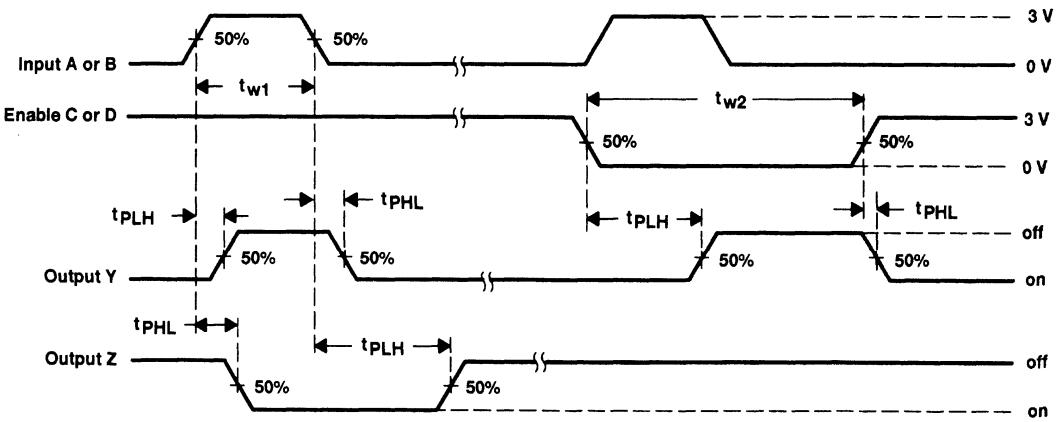
switching characteristics, $V_{CC\pm}$ = ±5 V, T_A = 25°C

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y or Z	C_L = 40 pF, R_L = 50 Ω, See Figure 1		9	15	ns
t_{PHL}					9	15	ns
t_{PLH}	C or D	Y or Z			16	25	ns
t_{PHL}					13	25	ns

† t_{PLH} = Propagation delay time, low-to-high-level output
t_{PHL} = Propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION





VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_O = 50 Ω, $t_r = t_f$ = 10 ± 5 ns, t_{w1} = 500 ns, PRR ≤ 1 MHz, t_{w2} = 1 µs, PRR ≤ 500 kHz.
B. C_L includes probe and jig capacitance.
C. For simplicity, only one channel and the enable connections are shown.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

SN55109A, SN75109A

ON-STATE OUTPUT CURRENT
vs
NEGATIVE SUPPLY VOLTAGE

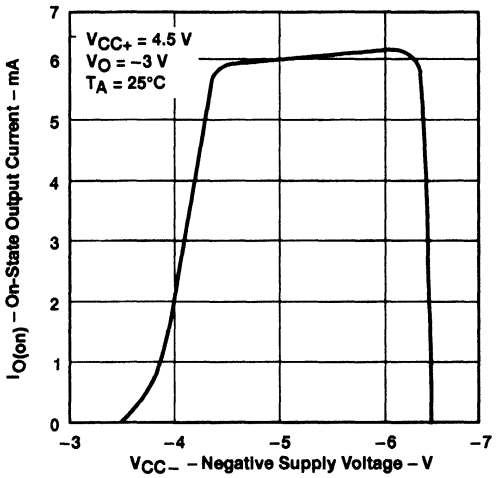


Figure 2

SN55110A, SN75110A

ON-STATE OUTPUT CURRENT
vs
NEGATIVE SUPPLY VOLTAGE

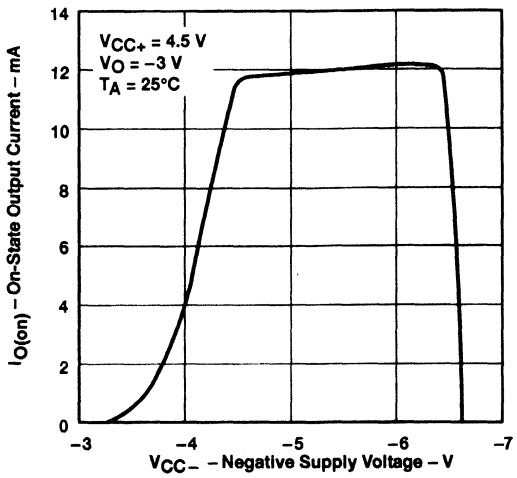


Figure 3

SN75112

ON-STATE OUTPUT CURRENT
vs
NEGATIVE SUPPLY VOLTAGE

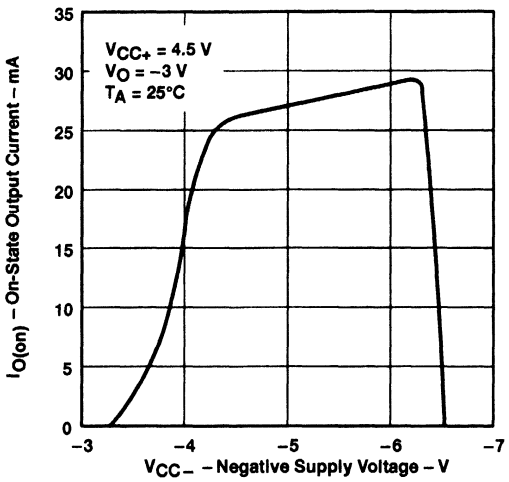


Figure 4

APPLICATION INFORMATION

special pulse-control circuit

Figure 5 shows a circuit that may be used as a pulse generator output or in many other testing applications.

INPUT	OUTPUTS	
A	Y	Z
High	Off	On
Low	On	Off

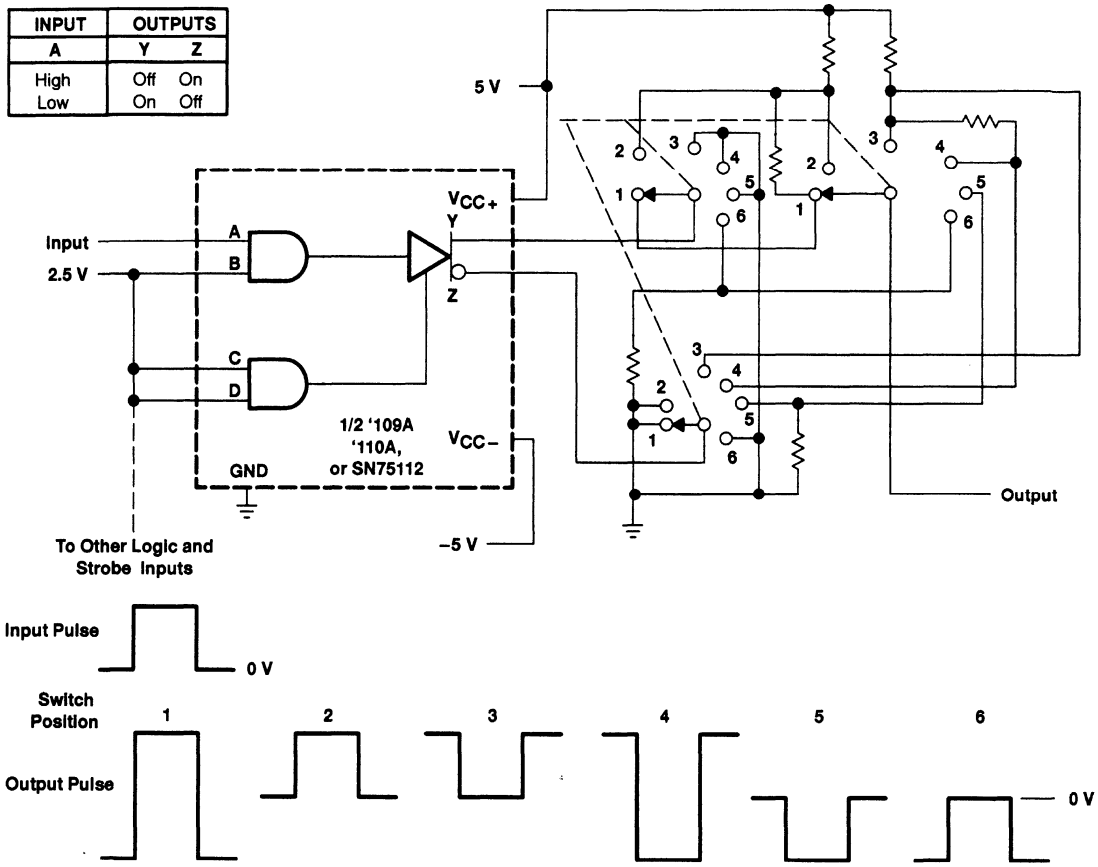


Figure 5. Pulse-Control Circuit

APPLICATION INFORMATION

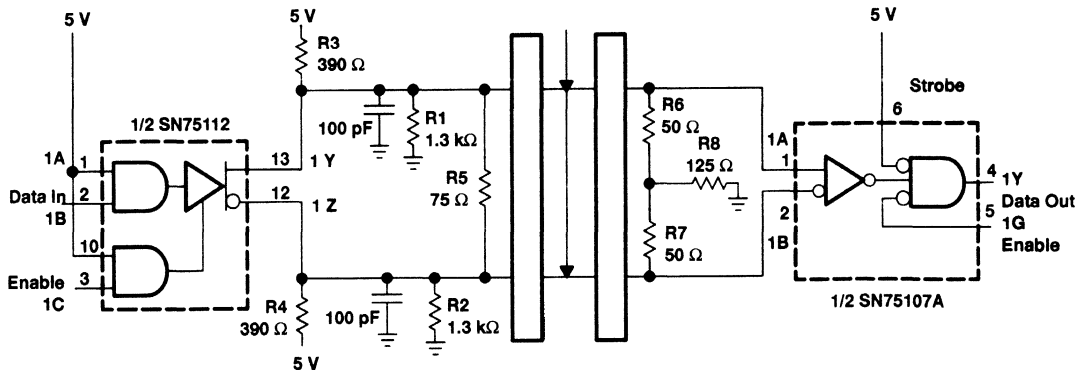
using the SN75112 as a CCITT recommended V.35 line driver

The SN75112 dual line driver, the SN75107A dual line receiver, and some external resistors can be used to implement the data interchange circuit of CCITT recommendation V.35 (1976) modem specification. The circuit of one channel is shown in Figure 1 and meets the requirement of the interface as specified by Appendix 11 of CCITT V.35 and summarized in Table 1 (V.35 has been replaced by ITU V.11).

Table 1. CCITT V.35 Electrical Requirements

	MIN	MAX	UNIT
GENERATOR			
Source impedance, Z_{source}	50	150	Ω
Resistance to ground, R	135	165	Ω
Differential output voltage, V_{OD}	440	660	mV
10% to 90% rise time, t_r	40		ns
or		0.01 × ui †	
Common-mode output voltage, V_{OC}	– 0.6	0.6	V
LOAD (RECEIVER)			
Input impedance, Z_I	90	110	Ω
Resistance to ground, R	135	165	Ω

† ui = unit interval or minimum signal element pulse width

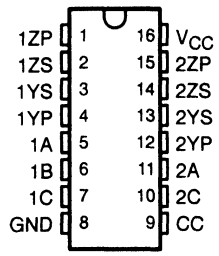


All resistors are 5%, 1/4 W.

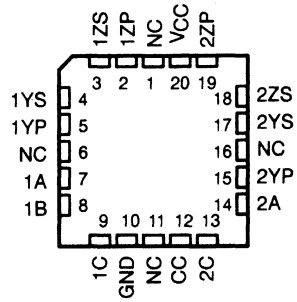
Figure 6. CCITT Recommended V.35 Interface Using the SN75112 and SN75107A

- Choice of Open-Collector, Open-Emitter, or 3-State Outputs
- High-Impedance Output State for Party-Line Applications
- Single-Ended or Differential AND/NAND Outputs
- Single 5-V Supply
- Dual Channel Operation
- Compatible With TTL
- Short-Circuit Protection
- High-Current Outputs
- Common and Individual Output Controls
- Clamp Diodes at Inputs and Outputs
- Easily Adaptable to SN55114 and SN75114 Applications
- Designed for Use With SN55115 and SN75115

SN55113 . . . J OR W PACKAGE
SN75113 . . . D OR N PACKAGE
(TOP VIEW)



SN55113 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN55113 and SN75113 dual differential line drivers with 3-state outputs are designed to provide all the features of the SN55114 and SN75114 line drivers with the added feature of driver output controls. Individual controls are provided for each output pair, as well as a common control for both output pairs. If any output is low, the associated output is in a high-impedance state and the output can neither drive nor load the bus. This permits many devices to be connected together on the same transmission line for party-line applications.

The output stages are similar to TTL totem-pole outputs, but with the sink outputs, YS and ZS, and the corresponding active pullup terminals, YP and ZP, available on adjacent package pins.

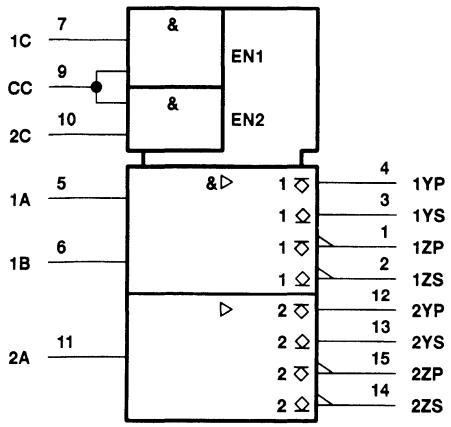
The SN55113 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN75113 is characterized for operation over the temperature range of 0°C to 70°C.

FUNCTION TABLE

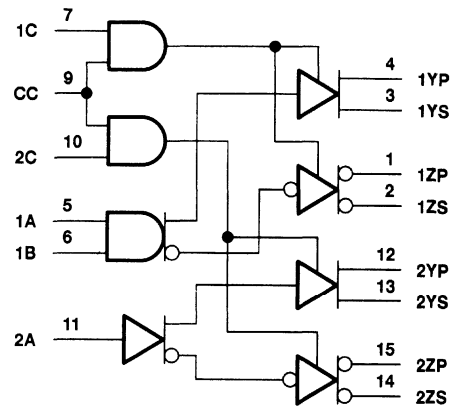
INPUTS				OUTPUTS	
OUTPUT CONTROL		DATA		AND	NAND
C	CC	A	B†	Y	Z
L	X	X	X	Z	Z
X	L	X	X	Z	Z
H	H	L	X	L	H
H	H	X	L	L	H
H	H	H	H	H	L

H = high level, L = low level, X = irrelevant,
Z = high impedance (off)
† B input and 4th line of function table are applicable only to driver number 1.

logic symbol†

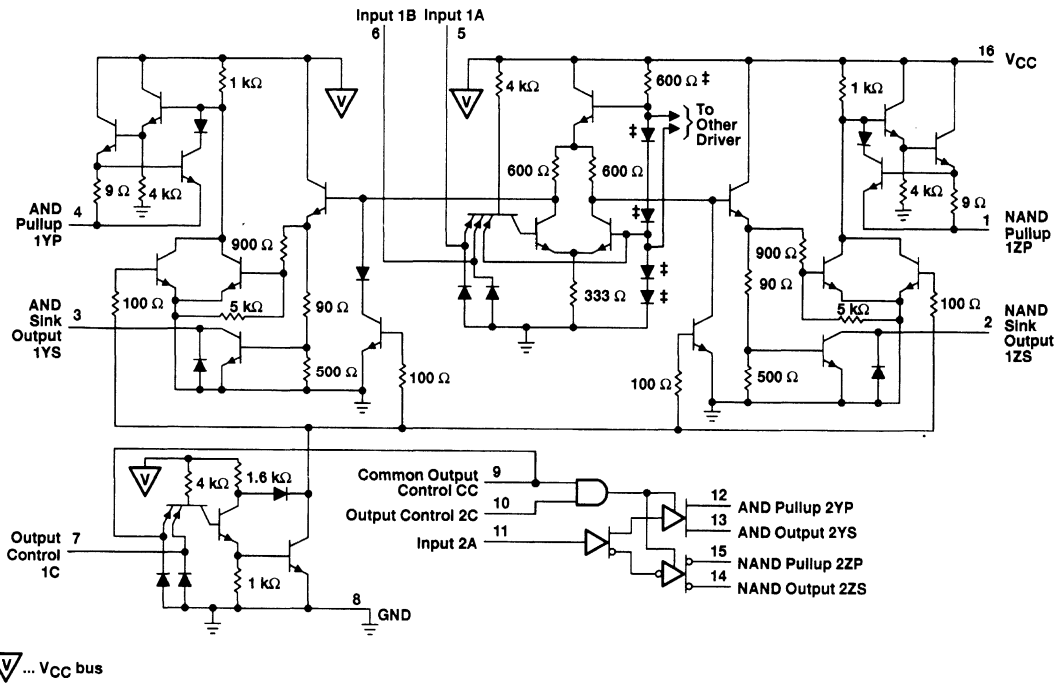


logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

schematic



▽ ... V_{CC} bus

‡ These components are common to both drivers.
Resistor values shown are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 5.5 V
Off-state voltage applied to open-collector outputs ..... 12 V
Continuous total power dissipation (see Note 2) ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN55113 ..... −55°C to 125°C
SN75113 ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package ..... 260°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network ground terminal.
2. In the J, FK, and W packages, SN55113 chips are alloy mounted; SN75113 chips are glass mounted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	N/A
W	1000 mW	8.0 mW/°C	640 mW	200 mW

recommended operating conditions

	SN55113			SN75113			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
High-level output current, I_{OH}			−40			−40	mA
Low-level output current, I_{OL}			40			40	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

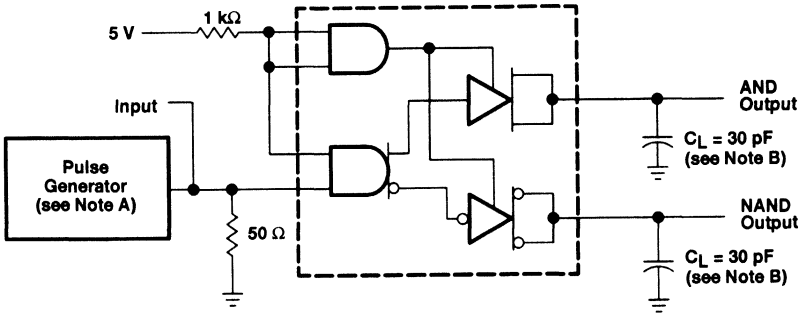
PARAMETER			TEST CONDITIONS†			SN55113			SN75113			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−0.9	−1.5		−0.9	−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V		I_{OH} = −10 mA	2.4	3.4		2.4	3.4		V
					I_{OH} = −40 mA	2	3.0		2	3.0		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 40 mA		V_{IL} = 0.8 V,		0.23	0.4		0.23	0.4	V
V_{OK}	Output clamp voltage		V_{CC} = MAX, I_O = −40 mA				−1.1	−1.5		−1.1	−1.5	V
$I_{O(off)}$	Off-state open-collector output current		V_{CC} = MAX	V_{OH} = 12 V	T_A = 25°C		1	10				μA
					T_A = 125°C			200				
				V_{OH} = 5.25 V	T_A = 25°C					1	10	
					T_A = 70°C						20	
I_{OZ}	Off-state (high-impedance-state) output current		V_{CC} = MAX, Output controls at 0.8 V	T_A = 25°C,	V_O = 0 to V_{CC}			±10			±10	μA
				T_A = MAX	V_O = 0			−150			−20	
					V_O = 0.4 V			±80			±20	
					V_O = 2.4 V			±80			±20	
					V_O = V_{CC}			80			20	
I_I	Input current at maximum input voltage	A, B, C	V_{CC} = MAX, V_I = 5.5 V					1			1	mA
		CC						2			2	
I_{IH}	High-level input current	A, B, C	V_{CC} = MAX, V_I = 2.4 V					40			40	μA
		CC						80			80	
I_{IL}	Low-level input current	A, B, C	V_{CC} = MAX, V_I = 0.4 V					−1.6			−1.6	mA
		CC						−3.2			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX, V_O = 0		T_A = 25°C	−40	−90	−120	−40	−90	−120	mA
I_{CC}	Supply current (both drivers)		All inputs at 0 V, T_A = 25°C	No load,	V_{CC} = MAX		47	65		47	65	mA
					V_{CC} = 7 V		65	85		65	85	

† All parameters with the exception of off-state open-collector output current are measured with the active pullup connected to the sink output. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at T_A = 25°C and V_{CC} = 5 V, with the exception of I_{CC} at 7 V.
§ Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

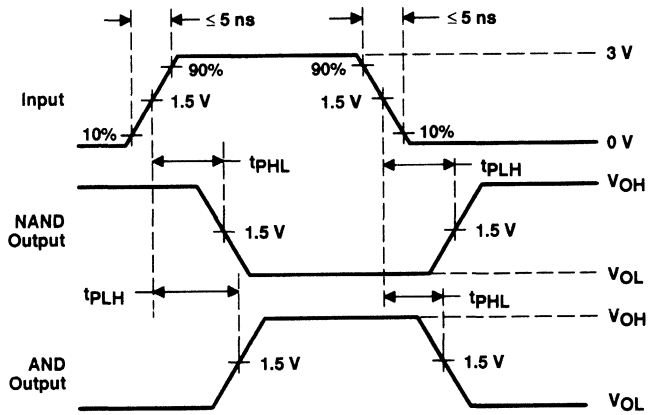
switching characteristics, V_{CC} = 5 V, C_L = 30 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN55113			SN75113			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high level output	See Figure 1		13	20		13	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output			12	20		12	30	ns
t_{PZH}	Output enable time to high level	R_L = 180 Ω, See Figure 2		7	15		7	20	ns
t_{PZL}	Output enable time to low level	R_L = 250 Ω, See Figure 3		14	30		14	40	ns
t_{PHZ}	Output disable time from high level	R_L = 180 Ω, See Figure 2		10	20		10	30	ns
t_{PLZ}	Output disable time from low level	R_L = 250 Ω, See Figure 3		17	35		17	35	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

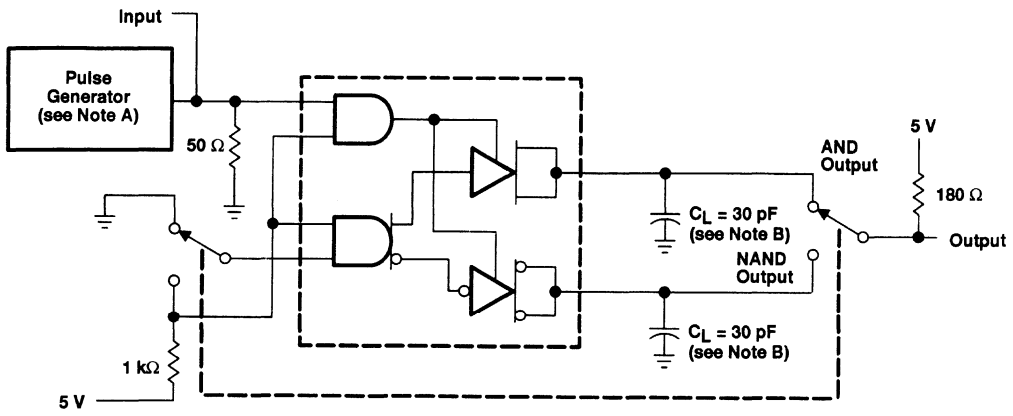


VOLTAGE WAVEFORMS

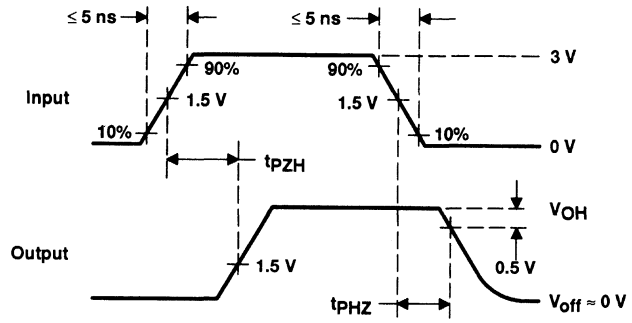
NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, PRR ≤ 500 kHz, t_w = 100 ns.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms t_{PLH} and t_{PHL}

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

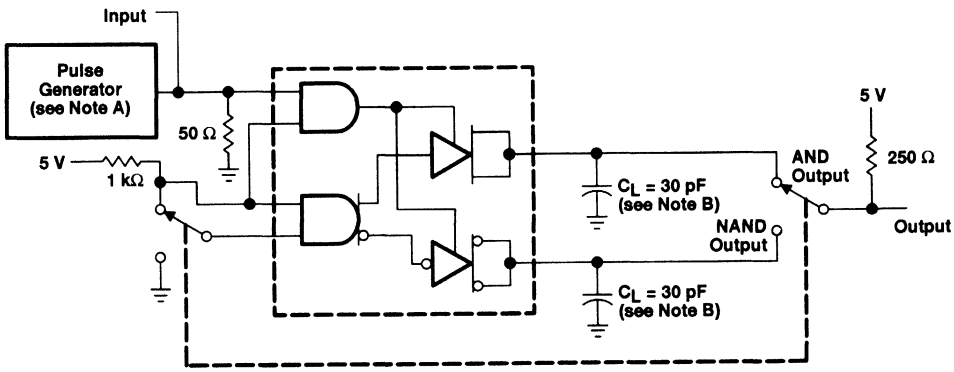


VOLTAGE WAVEFORMS

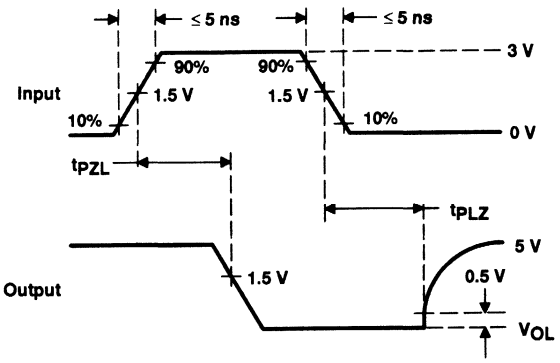
NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, PRR ≤ 500 kHz, t_w = 100 ns.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms t_{PZH} and t_{PHZ}

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, PRR ≤ 500 kHz, t_w = 100 ns.
B. C_L includes probe and jig capacitance.

Figure 3. Test Circuit and Voltage Waveforms, t_{PZL} and t_{PLZ}

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

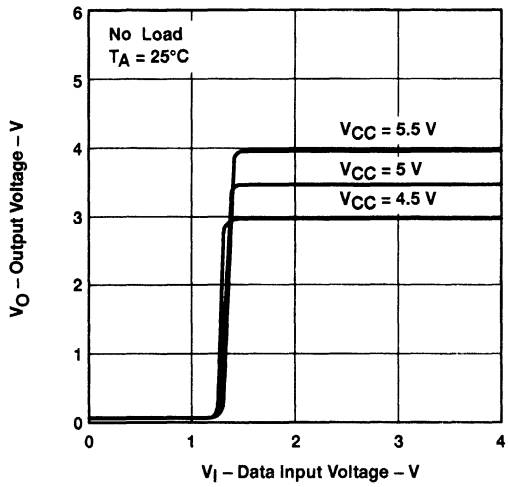


Figure 4

OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

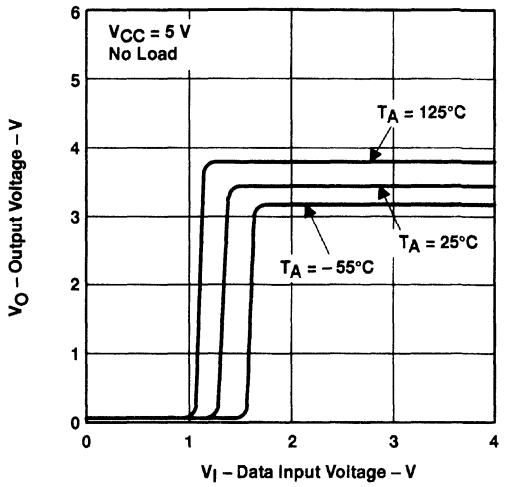


Figure 5

OUTPUT VOLTAGE
vs
INPUT VOLTAGE (OUTPUT CONTROL)

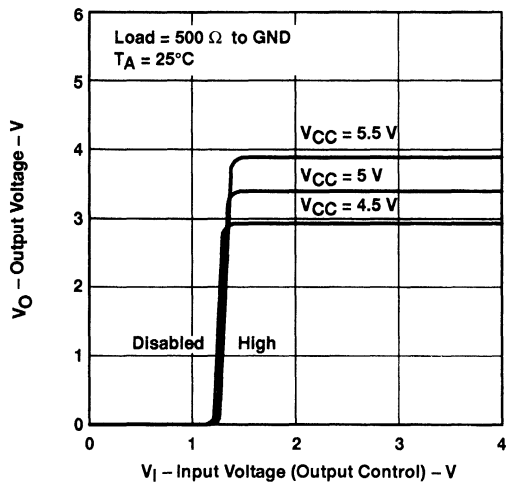


Figure 6

OUTPUT VOLTAGE
vs
INPUT VOLTAGE (OUTPUT CONTROL)

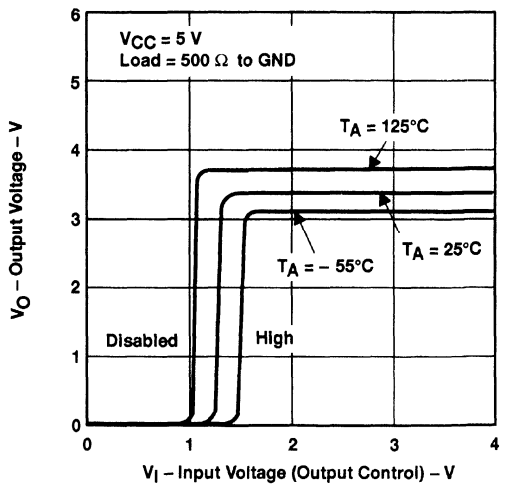


Figure 7

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55113 circuits only. These parameters were measured with the active pullup connected to the sink output.

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
INPUT VOLTAGE (OUTPUT CONTROL)

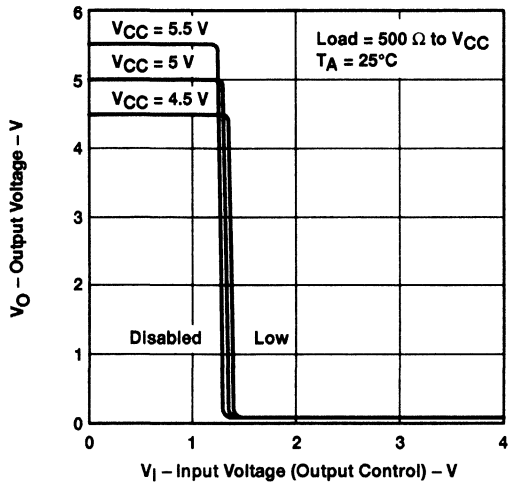


Figure 8

OUTPUT VOLTAGE
vs
INPUT VOLTAGE (OUTPUT CONTROL)

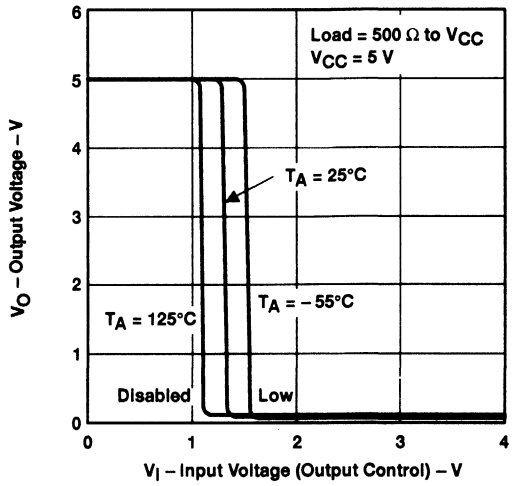


Figure 9

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

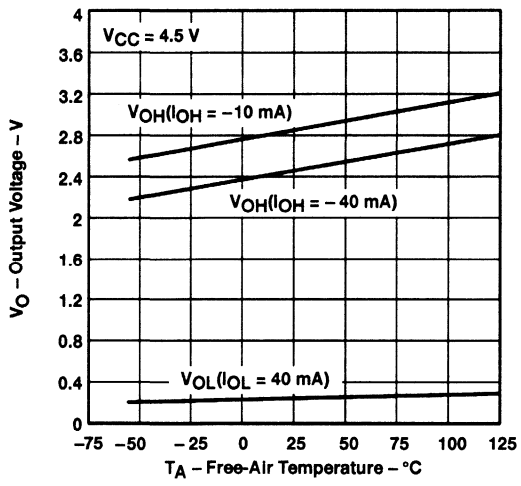


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

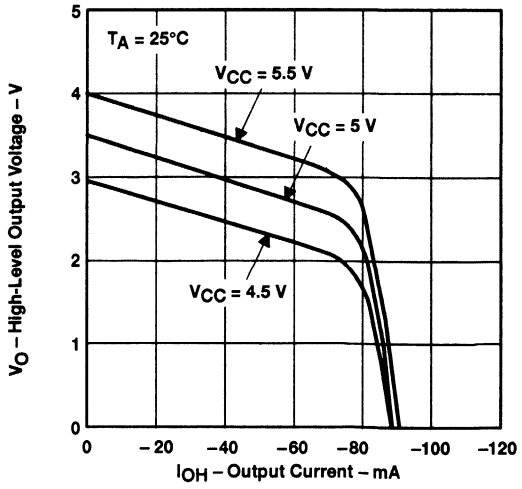


Figure 11

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55113 circuits only. These parameters were measured with the active pullup connected to the sink output.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

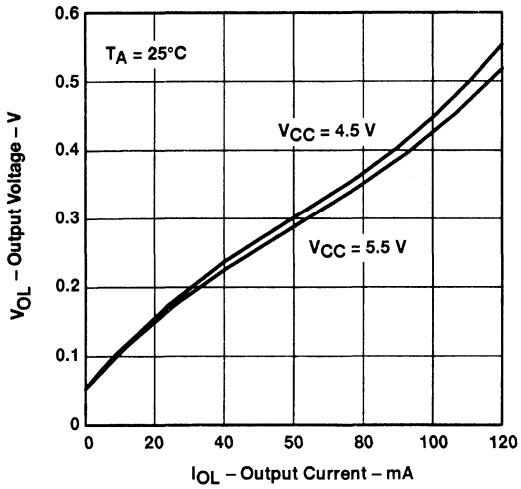


Figure 12

SUPPLY CURRENT
(BOTH DRIVERS)
vs
SUPPLY VOLTAGE

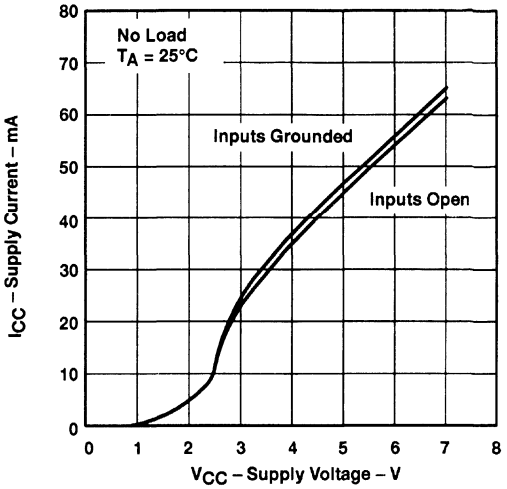


Figure 13

SUPPLY CURRENT
(BOTH DRIVERS)
vs
OUTPUT CURRENT

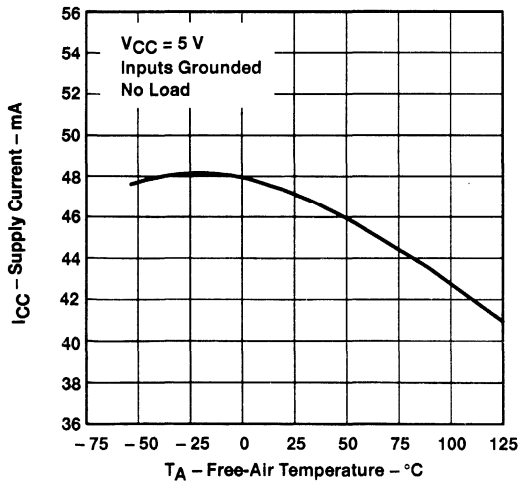


Figure 14

SUPPLY CURRENT
(BOTH DRIVERS)
vs
SUPPLY VOLTAGE

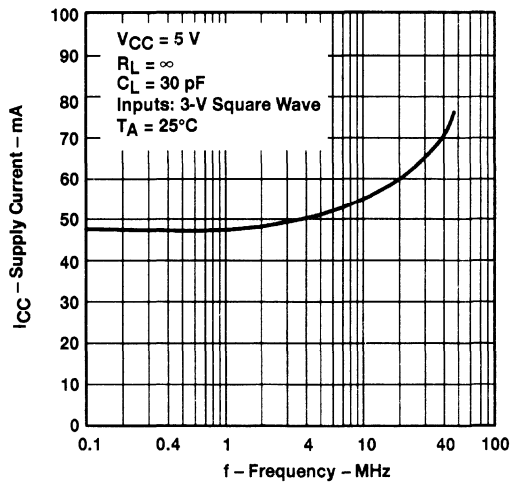


Figure 15

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55113 circuits only. These parameters were measured with the active pullup connected to the sink output.

TYPICAL CHARACTERISTICS†

PROPAGATION DELAY TIMES FROM DATA INPUTS vs FREE-AIR TEMPERATURE

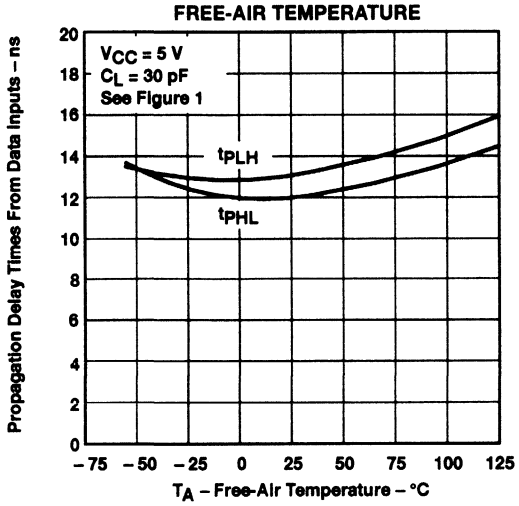


Figure 16

OUTPUT ENABLE AND DISABLE TIMES vs FREE-AIR TEMPERATURE

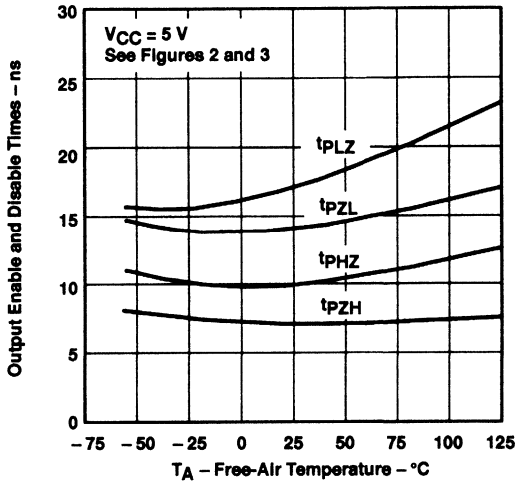
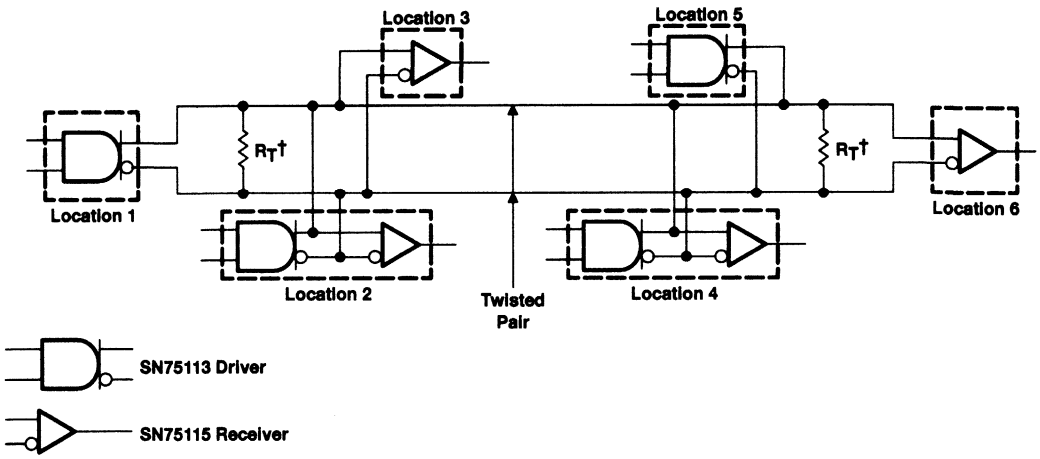


Figure 17

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55113 circuits only. These parameters were measured with the active pullup connected to the sink output.

APPLICATION INFORMATION



† $R_T = Z_O$. A capacitor may be connected in series with R_T to reduce power dissipation.

Figure 18. Basic Party-Line or Data-Bus Differential Data Transmission

SLLS071B – SEPTEMBER 1973 – REVISED MAY 1995

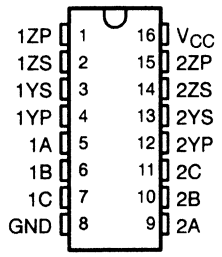
- **Choice of Open-Collector, Open-Emitter, or Totem-Pole Outputs**
- **Single-Ended or Differential AND/NAND Outputs**
- **Single 5-V Supply**
- **Dual-Channel Operation**
- **TTL Compatible**
- **Short-Circuit Protection**
- **High-Current Outputs**
- **Triple Inputs**
- **Clamp Diodes at Inputs and Outputs**
- **Designed for Use With SN55115 and SN75115 Differential Line Receivers**
- **Designed to Be Interchangeable With National DS9614 Line Driver**

description

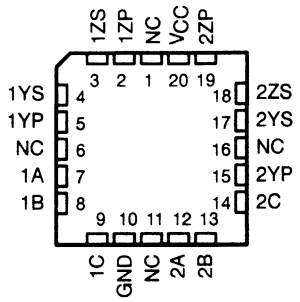
The SN55114 and SN75114 dual differential line drivers are designed to provide differential output signals with the high-current capability for driving balanced lines, such as twisted pair, at normal line impedances without high power dissipation. The output stages are similar to TTL totem-pole outputs, but with the sink outputs, YS and ZS, and the corresponding active pullup terminals, YP and ZP, available on adjacent package pins. Since the output stages provide TTL-compatible output levels, these devices may also be used as TTL expanders or phase splitters.

The SN55114 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN75114 is characterized for operation from 0°C to 70°C.

SN55114 . . . J OR W PACKAGE
SN75114 . . . D OR N PACKAGE
(TOP VIEW)



SN55114 . . . FK PACKAGE
(TOP VIEW)



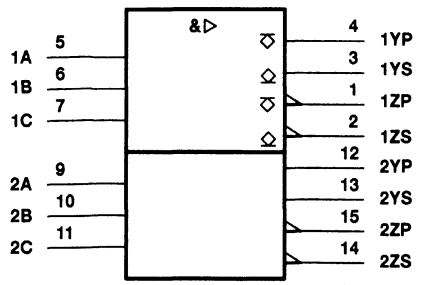
NC – No internal connection

FUNCTION TABLE

INPUTS			OUTPUTS	
A	B	C	Y	Z
H	L	H	H	L
All other inputs combinations			L	H

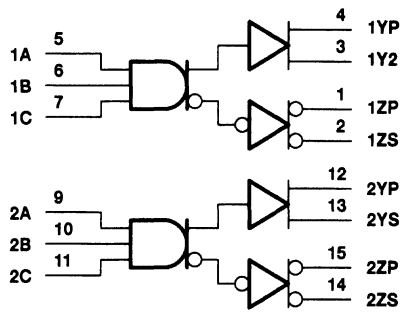
H = high level, L = low level

logic symbol†

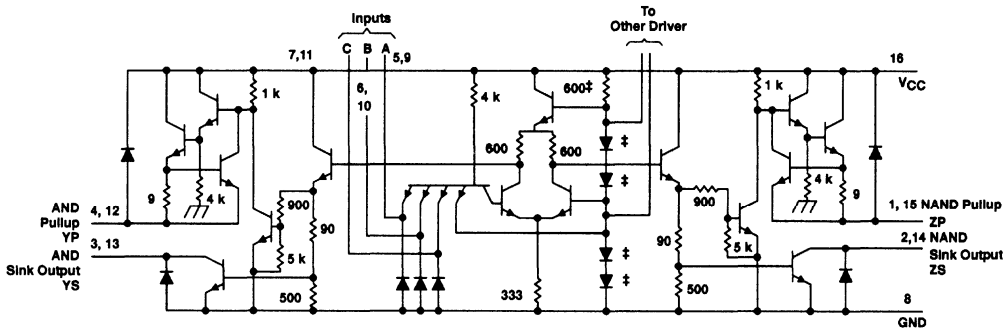


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)



schematic (each driver)



‡ These components are common to both drivers. Resistor values shown are nominal and in ohms.
Pin numbers shown are for the D, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

	SN55114	SN75114	UNIT
Supply voltage, V_{CC} (see Note 1)	7	7	V
Input voltage, V_I	5.5	5.5	V
Off-state voltage applied to open-collector outputs	12	12	V
Continuous total power dissipation	See Dissipation Rating Table		
Operating free-air temperature range, T_A	−55 to 125	0 to 70	°C
Storage temperature range, T_{stg}	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds, T_C: FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package	300		°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package		260	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	—
FK‡	1375 mW	11.0 mW/°C	880 mW	275 mW
J‡	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—
W‡	1000 mW	8.0 mW/°C	640 mW	200 MW

‡ In the FK, J, and W packages, SN55114 chips are either silver glass or alloy mounted.

recommended operating conditions

	SN55114			SN75114			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
High-level output current, I_{OH}			−40			−40	mA
Low-level output current, I_{OL}			40			40	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

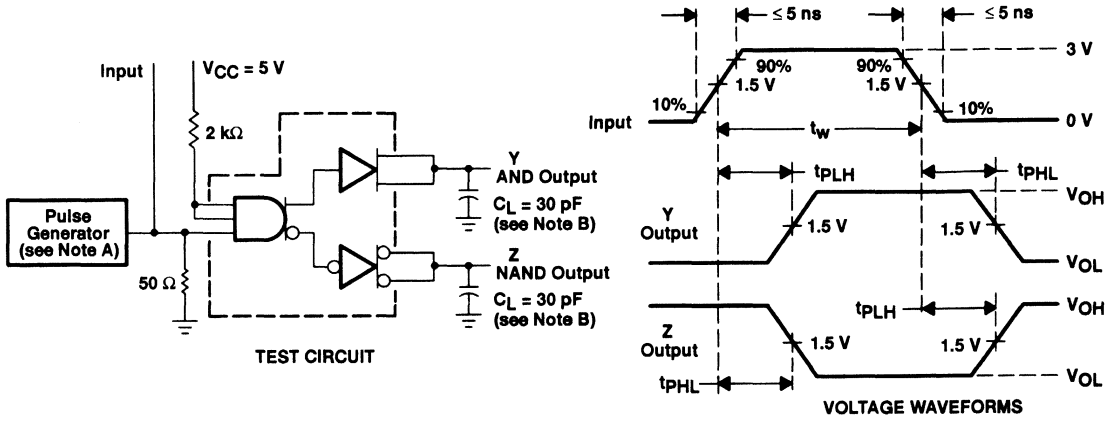
PARAMETER		TEST CONDITIONS†			SN55114			SN75114			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−0.9	−1.5		−0.9	−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V		I_{OH} = −10 mA	2.4	3.4		2.4	3.4		V
				I_{OH} = −40 mA	2	3		2	3		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 40 mA				0.2	0.4		0.2	0.45	V
V_{OK}	Output clamp voltage	V_{CC} = 5 V, I_O = 40 mA,		T_A = 25°C		6.1	6.5		6.1	6.5	V
		V_{CC} = MAX, I_O = −40 mA,		T_A = 25°C		−1.1	−1.5		−1.1	−1.5	
$I_{O(off)}$	Off-state open collector output current	V_{CC} = MAX	V_{OH} = 12 V	T_A = 25°C		1	100				μA
				T_A = 125°C			200				
			V_{OH} = 5.25 V	T_A = 25°C					1	100	
				T_A = 70°C						200	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V					1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V					40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.1	−1.6		−1.1	−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX, V_O = 0,		T_A = 25°C	−40	−90	−120	−40	−90	−120	mA
I_{CC}	Supply current (both drivers)	All inputs at 0 V, No load, T_A = 25°C		V_{CC} = MAX		37	50		37	50	mA
				V_{CC} = 7 V		47	65		47	70	

† All parameters with the exception of off-state open-collector output current are measured with the active pullup connected to the sink output. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at T_A = 25°C and V_{CC} = 5 V, with the exception of I_{CC} at 7 V.
§ Only one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN55114			SN75114			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 30 pF, See Figure 1		15	20		15	30	ns
t_{PHL}	Propagation delay time, high- to low-level output			11	20		11	30	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: Z_O = 500 Ω, PRR ≤ 500 kHz, t_w ≤ 100 ns.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

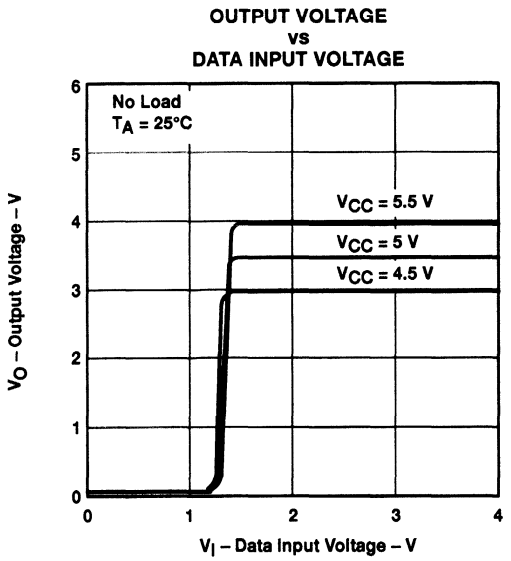


Figure 2

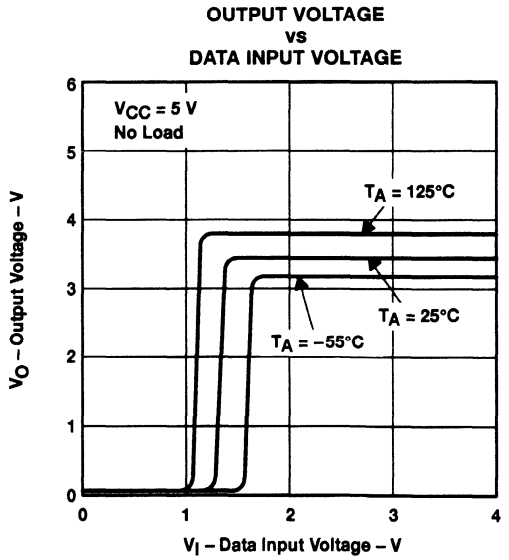


Figure 3

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55114 circuits only. These parameters were measured with the active pullup connected to the sink output.

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

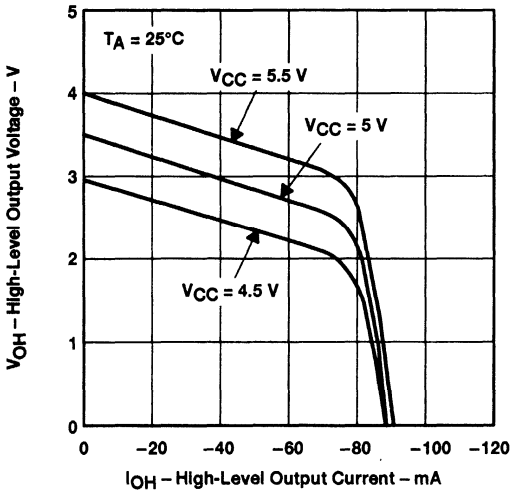


Figure 4

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

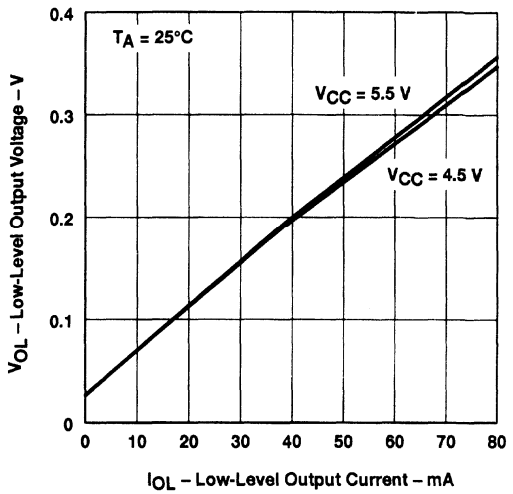


Figure 5

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

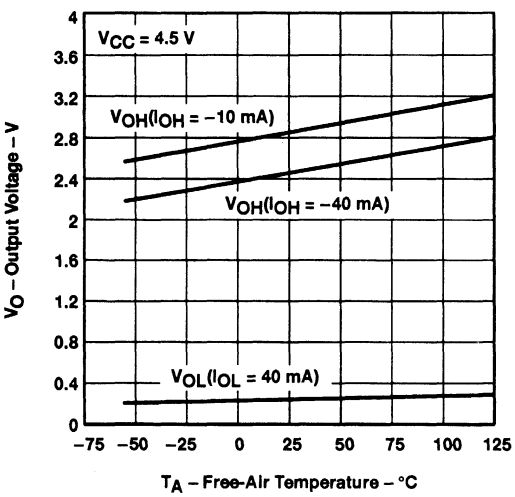


Figure 6

PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

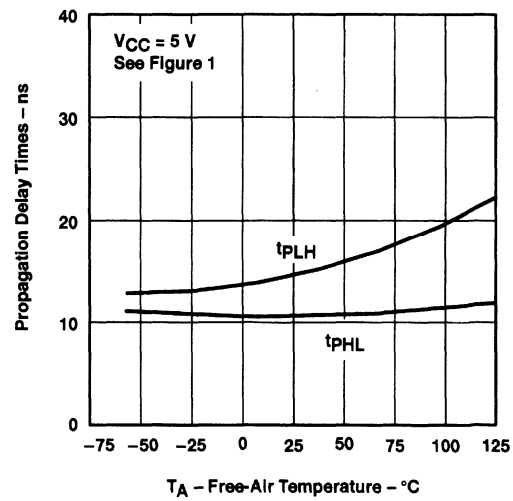


Figure 7

† Data for temperatures below 0°C and above 70°C are applicable to SN55114 circuits only. These parameters were measured with the active pullup connected to the sink output.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT (BOTH DRIVERS) VS SUPPLY VOLTAGE

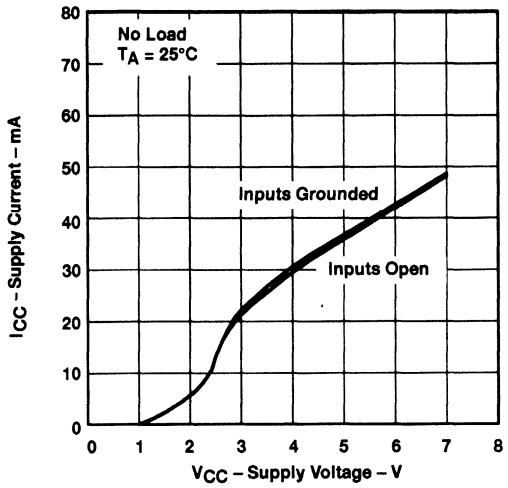


Figure 8

SUPPLY CURRENT (BOTH DRIVERS) VS FREE-AIR TEMPERATURE

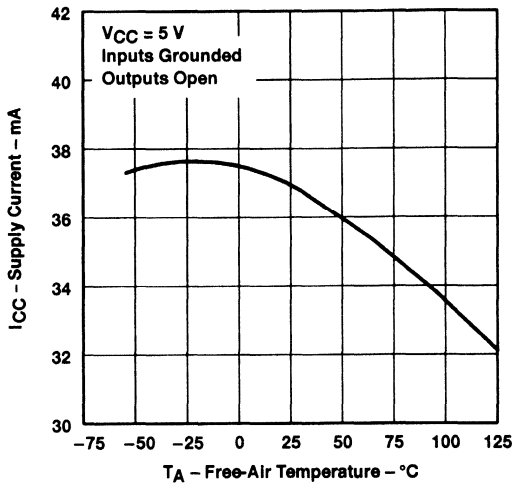


Figure 9

SUPPLY CURRENT (BOTH DRIVERS) VS FREQUENCY

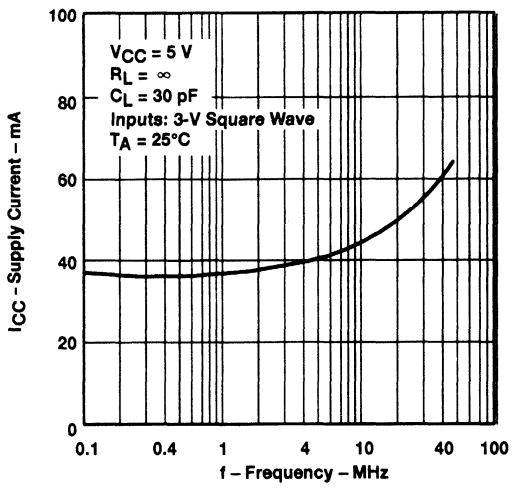
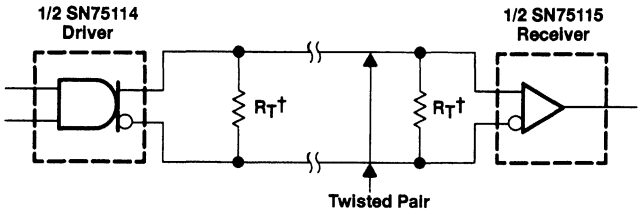


Figure 10

† Data for temperatures below 0°C and above 70°C are applicable to SN55114 circuits only. These parameters were measured with the active pullup connected to the sink output.

APPLICATION INFORMATION



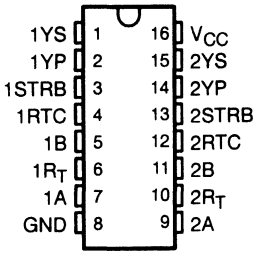
† $R_T = Z_O$. A capacitor may be connected in series with R_T to reduce power dissipation.

Figure 11. Basic Party-Line or Data-Bus Differential Data Transmission

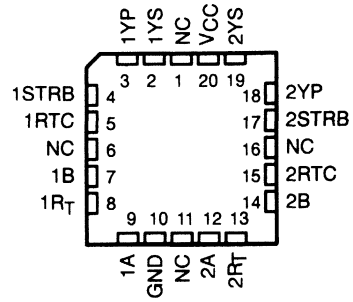
SLLS072B – SEPTEMBER 1973 – REVISED MAY 1995

- **Choice of Open-Collector or Active Pullup (Totem-Pole) Outputs**
- **Single 5-V Supply**
- **Differential Line Operation**
- **Dual-Channel Operation**
- **TTL Compatible**
- **±15-V Common-Mode Input Voltage Range**
- **Optional-Use Built-In 130-Ω Line-Terminating Resistor**
- **Individual Frequency Response Controls**
- **Individual Channel Strobes**
- **Designed for Use With SN55113, SN75113, SN55114, and SN75114 Drivers**
- **Designed to Be Interchangeable With National DS9615 Line Receivers**

SN55115 . . . J OR W PACKAGE
SN75115 . . . D OR N PACKAGE
(TOP VIEW)



SN55114 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN55115 and SN75115 dual differential line receivers are designed to sense small differential signals in the presence of large common-mode noise. These devices give TTL-compatible output signals as a function of the differential input voltage. The open-collector output configuration permits the wire-ANDing of similar TTL outputs (such as SN5401/SN7401) or other SN55115/SN75115 line receivers. This permits a level of logic to be implemented without extra delay. The output stages are similar to TTL totem-pole outputs, but with sink outputs, 1YS and 2YS, and the corresponding active pullup terminals, 1YP and 2YP, available on adjacent package pins. The frequency response and noise immunity may be provided by a single external capacitor. A strobe input is provided for each channel. With the strobe in the low level, the receiver is disabled and the outputs are forced to a high level.

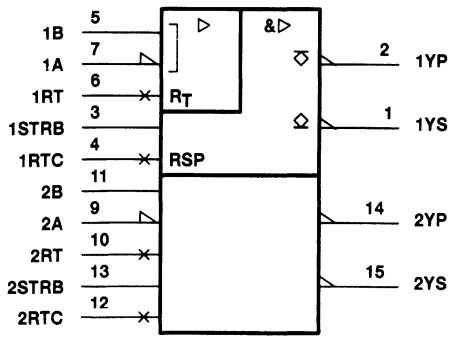
FUNCTION TABLE

STRB	DIFF INPUT (A AND B)	OUTPUT (YP AND YS TIED TOGETHER)
L	X	H
H	L	H
H	H	L

$H = V_I \geq V_{IH}$ min or V_{ID} more positive than V_{T+} max
$L = V_I \leq V_{IL}$ max or V_{ID} more negative than V_{T-} max
X = irrelevant

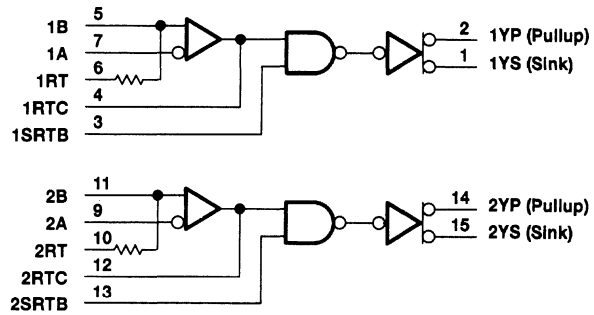
The SN55115 is characterized for operation over the full military range of −55°C to 125°C. The SN75115 is characterized for operation from 0°C to 70°C.

logic symbol†

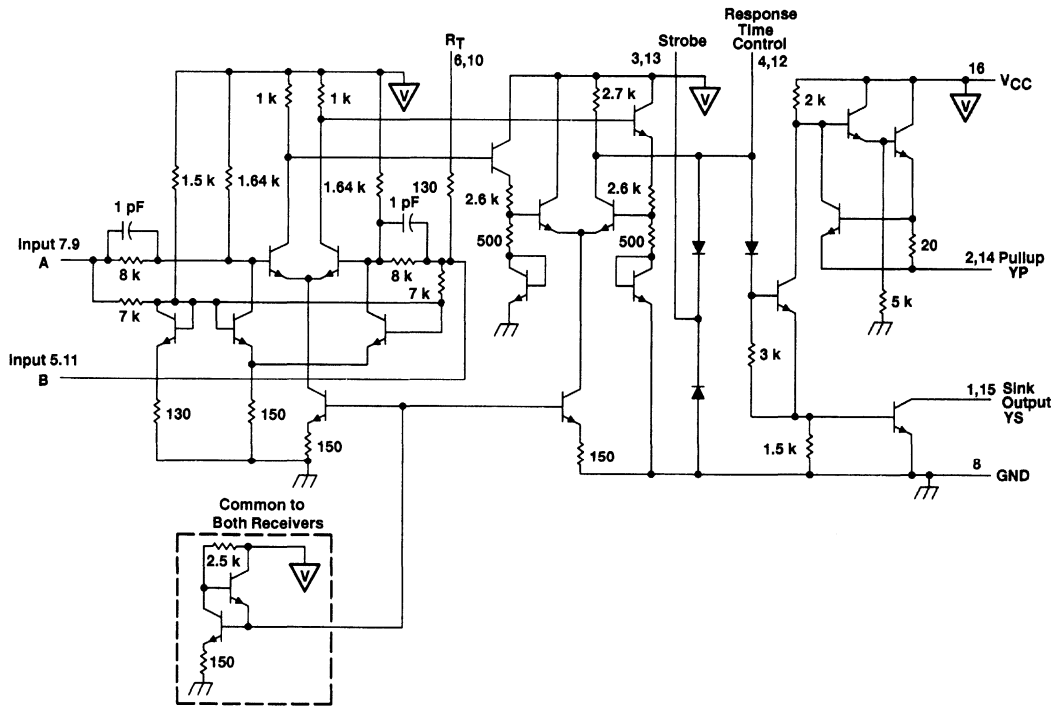


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic (each receiver)



Resistor values are nominal and in ohms.
Pin numbers shown are for D, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

	SN55115	SN75115	UNIT
Supply voltage, V_{CC} (see Note 1)	7	7	V
Input voltage, V_I (A, B, and R_T)	±25	±25	V
Input voltage, V_I (STRB)	5.5	5.5	V
Off-state voltage applied to open-collector outputs	14	14	V
Continuous total power dissipation	See Dissipation Rating Table		
Operating free-air temperature range, T_A	−55 to 125	0 to 70	°C
Storage temperature range, T_{stg}	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds: FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package	300		°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package		260	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential input voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	—
FK†	1375 mW	11.0 mW/°C	880 mW	275 mW
J†	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—
W†	1000 mW	8.0 mW/°C	640 mW	200 mW

† In the FK, J, and W packages, SN55115 chips are either silver glass or alloy mounted. SN75115 chips are glass mounted.

recommended operating conditions

	SN55115			SN75115			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage at STRB, V_{IH}	2.4			2.4			V
Low-level input voltage at STRB, V_{IL}			0.4			0.4	V
High-level output current, I_{OH}			−5			−5	mA
Low-level output current, I_{OL}			15			15	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

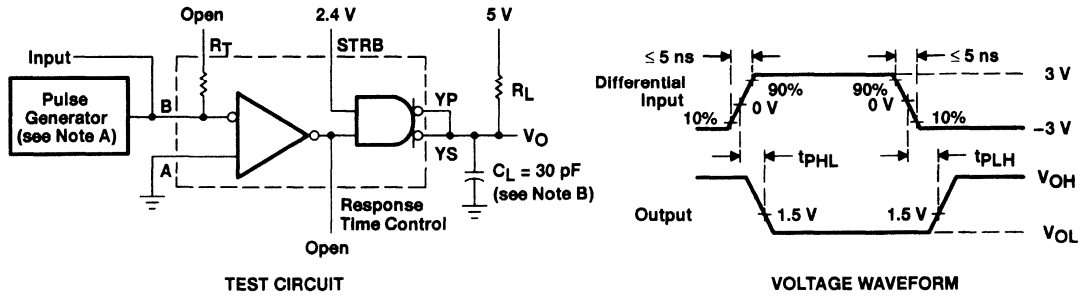
PARAMETER		TEST CONDITIONS†		SN55115			SN75115			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IT+}§	Positive-going threshold voltage	V_O = 0 .4 V, I_{OL} = 15 mA, V_{IC} = 0				500			500	mV
V_{IT-}§	Negative-going threshold voltage	V_O = 2 .4 V, I_{OH} = −5 mA, V_{IC} = 0		−500¶			−500¶			mV
V_{ICR}	Common-mode input voltage range	V_{ID} = ±1 V		+15 to −15	+24 to −19		+15 to −15	+24 to −19		V
V_{OH}	High-level ouput voltage	V_{CC} = MIN, V_{ID} = −0.5 V, I_{OH} = −5 mA	T_A = MIN	2.2			2.4			V
			T_A = 25°C	2.4	3.4		2.4	3.4		
			T_A = MAX	2.4			2.4			
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{ID} = −0.5 V, I_{OL} = 15 mA			0.22	0.4		0.22	0.45	V
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V, Other input at 5.5 V	T_A = MIN			−0.9			−0.9	mA
			T_A = 25°C		−0.5	−0.7		−0.5	−0.7	
			T_A = MAX			−0.7			−0.7	
I_{SH}	High-level strobe current	V_{CC} = MIN, V_{ID} = −0.5 V, V_{strobe} = 4.5 V	T_A = 25°C			2			5	µA
			T_A = MAX			5			10	
I_{SL}	Low-level strobe current	V_{CC} = MAX, V_{ID} = 0.5 V, V_{strobe} = 0.4 V	T_A = 25°C		−1.15	−2.4		−1.15	−2.4	mA
$I_{(RTC)}$	Response-time-control current	V_{CC} = MAX, V_{ID} = 0.5 V, V_{RC} = 0	T_A = 25°C	−1.2	−3.4		−1.2	−3.4		mA
$I_{O(off)}$	Off-state open-collector output current	V_{CC} = MIN, V_{OH} = 12 V, V_{ID} = −4.5 V	T_A = 25°C			100				µA
			T_A = MAX			200				
		V_{CC} = MIN, V_{OH} = 5.25 V, V_{ID} = −4.75 V	T_A = 25°C						100	
			T_A = MAX						200	
R_T	Line-terminating resistance	V_{CC} = 5 V	T_A = 25°C	77	130	167	74	130	179	Ω
I_{OS}	Supply-circuit output current#	V_{CC} = MAX, V_{ID} = −0.5 V, V_O = 0	T_A = 25°C	−15	−40	−80	−14	−40	−100	mA
I_{CC}	Supply current (both receivers)	V_{CC} = MAX, V_{ID} = 0.5 V, V_{IC} = 0	T_A = 25°C		32	50		32	50	mA

† Unless otherwise noted, V_{strobe} = 2.4 V. All parameters with the exception of off-state open-collector output current are measured with the active pull-up connected to the sink output.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C, and V_{IC} = 0.
§ Differential voltages are at the B input terminal with respect to the A input terminal.
¶ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltages only.
# Only one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, C_L = 30 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN55115			SN75115			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high level output	R_L = 3.9 kΩ, See Figure 1		18	50		18	75	ns
t_{PHL}	Propagation delay time, high-to-low level output	R_L = 390 Ω, See Figure 1		20	50		20	75	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORM

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, PRR ≤ 500 kHz, t_w ≤ 100 ns, duty cycle = 50%.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

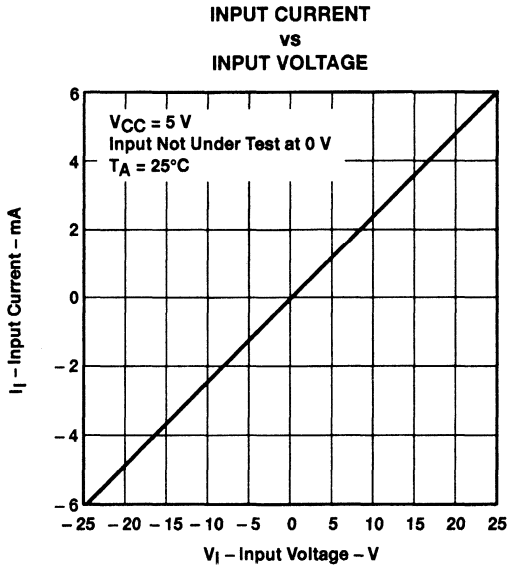


Figure 2

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

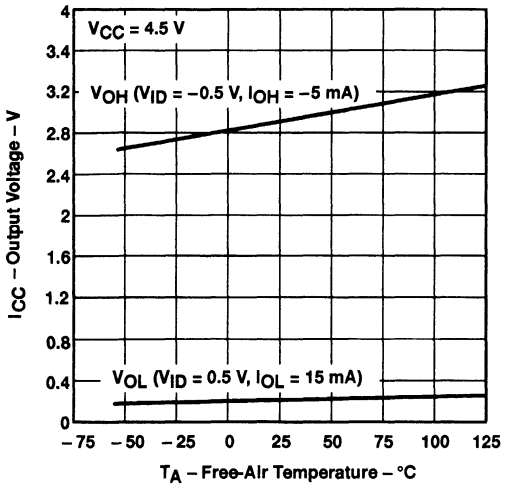


Figure 3

OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

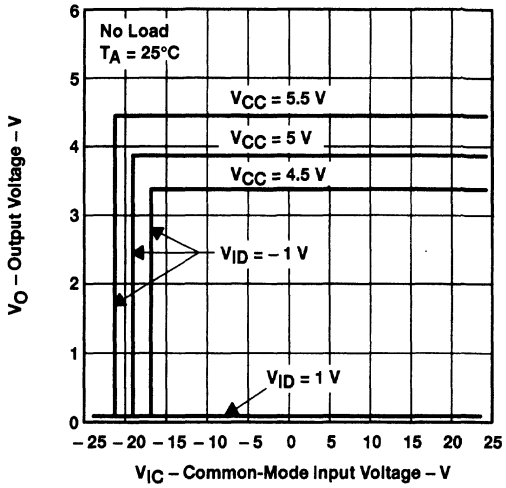


Figure 4

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

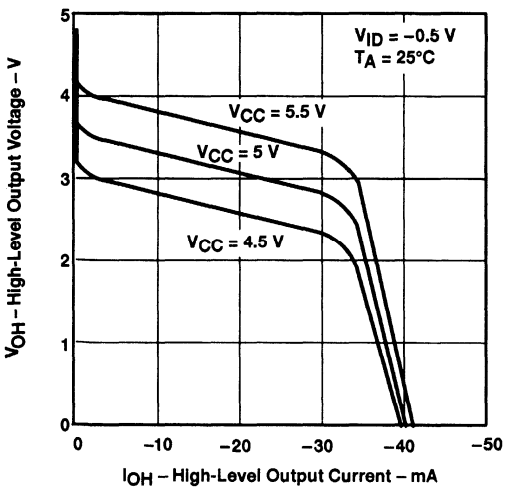


Figure 5

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL 1OUTPUT CURRENT

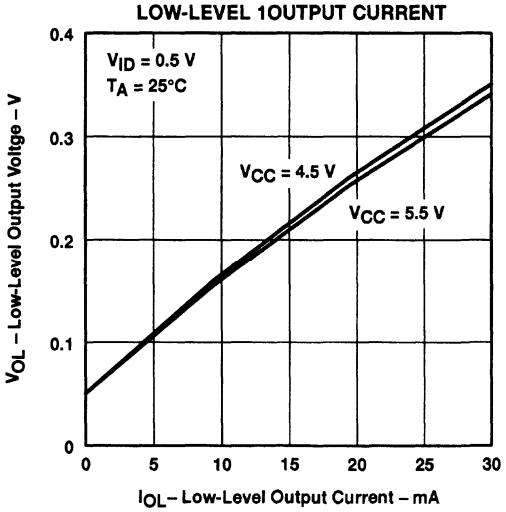


Figure 6

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55115 circuits only. These parameters were measured with the active pullup connected to the sink output.

TYPICAL CHARACTERISTICS†

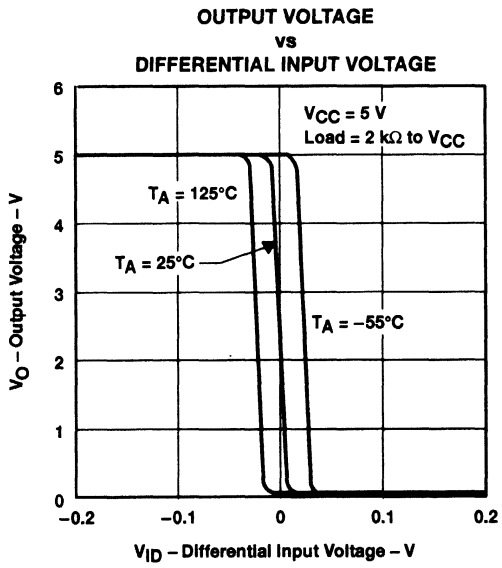


Figure 7

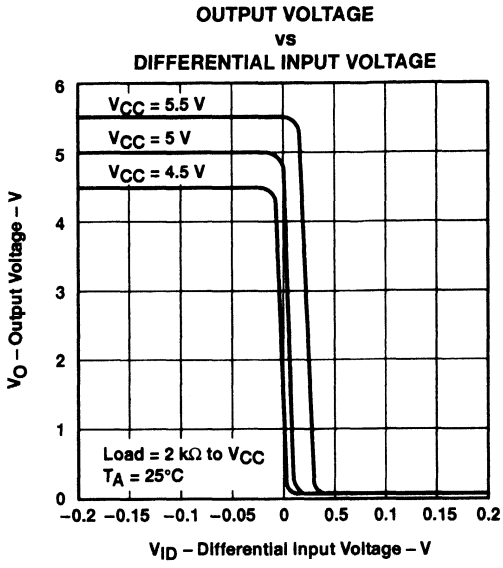


Figure 8

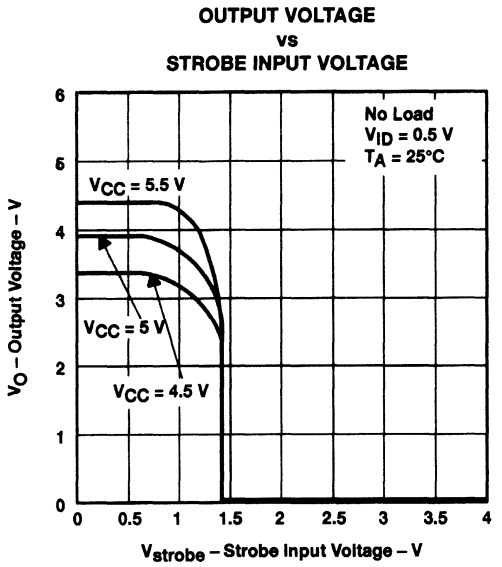


Figure 9

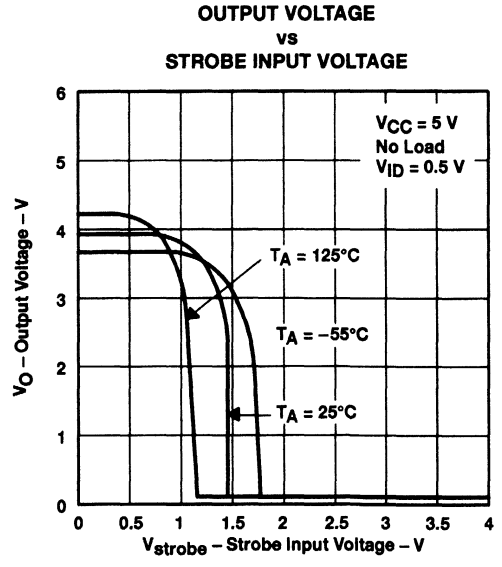


Figure 10

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55115 circuits only. These parameters were measured with the active pullup connected to the sink output.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
(BOTH RECEIVERS)
vs
SUPPLY VOLTAGE

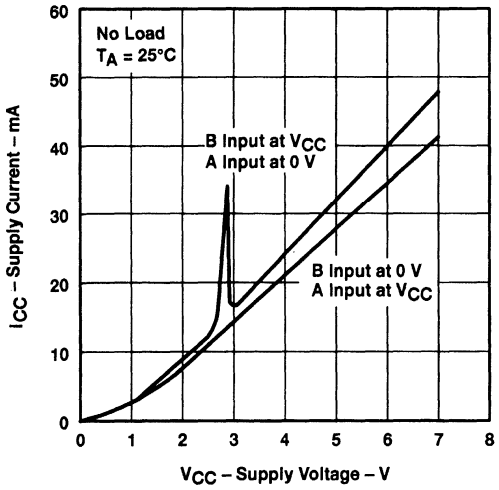


Figure 11

SUPPLY CURRENT
(BOTH RECEIVERS)
vs
FREE-AIR TEMPERATURE

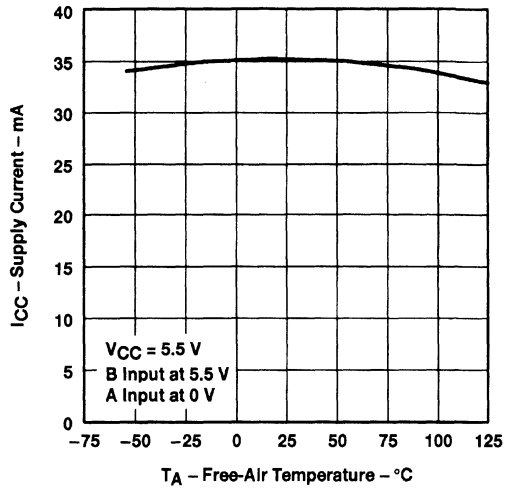


Figure 12

PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

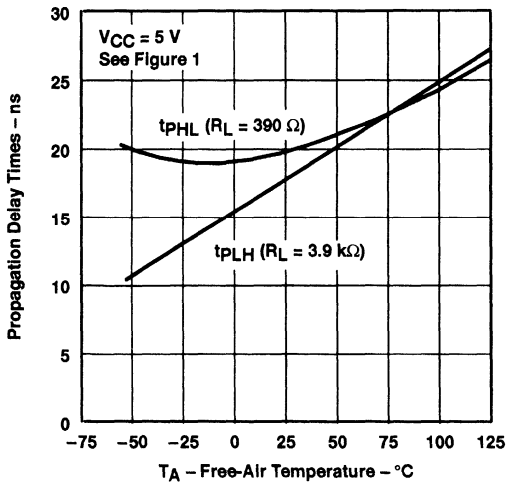


Figure 13

MAXIMUM OPERATING FREQUENCY
vs
RESPONSE-TIME-CONTROL CAPACITANCE

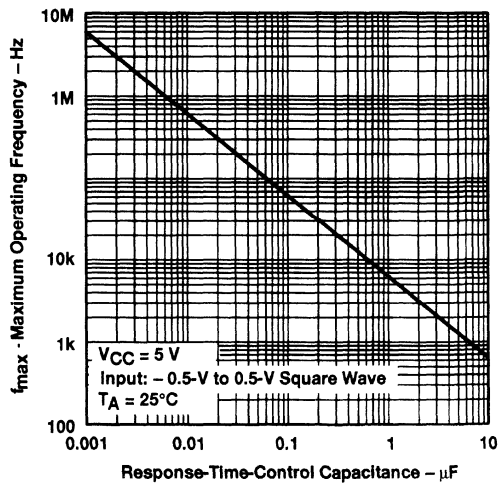
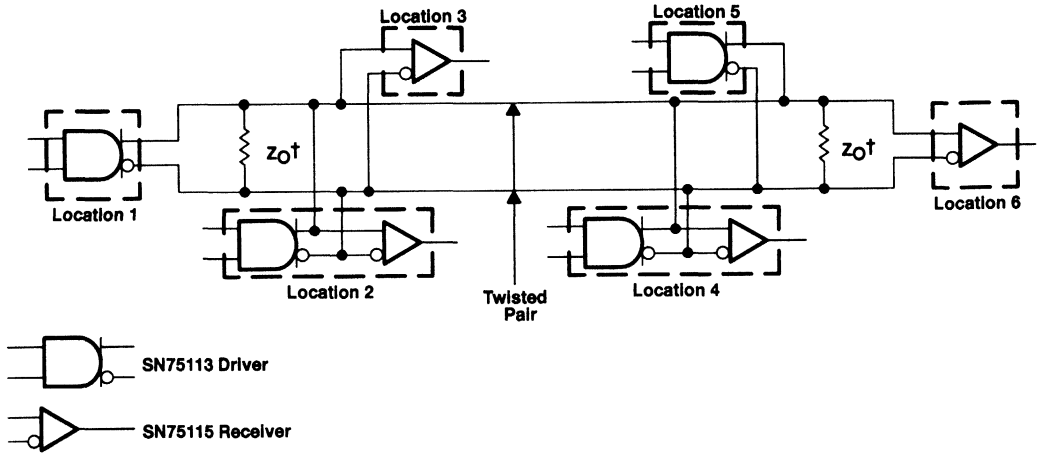


Figure 14

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55115 circuits only. These parameters were measured with the active pullup connected to the sink output.

APPLICATION INFORMATION



† $Z_O = R_T$. A capacitor may be connected in series with Z_O to reduce power dissipation.

Figure 15. Basic Party-Line or Data-Bus Differential Data Transmission

SN55116, SN75116, THRU SN75119
DIFFERENTIAL LINE TRANSCEIVERS

SLLS073B – MAY 1976 – REVISED MAY 1995

features common to all types

- Single 5-V Supply
- 3-State Driver Output Circuitry
- TTL-Compatible Driver Inputs
- TTL-Compatible Receiver Output
- Differential Line Operation
- Receiver Output Strobe ('116, SN75117) or Enable (SN75118, SN75119)
- Designed for Party-Line (Data-Bus) Applications
- Choice of Ceramic or Plastic Packages

additional features of the SN55116/SN75116

- Independent Driver and Receiver
- Choice of Open-Collector or Totem-Pole Outputs on Both Driver and Receiver
- Dual Data Inputs on Driver
- Optional Line-Termination Resistor in Receiver
- ±15-V Receiver Common-Mode Capability
- Receiver Frequency Response Control

additional features of the SN75117

- Driver Output Internally Connected to Receiver Input

The SN75118 is an SN75116 With 3-State Receiver Output Circuitry
The SN75119 is an SN75117 With 3-State Receiver Output Circuitry

description

These integrated circuits are designed for use in interfacing between TTL-type digital systems and differential data-transmission lines. They are especially useful for party-line (data-bus) applications. Each of these circuit types combine in one package a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver inputs and the receiver outputs are TTL compatible. The driver employed is similar to the SN55113/SN75113 3-state line driver, and the receiver is similar to the SN55115/SN75115 line receiver.

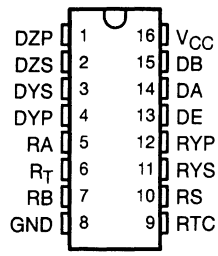
The '116 and SN75118 circuits offer all the features of the SN55113/SN75113 driver and the SN55115/SN75115 receiver combined. The driver performs the dual input AND and NAND functions when enabled or presents a high impedance to the load when in the disabled state. The driver output stages are similar to TTL totem-pole outputs, but have the current-sink portion separated from the current-sourcing portion and both are brought out to adjacent package terminals. This feature allows the user the option of using the driver in the open-collector output configuration, or, by connecting the adjacent source and sink terminals together, of using the driver in the normal totem-pole output configuration.

The receiver portion of the '116 and SN75118 features a differential input circuit having a common-mode voltage range of ±15 V. An internal 130-Ω resistor is also provided, which may optionally be used for terminating the transmission line. A frequency response control terminal allows the user to reduce the speed of the receiver or to improve differential noise immunity. The receiver of the '116 also has an output strobe and a split totem-pole output. The receiver of the SN75118 has an output-enable for the 3-state split totem-pole output. The receiver section of either circuit is independent of the driver section except for the V_{CC} and ground terminals.

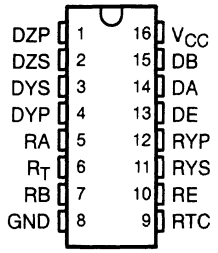
The SN75117 and SN75119 circuits provide the basic driver and receiver functions of the '116 and SN75118, but use a package that is only half as large. The SN75117 and SN75119 are intended primarily for party-line or bus-organized systems as the driver outputs are internally connected to the receiver inputs. The driver has a single data input and a single enable input, and the SN75117 receiver has an output strobe while the SN75119 receiver has a 3-state-output enable. These devices do not, however, provide output connection options, line termination resistors, or receiver frequency-response controls.

The SN55116 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN75116, SN75117, SN75118, and SN75119 are characterized for operation from 0°C to 70°C.

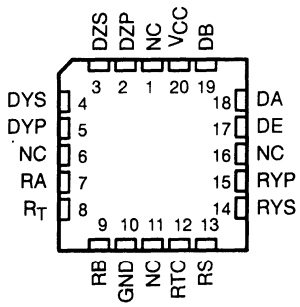
SN55116 . . . J PACKAGE
SN75116 . . . D OR N PACKAGE
(TOP VIEW)



SN75118 . . . D OR N PACKAGE
(TOP VIEW)

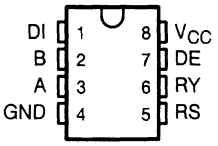


SN55116 . . . FK PACKAGE
(TOP VIEW)

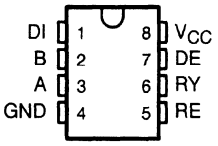


NC – No internal connection

SN75117 . . . D OR P PACKAGE
(TOP VIEW)



SN75119 . . . D OR P PACKAGE
(TOP VIEW)



Function Tables

'116, SN75118
DRIVER

INPUTS			OUTPUTS	
DE	DA	DB	DY	DZ
L	X	X	Z	Z
H	L	X	L	H
H	X	L	L	H
H	H	H	H	L

SN75117, SN75119
DRIVER

INPUTS		OUTPUTS	
DI	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

'116, SN75118
RECEIVER

RS/RE	DIFF INPUT	OUTPUTS RY	
		'116	SN75118
L	X	H	Z
H	L	H	H
H	H	L	L

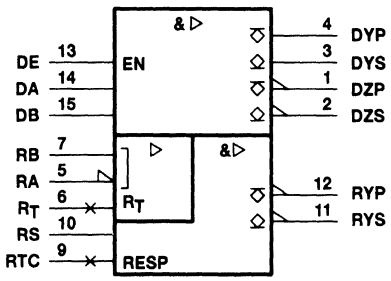
SN75117, SN75119
RECEIVER

INPUTS			OUTPUT RY	
A	B	RS/RE	SN75117	SN75119
H	L	H	H	H
L	H	H	L	L
X	X	L	H	Z

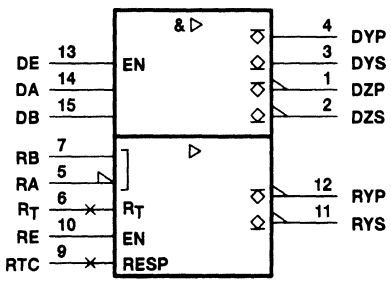
H = high level ($V_I \geq V_{IH}$ min or V_{ID} more positive than V_{TH} max)
L = low level ($V_I \leq V_{IL}$ max or V_{ID} more negative than V_{TL} max)
X = irrelevant
Z = high impedance (off)

logic symbols†

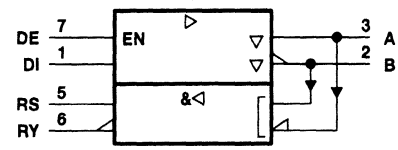
'116



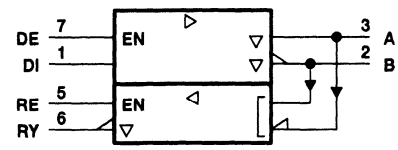
SN75118



SN75117



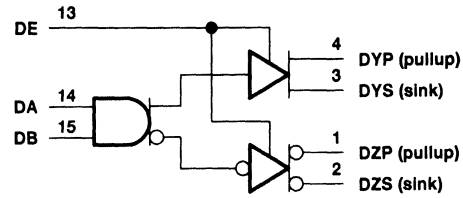
SN75119



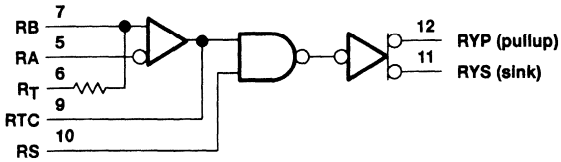
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

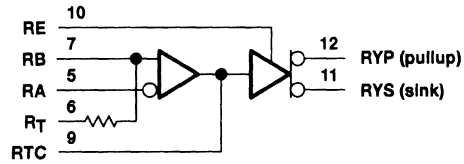
'116 and SN75118



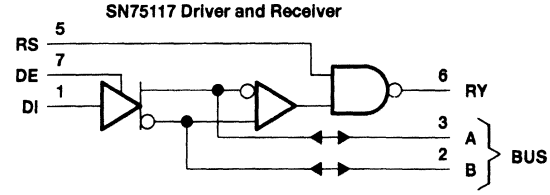
'116 Receiver



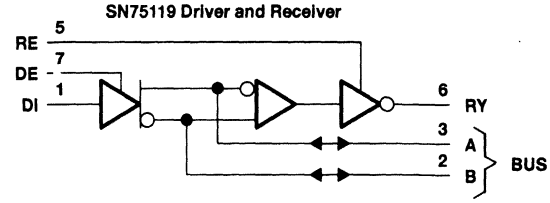
SN75118 Receiver



SN75117 Driver and Receiver



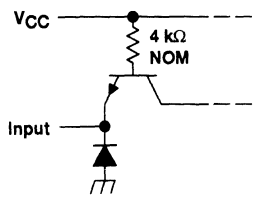
SN75119 Driver and Receiver



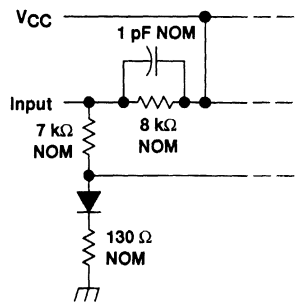
Pin numbers shown for the SN55116 are for the J package, those shown for the SN75118 are for the N package, those shown for SN75117 and SN75119 are for the P package.

schematics of inputs and outputs

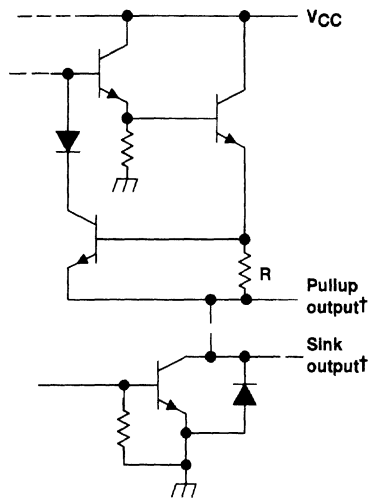
EQUIVALENT OF EACH DRIVER INPUT AND EACH RE AND RS INPUT



EQUIVALENT OF EACH RECEIVER INPUT (EXCLUDING ENABLES AND STROBES)



TYPICAL OF ALL OUTPUTS



Driver output R = 9 Ω NOM
Receiver output R = 20 Ω NOM
†On SN75117 and SN75119, common outputs replace the separate pullup and sink outputs.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

		'116, SN75118	SN75117, SN75119	UNIT
Supply voltage, V_{CC} (see Note 1)		7	7	V
Input voltage, V_I	DA, DB, DE, DI, RE, RS	5.5	5.5	V
	RA, RB, RT	±25		
	A and B		0 to 6	
Off-state voltage applied to open-collector outputs		12		V

	SN55116	SN75116 THRU SN75119	UNIT
Continuous total power dissipation (see Note 2)	See Dissipation Rating Table		
Operating free-air temperature range, T_A	−55 to 125	0 to 70	°C
Storage temperature range, T_{stg}	−65 to 50	−65 to 50	°C
Case temperature for 60 seconds, T_C: FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or P package		260	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network ground terminal.
2. In the FK and J packages, SN55116 chip is alloy mounted and SN75116 through SN75119 chips are glass mounted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D (8 pin)	725 mW	5.8 mW/°C	464 mW	—
D (16 pin)	950 mW	7.6 mW/°C	608 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—
P	1000 mW	8.0 mW/°C	640 mW	—

recommended operating conditions

PARAMETER		SN55116			SN75'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High-level input voltage, V_{IH}	All inputs except differential inputs	2			2			V
Low-level input voltage, V_{IL}				0.8			0.8	V
High-level output current, I_{OH}	Drivers			−40			−40	mA
	Receivers			−5			−5	
Low-level output current, I_{OL}	Drivers			40			40	mA
	Receivers			15			15	
Receiver input voltage, V_I	'116, '118			±15			±15	V
	'117, '119	0		6	0		6	
Common-mode receiver input voltage, V_{ICR}	'116, '118			±15			±15	V
	'117, '119	0		6	0		6	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

driver section

PARAMETER			TEST CONDITIONS†			'116, SN75118			SN75117, SN75119			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−0.9	−1.5		−0.9	−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V, I_{IH} = 2 V	T_A = 25°C (SN55116), T_A = 0°C to 70°C (SN75')	I_{OH} = −10 mA	2.4	3.4		2.4	3.4		V
					I_{OH} = −40 mA	2	3		2	3		
				T_A = −55°C to 125°C (SN55')	I_{OH} = −10 mA	2			2			
					I_{OH} = −40 mA	1.8			1.8			
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 40 mA					0.4			0.4	V
V_{OK}	Output clamp voltage		V_{CC} = MAX, I_O = −40 mA, DE at 0.8 V					−1.5			−1.5	V
$I_{O(off)}$	Off-state open-collector output current		V_{CC} = MAX, V_O = 12 V	T_A = 25°C			1	10				µA
				T_A = MAX	SN55116			200				
					SN75'			20				
I_{OZ}	Off-state (high-impedance-state) output current		V_{CC} = MAX, V_O = 0 to V_{CC}, DE at 0.8 V, T_A = 25°C					±10				µA
			V_{CC} = MAX, DE at 0.8 V, T_A = MAX	V_O = 0	SN55116			−300				
				V_O = 0.4 V to V_{CC}	SN55116			±150				
				V_O = 0 to V_{CC}	SN75'			±20				
I_I	Input current at maximum input voltage	Driver or enable input	V_{CC} = MAX, V_I = 5.5 V					1			1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.4 V					40			40	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4 V					−1.6			−1.6	mA
I_{OS}	Short-circuit output current§		V_{CC} = MAX, V_O = 0, T_A = 25°C			−40		−120	−40		−120	mA
I_{CC}	Supply current (driver and receiver combined)		V_{CC} = MAX, T_A = 25°C				42	60	42		60	mA

† All parameters with the exception of off-state open-collector output current are measured with the active pullup connected to the sink output. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

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switching characteristics, V_{CC} = 5 V, C_L = 30 pF, T_A = 25°C

driver section

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	See Figure 13			14	30	ns
t_{PHL}	Propagation delay time, high-to-low level output				12	30	
t_{PZH}	Output enable time to high level	R_L = 180 Ω,	See Figure 14		8	20	ns
t_{PZL}	Output enable time to low level	R_L = 250 Ω,	See Figure 15		17	40	ns
t_{PHZ}	Output disable time from high level	R_L = 180 Ω,	See Figure 14		16	30	ns
t_{PLZ}	Output disable time from low level	R_L = 250 Ω,	See Figure 15		20	35	ns

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

receiver section

PARAMETER			TEST CONDITIONS†			'116, SN75118 MIN	'116, SN75118 TYP‡	'116, SN75118 MAX	SN75117, SN75119 MIN	SN75117, SN75119 TYP‡	SN75117, SN75119 MAX	UNIT
V_{IT+}	Positive-going threshold voltage§		V_O = 0.4 V, See Note 3	I_{OL} = 15 mA,	V_{CC} = MIN, V_{ICR} = 0, See Note 4			0.5			0.5	V
					V_{CC} = 5 V, V_{ICR} = MAX, See Note 5			1			1	
V_{IT-}	Negative-going threshold voltage§		V_O = 2.4 V, See Note 3	I_{OL} = −5 mA,	V_{CC} = MIN, V_{ICR} = 0, See Note 4	−0.5¶			−0.5¶			V
					V_{CC} = 5 V, V_{ICR} = MAX, See Note 5	−1¶			−1¶			
V_I	Input voltage range#		V_{CC} = 5 V,	V_{ID} = −1 V or 1 V,	See Note 3	15 to −15			6 to 0			V
V_{OH}	High-level output voltage		I_{OH} = −5 mA, See Note 3	V_{CC} = MIN, V_{ICR} = 0,	V_{ID} = −0.5 V, See Notes 4 and 6	2.4			2.4			V
				V_{CC} = 5 V, V_{ICR} = MAX,	V_{ID} = −1 V, See Note 5	2.4			2.4			
V_{OL}	Low-level output voltage		I_{OL} = 15 mA, See Note 3	V_{CC} = MIN, V_{ICR} = 0,	V_{ID} = 0.5 V, See Notes 4 and 7			0.4			0.4	V
				V_{CC} = 5 V, V_{ICR} = MAX,	V_{ID} = 1 V, See Note 5			0.4			0.4	
$I_{I(rec)}$	Receiver input current		V_{CC} = MAX, See Note 3	V_I = 0,	Other input at 0 V		−0.5	−0.9		−0.5	−1	mA
				V_I = 0.4 V,	Other input at 2.4 V		−0.4	−0.7		−0.4	−0.8	
				V_I = 2.4 V,	Other input at 0.4 V		0.1	0.3		0.1	0.4	
I_I	Input current at maximum input voltage	Strobe	V_{CC} = MIN, V_{strobe} = 4.5 V	V_{ID} = −0.5 V,	'116, SN75117			5			5	µA
		Enable	V_{CC} = MAX,	V_I = 5.5 V	SN75118, SN75119			1			1	mA

† Unless otherwise noted, V_{strobe} = 2.4 V. All parameters with the exception of off-state open-collector output current are measured with the active pullup connected to the sink output. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C, and V_{IC} = 0.

§ Differential voltages are at the B input terminal with respect to the A input terminal. Neither receiver input of the SN75117 or SN75119 should be taken negative with respect to GND.

¶ The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltages only.

Input voltage range is the voltage range that, if exceeded at either input, will cause the receiver to cease functioning properly.

NOTES: 3. Measurement of these characteristics on the SN75117 and SN75119 requires the driver to be disabled with the driver enable at 0.8 V.
4. This applies with the less positive receiver input grounded.
5. For '116 and SN75118, this applies with the more positive receiver input at 15 V or the more negative receiver input at – 15 V. For SN75117 and SN75119, this applies with the more positive receiver input at 6 V.
6. For SN55116, V_{ID} = −1 V
7. For SN55116, V_{ID} = 1 V

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

receiver section (continued)

PARAMETER			TEST CONDITIONS†			'116, SN75118			SN75117, SN75119			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
I_{IH}	High-level input current	Enable	V_{CC} = MAX,	V_I = 2.4 V	SN75118, SN75119			40			40	μA
I_I	Low-level input current	Strobe	V_{CC} = MAX, V_{strobe} = 0.4 V,	V_{ID} = 0.5 V, See Notes 4 and 7	'116, SN75117			−2.4			−2.4	mA
		Enable	V_{CC} = MAX,	V_I = 0.4 V	SN75118, SN75119			−1.6			−1.6	
$I_{(RTC)}$	Response-time-control current (RTC)		V_{CC} = MAX, RC at 0 V,	V_{ID} = 0.5 V, See Notes 4 and 7	T_A = 25°C	−1.2						mA
$I_{O(off)}$	Off-state open-collector output current		V_{CC} = MAX, V_O = 12 V, V_{ID} = −1 V	T_A = 25°C			1	10				μA
				T_A = MAX	SN55116			200				
					SN75_			20				
I_{OZ}	Off-state (high-impedance-state) output current		V_{CC} = MAX, V_O = 0 to V_{CC}, RE at 0.4 V	T_A = 25°C	SN75118, SN75119			±10			±10	μA
				T_A = MAX	SN75118			±20				
					SN75119						±20	
R_T	Line-terminating resistance		V_{CC} = 5 V		T_A = 25°C	77		167				Ω
I_{OS}	Short-circuit output current§		V_{CC} = MAX, V_{ID} = −0.5 V,	V_O = 0, See Notes 4 and 6	T_A = 25°C	−15		−80	−15		−80	mA
I_{CC}	Short current (driver and receiver combined)		V_{CC} = MAX, See Notes 4 and 7	V_{ID} = 0.5 V,	T_A = 25°C		42	60		42	60	mA

† Unless otherwise noted V_{strobe} = 2.4 V. All parameters with the exception of off-state open-collector output current are measured with the active pullup connected to the sink output. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C, and V_{IC} = 0.

§ Not more than one output should be shorted at a time.

NOTES: 4. This applies with the less positive receiver input grounded.
6. For SN55116, V_{ID} = −1 V
7. For SN55116, V_{ID} = 1 V

switching characteristics, V_{CC} = 5 V, C_L = 30 pF, T_A = 25°C

receiver section

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		R_L = 400 Ω,	See Figure 16		20	75	ns
t_{PHL}	Propagation delay time, high-to-low-level output					17	75	ns
t_{PZH}	Output enable time to high level	SN75118 and SN75119 only	R_L = 480 Ω,	See Figure 14		9	20	ns
t_{PZL}	Output enable time to low level		R_L = 250 Ω,	See Figure 15		16	35	ns
t_{PHZ}	Output disable time from high level		R_L = 480 Ω,	See Figure 14		12	30	ns
t_{PLZ}	Output disable time from low level		R_L = 250 Ω,	See Figure 15		17	35	ns

TYPICAL CHARACTERISTICS

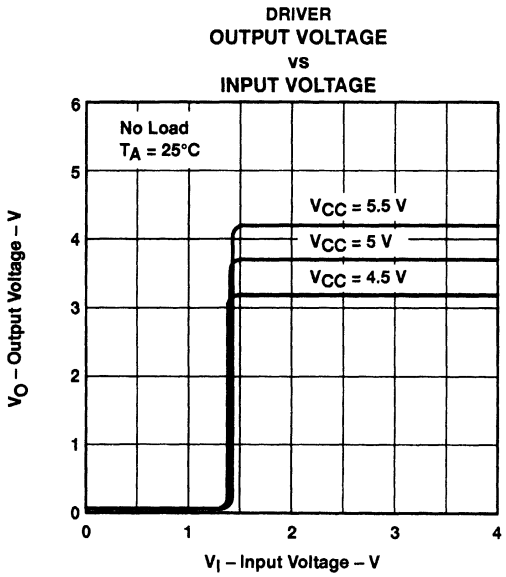
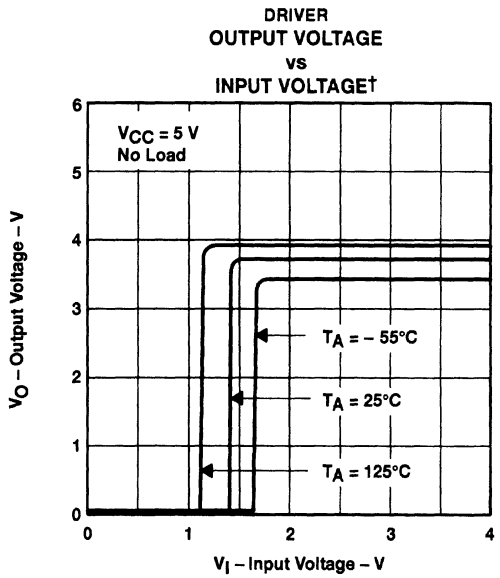


Figure 1



† Data for temperatures below 0°C and above 70°C are only applicable to SN55116.

Figure 2

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

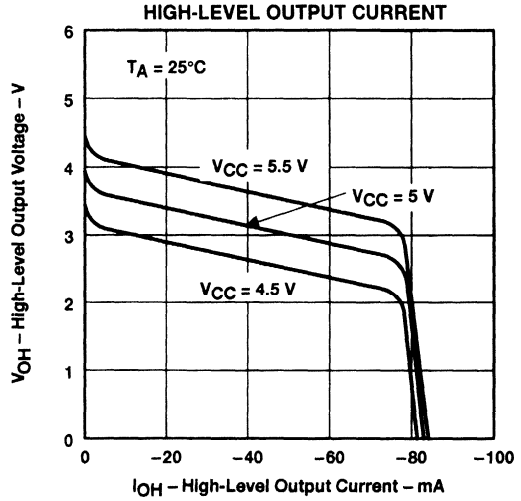


Figure 3

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

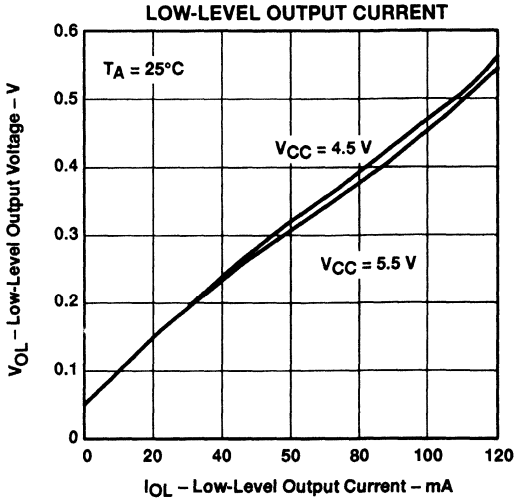


Figure 4

DRIVER
PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE†

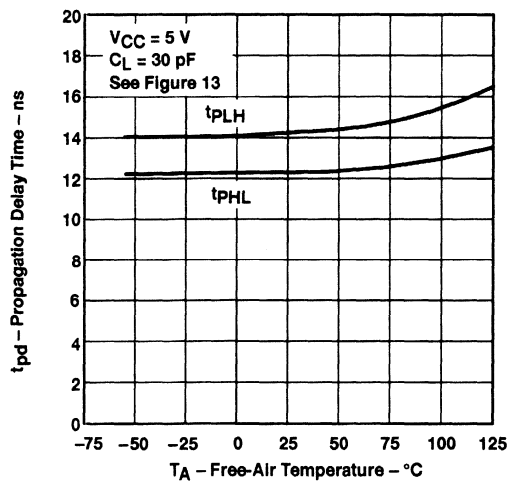


Figure 5

DRIVER
OUTPUT ENABLE AND DISABLE TIME
vs
FREE-AIR TEMPERATURE†

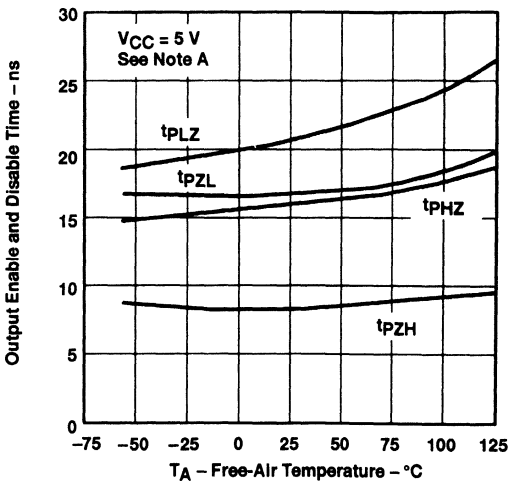


Figure 6

† Data for temperatures below 0°C and above 70°C are only applicable to SN55116.
NOTE A: For t_{PZH} and t_{PHZ}: R_L = 180 Ω, see Figure 14. For t_{PZL} and t_{PLZ}: R_L = 250 Ω, see Figure 15.

TYPICAL CHARACTERISTICS

RECEIVER
OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

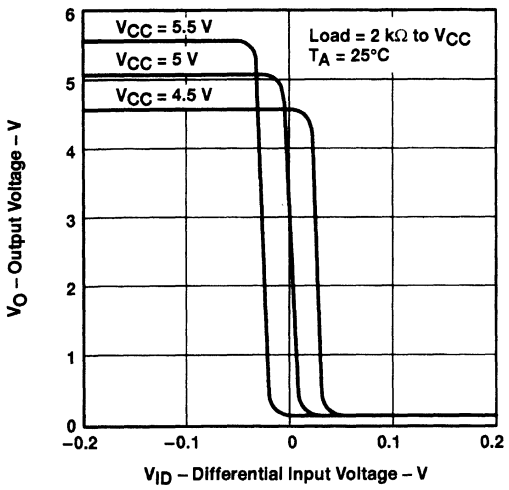


Figure 7

RECEIVER
OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE†

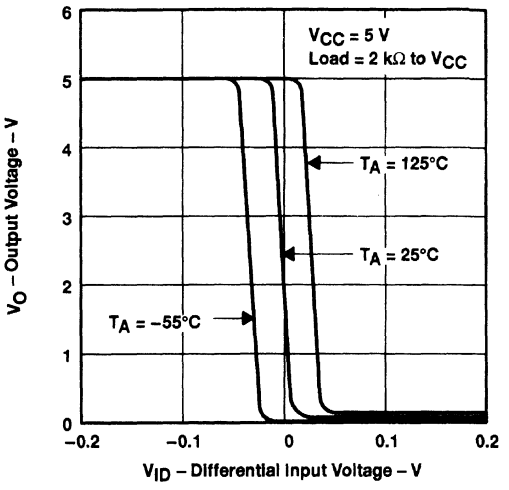


Figure 8

RECEIVER
PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE†

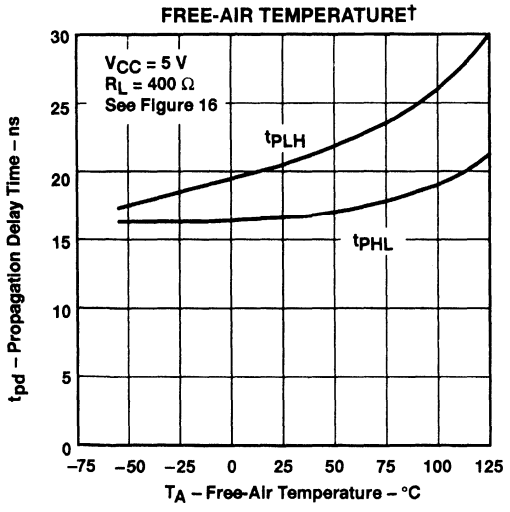


Figure 9

RECEIVER
OUTPUT ENABLE AND DISABLE TIME
vs
FREE-AIR TEMPERATURE†

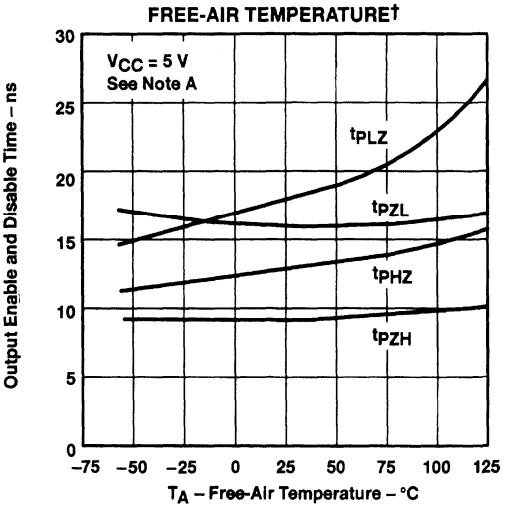


Figure 10

† Data for temperatures below 0°C and above 70°C are only applicable to SN55116.
NOTE A: For t_{PZH} and t_{PHZ} :R_L= 480 Ω, see Figure 14. For t_{PZL} and t_{PLZ}: R_L = 250 Ω, see Figure 15.

TYPICAL CHARACTERISTICS

DRIVER AND RECEIVER
SUPPLY CURRENT
vs
SUPPLY VOLTAGE

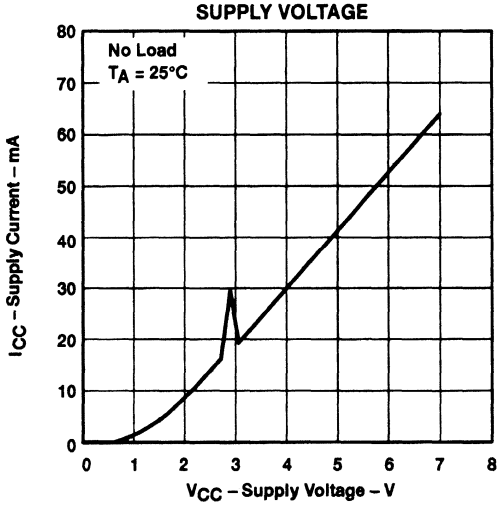
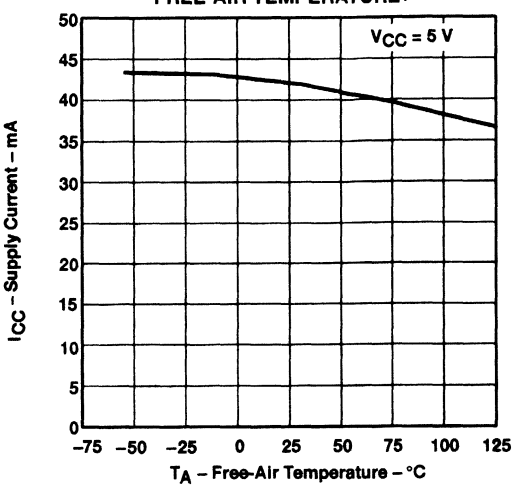


Figure 11

DRIVER AND RECEIVER
SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE†



† Data for temperatures below 0°C and above 70°C are only applicable to SN55116.

Figure 12

PARAMETER MEASUREMENT INFORMATION

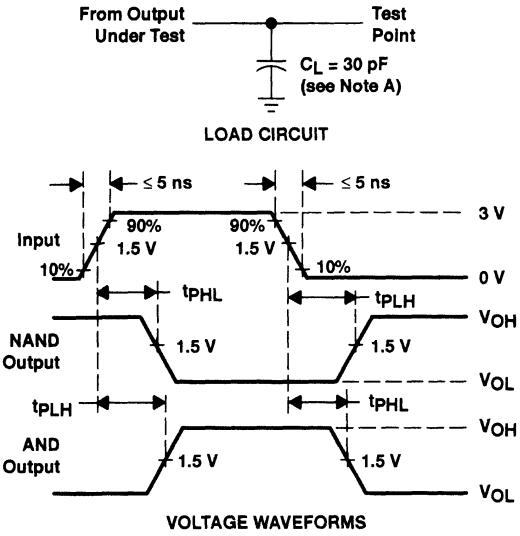


Figure 13. t_{PLH} and t_{PHL} (drivers only)

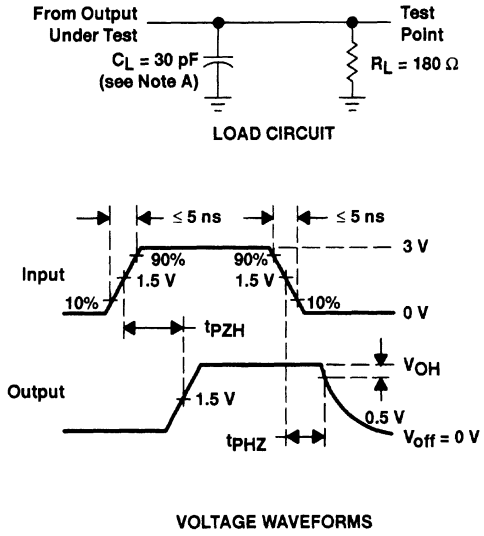


Figure 14. t_{PZH} and t_{PHZ}

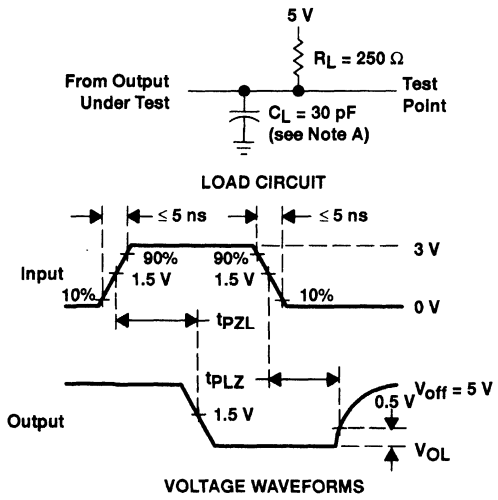


Figure 15. t_{PZL} and t_{PLZ} ('118 and '119 receivers only)

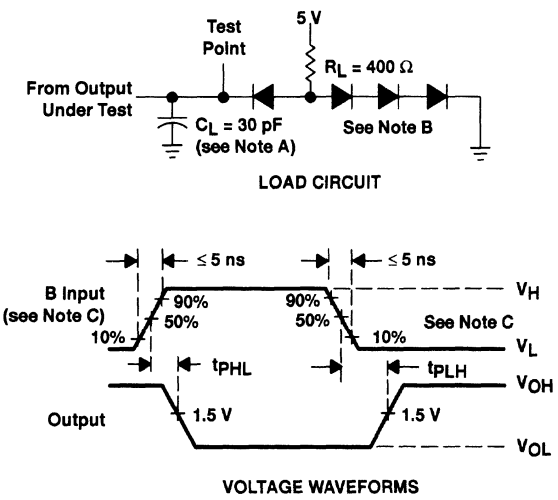


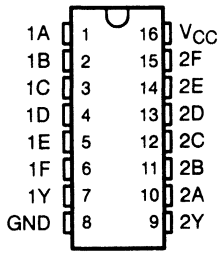
Figure 16. t_{PLH} and t_{PHL} (receivers only)

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. For '116 and SN75118, V_H = 3 V, V_L = – 3 V, the A input is at 0 V.
For SN75117 and SN75119, V_H = 3 V, V_L = 0, the A input is at 1.5 V.
D. When testing the '116 and SN75118 receiver sections, the response-time control and the termination resistor pins are left open.

SLLS086B – SEPTEMBER 1973 – REVISED MAY 1995

- **Meet or Exceed the Requirements of IBM™ System 360 Input/Output Interface Specification**
- **Operate From Single 5-V Supply**
- **TTL Compatible**
- **3.11-V Output at I_{OH} = –59.3 mA**
- **Uncommitted Emitter-Follower Output Structure for Party-Line Operation**
- **Short-Circuit Protection**
- **AND-OR Logic Configuration**
- **Designed for Use With Triple Line Receiver SN75124**
- **Designed to Be Interchangeable With Signetics N8T13 and N8T23**

D OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS						OUTPUT
A	B	C	D	E	F	Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All other input combinations						L

H = high level, L = low level, X = irrelevant

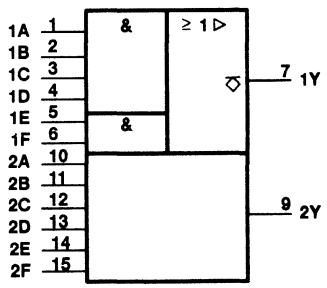
description

The N8T13, N8T23, and SN75123 are dual line drivers specifically designed to meet the input/output interface specifications for IBM System 360. It is also compatible with standard-TTL logic and supply-voltage levels.

The N8T13, N8T23, and SN75123 low-impedance emitter-follower outputs drive terminated lines such as coaxial cable or twisted pair. Having the outputs uncommitted allows wired-OR logic to be performed in party-line applications. Output short-circuit protection is provided by an internal clamping network that turns on when the output voltage drops below approximately 1.5 V. All the inputs are in conventional TTL configuration, and the gating can be used during power-up and power-down sequences to ensure that no noise is introduced to the line.

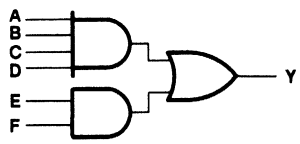
The N8T13, N8T23, and SN75123 are characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



THE SN751730 IS RECOMMENDED FOR NEW IBM 360/370 INTERFACE DESIGNS.

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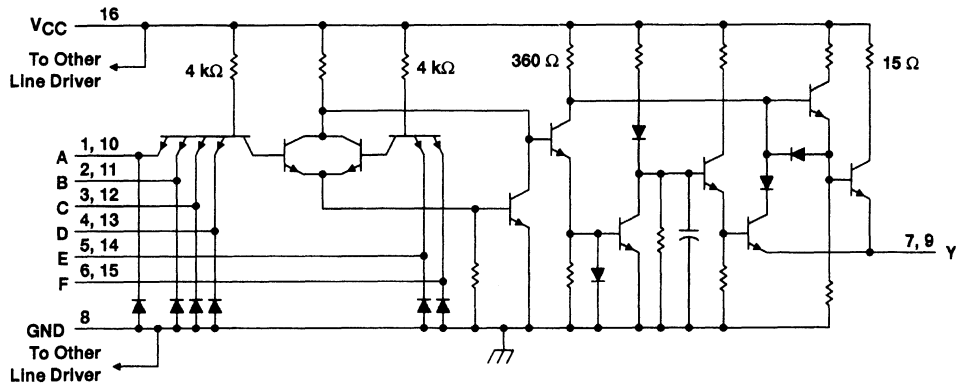
schematic (each driver)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 5.5 V
Output voltage, V_O ..... 7 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): D package .... 950 mW
N package ... 1150 mW
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the D package to 608 mW at 70°C at the rate of 7.6 mW/°C and the N package to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−100	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics, V_{CC} = 4.75 V to 5.25 V, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 5 V,	I_I = −12 mA			−1.5	V
$V_{I(BR)}$	Input breakdown voltage	V_{CC} = 5 V,	I_I = 10 mA		5.5		V
V_{OH}	High-level output voltage	V_{CC} = 5 V, I_{OH} = −59.3 mA,	V_{IH} = 2 V, See Note 3	T_A = 25°C	3.11		V
				T_A = 0°C to 70°C	2.9		
V_{OL}	Low-level output voltage	V_{IL} = 0.8 V,	I_{OL} = −240 μA,	See Note 3		0.15	V
I_{OH}	High-level output current	V_{CC} = 5 V, T_A = 25°C,	V_{IH} = 4.5 V, See Note 3	V_{OH} = 2 V,	−100	−250	mA
$I_{O(off)}$	Off-state output current	V_{CC} = 0,	V_O = 3 V			40	μA
I_{IH}	High-level input current	V_I = 4.5 V				40	μA
I_{IL}	Low-level input current	V_I = 0.4 V			−0.1	−1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = 5 V,	T_A = 25°C			−30	mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V,	All inputs at 2 V,	Outputs open		28	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V,	All inputs at 0.8 V,	Outputs open		60	mA

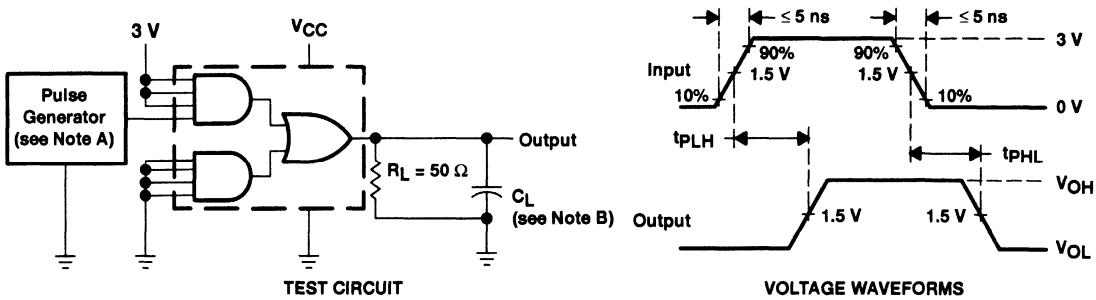
† Not more than one output should be shorted at a time.

NOTE 3: The output voltage and current limits are valid for any appropriate combination of high and low inputs specified by the function table for the desired output.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 50 Ω,	C_L = 15 pF,	See Figure 1		12	20	ns
t_{PHL}	Propagation delay time, high- to low-level output					12	20	
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 50 Ω,	C_L = 100 pF,	See Figure 1		20	35	ns
t_{PHL}	Propagation delay time, high- to low-level output					15	25	

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω; t_W = 200 ns, duty cycle = 50%.
B. C_L Includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

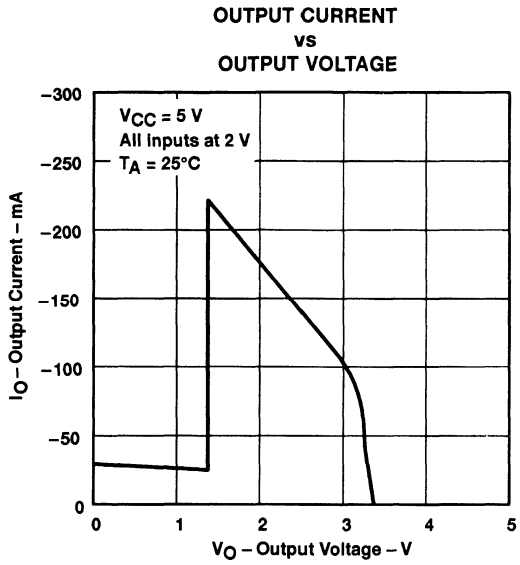


Figure 2

APPLICATION INFORMATION

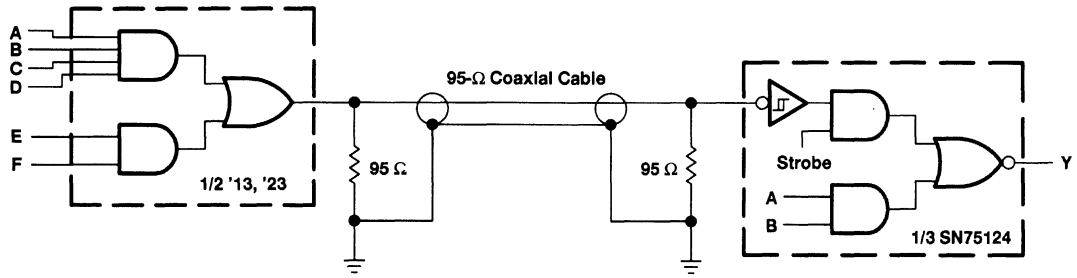


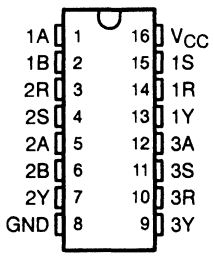
Figure 3. Unbalanced Line Communication Using '13, '23, and '124

SN75124
TRIPLE LINE RECEIVER

SLLS058B – SEPTEMBER 1973 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of IBM™ System 360 Input/Output Interface Specification**
- **Operates From Single 5-V Supply**
- **TTL Compatible**
- **Built-In Input Threshold Hysteresis**
- **High Speed . . . Typical Propagation Delay Time = 20 ns**
- **Independent Channel Strobes**
- **Input Gating Increases Application Flexibility**
- **Designed for Use With Dual Line Driver SN75123**
- **Designed to Be Interchangeable With Signetics N8T24**

D OR N PACKAGE
(TOP VIEW)



description

The SN75124 triple line receiver is specifically designed to meet the input/output interface specifications for IBM System 360. It is also compatible with standard TTL logic and supply voltage levels.

The SN75124 has receiver inputs with built-in hysteresis to provide increased noise margin for single-ended systems. An open line affects the receiver input as does a low-level input voltage, and the receiver input can withstand a level of −0.15 V with power on or off. The other inputs are in TTL configuration. The S input must be high to enable the receiver input. Two of the line receivers have A and B inputs that, if both are high, hold the output low. The third receiver has only an A input that, if high, holds the output low.

See the SN751730 for new IBM 360/370 interface designs.

The SN75124 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS				OUTPUT
A	B†	R	S	Y
H	H	X	X	L
X	X	L	H	L
L	X	H	X	H
L	X	X	L	H
X	L	H	X	H
X	L	X	L	H

† B input and last two lines of the function table are applicable to receivers 1 and 2 only

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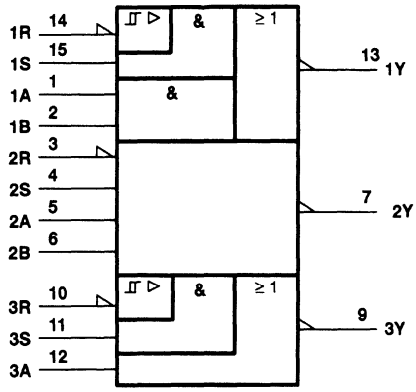
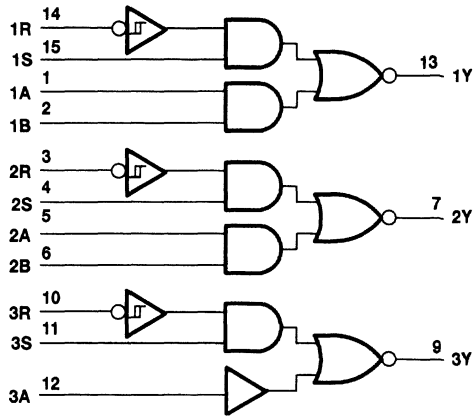
logic symbol†

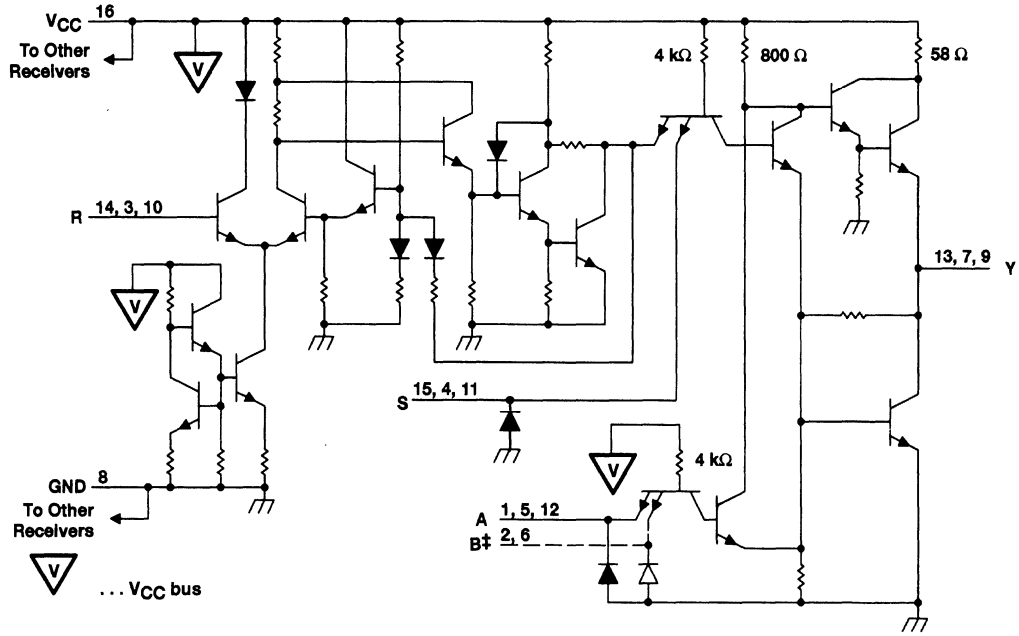


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematic (each receiver)



‡ B input is provided on receivers 1 and 2 only
Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I: R input with V_{CC} applied ..... 7 V
R input with V_{CC} not applied ..... 6 V
A, B, or S input ..... 5.5 V
Output voltage, V_O ..... 7 V
Output current, I_O ..... ±100 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to network ground terminal

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	A, B, or S	2			V
	R	1.7			
Low-level input voltage, V_{IL}	A, B, or S			0.8	V
	R			0.7	
High-level output current, I_{OH}				−800	μA
Low-level output current, I_{OL}				16	mA
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)	R	V_{CC} = 5 V,	T_A = 25°C	0.2	0.5		V
V_{IK}	Input clamp voltage	A, B, or S	V_{CC} = 5 V,	I_I = −12 mA			−1.5	V
$V_{I(BR)}$	Input breakdown voltage	A, B, or S	V_{CC} = 5 V,	I_I = 10 mA	5.5			V
V_{OH}	High-level output voltage		$V_{IH} = V_{IH}$min, I_{OH} = −800 μA,	$V_{IL} = V_{IL}$max, See Note 2	2.6			V
V_{OL}	Low-level output voltage		$V_{IH} = V_{IH}$min, I_{OL} = 16 mA,	$V_{IL} = V_{IL}$max, See Note 2			0.4	V
I_I	Input current at maximum input voltage	R	V_I = 7 V				5	mA
			V_I = 6 V,	V_{CC} = 0			5	
I_{IH}	High-level input current	A, B, or S	V_I = 4.5 V				40	μA
		R	V_I = 3.11 V				170	
I_{IL}	Low-level input current	A, B, or S	V_I = 0.4 V,	V_{IR} = 0.8 V	−0.1		−1.6	mA
I_{OS}	Short-circuit output current†				−50		−100	mA
I_{CC}	Supply current		All inputs = 0.8 V				72	mA
			All inputs = 2 V				100	

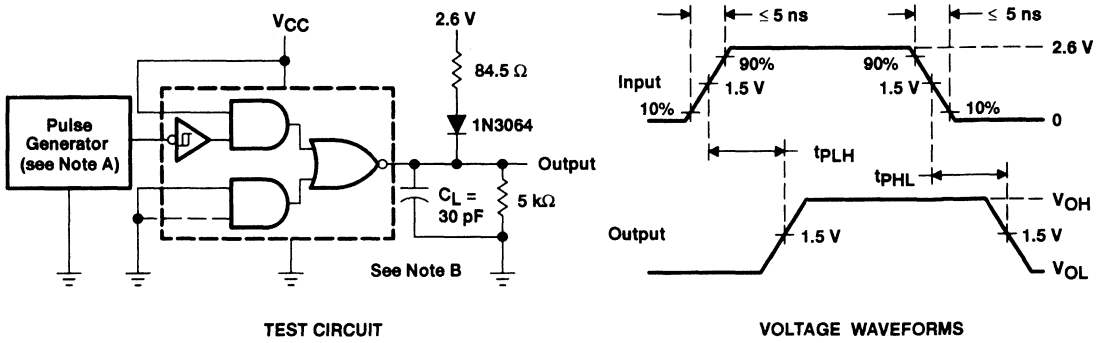
† Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

NOTE 2: The output voltage and current limits are characterized for any appropriate combination of high and low inputs specified by the function table for the desired output.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from R input	See Figure 1		20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from R input			20	30	

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $Z_O \approx 50\ \Omega$, PRR ≤ 5 MHz, duty cycle = 50%.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

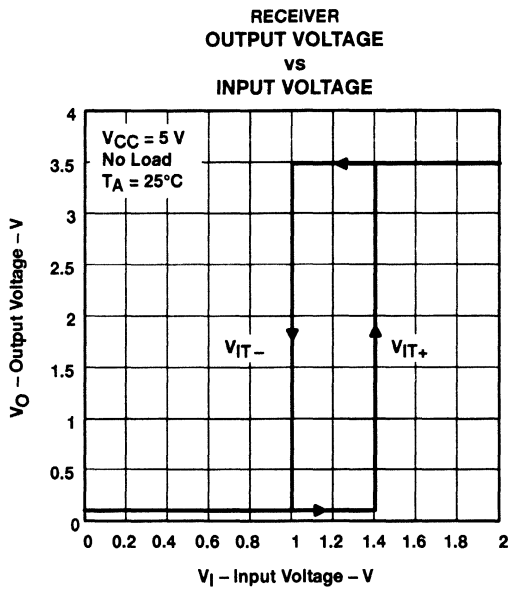


Figure 2

APPLICATION INFORMATION

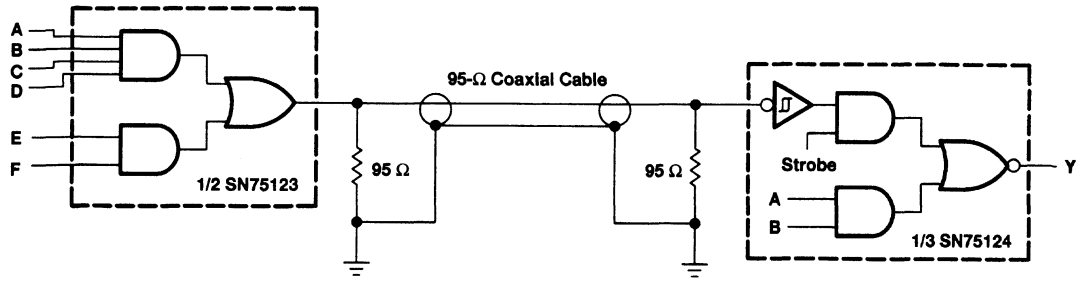
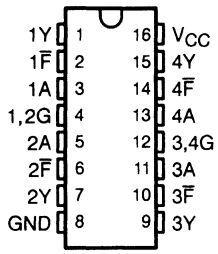


Figure 3. Unbalanced Line Communication Using SN75123 and SN75124

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

- **Meets or Exceeds the Requirements of IBM™ System 360/370 Input/Output Interface Specification GA22-6974-3**
- **Minimum Output Voltage of 3.11 V at I_{OH} = −59.3 mA**
- **Fault-Flag Circuit Output Signals Driver Output Fault**
- **Fault-Detection Current-Limit Circuit Minimizes Power Dissipation During a Fault Condition**
- **Dual Common Enable**
- **Individual Fault Flags**
- **Designed to Replace the MC3481**

D OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE

INPUTS		OUTPUTS	
G	A	Y	F̄
L	X	L	H
H	H	H	H
H	H	S	L

H = high level,
L = low level,
X = irrelevant,
S = shorted to ground

description

The SN75126 quadruple line driver is designed to meet the IBM 360/370 I/O specification A22-6974-3. The output voltage is 3.11 V minimum (at I_{OH} = −59.3 mA) over the recommended ranges of supply voltage (4.5 V to 5.95 V) and temperature. Driver outputs use a fault-detection current-limit circuit to allow high drive current but still minimize power dissipation when the output is shorted to ground. The SN75126 is compatible with standard TTL logic and supply voltages.

Fault-flag circuitry is designed to sense and signal a line short on any Y line. Upon detecting an output fault condition, the fault-flag circuit forces the driver output into a low state and signals a fault condition by causing the fault-flag output to go low.

The SN75126 can drive a 50-Ω load or a 90-Ω load as used in many I/O systems. Optimum performance can be achieved when the device is used with either the SN75128 or SN75129 line receivers. Also, see the SN751730 for new 360/370 interface designs.

The SN75126 is characterized for operation from 0°C to 70°C.

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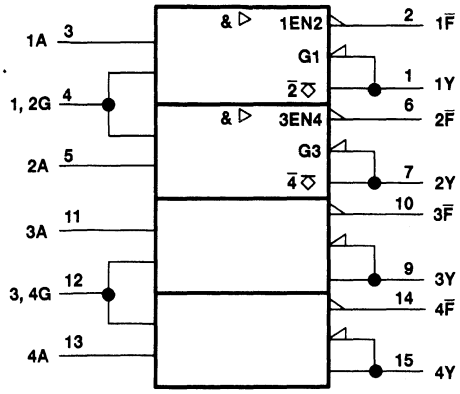
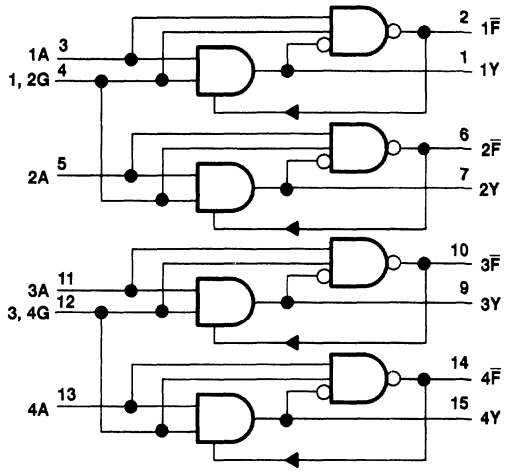
logic symbol†

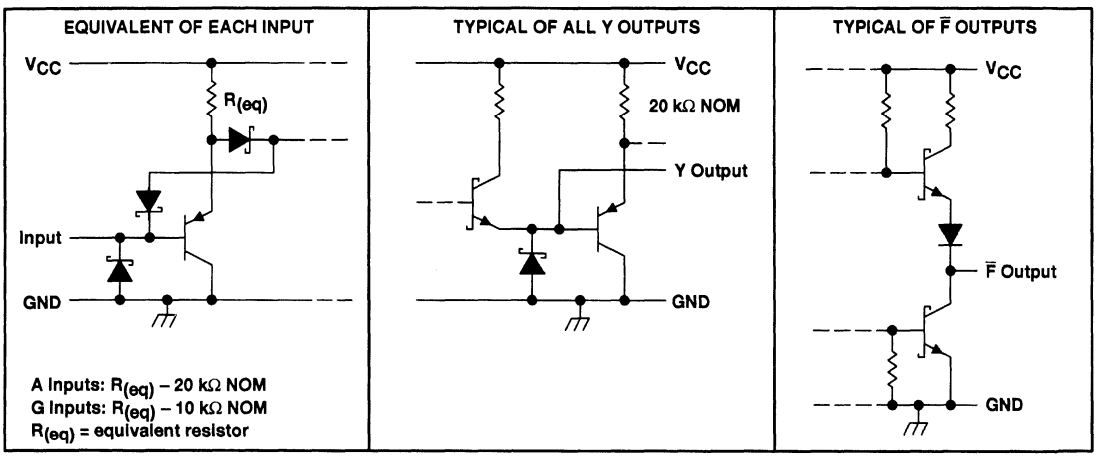


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} ..... 7 V
Input voltage, V_I ..... 7 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.95	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−59.3	mA
Operating free-air temperature, T_A	0		70	°C

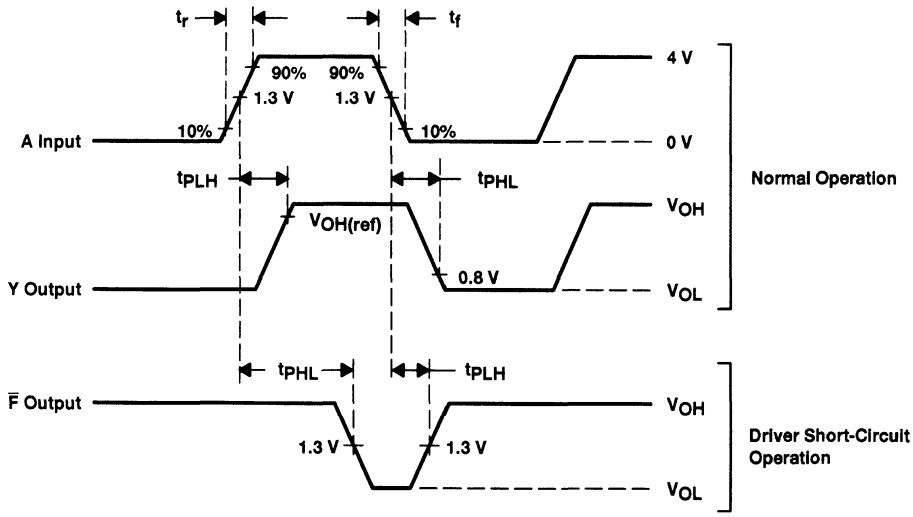
electrical characteristics over recommended operating free-air temperature range

PARAMETER			TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}	Input clamp voltage	A,G	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5	V
V_{OH}	High-level output voltage	Y	V_{CC} = 4.5 V,	I_{OH} = −59.3 mA,	V_{IH} = 2 V	3.11		V
		Y	V_{CC} = 5.25 V,	I_{OH} = −41 mA,	V_{IH} = 2 V	3.9		
		$\overline{F}$	V_{CC} = 4.5 V,	I_{OH} = −400 μA,	V_{IH} = 2 V	2.5		
V_{OL}	Low-level output voltage	Y	V_{CC} = 5.5 V,	I_{OL} = −240 μA,	V_{IL} = 0.8 V		0.15	V
		Y	V_{CC} = 5.95 V,	I_{OL} = −1 mA,	V_{IL} = 0.8 V		0.15	
		$\overline{F}$	V_{CC} = 4.5 V, V_{IH} = 2 V	I_{OL} = 8 mA,	Y at 0 V,		0.5	
$I_{O(off)}$	Off-state output current	Y	V_{CC} = 4.5 V,	V_I = 0,	V_O = 3.11 V		100	μA
		Y	V_{CC} = 0,	V_I = 0,	V_O = 3.11 V		200	
I_I	Input current	A	V_{CC} = 4.5 V,	V_I = 5.5 V			100	μA
		G					200	
I_{IH}	High-level input current	A	V_{CC} = 4.5 V,	V_I = 2.7 V			20	μA
		G					40	
I_{IL}	Low-level input current	A	V_{CC} = 5.95 V,	V_I = 0.4 V			−250	μA
		G					−500	
I_{OS}	Short-circuit output current	Y	V_{CC} = 5.5 V,	V_O = 0,	V_{IH} = 2.7 V		−5	mA
		$\overline{F}$	V_{CC} = 5.5 V,	V_O = 0		−15	−100	
		Y	V_{CC} = 5.95 V,	V_O = 0,	V_{IH} = 2.7 V		−5	
		$\overline{F}$	V_{CC} = 5.95 V,	V_O = 0		−15	−110	
I_{CCH}	Supply current, all outputs high		V_{CC} = 5.5 V,	No load,	V_{IH} = 2 V		70	mA
			V_{CC} = 5.95 V,	No load,	V_{IH} = 2 V		80	
I_{CCL}	Supply current, Y outputs low		V_{CC} = 5.5 V,	No load,	V_{IL} = 0.8 V		55	mA
			V_{CC} = 5.95 V,	No load,	V_{IL} = 0.8 V		70	

switching characteristics at T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	A	Y	V_{CC} = 4.5 V to 5.5 V, R_L = 50 Ω, C_L = 50 pF, $V_{OH(ref)}$ = 3.11 V, See Figures 1 and 2		40	ns
t_{PHL}	Propagation delay time, high- to low-level output					37	ns
$\frac{t_{PLH}}{t_{PHL}}$	Ratio of propagation delay times				0.3	3	
t_{PLH}	Propagation delay time, low- to high-level output	A	Y	V_{CC} = 5.25 V to 5.95 V, R_L = 90 Ω, C_L = 50 pF, $V_{OH(ref)}$ = 3.9 V, See Figures 1 and 2		45	ns
t_{PHL}	Propagation delay time, high- to low-level output					45	ns
t_{PLH}	Propagation delay time, low- to high-level output	A	$\overline{F}$	V_{CC} = 5 V, C_L = 15 pF, R_L = 2 kΩ, See Figures 1 and 2		60	ns
t_{PHL}	Propagation delay time, high- to low-level output					100	ns

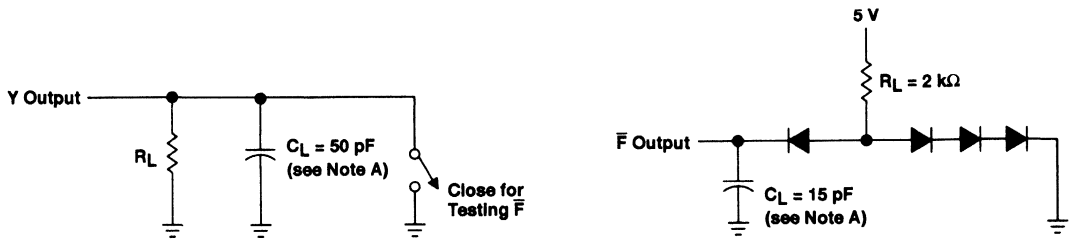
PARAMETER MEASUREMENT INFORMATION



NOTE: The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O ≈ 50 Ω.

Figure 1. Input and Output Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



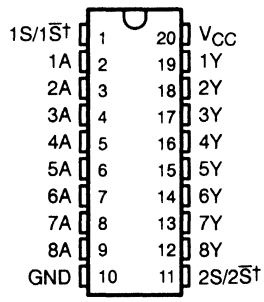
NOTE A: C_L includes probe and stray capacitance.

Figure 2. Switching Characteristics Load Circuits

SLLS076B – JANUARY 1977 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of IBM™ System 360/370 Input/Output Specification**
- **Input Resistance . . . 7 kΩ to 20 kΩ**
- **Output Compatible With TTL**
- **Schottky-Clamped Transistors**
- **Operates From a Single 5-V Supply**
- **High Speed . . . Low Propagation Delay**
- **Ratio Specification . . . t_{PLH} /t_{PHL}**
- **Common Strobe for Each Group of Four Receivers**
- **SN75128 . . . Active-High Strobes**
  SN75129 . . . Active-Low Strobes

N PACKAGE
(TOP VIEW)



† S and S̄ for SN75128 and SN75129, respectively

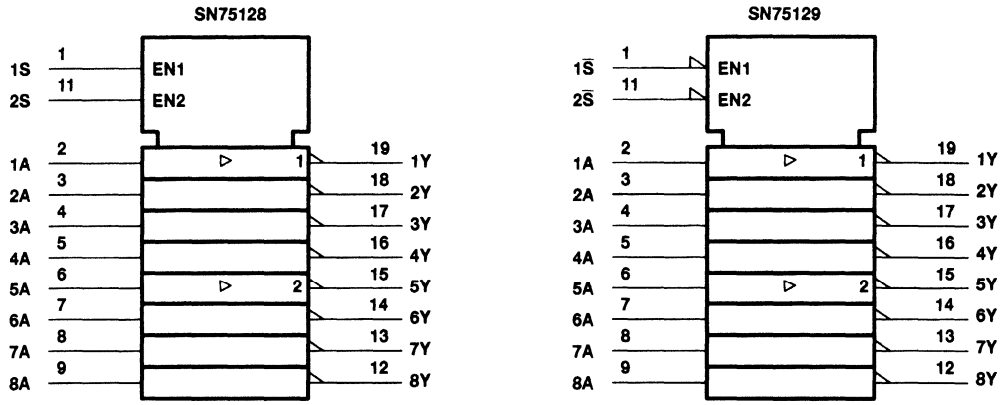
description

The SN75128 and SN75129 are eight-channel line receivers designed to satisfy the requirements of the input-output interface specification for IBM 360/370. Both devices feature common strobes for each group of four devices. The SN75128 has active-high strobes; the SN75129 has active-low strobes. Special low-power design and Schottky-diode-clamped transistors allow low supply-current requirements while maintaining fast switching speeds and high-current TTL outputs.

For new IBM 360/370 interface designs, see the SN751730.

The SN75128 and SN75129 are characterized for operation from 0°C to 70°C.

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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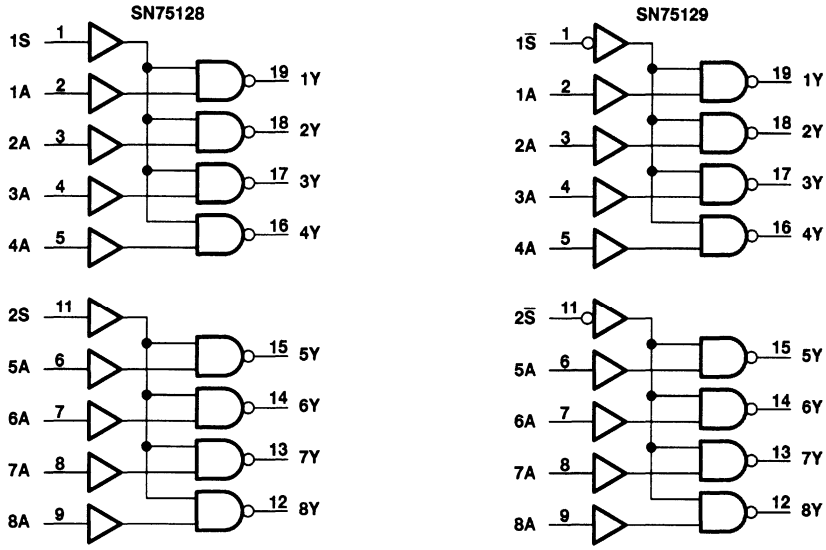
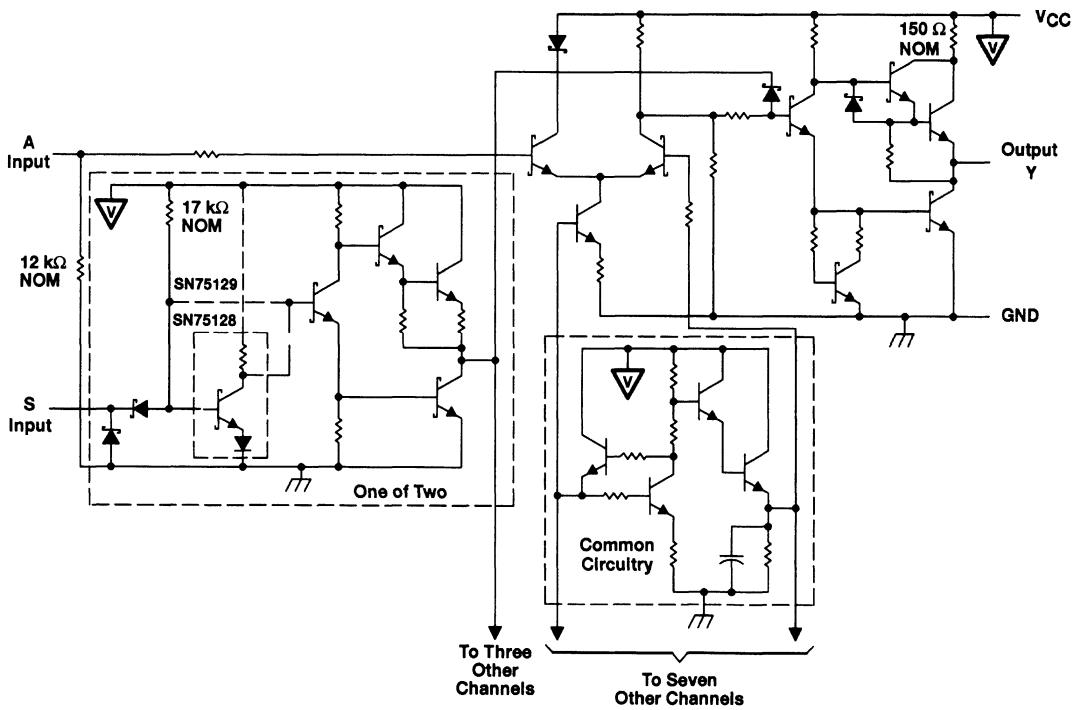
logic diagrams (positive logic)



schematic (each driver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage range, V_I (A) ..... −0.15 V to 7 V
Input voltage, V_I (S) ..... 7 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level input voltage, V_{IH}	A	1.7			V
	S	2			
Low-level input voltage, V_{IL}	A			0.7	V
	S			0.7	
High-level output current, I_{OH}				−0.4	mA
Low-level output current, I_{OL}				16	mA
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

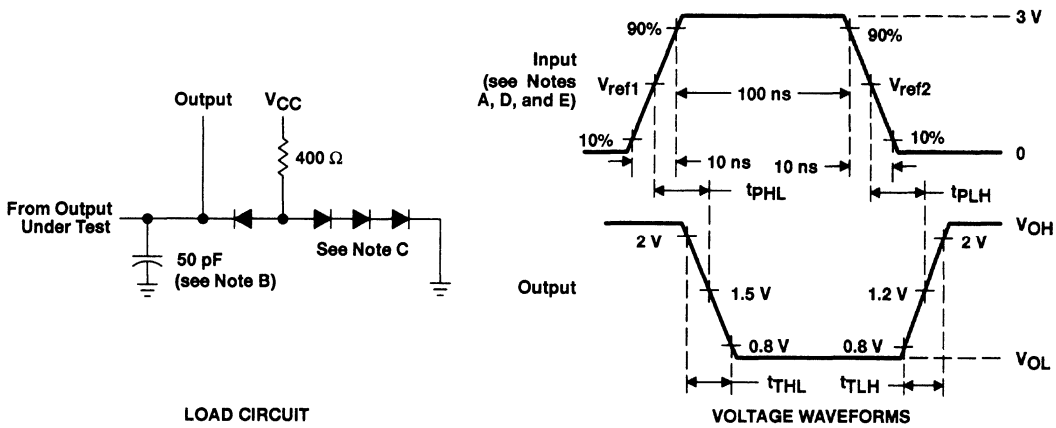
PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = 4.5 V,	V_{IL} = 0.7 V,	I_{OH} = −0.4 mA	2.4	3.1		V
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V,	V_{IH} = 1.7 V,	I_{OL} = 16 mA		0.4	0.5	V
V_{IK}	Input clamp voltage	S	V_{CC} = 4.5 V,	I_I = −18 mA				−1.5	V
I_{IH}	High-level input current	A	V_{CC} = 5.5 V,	V_I = 3.11 V			0.3	0.42	mA
		S	V_{CC} = 5.5 V,	V_I = 2.7 V				20	μA
I_{IL}	Low-level input current	A	V_{CC} = 5.5 V,	V_I = 0.15 V				30	μA
		S	V_{CC} = 5.5 V,	V_I = 0.4 V				−0.4	mA
I_{OS}	Short-circuit output current‡		V_{CC} = 5.5 V,	V_O = 0		−18		−60	mA
r_I	Input resistance		V_{CC} = 4.5 V,	0 V or open,	ΔV_I = 0.15 V to 4.15 V	7		20	kΩ
I_{CC}	Supply current	SN75128	V_{CC} = 5.5 V,	Strobe at 2.4 V,	All A inputs at 0.7 V		19	31	mA
		SN75129	V_{CC} = 5.5 V,	Strobe at 0.4 V,	All A inputs at 0.7 V		19	31	
		SN75128	V_{CC} = 5.5 V,	Strobe at 2.4 V,	All A inputs at 4 V		32	53	
		SN75129	V_{CC} = 5.5 V,	Strobe at 0.4 V,	All A inputs at 4 V		32	53	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM	TEST CONDITIONS	SN75128			SN75129			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	A	R_L = 400 Ω, C_L = 50 pF, See Figure 1	7	14	25	7	14	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			10	18	30	10	18	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output	S			26	40		20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output				22	35		16	30	ns
$\frac{t_{PLH}}{t_{PHL}}$	Ratio of propagation delay times	A		0.5	0.8	1.3	0.5	0.8	1.3	
t_{TLH}	Transition time, low-to-high-level output			1	7	12	1	7	12	ns
t_{THL}	Transition time, high-to-low-level output			1	3	12	1	3	12	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Input pulses are supplied by a generator having the following characteristics: Z_O = 50 Ω, PRR ≤ 5 MHz.
B. Includes probe and jig capacitance
C. All diodes are 1N3064 or equivalent.
D. The strobe inputs of SN75129 are in phase with the output.
E. V_{ref1} = 0.7 V and V_{ref2} = 1.7 V for testing data (A) inputs, V_{ref1} = V_{ref2} = 1.3 V for strobe inputs.

Figure 1. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

VOLTAGE TRANSFER CHARACTERISTICS

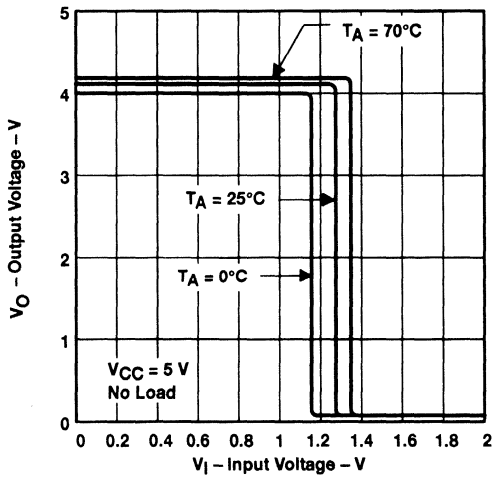


Figure 2

VOLTAGE TRANSFER CHARACTERISTICS
FROM A INPUTS

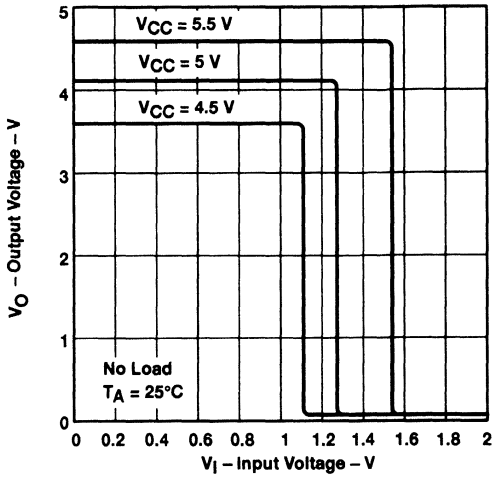


Figure 3

INPUT CURRENT
vs
INPUT VOLTAGE

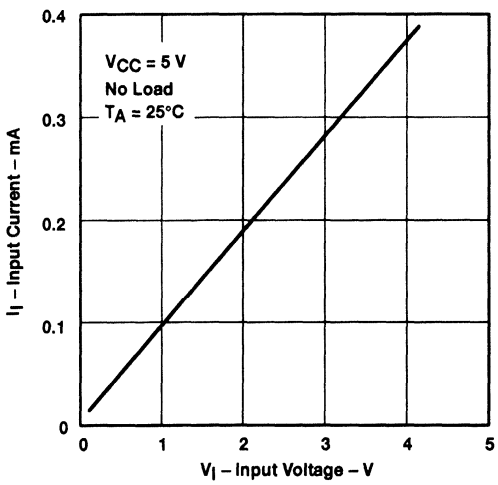


Figure 4

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

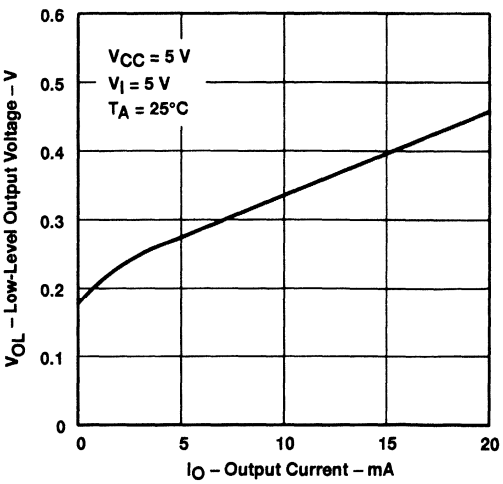
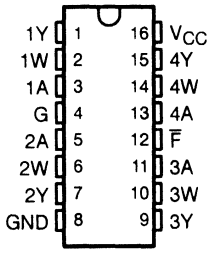


Figure 5

SLLS077B – FEBRUARY 1990 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of IBM 360/370 Input/Output Interface Specification GA22-6974-3**
- **Minimum Output Voltage of 3.11 V at I_{OH} = −59.3 mA**
- **Fault-Flag Circuit Output Signals Driver Output Fault**
- **Fault-Detection Current-Limit Circuit Minimizes Power Dissipation During a Fault Condition**
- **Common Enable and Common Fault Flag**
- **Designed to Be an Improved Replacement for the MC3485**

D OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE, EACH DRIVER

INPUTS		OUTPUTS		
G†	A	Y	F̄	W
L	X	L	H	H
X	L	L	H	H
H	H	H	H	L
H	H	S	L	H

H = high level, L = low level, X = irrelevant,
S = shorted to ground

† G and F̄ are common to the four drivers. If any of the four Y outputs is shorted, the fault flag will respond.

description

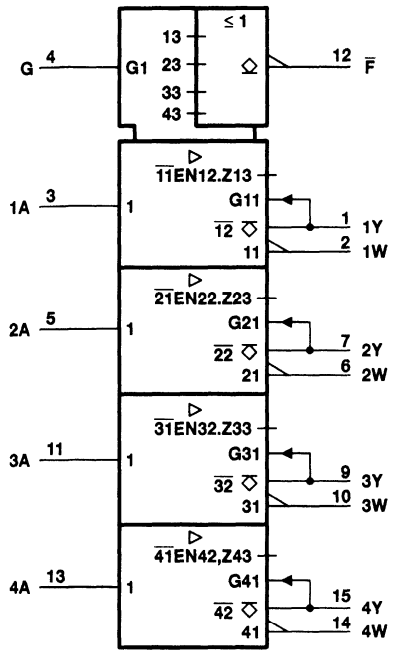
The SN75130 quadruple line driver is designed to meet the IBM 360/370 I/O specification GA22-6974-3. The output voltage is 3.11 V minimum (at I_{OH} = −59.3 mA) over the recommended ranges of supply voltage (4.5 V to 5.95 V) and temperature (0°C to 70°C). Driver outputs use a fault-detection current-limit circuit to allow high drive current but still minimize power dissipation when the output is shorted to ground. The SN75130 is compatible with standard TTL logic and supply voltages.

Fault-flag circuitry is designed to sense and signal a line short on any Y line. Upon detecting an output fault condition, the fault-flag circuit forces the driver output into the off (low) state and signals a fault condition by causing the fault-flag output to go low.

The SN75130 can drive a 50-Ω load or a 90-Ω load as used in many I/O systems. Optimum performance can be achieved when the device is used with either the SN75128 or SN75129 line receiver. Also, see the SN751730 for new 360/370 interface designs.

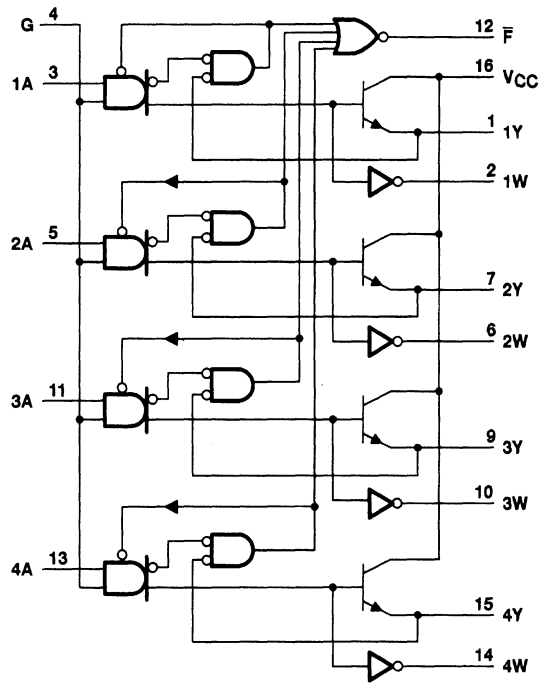
The SN75130 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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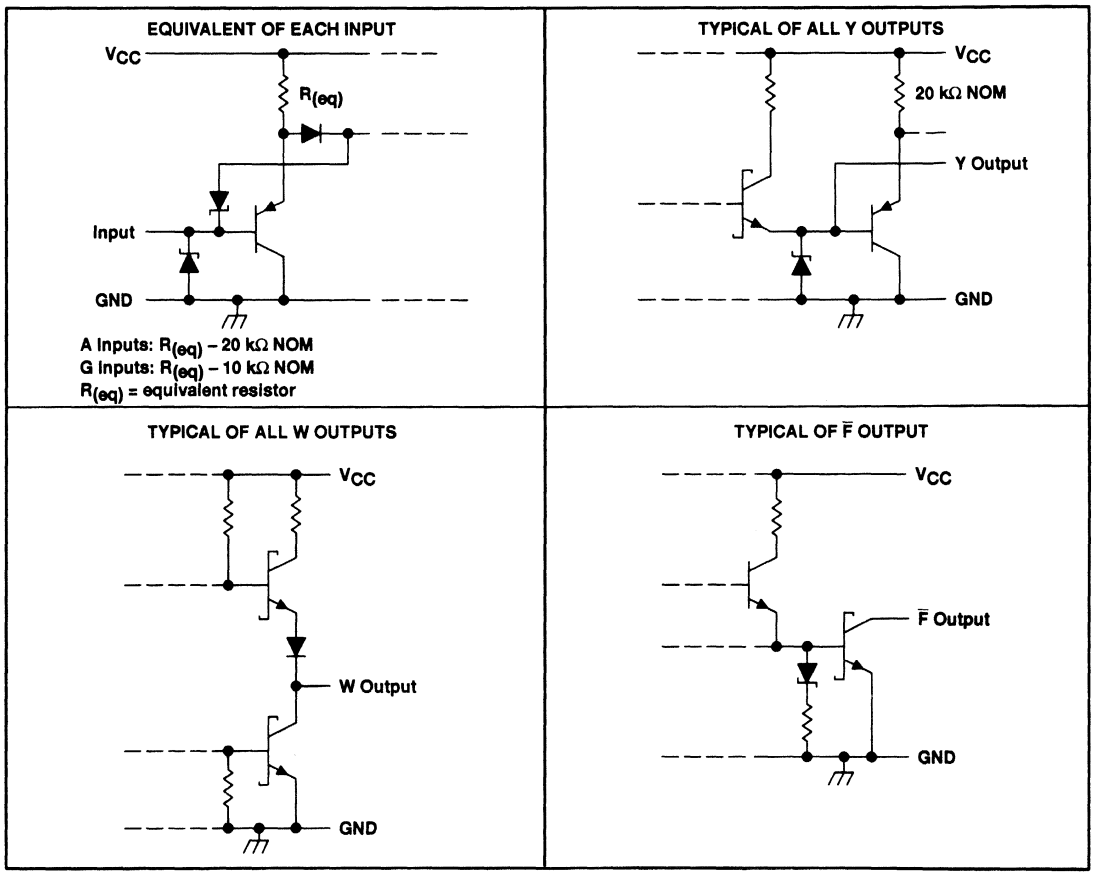
schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.95	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−59.3	mA
Operating free-air temperature, T_A	0		70	°C

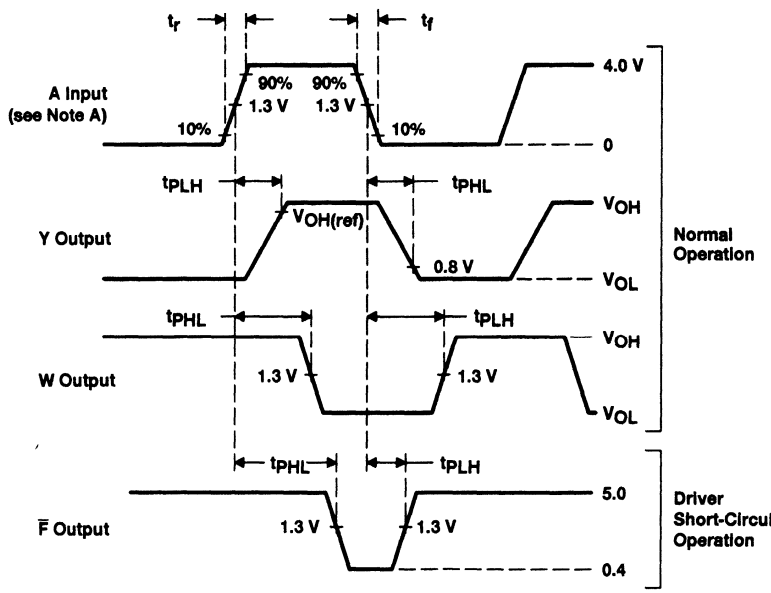
electrical characteristics over recommended operating free-air temperature range

PARAMETER			TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}	Input clamp voltage	A,G	$I_I = -18$ mA				−1.5	V
V_{OH}	High-level output voltage	Y	$V_{CC} = 4.5$ V,	$I_{OH} = -59.3$ mA,	$V_{IH} = 2$ V	3.11		V
		Y	$V_{CC} = 5.25$ V,	$I_{OH} = -41$ mA,	$V_{IH} = 2$ V	3.9		
		W	$V_{CC} = 4.5$ V,	$I_{OH} = -400$ µA,	$V_{IH} = 2$ V	2.5		
V_{OL}	Low-level output voltage	Y	$V_{CC} = 5.5$ V,	$I_{OL} = 240$ µA,	$V_{IL} = 0.8$ V		0.15	V
		Y	$V_{CC} = 5.95$ V,	$I_{OL} = 1$ mA,	$V_{IL} = 0.8$ V		0.15	
		F̄	$V_{CC} = 4.5$ V,	$I_{OL} = 8$ mA,	Y at 0 V		0.5	
		W	$V_{CC} = 4.5$ V,	$I_{OL} = 8$ mA			0.5	
$I_{O(off)}$	Off-state output current	Y	$V_{CC} = 4.5$ V,	$V_{IL} = 0$,	$V_O = 3.11$ V		100	µA
		Y	$V_{CC} = 0$,	$V_{IL} = 0$,	$V_O = 3.11$ V		200	
I_{OH}	High-level output current	F̄	$V_{CC} = 5.95$ V,	$V_{OH} = 5.95$ V			100	µA
I_I	Input current	A	$V_{CC} = 4.5$ V,	$V_{IH} = 5.5$ V			100	µA
		G					400	
I_{IH}	High-level input current	A	$V_{CC} = 4.5$ V,	$V_{IH} = 2.7$ V			20	µA
		G					80	
I_{IL}	Low-level input current	A	$V_{CC} = 5.95$ V,	$V_{IL} = 0.4$ V			250	µA
		G					−1000	
I_{OS}	Short-circuit output current	Y	$V_{CC} = 5.5$ V,	$V_O = 0$			−5	mA
		W				−15	−100	
		Y	$V_{CC} = 5.95$ V,	$V_O = 0$			−5	
		W				−15	−110	
I_{CCH}	Supply current, all outputs high		$V_{CC} = 5.5$ V,	$V_I = 2$ V			75	mA
			$V_{CC} = 5.95$ V,	$V_I = 2$ V			85	
I_{CCL}	Supply current, Y outputs low		$V_{CC} = 5.5$ V,	$V_I = 0.8$ V			55	mA
			$V_{CC} = 5.95$ V,	$V_I = 0.8$ V			70	

switching characteristics over recommended operating free-air temperature range

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	A	Y	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, Input f = 1 MHz,	$V_{OH(ref)}$ = 3.11 V, R_L = 50 Ω, See Figures 1 and 2		40	ns
t_{PHL}	Propagation delay time, high- to low-level output						37	ns
$\frac{t_{PLH}}{t_{PHL}}$	Ratio of propagation delay times					0.3	3	
t_{PLH}	Propagation delay time, low- to high-level output	A	Y	V_{CC} = 5.25 V to 5.59 V, C_L = 50 pF, Input f = 5 MHz,	$V_{OH(ref)}$ = 3.9 V, R_L = 90 Ω, See Figures 1 and 2		45	ns
t_{PHL}	Propagation delay time, high- to low-level output						45	ns
t_{PLH}	Propagation delay time, low- to high-level output	A	W	V_{CC} = 5 V, C_L = 15 pF,	R_L = 2 kΩ, See Figures 1 and 2		45	ns
t_{PHL}	Propagation delay time, high- to low-level output						28	ns
t_{PLH}	Propagation delay time, low- to high-level output	A	$\overline{F}$	V_{CC} = 5 V, C_L = 15 pF,	R_L = 2 kΩ, See Figures 1 and 2		60	ns
t_{PHL}	Propagation delay time, high- to low-level output						100	ns

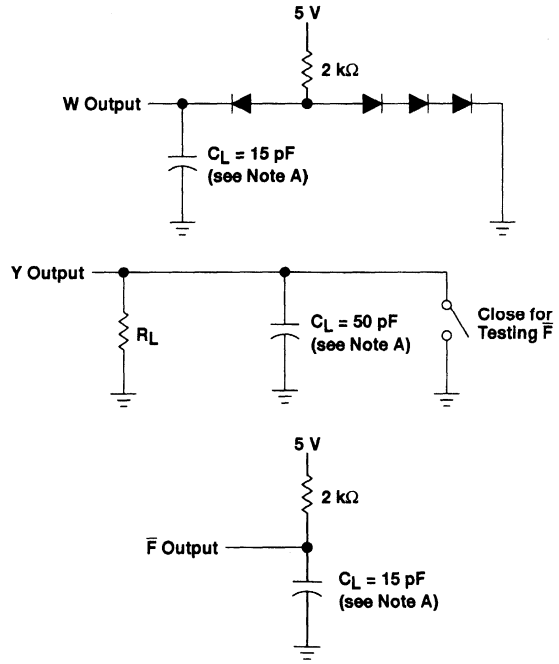
PARAMETER MEASUREMENT INFORMATION



NOTE A: The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \le 6$ ns, $t_f \le 6$ ns, Z_O = 50 Ω

Figure 1. Input and Output Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



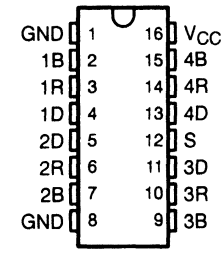
NOTE A: C_L includes probe and stray capacitance.

Figure 2. Switching Characteristics Load Circuits

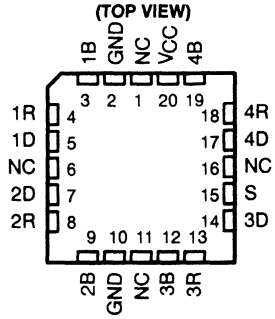
SLLS079B – SEPTEMBER 1973 – REVISED MAY 1995

- **Single 5-V Supply**
- **High-Input-Impedance, High-Threshold Receivers**
- **Common Driver Strobe**
- **TTL-Compatible Driver and Strobe Inputs With Clamp Diodes**
- **High-Speed Operation**
- **100-mA Open-Collector Driver Outputs**
- **Four Independent Channels**
- **TTL-Compatible Receiver Output**

SN55138 . . . J OR W PACKAGE
SN75138 . . . D OR N PACKAGE
(TOP VIEW)



SN55138 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN55138 and SN75138 quadruple bus transceivers are designed for two-way data communication over single-ended transmission lines. Each of the four identical channels consists of a driver with TTL inputs and a receiver with a TTL output. The driver open-collector output is designed to handle loads up to 100-mA open collector. The receiver input is internally connected to the driver output, and has a high impedance to minimize loading of the transmission line. Because of the high driver-output current and the high receiver-input impedance, a very large number (typically hundreds) of transceivers may be connected to a single data bus.

The receiver design also features a threshold of 2.3 V (typical), providing a wider noise margin than would be possible with a receiver having the usual TTL threshold. A strobe turns off all drivers (high impedance) but does not affect receiver operation. These circuits are designed for operation from a single 5-V supply and include a provision to minimize loading of the data bus when the power-supply voltage is zero.

The SN55138 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN75138 is characterized for operation from 0°C to 70°C.

Function Tables

TRANSMITTING

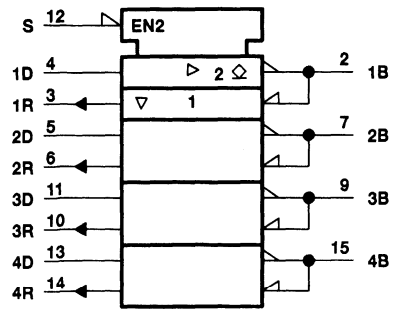
INPUTS		OUTPUTS	
S	D	B	R
L	H	L	H
L	L	H	L

RECEIVING

INPUTS			OUTPUT
S	B	D	R
H	H	X	L
H	L	X	H

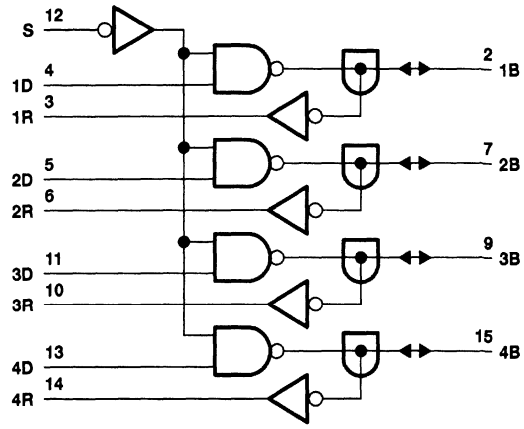
H = high level, L = low level, X = irrelevant

logic symbol†

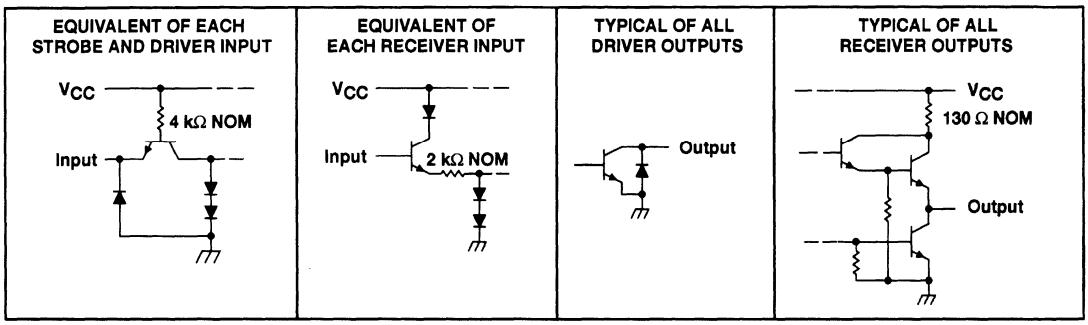


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

	SN55138	SN75138	UNIT
Supply voltage, V_{CC} (see Note 1)	7	7	V
Input voltage, V_I	5.5	5.5	V
Driver off-state output voltage	7	7	V
Low-level output current into the driver output	150	150	mA
Continuous total power dissipation	See Dissipation Rating Table		
Operating free-air temperature range, T_A	−55 to 125	0 to 70	°C
Storage temperature range, T_{stg}	−65 to 125	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or W package		260	°C
Case temperature for 60 seconds, T_C: FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300	300	°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to both ground terminals connected together.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	—
FK†	1375 mW	11.0 mW/°C	880 mW	275 mW
J†	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—
W	1000 mW	8.0 mW/°C	640 mW	200 mW

† In the FK and J packages, the SN55138 chip is alloy mounted.

recommended operating conditions

		SN55138			SN75138			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5		5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	Driver or strobe	2			2			V
	Receiver	3.2			2.9			
Low-level input voltage, V_{IL}	Driver or strobe			0.8			0.8	V
	Receiver			1.5			1.8	
High-level output current, I_{OH}	Receiver output			−400			−400	μA
Low-level output current, I_{OL}	Driver output			100			100	mA
	Receiver output			16			16	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN55138			SN75138			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage	Driver or strobe	V_{CC} = MIN,	I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	Receiver	V_{CC} = MIN, $V_{IL(R)}$ = V_{IL} max,	$V_{IH(S)}$ = 2 V, I_{OH} = −400 μA	2.4	3.5		2.4	3.5		V
V_{OL}	Low-level output voltage	Driver	V_{CC} = MIN, $V_{IL(S)}$ = 0.8 V,	$V_{IH(D)}$ = 2 V, I_{OL} = 100 mA			0.45			0.45	V
		Receiver	V_{CC} = MIN, $V_{IH(S)}$ = 2 V,	$V_{IH(R)}$ = V_{IH} min, I_{OL} = 16 mA			0.4			0.4	
$I_{I(max)}$	Input current at maximum input voltage	Driver or strobe	V_{CC} = MAX,	V_I = V_{CC}			1			1	mA
I_{IH}	High-level input current	Driver or strobe	V_{CC} = MAX,	V_I = 2.4 V			40			40	μA
		Receiver	V_{CC} = 5 V, $V_{I(S)}$ = 2 V	$V_{I(R)}$ = 4.5 V,		25	300		25	300	
I_{IL}	Low-level input current	Driver or strobe	V_{CC} = MAX,	V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
		Receiver	V_{CC} = MAX, $V_{I(S)}$ = 2 V	$V_{I(R)}$ = 0.45 V,			−50			−50	μA
$I_{I(off)}$	Input current with power off	Receiver	V_{CC} = 0,	V_I = 4.5 V		1.1	1.5		1.1	1.5	mA
I_{OS}	Short-circuit output current§	Receiver	V_{CC} = MAX		−20		−55	−18		−55	mA
I_{CC}	Supply current	All driver outputs low	V_{CC} = MAX, $V_{I(S)}$ = 0.8 V	$V_{I(D)}$ = 2 V,		50	65		50	65	mA
		All driver outputs high	V_{CC} = MAX, $V_{I(S)}$ = 2 V, Receiver outputs open	$V_{I(R)}$ = 3.5 V,		42	55		42	55	

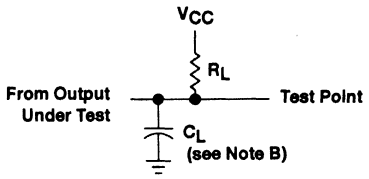
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. Parenthetical letters D, R, and S used with V_I refer to the driver input, receiver input, and strobe input, respectively.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

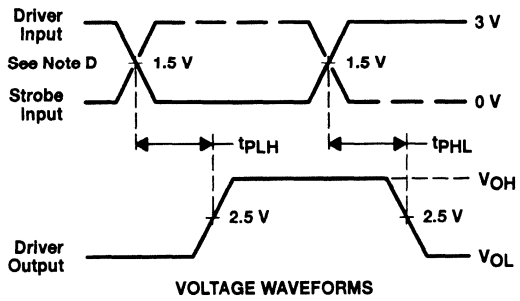
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Driver	Driver	C_L = 50 pF, R_L = 50 Ω,	See Figure 1		15	24	ns
t_{PHL}						14	24	
t_{PLH}	Strobe	Driver				18	28	ns
t_{PHL}						22	32	
t_{PLH}	Receiver	Receiver	C_L = 15 pF R_L = 400 Ω,	See Figure 2		7	15	ns
t_{PHL}						8	15	

¶ t_{PLH} = propagation delay time, low- to high-level output
t_{PHL} = propagation delay time, high- to low-level output

PARAMETER MEASUREMENT INFORMATION

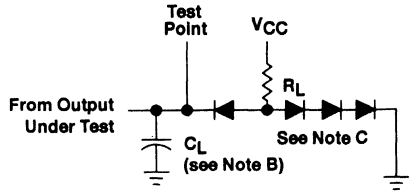


TEST CIRCUIT

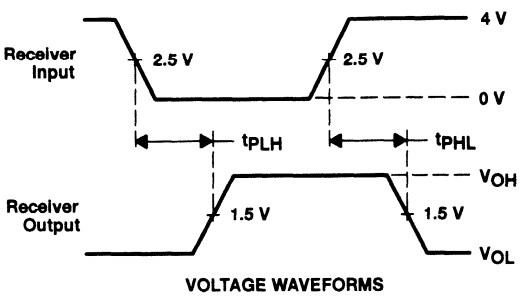


VOLTAGE WAVEFORMS

Figure 1. Propagation Delay Times From Data and Strobe Inputs



TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 2. Propagation Delay Times From Receiver Input

NOTES: A. Input pulses are supplied by generators having the following characteristics: t_W = 100 ns, PRR ≤ 1 MHz, t_r ≤ 10 ns, t_f ≤ 10 ns, $Z_O \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or 1N3064.
D. When testing driver input (solid line) strobe must be low; when testing strobe input (dashed line) driver input must be high.

TYPICAL CHARACTERISTICS†

DRIVER TRANSFER CHARACTERISTICS

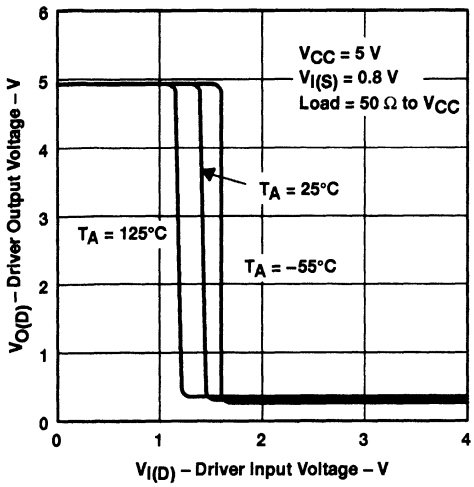


Figure 3

DRIVER TRANSFER CHARACTERISTICS

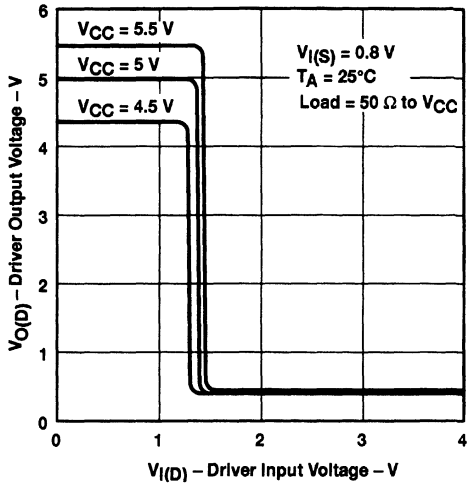


Figure 4

STROBE-TO-DRIVER OUTPUT TRANSFER CHARACTERISTICS

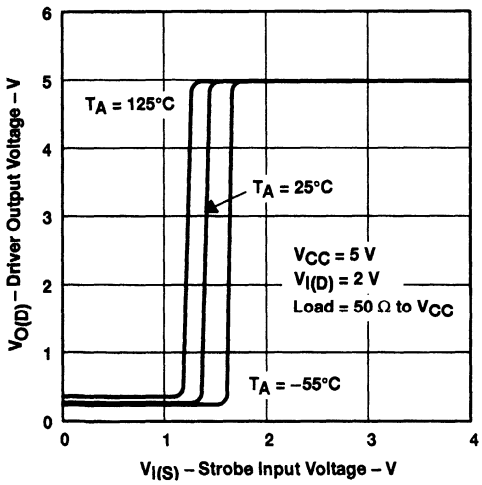


Figure 5

STROBE-TO-DRIVER OUTPUT TRANSFER CHARACTERISTICS

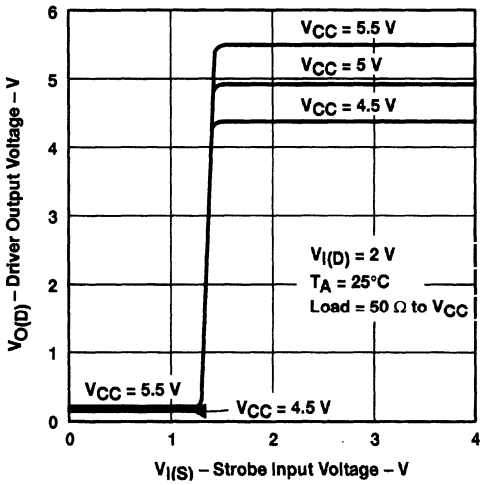


Figure 6

† Data for temperatures below 0°C and above 70°C is applicable to SN55138 circuits only.

TYPICAL CHARACTERISTICS†

RECEIVER TRANSFER CHARACTERISTICS

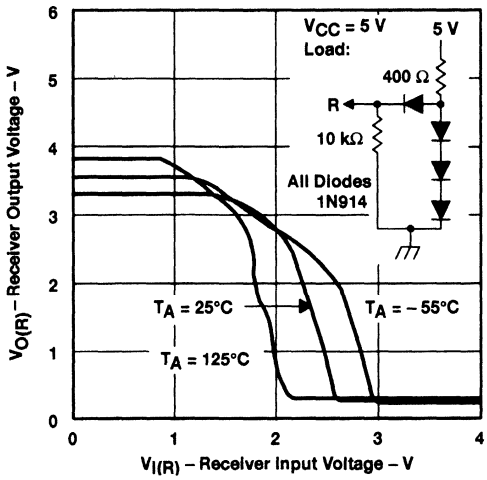


Figure 7

RECEIVER TRANSFER CHARACTERISTICS

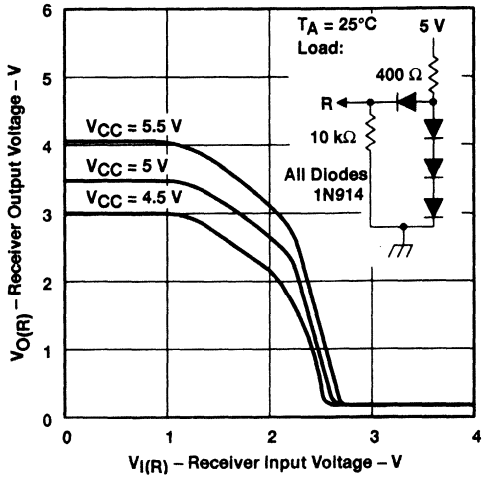


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT (RECEIVER)

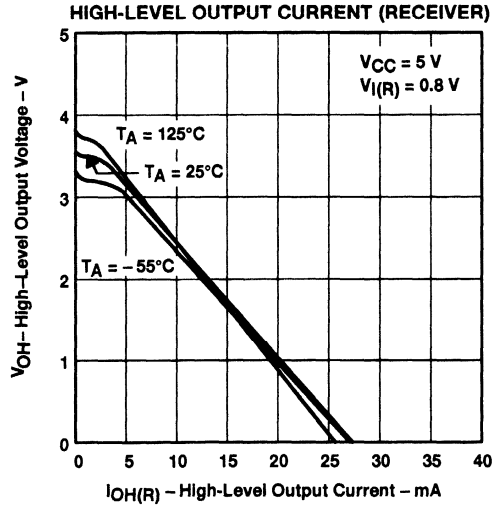


Figure 9

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT (RECEIVER)

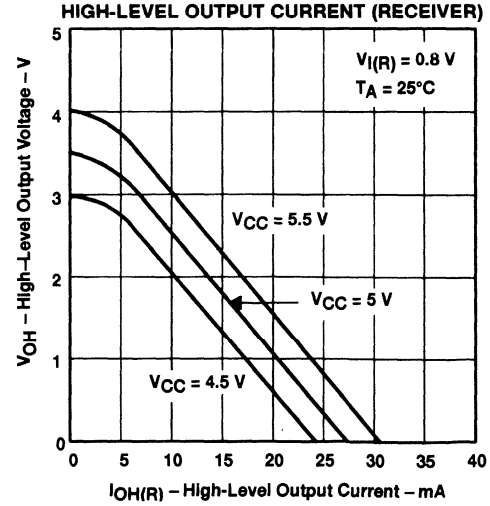


Figure 10

† Data for temperatures below 0°C and above 70°C is applicable to SN55138 circuits only.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT (RECEIVER)

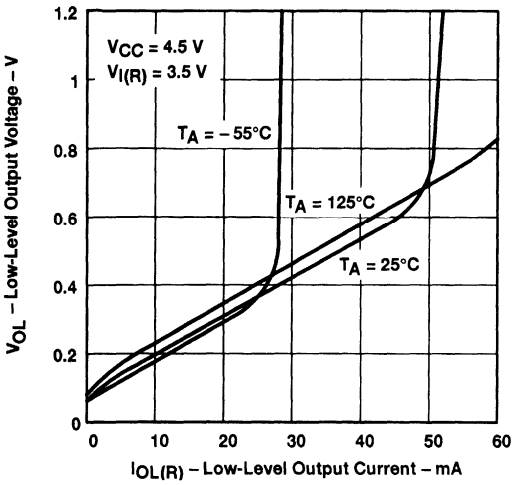


Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT (DRIVER)

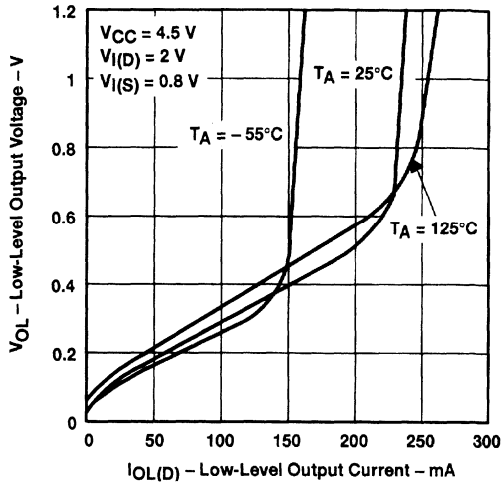


Figure 12

RECEIVER INPUT CURRENT
vs
RECEIVER INPUT VOLTAGE

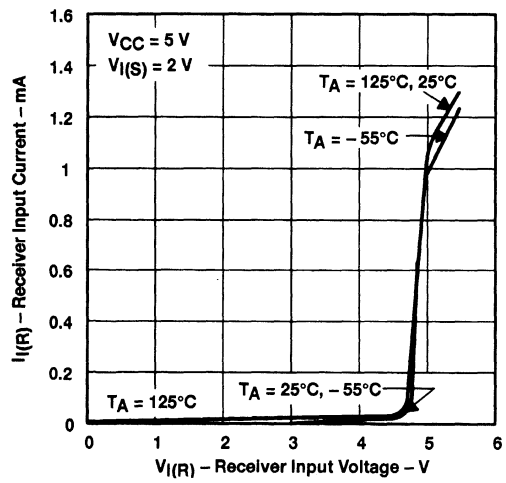


Figure 13

RECEIVER INPUT CURRENT
vs
RECEIVER INPUT VOLTAGE

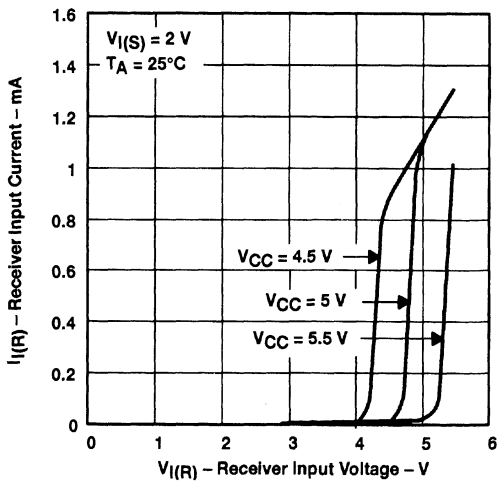


Figure 14

† Data for temperatures below 0°C and above 70°C is applicable to SN55138 circuits only.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE
(ALL DRIVER OUTPUTS LOW)

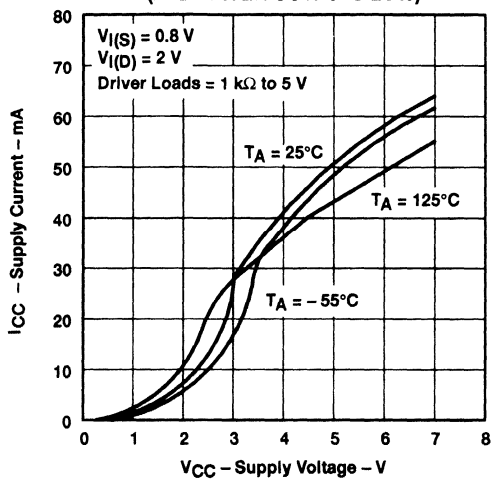


Figure 15

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

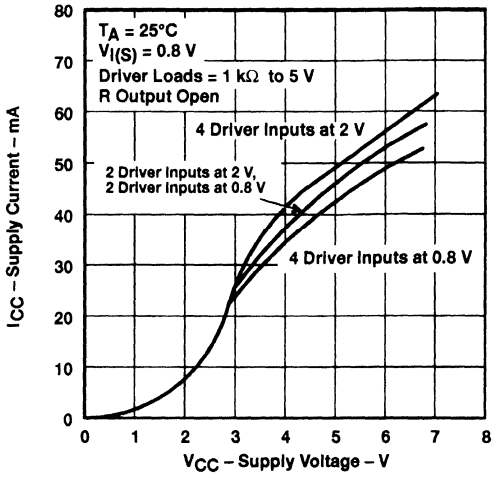


Figure 16

PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

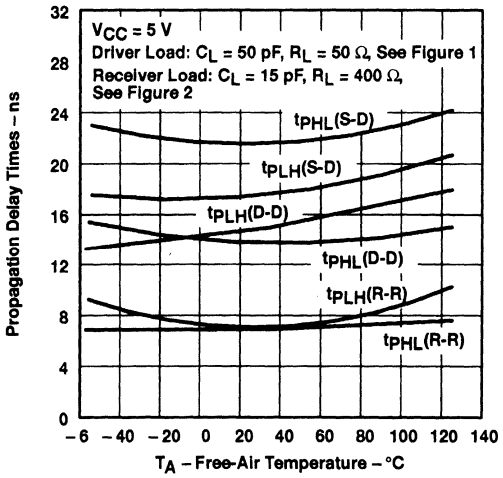


Figure 17

PROPAGATION DELAY TIMES
vs
SUPPLY VOLTAGE

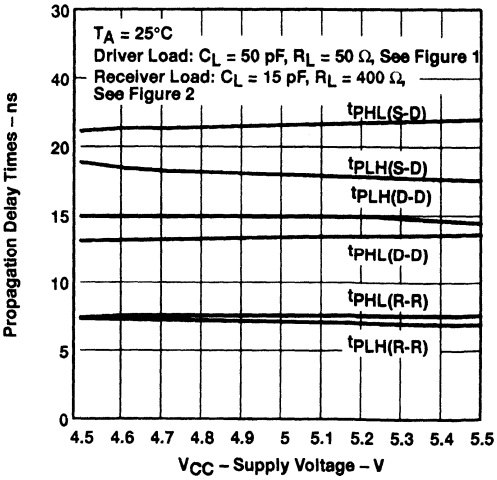


Figure 18

† Data for temperatures below 0°C and above 70°C is applicable to SN55138 circuits only.

TYPICAL CHARACTERISTICS

DRIVER
PROPAGATION DELAY TIMES
vs
LOAD CAPACITANCE

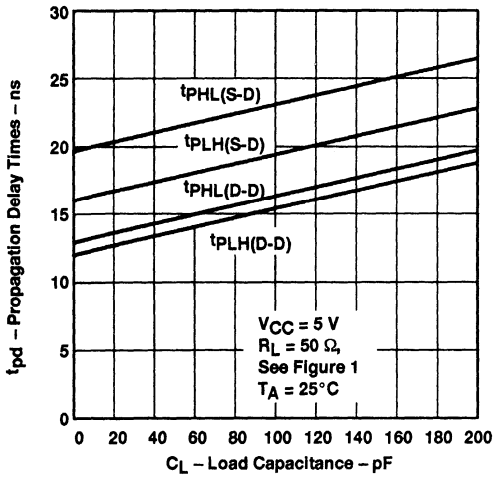


Figure 19

RECEIVER
PROPAGATION DELAY TIMES
vs
LOAD CAPACITANCE

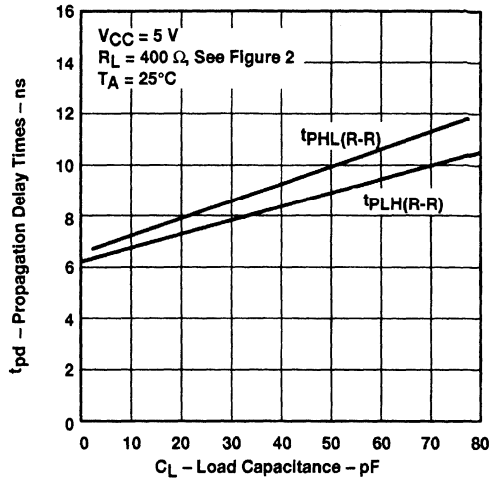
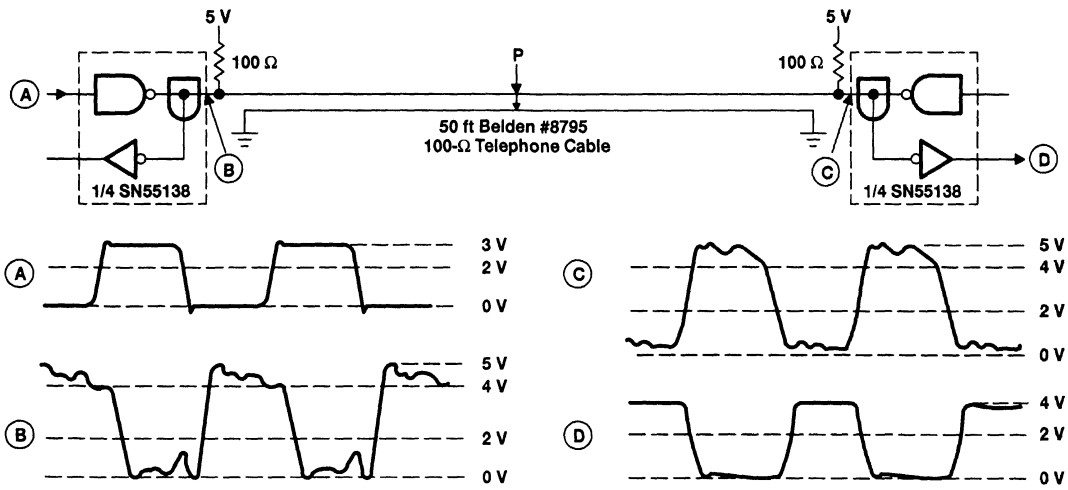


Figure 20

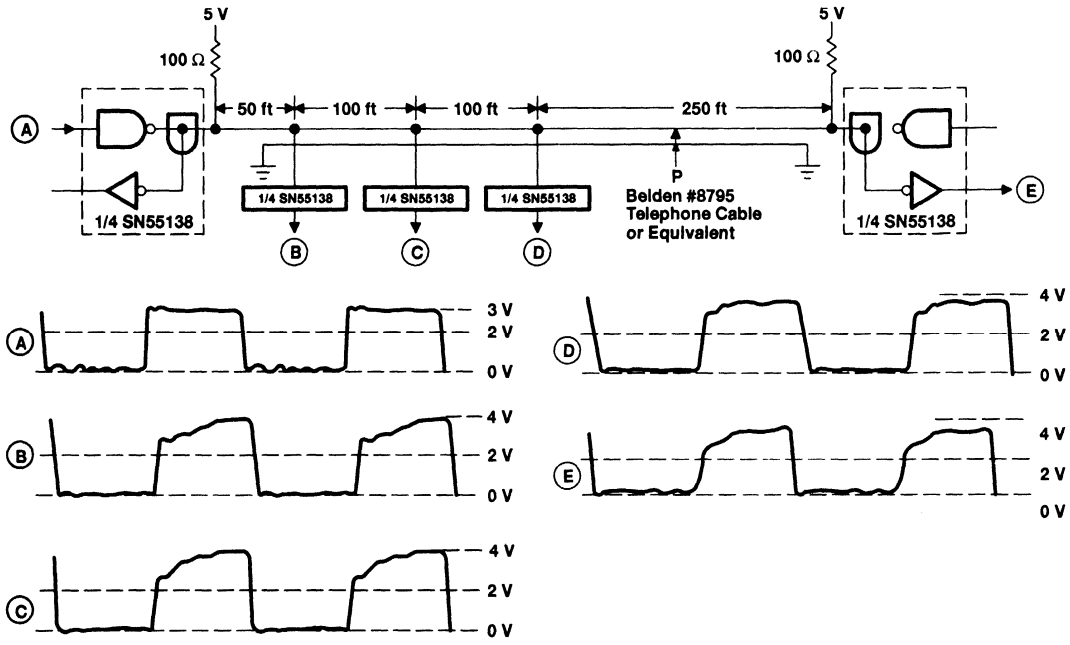
APPLICATION INFORMATION



TYPICAL VOLTAGE WAVEFORMS

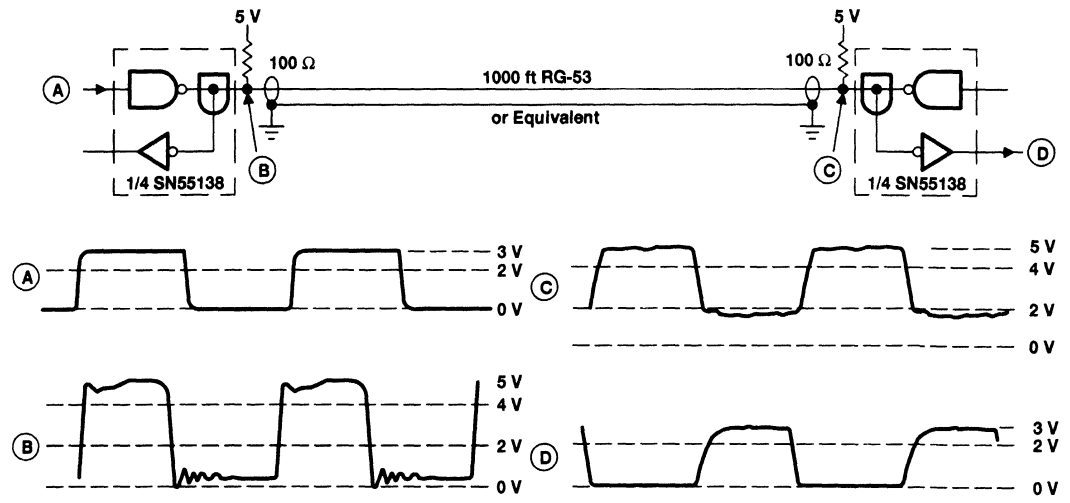
Figure 21. Point-to-Point Communication Over 50 Feet of Twisted Pair at 5 MHz

APPLICATION INFORMATION



TYPICAL VOLTAGE WAVEFORMS

Figure 22. Party-Line Communication on 500 Feet of Twisted Pair at 1 MHz



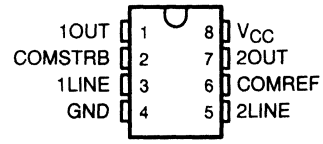
TYPICAL VOLTAGE WAVEFORMS

Figure 23. Point-to-Point Communication Over 1000 Feet of Coaxial Cable at 1 MHz

SLLS080B – JANUARY 1977 – REVISED MAY 1995

- **Single 5-V Supply**
- **±100-mV Sensitivity**
- **For Application as:**
  - **Single-Ended Line Receiver**
  - **Gated Oscillator**
  - **Level Comparator**
- **Adjustable Reference Voltage**
- **TTL Outputs**
- **TTL-Compatible Strobe**
- **Designed for Party-Line (Data-Bus) Applications**
- **Common Reference Voltage Pin**
- **Common Strobe**
- **SN75141 Has Diode-Protected Input Stage for Power-Off Condition**

P OR PS† PACKAGE
(TOP VIEW)



† The PS package is only available left-ended taped and reeled (order SN75140 PSLE).

THE SN75141 IS NOT RECOMMENDED FOR NEW DESIGNS

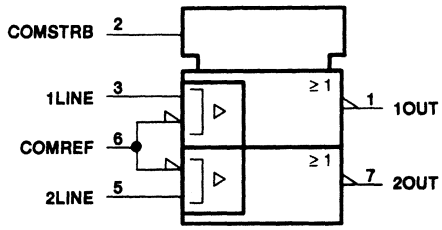
description

Each of these devices consists of a dual single-ended line receiver with TTL-compatible strobes and outputs. The reference voltage (switching threshold) is applied externally and can be adjusted from 1.5 V to 3.5 V, making it possible to optimize noise immunity for a given system design. Due to their low input current (less than 100 μA), they are ideally suited for party-line (data-bus) systems.

The SN75140 has a common reference voltage pin and a common strobe. The SN75141 is the same as the SN75140 except that the input stage is diode protected.

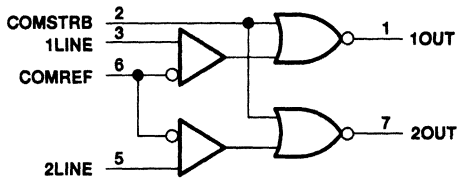
The SN75140 and SN75141 are characterized for operation from 0°C to 70°C.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

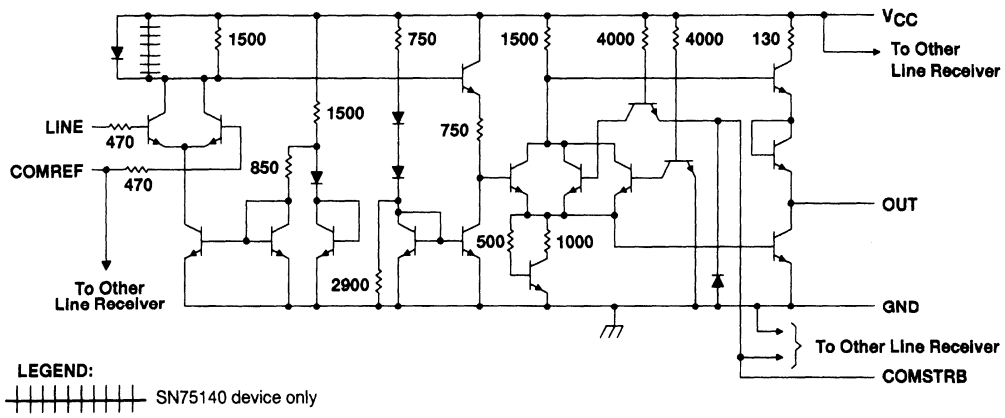


FUNCTION TABLE
(each receiver)

LINE INPUT	STROBE	OUTPUT
≤ V_{ref} – 100 mV	L	H
≥ V_{ref} + 100 mV	X	L
X	H	L

H = high level, L = low level, X = irrelevant

schematic (each receiver)



Resistor values shown are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Reference input voltage, V_{ref} ..... 5.5 V
Line input voltage range with respect to GND ..... −2 V to 5.5 V
Line input voltage with respect to V_{ref} ..... ±5 V
Strobe input voltage ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Unless otherwise specified, voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW
PS	450 mW	3.6 mW/°C	288 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Reference input voltage, V_{ref}	1.5		3.5	V
High-level line input voltage, $V_{IH(L)}$	$V_{ref}+0.1$		$V_{CC}-1$	V
Low-level line input voltage, $V_{IL(L)}$	0		$V_{ref}-0.1$	V
High-level strobe input voltage, $V_{IH(S)}$	2		5.5	V
Low-level strobe input voltage, $V_{IL(S)}$	0		0.8	V

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ±10%, V_{ref} = 1.5 V to 3.5 V (unless otherwise noted)

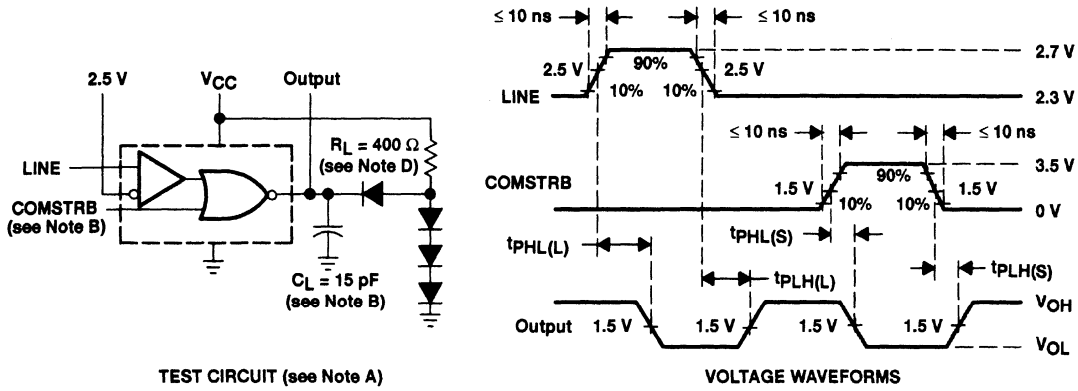
PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Strobe input clamp voltage		$I_{I(S)}$ = −12 mA				−1.5	V
V_{OH}	High-level output voltage		$V_{IL(L)}$ = V_{ref} − 100 mV, I_{OH} = −400 µA	$V_{IL(S)}$ = 0.8 V,	2.4			V
V_{OL}	Low-level output voltage		$V_{IH(L)}$ = V_{ref} + 100 mV, I_{OL} = 16 mA	$V_{IL(S)}$ = 0.8 V,			0.4	V
			$V_{IL(L)}$ = V_{ref} − 100 mV, I_{OL} = 16 mA	$V_{IH(S)}$ = 2 V,			0.4	
$I_{I(S)}$	Strobe input current at maximum input voltage	Strobe	$V_{I(S)}$ = 5.5 V				1	mA
		COMSTRB					2	
I_{IH}	High-level input current	Strobe	$V_{I(S)}$ = 2.4 V				40	µA
		COMSTRB					80	
		LINE	$V_{I(L)}$ = 3.5 V,	V_{ref} = 1.5 V		35	100	
		Reference	$V_{I(L)}$ = 0,	V_{ref} = 3.5 V		35	100	
		COMREF				70	200	
I_{IL}	Low-level input current	Strobe	$V_{I(S)}$ = 0.4 V				−1.6	mA
		COMSTRB					−3.2	
		LINE	$V_{I(L)}$ = 0,	V_{ref} = 1.5 V			−10	µA
		Reference	$V_{I(L)}$ = 1.5 V,	V_{ref} = 0			−10	
		COMREF					−20	
I_{OS}	Short-circuit output current‡		V_{CC} = 5.5 V		−18		−55	mA
I_{CCH}	Supply current, output high		$V_{I(S)}$ = 0,	$V_{I(L)}$ = V_{ref} − 100 mV		18	30	mA
I_{CCL}	Supply current, output low		$V_{I(S)}$ = 0,	$V_{I(L)}$ = V_{ref} + 100 mV		20	35	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Only one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, V_{ref} = 2.5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH(L)}$	Propagation delay time, low- to high-level output from LINE	C_L = 15 pF, R_L = 400 kΩ, See Figure 1		22	35	ns
$t_{PHL(L)}$	Propagation delay time, high- to low-level output from LINE			22	30	
$t_{PLH(S)}$	Propagation delay time, low- to high-level output from COMSTRB			12	22	ns
$t_{PHL(S)}$	Propagation delay time, high- to low-level output from COMSTRB			8	15	

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT (see Note A)

VOLTAGE WAVEFORMS

NOTES: A. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_O = 50 Ω.
B. Unused strobes are to be grounded.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N3064.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

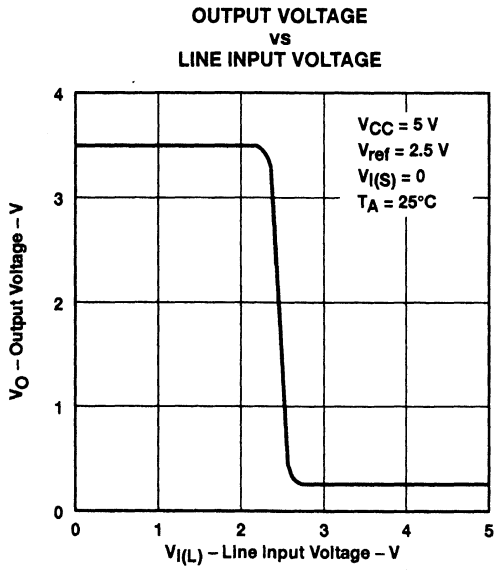


Figure 2

APPLICATION INFORMATION

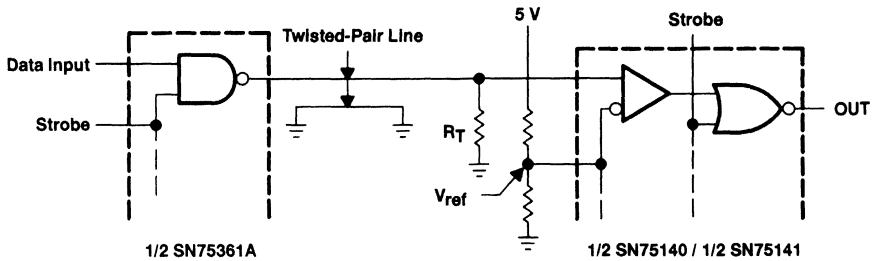
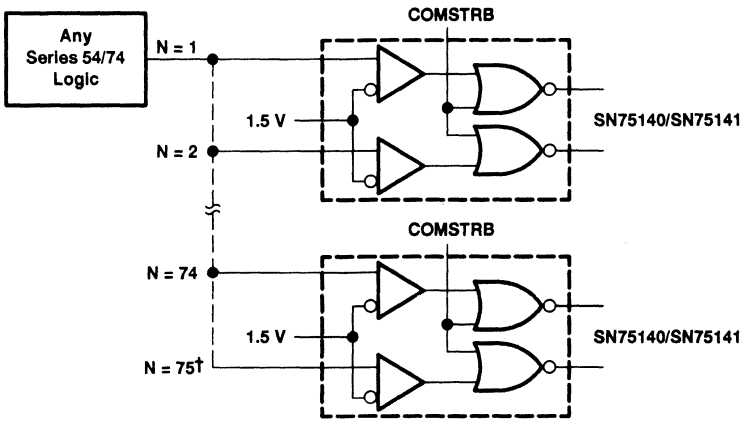


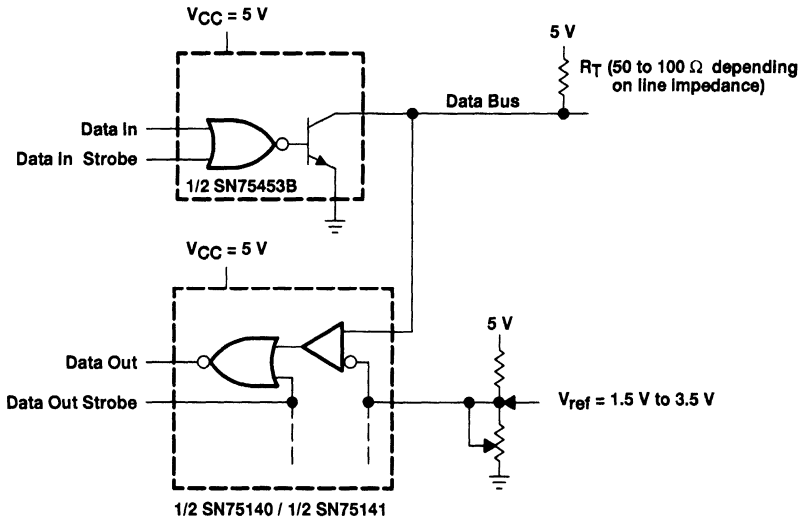
Figure 3. Line Receiver



† Although most Series 54/74 circuits have a 2.4-V output at 400 μA, they are typically capable of maintaining a 2.4-V output level under a load of 7.5 mA.

Figure 4. High Fanout From Standard TTL Gate

APPLICATION INFORMATION



NOTE A: Using this arrangement, as many as 100 transceivers can be connected to a single data bus. The adjustable reference voltage feature allows the noise margin to be optimized for a given system. The complete dual bus transceiver (SN75453B driver and SN75140 receiver) can be assembled in approximately the same space required by a single 16-pin package and only one power supply is required (5 V). Data in and data out are TTL compatible.

Figure 5. Dual Bus Transceiver

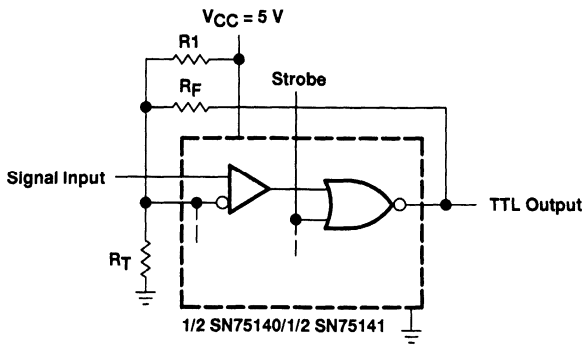
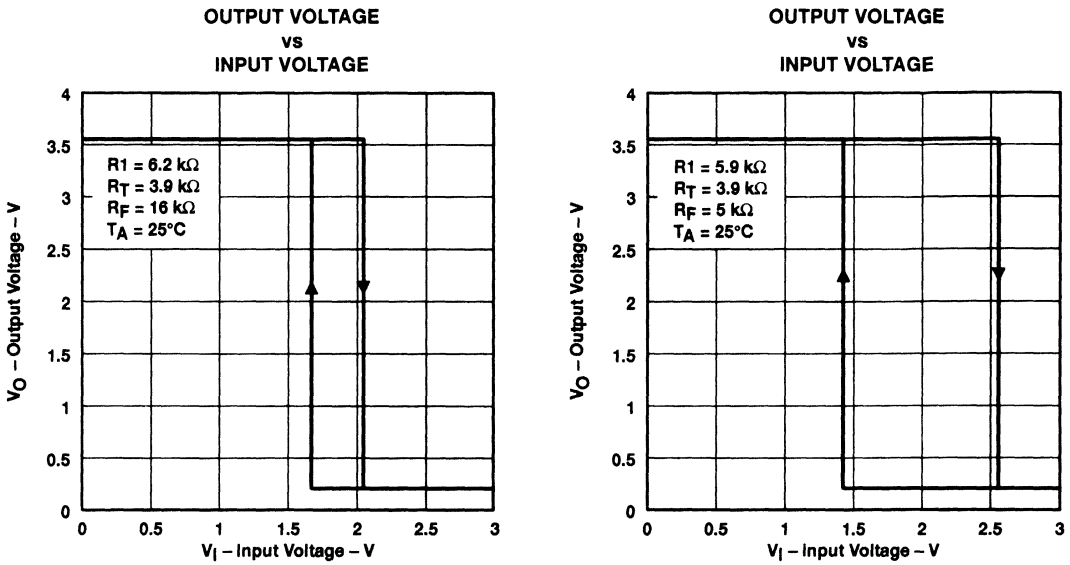


Figure 6. Schmitt Trigger

APPLICATION INFORMATION



NOTE A: Slowly changing input levels from data lines, optical detectors, and other types of transducers may be converted to standard TTL signals with this Schmitt trigger circuit. R_1, R_F, and R_T may be adjusted for the desired hysteresis and trigger levels.

Figure 7. Examples of Transfer Characteristics

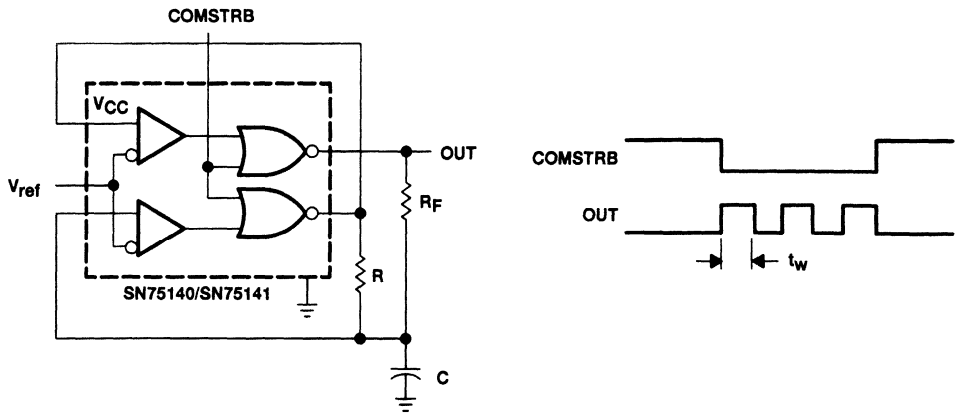


Figure 8. Gated Oscillator

APPLICATION INFORMATION

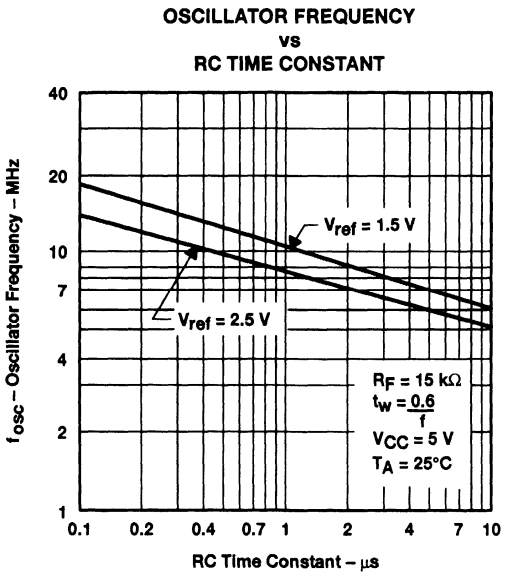


Figure 9

SLLS015B – FEBRUARY 1986 – REVISED MAY 1995

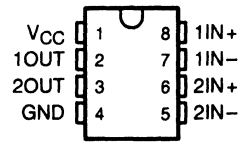
- **Meets or Exceeds the Requirements of ANSI EIA/TIA-422-B and -423-B**
- **Meets or Exceeds the Requirements of ANSI EIA/TIA-232-E and ITU Recommendation V.28 With External Components**
- **Meets Federal Standards 1020 and 1030**
- **Built-in 5-MHz Low-Pass Filter**
- **Operates From Single 5-V Power Supply**
- **Wide Common-Mode Voltage Range**
- **High Input Impedance**
- **TTL-Compatible Outputs**
- **8-Pin Dual-In-Line Package**
- **Pinout Compatible With the μA9637 and μA9639**

description

The SN75146 is a dual differential line receiver designed to meet ANSI Standards EIA/TIA-422-B and -423-B. The receiver is designed to have a constant impedance with input voltages of ±3 V to ±25 V allowing it to meet the requirements of EIA/TIA-232-E and ITU recommendation V.28 with the addition of an external bias resistor. This receiver is designed for low-speed operation below 355 kHz and has a built-in 5-MHz low-pass filter to attenuate high-frequency noise. The inputs are compatible with either a single-ended or a differential line system and the outputs are TTL compatible. This device operates from a single 5-V power supply and is supplied in both the 8-pin dual-in-line and small-outline packages.

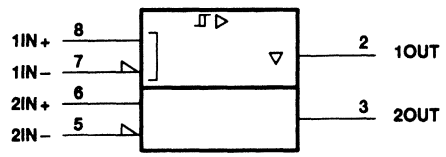
The SN75146 is characterized for operation from 0°C to 70°C.

D OR P PACKAGE
(TOP VIEW)



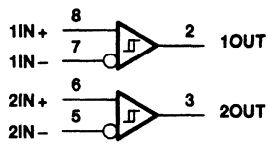
THE SN75146 IS NOT RECOMMENDED FOR NEW DESIGNS.

logic symbol†

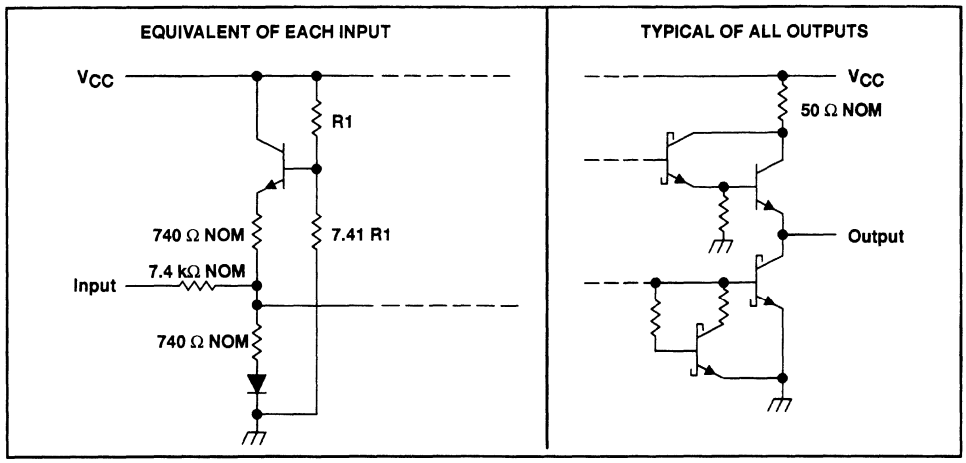


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Input voltage, V_I ..... ±25 V
Differential input voltage, V_{ID} (see Note 2) ..... ±25 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to 5.5 V
Low-level output current, I_{OL} ..... 50 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Operating free-air temperature, T_A	0	25	70	°C

electrical characteristics over recommended ranges of supply voltage, common-mode input voltage, and operating free-air temperature (unless otherwise noted)

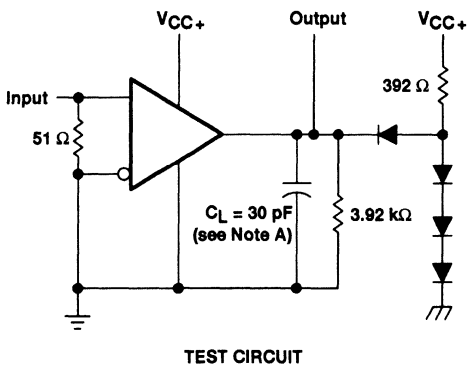
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT}	Threshold input voltage (V_{IT+} and V_{IT-})			−0.2‡		0.2	V
		See Note 3		−0.4‡		0.4	
V_{hys}	Hysteresis ($V_{IT+} - V_{IT-}$)			70			mV
V_{IB}	Input bias voltage	$I_I = 0$		2		2.4	V
V_{OH}	High-level output voltage	$V_{ID} = 0.2$ V,	$I_O = -1$ mA	2.5	3.5		V
V_{OL}	Low-level output voltage	$V_{ID} = -0.2$ V,	$I_O = 20$ mA		0.35	0.5	V
r_i	Input resistance	$V_I = 3$ V to 25 V or $V_I = -3$ V to −25 V, See Note 4		6	7.8	10.5	kΩ
I_I	Input current	$V_{CC} = 0$ to 5.5 V, See Note 5	$V_I = 10$ V		1.1	3.25	mA
			$V_I = -10$ V		−1.6	−3.25	
I_{OS}	Short-circuit output current§	$V_O = 0$,	$V_{ID} = 0.2$ V	−40	−75	−100	mA
I_{CC}	Supply current	$V_{ID} = -0.5$ V,	No load		35	50	mA

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.
§ Only one output should be shorted at a time, and duration of the short circuit should not exceed one second.
NOTES: 3. The expanded threshold parameter is tested with a 500-Ω resistor in series with each input.
4. r_i is defined by $\Delta V_I/\Delta I_I$.
5. The input not under test is grounded.

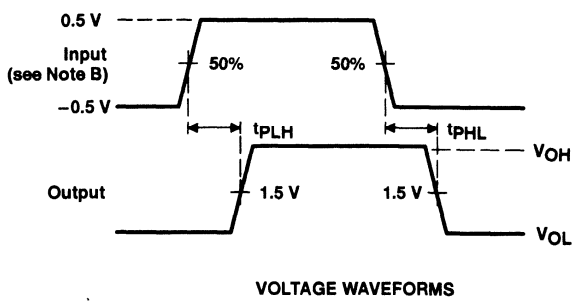
switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$C_L = 30$ pF,	See Figure 1	100	150	300	ns
t_{PHL}	Propagation delay time, high-to-low-level output			100	150	300	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $t_r \le 5$ ns, $t_f \le 5$ ns, PRR ≤ 300 kHz, duty cycle = 50%.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

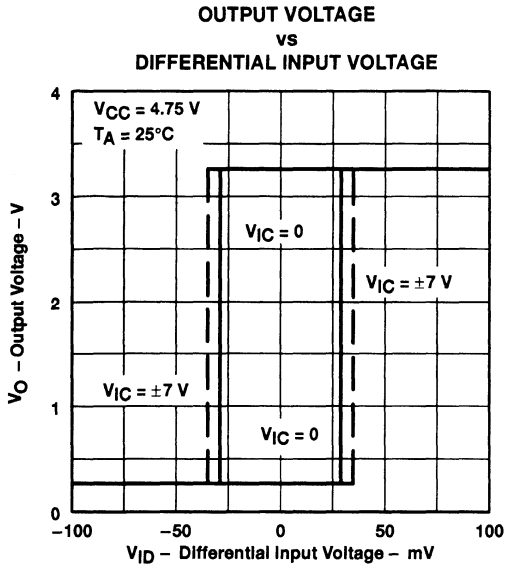


Figure 2

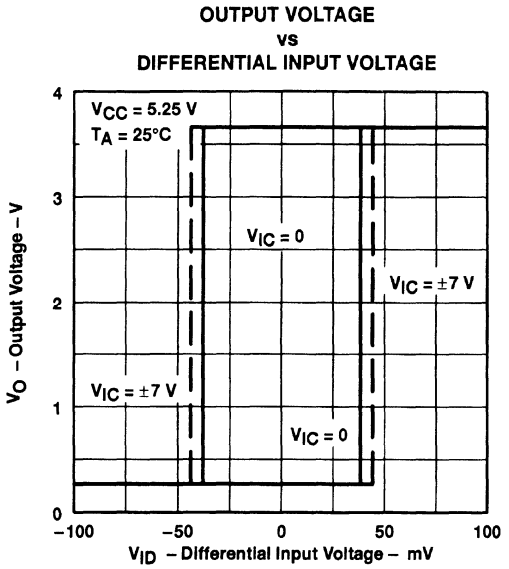
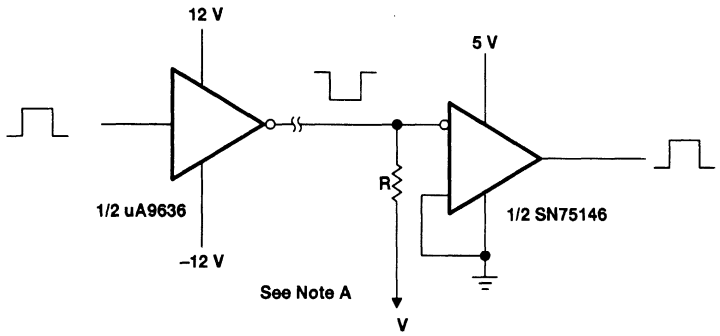


Figure 3

APPLICATION INFORMATION



NOTE A: In order to meet the input-impedance and open-circuit-input voltage requirements of ANSI Standard EIA/TIA-232-E and ITU recommendation V.28 and ensure open-circuit-input fail-safe operation, R and V are selected to satisfy the following equations:

$$V = -1.1\text{–}3.3\,\frac{R}{r_i} \text{ volts}$$

$$3\ \text{k}\Omega \le \frac{R(r_i)}{R + r_i} \le 7\ \text{k}\Omega$$

Figure 4. EIA/TIA-232-E System Applications

APPLICATION INFORMATION

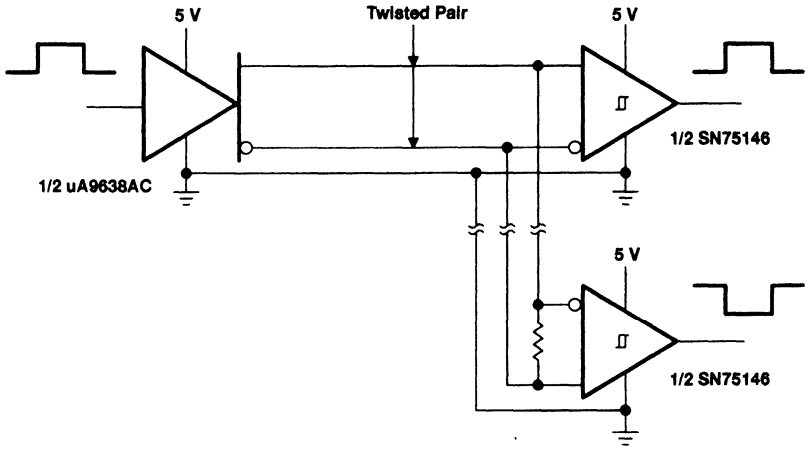


Figure 5. EIA/TIA-422-B System Applications

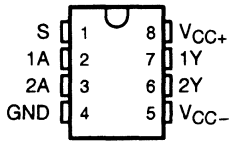
- **Meets or Exceeds the Requirement of ANSI EIA/TIA-232-E and ITU Recommendation V.28**
- **Withstands Sustained Output Short Circuit to Any Low-Impedance Voltage Between –25 V and 25 V**
- **2-μs Max Transition Time Through the 3-V to –3-V Transition Region Under Full 2500-pF Load**
- **Inputs Compatible With Most TTL Families**
- **Common Strobe Input**
- **Inverting Output**
- **Slew Rate Can Be Controlled With an External Capacitor at the Output**
- **Standard Supply Voltages . . . ±12 V**

description

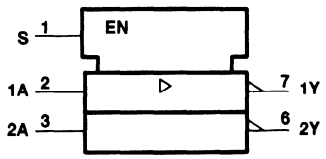
The SN75150 is a monolithic dual line driver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by ANSI EIA/TIA-232-E. A rate of 20000 bits per second can be transmitted with a full 2500-pF load. Other applications are in data-transmission systems using relatively short single lines, in level translators, and for driving MOS devices. The logic input is compatible with most TTL families. Operation is from 12-V and –12-V power supplies.

The SN75150 is characterized for operation from 0°C to 70°C.

D OR P PACKAGE
(TOP VIEW)

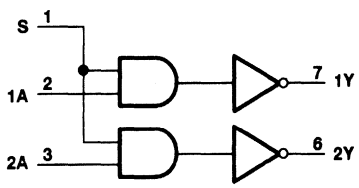


logic symbol†

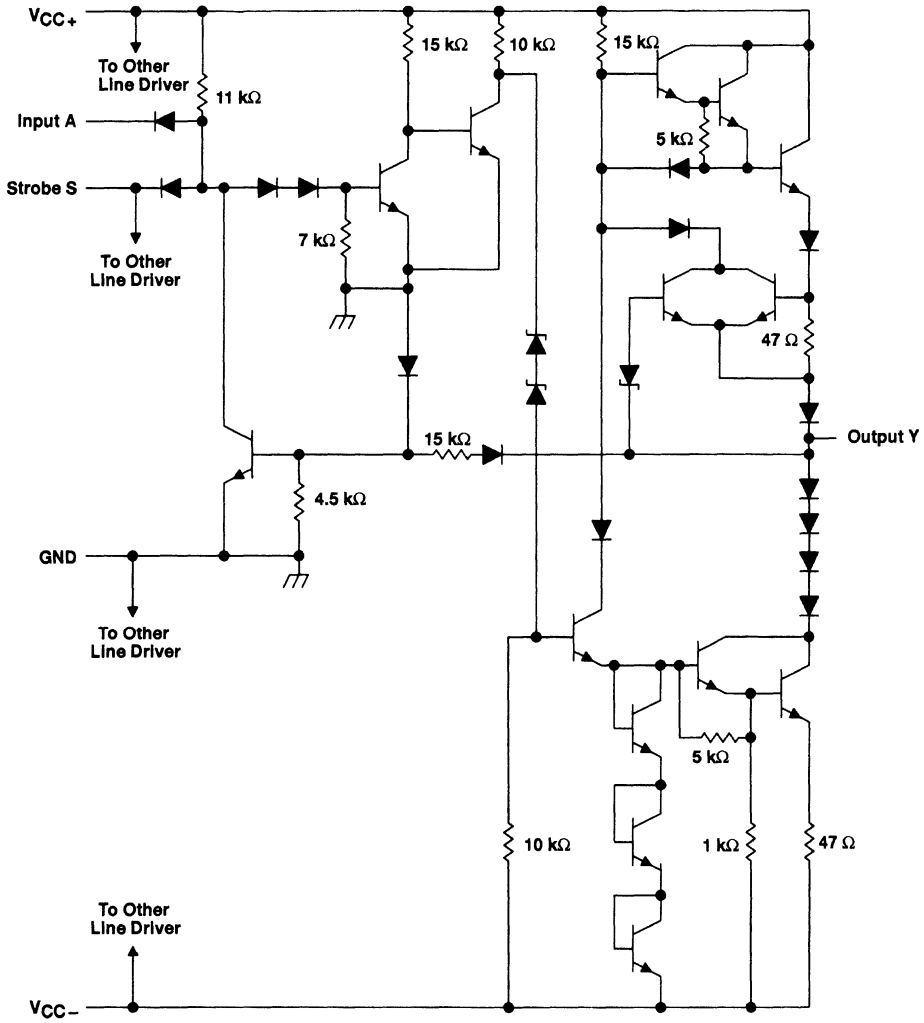


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic (each line driver)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) ..... 15 V
Supply voltage, V_{CC-} ..... −15 V
Input voltage, V_I ..... 15 V
Applied output voltage ..... ±25 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	10.8	12	13.2	V
Supply voltage, V_{CC-}	−10.8	−12	−13.2	V
High-level input voltage, V_{IH}	2		5.5	V
Low-level input voltage, V_{IL}	0		0.8	V
Driver output voltage, V_O			±15	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range, $V_{CC\pm}$ = ±13.2 V (unless otherwise noted)

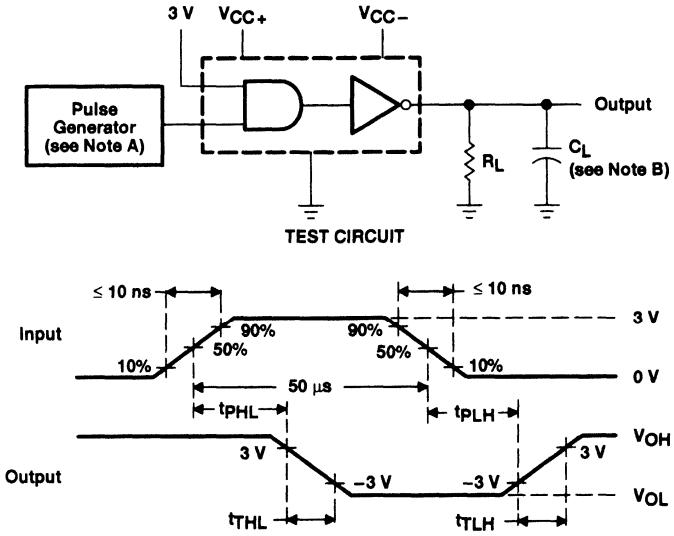
PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{CC+} = 10.8 V, V_{IL} = 0.8 V,	V_{CC-} = −10.8 V, R_L = 3 kΩ to 7 kΩ	5	8		V
V_{OL}	Low-level output voltage (see Note 2)		V_{CC+} = 10.8 V, V_{IH} = 2 V,	V_{CC-} = −10.8 V, R_L = 3 kΩ to 7 kΩ		−8	−5	V
I_{IH}	High-level input current	Data input	V_I = 2.4 V			1	10	μA
		Strobe input				2	20	
I_{IL}	Low-level input current	Data input	V_I = 0.4 V			−1	−1.6	mA
		Strobe input				−2	−3.2	
I_{OS}	Short-circuit output current‡		V_O = 25 V			2	8	mA
			V_O = −25 V			−3	−8	
			V_O = 0,	V_I = 3 V	10	15	30	
			V_O = 0,	V_I = 0	−10	−15	−30	
I_{CCH+}	Supply current from V_{CC+}, high-level output		V_I = 0, T_A = 25°C	R_L = 3 kΩ,		10	22	mA
I_{CCH-}	Supply current from V_{CC-}, high-level output					−1	−10	
I_{CCL+}	Supply current from V_{CC+}, low-level output		V_I = 3 V, T_A = 25°C	R_L = 3 kΩ,		8	17	mA
I_{CCL-}	Supply current from V_{CC-}, low-level output					−9	−20	

† All typical values are at V_{CC+} = 12 V, V_{CC-} = −12 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time.
NOTE 2: The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic levels only, e.g., when −5 V is the maximum, the typical value is a more negative voltage.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −12 V, T_A = 25°C (see Figure 1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{TLH}	Transition time, low-to-high-level output	C_L = 2500 pF,	R_L = 3 kΩ to 7 kΩ	0.2	1.4	2	μs
t_{THL}	Transition time, high-to-low-level output			0.2	1.5	2	μs
t_{TLH}	Transition time, low-to-high-level output	C_L = 15 pF,	R_L = 7 kΩ		40		ns
t_{THL}	Transition time, high-to-low-level output				20		ns
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF,	R_L = 7 kΩ		60		ns
t_{PHL}	Propagation delay time, high-to-low-level output				45		ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 50%, $Z_O \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT CURRENT vs APPLIED OUTPUT VOLTAGE

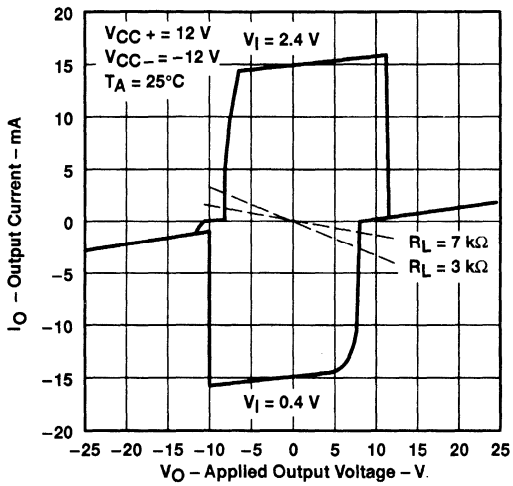


Figure 2

APPLICATION INFORMATION

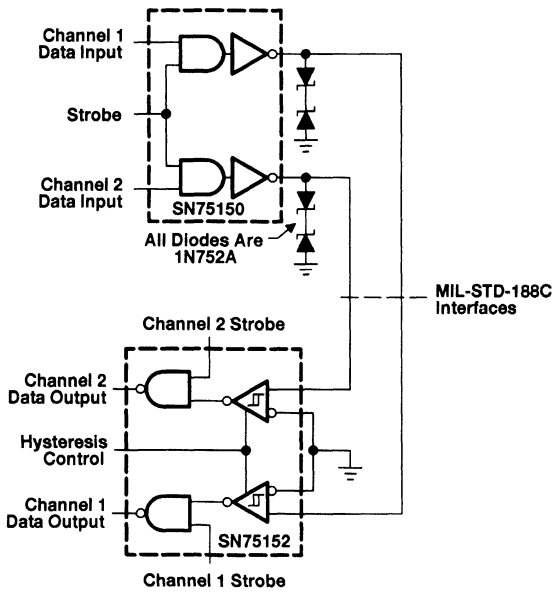
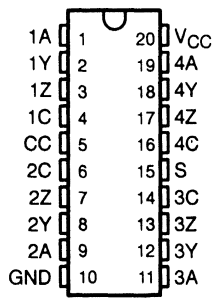


Figure 3. Dual-Channel Single-Ended Interface Circuit Meeting MIL-STD-188C, Paragraph 7.2.

SLLS082B – DECEMBER 1978 – REVISED MAY 1995

- **Meets or Exceeds the Requirement of ANSI EIA/TIA-422-B**
- **High-Impedance Output State for Party-Line Operation**
- **High Output Impedance in Power-Off Condition**
- **Low Input Current to Minimize Loading**
- **Single 5-V Supply**
- **40-mA Sink- and Source-Current Capability**
- **High-Speed Schottky Circuitry**
- **Low Power Requirements**

DW OR N PACKAGE
(TOP VIEW)



description

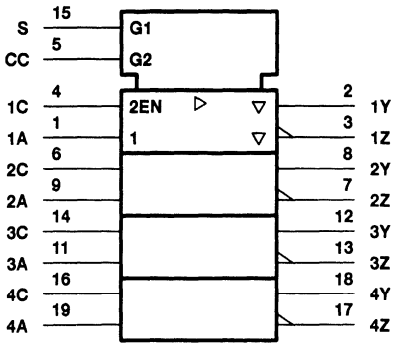
This line driver is designed to provide differential signals with high current capability on balanced lines. This circuit provides strobe and enable inputs to control all four drivers and provides an additional enable input for each driver. The output circuits have active pullup and pulldown resistors and are capable of sinking or sourcing 40 mA.

The SN75151 meets all requirements of ANSI EIA/TIA-422-B and Federal Standard 1020. The SN75151 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

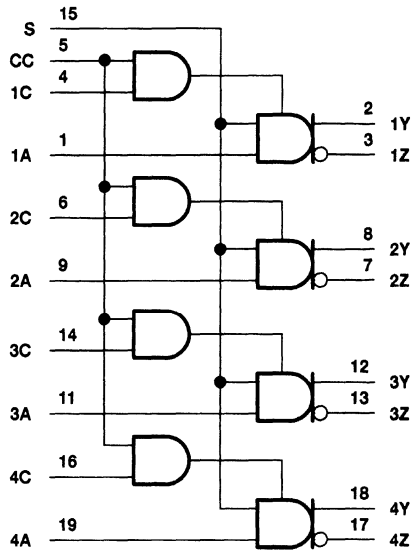
INPUTS				OUTPUTS	
ENABLE CC	ENABLE C	STROBE S	DATA A	Y	Z
L	X	X	X	Z	Z
X	L	X	X	Z	Z
H	H	L	X	L	H
H	H	X	L	L	H
H	H	H	H	H	L

logic symbol†

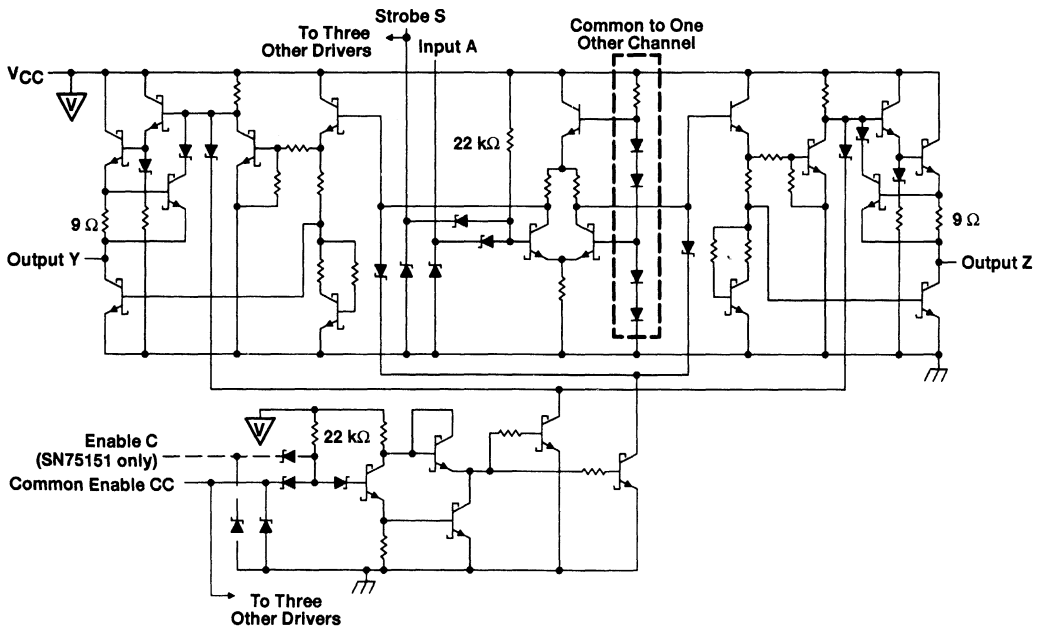


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 5.5 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential output voltage V_{OD}, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Common-mode output voltage, V_{OC}	−0.25		6	V
High-level output current, I_{OH}			−40	mA
Low-level output current, I_{OL}			40	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA	CC, S			−2	V
			All others		−0.9	−1.5	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OH} = −20 mA	2.5			V
			I_{OH} = −40 mA	2.4			
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V, I_{OL} = 40 mA				0.5	V
$\|V_{OD1}\|$	Differential output voltage	V_{CC} = MAX, I_O = 0			3.4	$2V_{OD2}$	V
$\|V_{OD2}\|$	Differential output voltage	V_{CC} = MIN	R_L = 100 Ω, See Figure 1	2	2.8		V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage§	V_{CC} = MIN			±0.01	±0.4	V
V_{OC}	Common-mode output voltage¶	V_{CC} = MAX			1.8	3	V
		V_{CC} = MIN			1.6	3	
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage§	V_{CC} = MIN or MAX			±0.02	±0.4	V
I_{OZ}	Off-state (high-impedance-state) output current	V_{CC} = MAX, Enable at 0.8 V	V_O = 0.5 V			−20	µA
			V_O = 2.5 V			20	
			V_O = V_{CC}			20	
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V		0.1	100	µA
			V_O = −0.25 V		−0.1	−100	
			V_O = −0.25 V to 6 V			±100	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V	C(SN75151), A			20	µA
			CC, S			80	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V	C(SN75151), A			−0.36	mA
			CC, S			−1.6	
I_{OS}	Short-circuit output current#	V_{CC} = MAX		−50	−90	−150	mA
I_{CC}	Supply current (both drivers)	V_{CC} = MAX, No load	Outputs disabled		30	60	mA
			Outputs enabled		60	80	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at T_A = 25°C and V_{CC} = 5 V except for V_{OC}, for which V_{CC} is as stated under test conditions.
§ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitudes of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
¶ In ANSI Standard EIA/TIA-422-B, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
# Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 30 pF, Termination A,	R_L = 100 Ω, See Figure 2		15	30	ns
t_{PHL}	Propagation delay time, high- to low-level output				15	30	ns
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 30 pF, See Figure 2	Termination B,		13	25	ns
t_{PHL}	Propagation delay time, high- to low-level output				13	25	ns
t_{TLH}	Transition time, low- to high-level output	C_L = 30 pF, Termination A,	R_L = 100 Ω, See Figure 2		12	20	ns
t_{THL}	Transition time, high- to low-level output				12	20	ns
t_{PZH}	Output enable time to high level	C_L = 30 pF, See Figure 3	R_L = 60 Ω,		18	35	ns
t_{PZL}	Output enable time to low level	C_L = 30 pF, See Figure 4	R_L = 111 Ω,		20	35	ns
t_{PHZ}	Output disable time from high level	C_L = 30 pF, See Figure 3	R_L = 60 Ω,		19	30	ns
t_{PLZ}	Output disable time from low level	C_L = 30 pF, See Figure 4	R_L = 111 Ω,		13	30	ns
	Overshoot factor	R_L = 100 Ω, See Figure 2	Termination C,			10	%

† All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

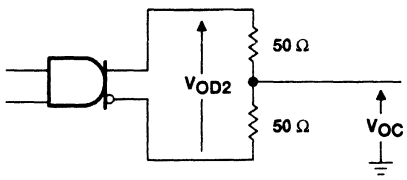
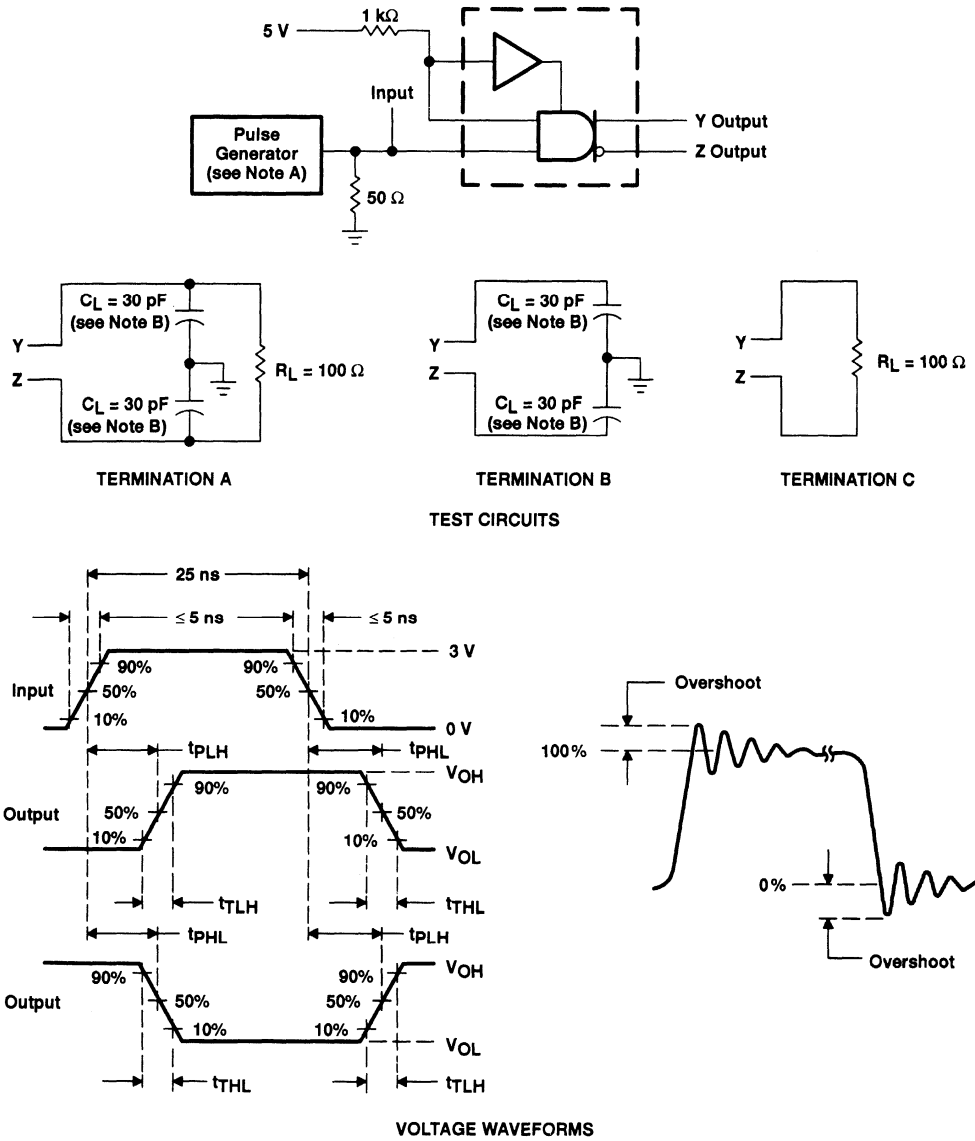


Figure 1. Differential and Common-Mode Output Voltages

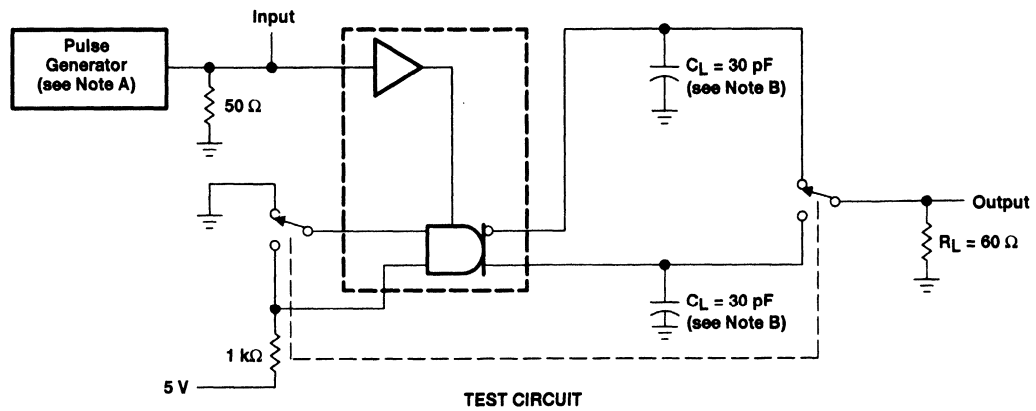
PARAMETER MEASUREMENT INFORMATION



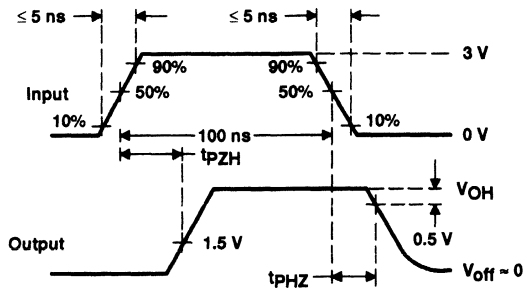
NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, PRR ≤ 10 MHz.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuits, Voltage Waveforms, and Overshoot Factor

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

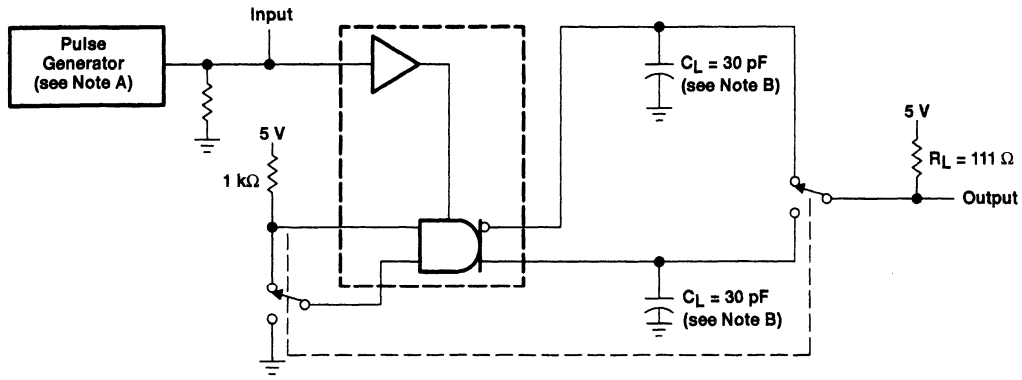


VOLTAGE WAVEFORMS

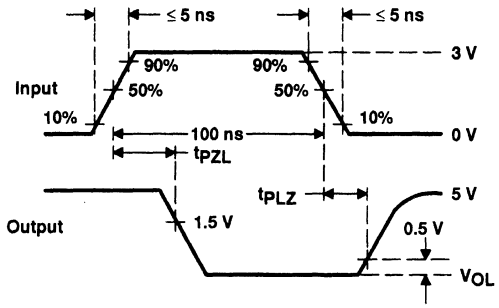
NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, PRR ≤ 500 kHz.
B. C_L includes probe and jig capacitance.

Figure 3. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_O = 50 Ω, PRR ≤ 500 kHz.
B. C_L includes probe and jig capacitance.

Figure 4. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

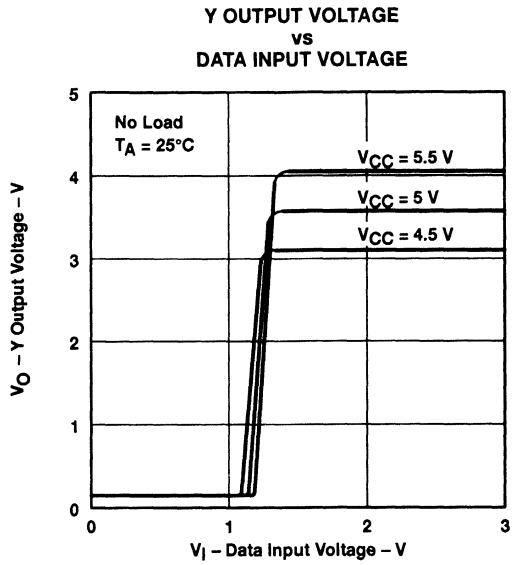
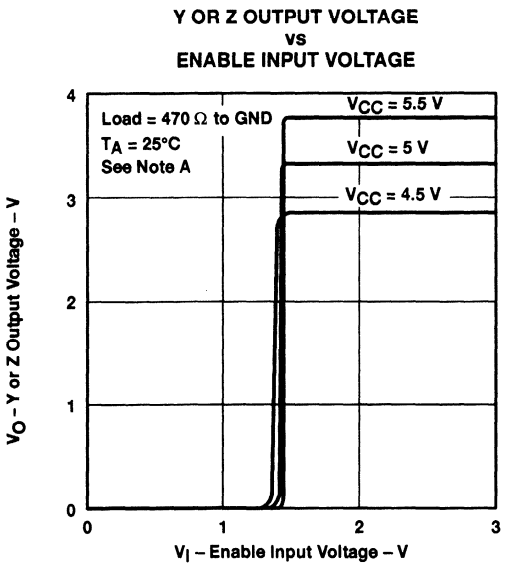
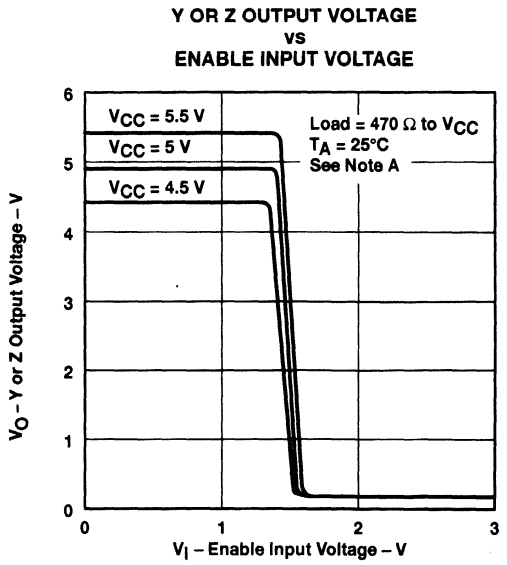


Figure 5



NOTE A: The A input is connected to V_{CC} during the testing of the Y outputs and to ground during testing of the Z outputs.

Figure 6



NOTE A: The A input is connected to GND during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

Figure 7

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

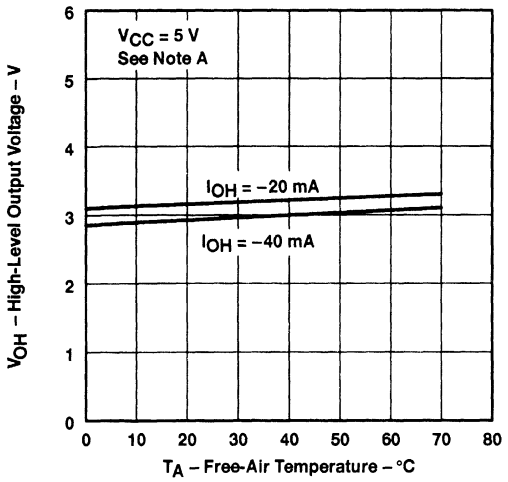


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

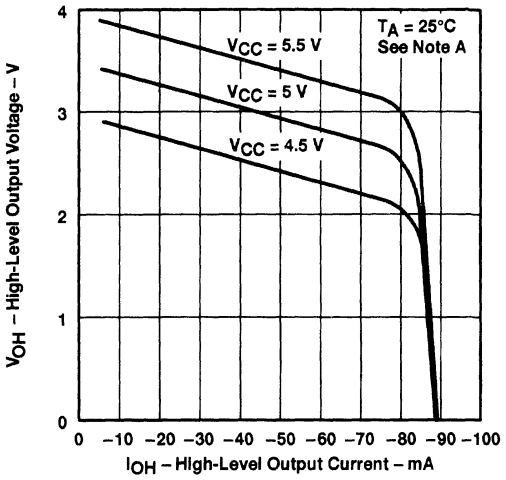


Figure 9

NOTE A: The A input is connected to V_{CC} during the testing of the Y outputs and to ground during testing of the Z outputs.

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

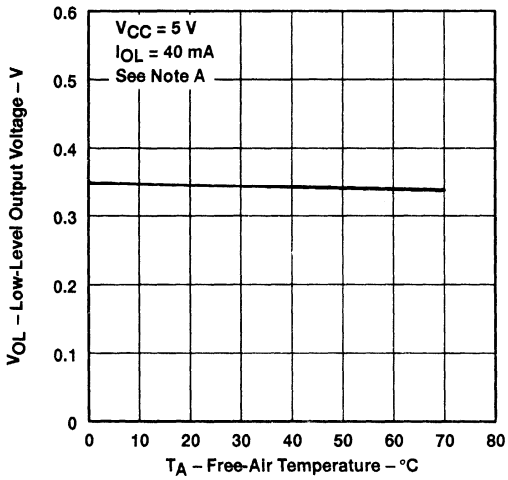


Figure 10

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

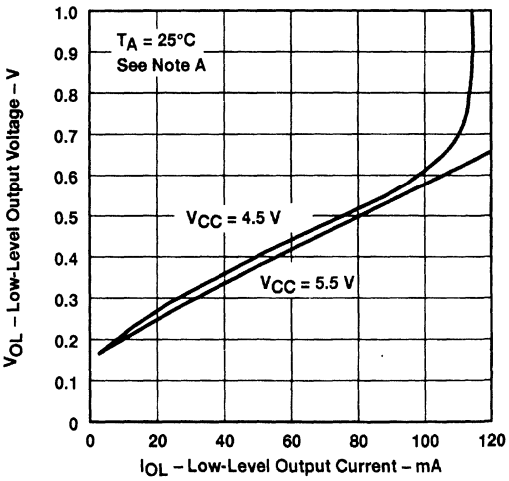


Figure 11

NOTE A: The A input is connected to GND during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

TYPICAL CHARACTERISTICS

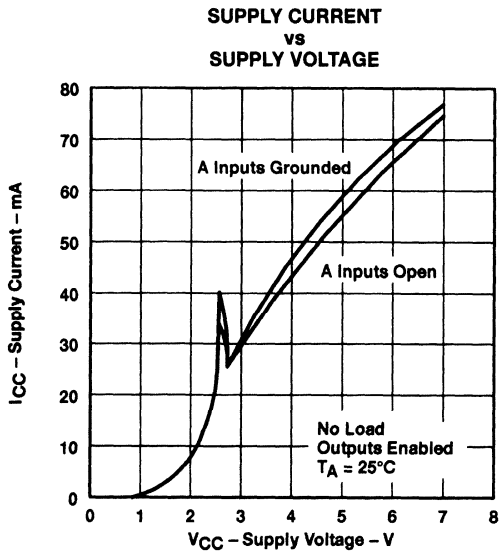


Figure 12

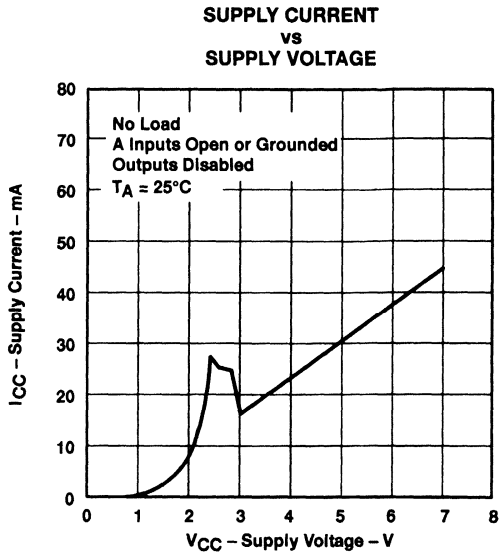
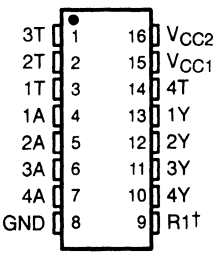


Figure 13

SLLS083B – NOVEMBER 1970 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of ANSI Standard EIA/TIA-232-E and ITU Recommendation V.28**
- **Input Resistance . . . 3 kΩ to 7 kΩ Over Full EIA/TIA-232-E Voltage Range**
- **Input Threshold Adjustable to Meet Fail-Safe Requirements Without Using External Components**
- **Built-In Hysteresis for Increased Noise Immunity**
- **Inverting Output Compatible With TTL**
- **Output With Active Pullup for Symmetrical Switching Speeds**
- **Standard Supply Voltages . . . 5 V or 12 V**

D OR N PACKAGE
(TOP VIEW)



† For function of R1, see schematic

description

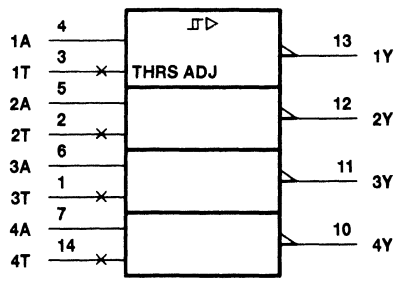
The SN75154 is a monolithic low-power Schottky line receiver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by ANSI Standard EIA/TIA-232-E. Other applications are for relatively short, single-line, point-to-point data transmission and for level translators. Operation is normally from a single 5-V supply; however, a built-in option allows operation from a 12-V supply without the use of additional components. The output is compatible with most TTL circuits when either supply voltage is used.

In normal operation, the threshold-control terminals are connected to the V_{CC1} terminal, even if power is being supplied via the alternate V_{CC2} terminal. This provides a wide hysteresis loop, which is the difference between the positive-going and negative-going threshold voltages. See typical characteristics. In this mode of operation, if the input voltage goes to zero, the output voltage will remain at the low or high level as determined by the previous input.

For fail-safe operation, the threshold-control terminals are open. This reduces the hysteresis loop by causing the negative-going threshold voltage to be above zero. The positive-going threshold voltage remains above zero as it is unaffected by the disposition of the threshold terminals. In the fail-safe mode, if the input voltage goes to zero or an open-circuit condition, the output will go to the high level regardless of the previous input condition.

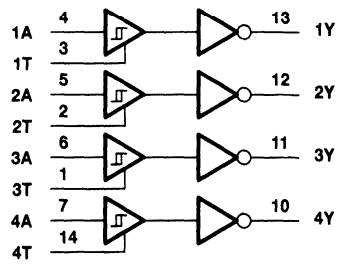
The SN75154 is characterized for operation from 0°C to 70°C.

logic symbol‡

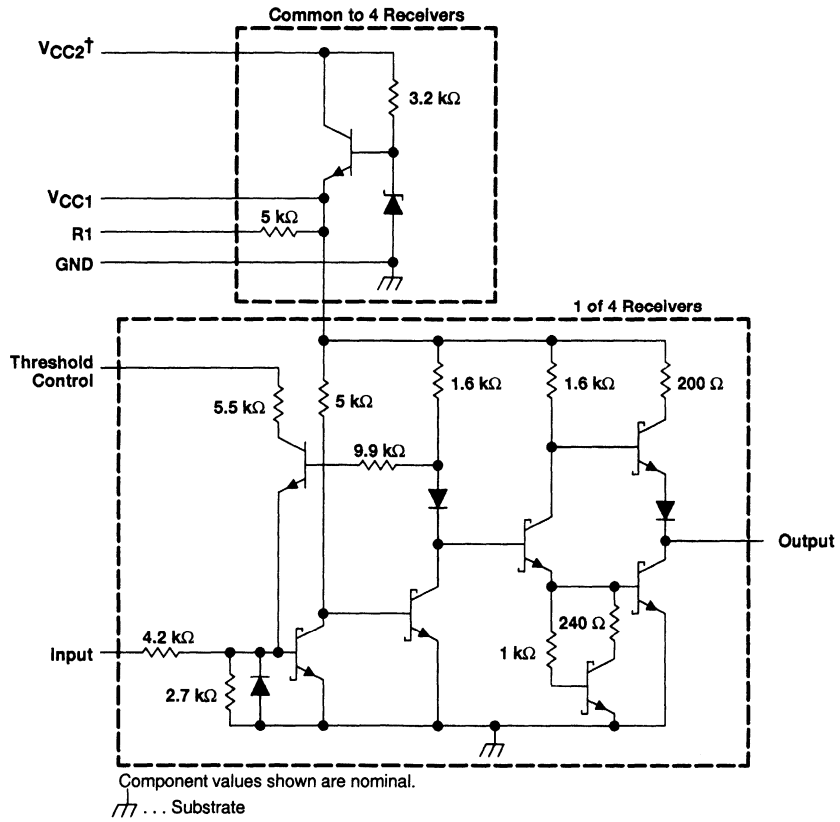


‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematic



† When V_{CC1} is used, V_{CC2} may be left open or shorted to V_{CC1}. When V_{CC2} is used, V_{CC1} must be left open or connected to the threshold control pins.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Normal supply voltage, V_{CC1} (see Note 1) ..... 7 V
Alternate supply voltage, V_{CC2} ..... 14 V
Input voltage, V_I ..... ±25 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to network GND terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW
NS	625 mW	5.0 mW/°C	400 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Normal supply voltage, V_{CC1}	4.5	5	5.5	V
Alternate supply voltage, V_{CC2}	10.8	12	13.2	V
High-level input voltage, V_{IH} (see Note 2)	3		15	V
Low-level input voltage, V_{IL} (see Note 2)	−15		−3	V
High-level output current, I_{OH}			−400	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

NOTE 2: The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic and threshold levels only, e.g., when 0 V is the maximum, the minimum limit is a more negative voltage.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

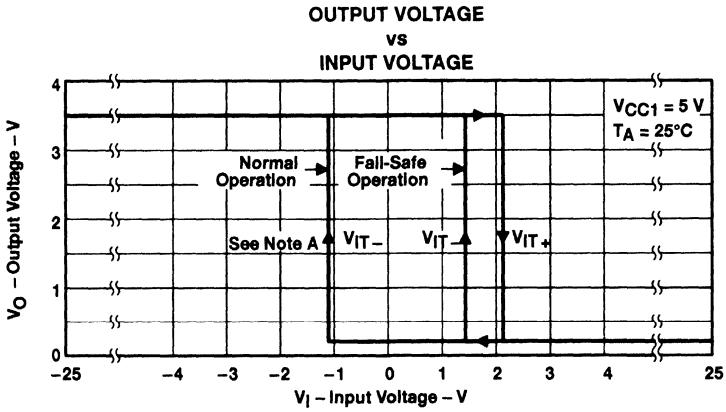
PARAMETER			TEST FIGURE	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	Normal operation	1		0.8	2.2	3	V
		Fail-safe operation			0.8	2.2	3	
V_{IT-}	Negative-going input threshold voltage	Normal operation	1		−3	−1.1	0	V
		Fail-safe operation			0.8	1.4	3	
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)	Normal operation	1		0.8	3.3	6	V
		Fail-safe operation			0	0.8	2.2	
V_{OH}	High-level output voltage		1	I_{OH} = −400 μA	2.4	3.5		V
V_{OL}	Low-level output voltage		1	I_{OL} = 16 mA		0.29	0.4	V
r_i	Input resistance		2	ΔV_I = −25 V to −14 V	3	5	7	kΩ
				ΔV_I = −14 V to −3 V	3	5	7	
				ΔV_I = −3 V to 3 V	3	6	8	
				ΔV_I = 3 V to 14 V	3	5	7	
				ΔV_I = 14 V to 25 V	3	5	7	
$V_{I(open)}$	Open-circuit input voltage		3	I_I = 0	0	0.2	2	V
I_{OS}	Short-circuit output current‡		4	V_{CC1} = 5.5 V, V_I = −5 V	−10	−20	−40	mA
I_{CC1}	Supply current from V_{CC1}		5	V_{CC1} = 5.5 V, T_A = 25°C		20	35	mA
I_{CC2}	Supply current from V_{CC2}			V_{CC2} = 13.2 V, T_A = 25°C		23	40	

† All typical values are at V_{CC1} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time.

switching characteristics, V_{CC1} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	6	C_L = 50 pF, R_L = 390 Ω		11		ns
t_{PHL}	Propagation delay time, high- to low-level output				8		ns
t_{TLH}	Transition time, low- to high-level output				7		ns
t_{THL}	Transition time, high- to low-level output				2.2		ns

TYPICAL CHARACTERISTICS



NOTE A: For normal operation, the threshold controls are connected to V_{CC1}. For fail-safe operation, the threshold controls are open.

Figure 1

PARAMETER MEASUREMENT INFORMATION

dc test circuits†

TEST TABLE

TEST	MEASURE	A	T	Y	V_{CC1}	V_{CC2}
Open-circuit input (fail safe)	V_{OH}	Open	Open	I_{OH}	4.5 V	Open
	V_{OH}	Open	Open	I_{OH}	Open	10.8 V
V_{IT+} min, V_{IT-} min (fail safe)	V_{OH}	0.8 V	Open	I_{OH}	5.5 V	Open
	V_{OH}	0.8 V	Open	I_{OH}	Open	13.2 V
V_{IT+} min (normal)	V_{OH}	Note A	V_{CC1}	I_{OH}	5.5 V and T	Open
	V_{OH}	Note A	V_{CC1}	I_{OH}	T	13.2 V
V_{IL} max, V_{IT+} min (normal)	V_{OH}	−3 V	V_{CC1}	I_{OH}	5.5 V and T	Open
	V_{OH}	−3 V	V_{CC1}	I_{OH}	T	13.2 V
V_{IH} min, V_{IT+} max, V_{IT-} max (fail safe)	V_{OL}	3 V	Open	I_{OL}	4.5 V	Open
	V_{OL}	3 V	Open	I_{OL}	Open	10.8 V
V_{IH} min, V_{IT+} max (normal)	V_{OL}	3 V	V_{CC1}	I_{OL}	4.5 V and T	Open
	V_{OL}	3 V	V_{CC1}	I_{OL}	T	10.8 V
V_{IT-} max (normal)	V_{OL}	Note B	V_{CC1}	I_{OL}	5.5 V and T	Open
	V_{OL}	Note B	V_{CC1}	I_{OL}	T	13.2 V

NOTES: A. Momentarily apply −5 V, then 0.8 V.
B. Momentarily apply 5 V, then GND.

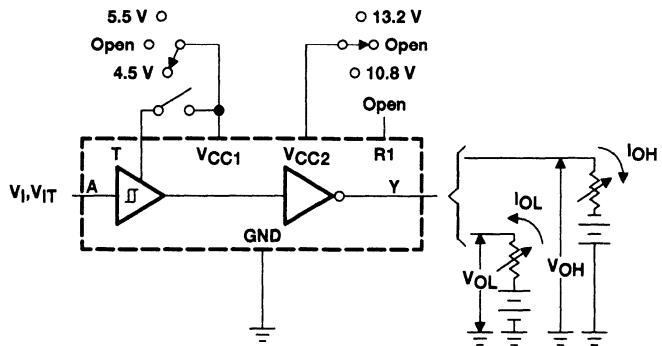
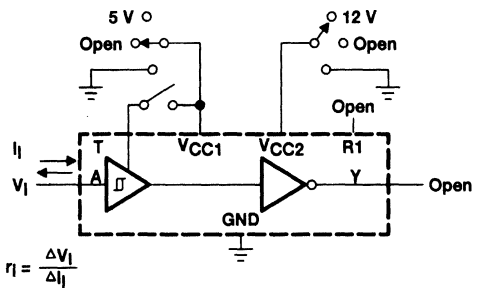


Figure 2. V_{IH}, V_{IL}, V_{IT+}, V_{IT-}, V_{OH}, V_{OL}

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

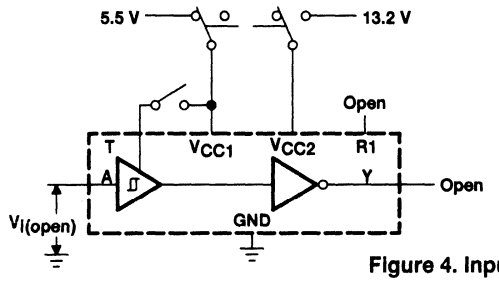
dc test circuits† (continued)



TEST TABLE

T	V_{CC1}	V_{CC2}
Open	5 V	Open
Open	GND	Open
Open	Open	Open
V_{CC1}	T and 5 V	Open
GND	GND	Open
Open	Open	12 V
Open	Open	GND
V_{CC1}	T	12 V
V_{CC1}	T	GND
V_{CC1}	T	Open

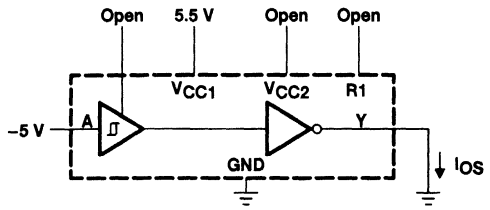
Figure 3. Input Resistance



TEST TABLE

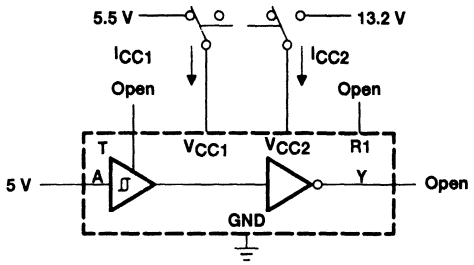
T	V_{CC1}	V_{CC2}
Open	5.5 V	Open
V_{CC1}	5.5 V	Open
Open	Open	13.2 V
V_{CC1}	T	13.2 V

Figure 4. Input Voltage (Open)



Each output is tested separately.

Figure 5. Output Short-Circuit Current

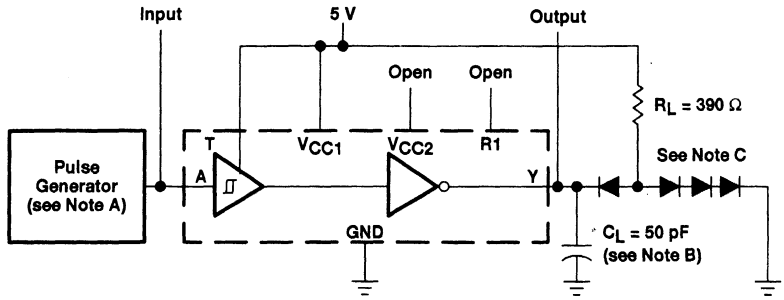


All four line receivers are tested simultaneously.

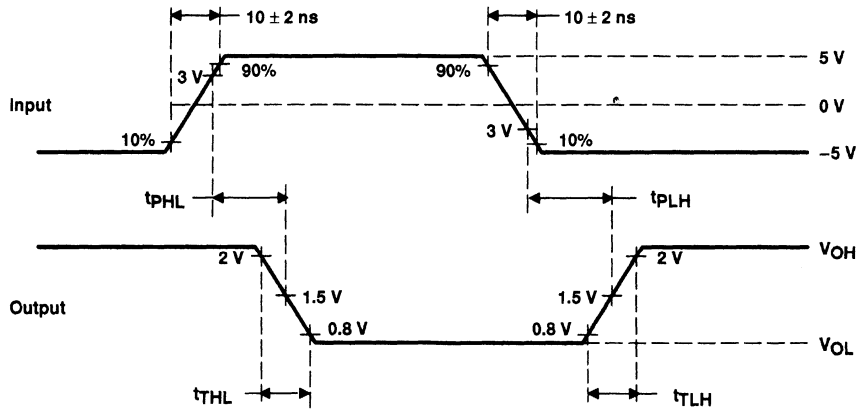
Figure 6. Supply Current

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, $t_W \leq 200$ ns, duty cycle ≤ 20%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

Figure 6. Test Circuit and Voltage Waveforms

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

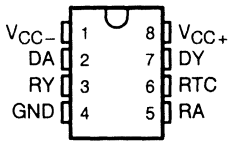
- **Meets or Exceeds the Requirements of ANSI EIA/TIA-232-E and ITU Recommendation V.28**
- **10-mA Current Limited Output**
- **Wide Range of Supply Voltage**
  V_{CC} = 4.5 V to 15 V
- **Low Power . . . 130 mW**
- **Built-In 5-V Regulator**
- **Response Control Provides:**
  Input Threshold Shifting
  Input Noise Filtering
- **Power-Off Output Resistance . . . 300 Ω Typ**
- **Driver Input TTL Compatible**

description

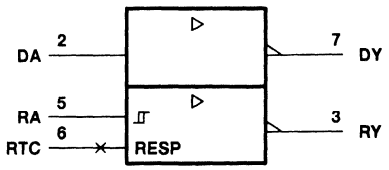
The SN75155 monolithic line driver and receiver is designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by ANSI EIA/TIA-232-E. A response control input is provided for the receiver. A resistor or a resistor and a bias voltage can be connected between the response control input and ground to provide noise filtering. The driver used is similar to the SN75188. The receiver used is similar to the SN75189A.

The SN75155 is characterized for operation from 0°C to 70°C.

D OR P PACKAGE
TOP VIEW

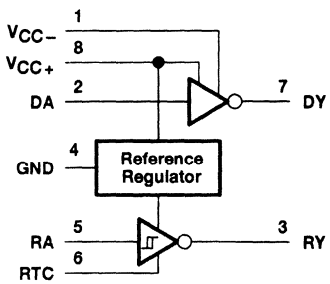


logic symbol†

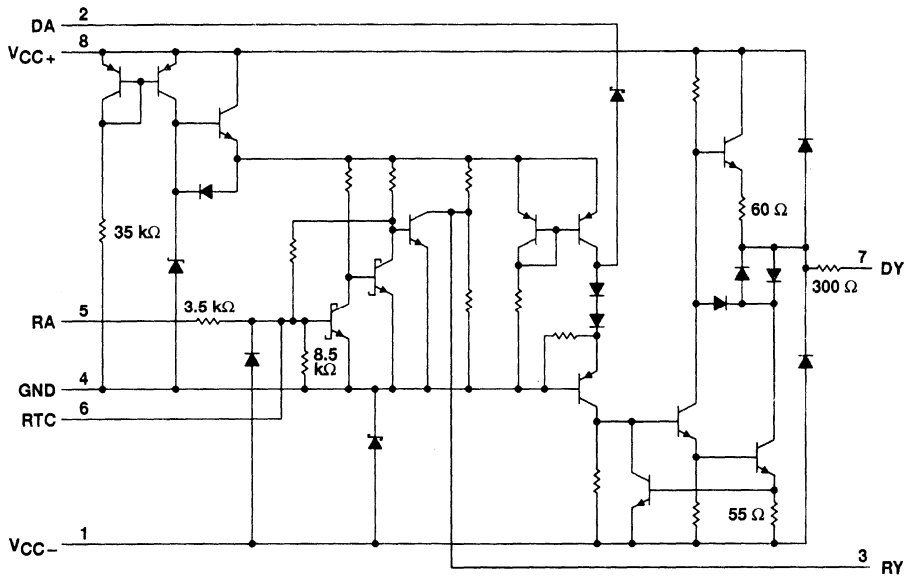


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

logic diagram



schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) ..... 15 V
Supply voltage, V_{CC-} (see Note 1) ..... −15 V
Input voltage range, V_I: Driver ..... −15 V to 15 V
Receiver ..... −30 V to 30 V
Output voltage range (driver), V_O ..... −15 V to 15 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	4.5	12	15	V
Supply voltage, V_{CC-}	−4.5	−12	−15	V
Output voltage, driver, $V_{O(D)}$			±15	V
Input voltage, receiver, $V_{I(R)}$	−25		25	V
High-level input voltage, driver, V_{IH}	2			V
Low-level input voltage, driver, V_{IL}			0.8	V
Response control current			±5.5	mA
Output current, receiver, $I_{O(R)}$			24	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

total device

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
I_{CCH+}	High-level supply current	V_{CC+} = 5 V,	V_{CC-} = −5 V	$V_{I(D)}$ = 2 V, $V_{I(R)}$ = 2.3 V, Output open		6.3	8.1	mA
		V_{CC+} = 9 V,	V_{CC-} = −9 V			9.1	11.9	
		V_{CC+} = 12 V,	V_{CC-} = −12 V			10.4	14	
I_{CCL+}	Low-level supply current	V_{CC+} = 5 V,	V_{CC-} = −5 V	$V_{I(D)}$ = 0.8 V, $V_{I(R)}$ = 0.6 V, Output open		2.5	3.4	mA
		V_{CC+} = 9 V,	V_{CC-} = −9 V			3.7	5.1	
		V_{CC+} = 12V,	V_{CC-} = −12 V			4.1	5.6	
I_{CC+}	Supply current	V_{CC+} = 5 V,	V_{CC-} = 0	$V_{I(R)}$ = 2.3 V, $V_{I(D)}$ = 0		4.8	6.4	mA
		V_{CC+} = 9 V,	V_{CC-} = 0			6.7	9.1	
I_{CCH-}	High-level supply current	V_{CC+} = 5 V,	V_{CC-} = −5 V	$V_{I(D)}$ = 2 V, $V_{I(R)}$ = 2.3 V Output open		−2.4	−3.1	mA
		V_{CC+} = 9 V,	V_{CC-} = −9 V			−3.9	−4.9	
		V_{CC+} = 12 V,	V_{CC-} = −12 V			−4.8	−6.1	
I_{CCL-}	Low-level supply current	V_{CC+} = 5 V,	V_{CC-} = −5 V	$V_{I(D)}$ = 0.8 V, $V_{I(R)}$ = 0.6 V, Output open		−0.2	−0.35	mA
		V_{CC+} = 9 V,	V_{CC-} = −9 V			−0.25	−0.4	
		V_{CC+} = 12 V,	V_{CC-} = −12 V			−0.27	−0.45	

† All typical values are at T_A = 25°C.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 12 V, V_{CC-} = −12 V (unless otherwise noted)

driver section

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{IL} = 0.8 V, R_L = 3 kΩ	V_{CC+} = 5 V,	V_{CC-} = −5 V	3.2	3.7		V
			V_{CC+} = 9 V,	V_{CC-} = −9 V	6.5	7.2		
			V_{CC+} = 12 V,	V_{CC-} = −12 V	8.9	9.8		
V_{OL}	Low-level output voltage (see Note 2)	V_{IH} = 2 V, R_L = 3 kΩ	V_{CC+} = 5 V,	V_{CC-} = −5 V		−3.6	−3.2	V
			V_{CC+} = 9 V,	V_{CC-} = −9 V		−7.1	−6.4	
			V_{CC+} = 12 V,	V_{CC-} = −12 V		−9.7	−8.8	
I_{IH}	High-level input current	V_I = 7 V					5	μA
I_{IL}	Low-level input current	V_I = 0				−0.73	−1.2	mA
$I_{OS(H)}$	High-level short-circuit output current	V_I = 0.8 V, V_O = 0			−7	−12	−14.5	mA
$I_{OS(L)}$	Low-level short-circuit output current	V_I = 2 V, V_O = 0			6.5	11.5	15	mA
r_O	Output resistance with power off	V_O = −2 V to 2 V				300		Ω

receiver section (see Figure 1)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshhold voltage				1.2	1.9	2.3	V
V_{IT-}	Negative-going input threshhold voltage				0.6	0.95	1.2	V
V_{hys}	Hystresis voltage ($V_{IT+} - V_{IT-}$)				0.6			V
$V_{O(H)}$	High-level output voltage	V_I = 0.6 V, I_{OH} = 10 μA	V_{CC+} = 5 V,	V_{CC-} = −5 V	3.7	4.1	4.5	V
			V_{CC+} = 12 V,	V_{CC-} = −12 V	4.4	4.7	5.2	
		V_I = 0.6 V, I_{OH} = 0.4 mA	V_{CC+} = 5 V,	V_{CC-} = −5 V	3.1	3.4	3.8	
			V_{CC+} = 12 V,	V_{CC-} = −12 V	3.6	4	4.5	
$V_{O(L)}$	Low-level output voltage	V_I = 2.3 V,	I_{OL} = 24 mA			0.2	0.3	V
I_{IH}	High-level input current	V_I = 2 5 V			3.6	6.7	10	mA
		V_I = 3 V			0.43	0.67	1	mA
I_{IL}	Low-level input current	V_I = −25 V			−3.6	−6.7	−10	mA
		V_I = −3 V			−0.43	−0.67	−1	mA
I_{OS}	Short-circuit output current	V_I = 0.6 V				−2.8	−3.7	mA

† All typical values are at T_A = 25°C.

NOTE 2: The algebraic limit system, in which the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic voltage levels only (e.g., if −8.8 V is the maximum, the typical value is a more negative value).

switching characteristics over recommended operating free-air temperature range, V_{CC+} = 5 V, V_{CC-} = −5 V, C_L = 50 pF (unless otherwise noted)

driver section (see Figure 2)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high level output	R_L = 3 kΩ		250	480	ns
t_{PHL}	Propagation delay time, high- to low level output			80	150	
t_r	Output rise time	R_L = 3 kΩ		67	180	ns
		R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF		2.4	3	µs
t_f	Output fall time	R_L = 3 kΩ		48	160	ns
		R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF		1.9	3	µs

receiver section (see Figure 3)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high level output	R_L = 400 Ω		175	245	ns
t_{PHL}	Propagation delay time, high- to low level output			37	100	
t_r	Output rise time	R_L = 400 Ω		255	360	ns
t_f	Output fall time	R_L = 400 Ω		23	50	ns

† All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

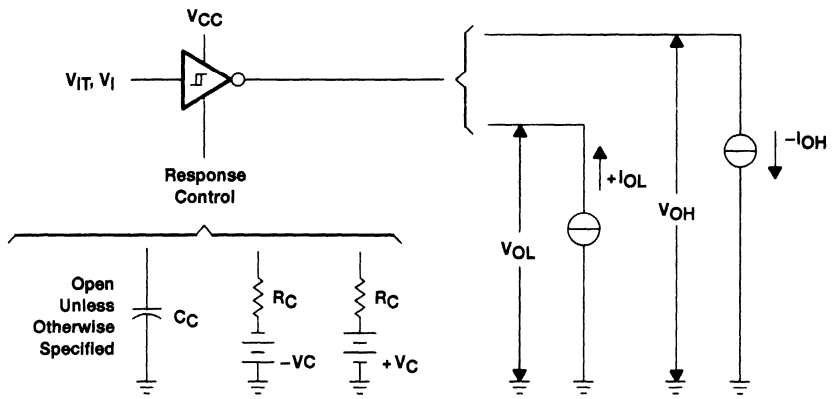


Figure 1. Receiver Section Test Circuit (V_{IT+}, V_{IT-}, V_{OH}, V_{OL})

PARAMETER MEASUREMENT INFORMATION

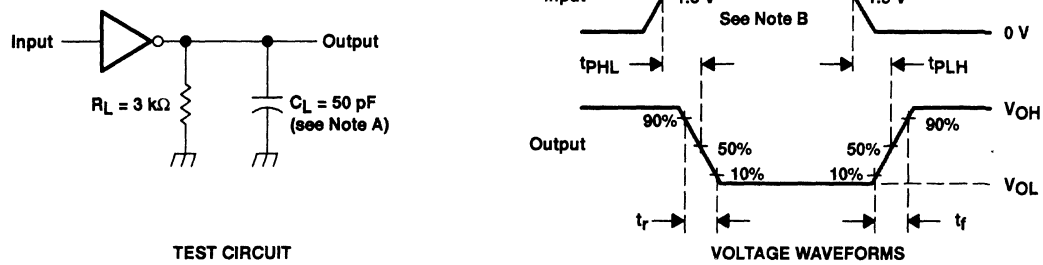


Figure 2. Driver Section Switching Test Circuit and Voltage Waveforms

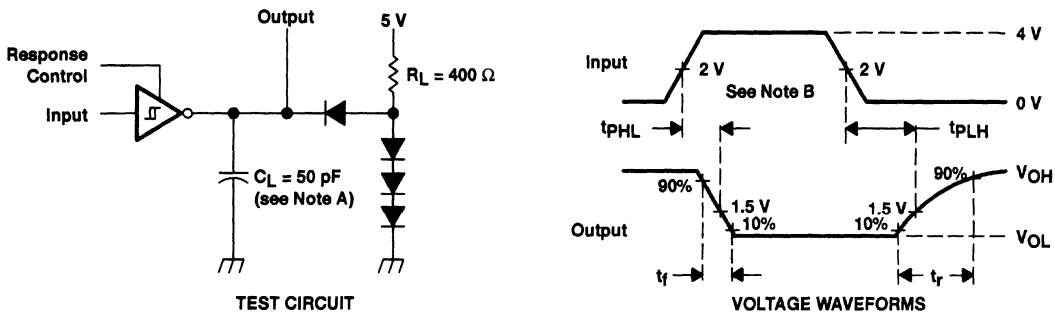


Figure 3. Receiver Section Switching Test Circuit and Voltage Waveforms

NOTES: A. C_L includes probe and jig capacitance.
B. The input waveform is supplied by a generator with the following characteristics: Z_O = 50 Ω, t_w = 1 μs, $t_r \le 10$ ns, $t_f \le 10$ ns.

TYPICAL CHARACTERISTICS

DRIVER
VOLTAGE TRANSFER CHARACTERISTICS

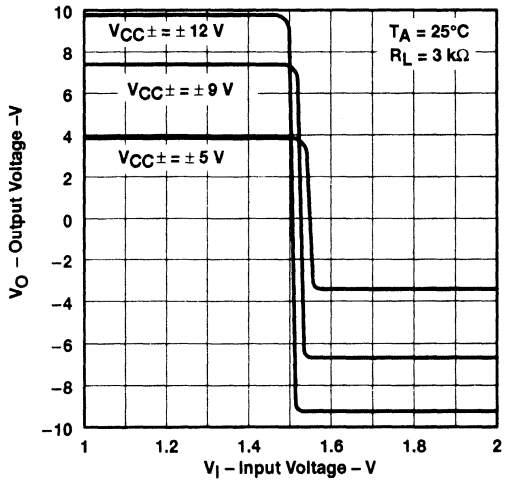


Figure 4

DRIVER
OUTPUT CURRENT
vs
OUTPUT VOLTAGE

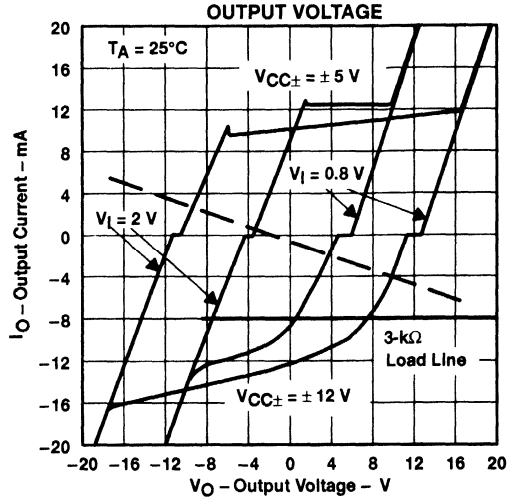


Figure 5

DRIVER
SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

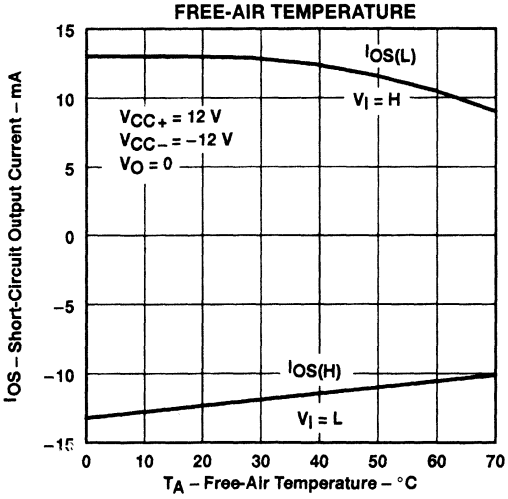


Figure 6

DRIVER
SLEW RATE
vs
LOAD CAPACITANCE

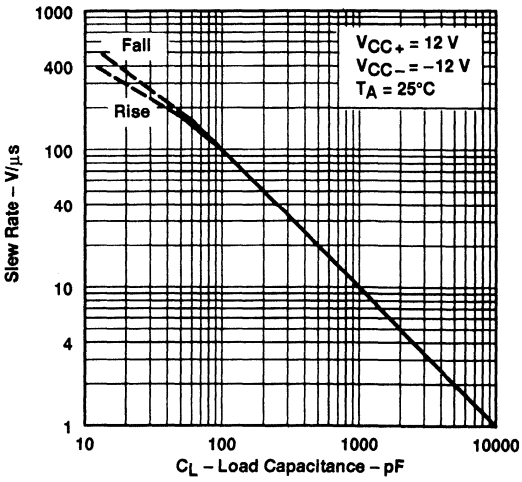


Figure 7

TYPICAL CHARACTERISTICS

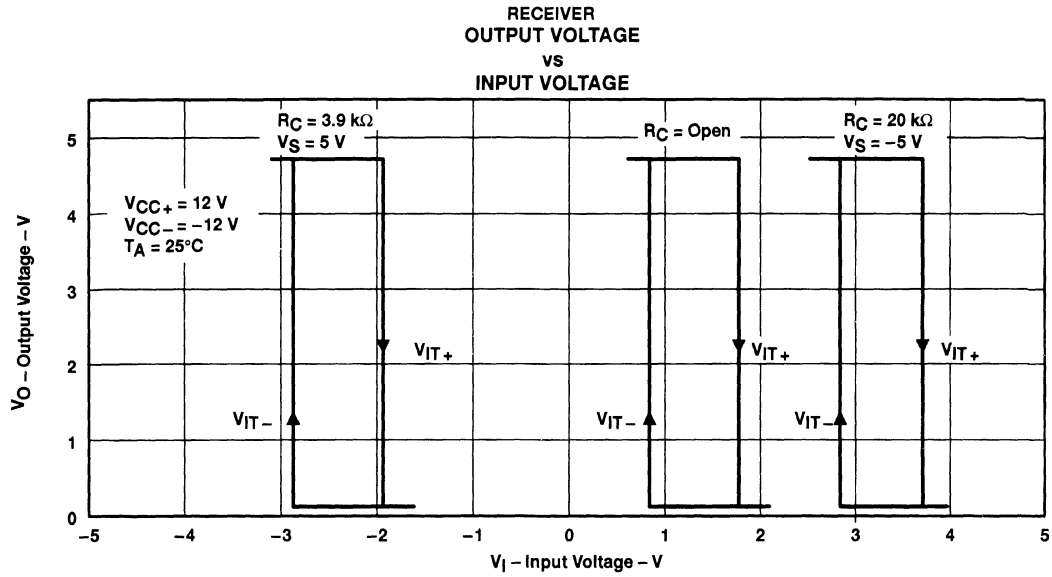


Figure 8

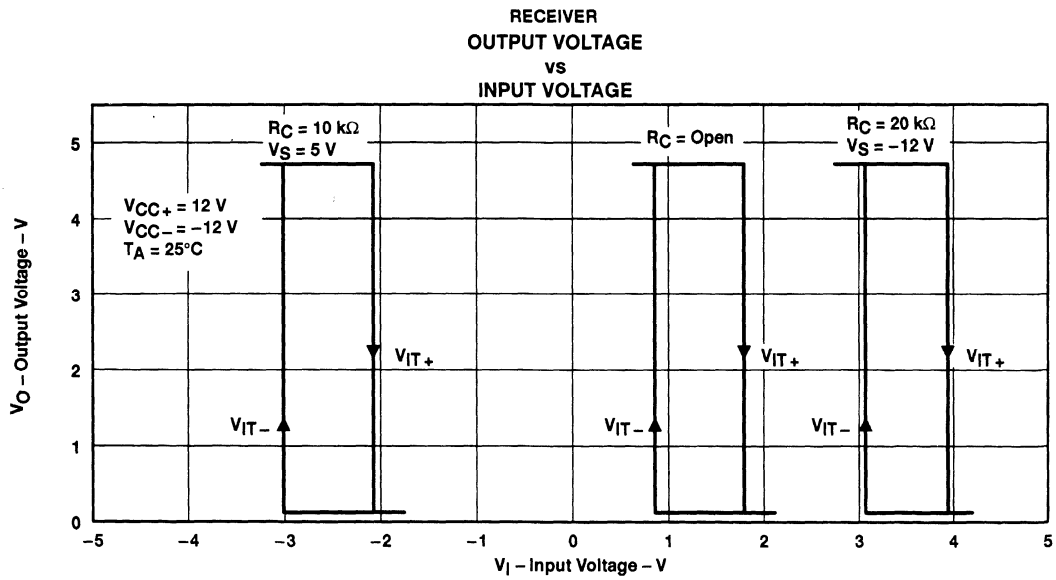


Figure 9

TYPICAL CHARACTERISTICS

RECEIVER
INPUT THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

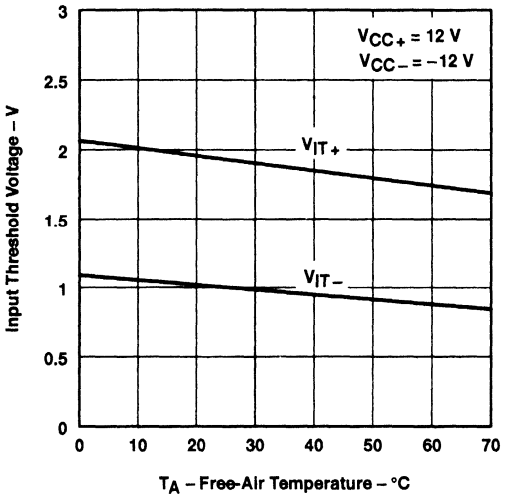


Figure 10

RECEIVER
INPUT CURRENT
vs
INPUT VOLTAGE

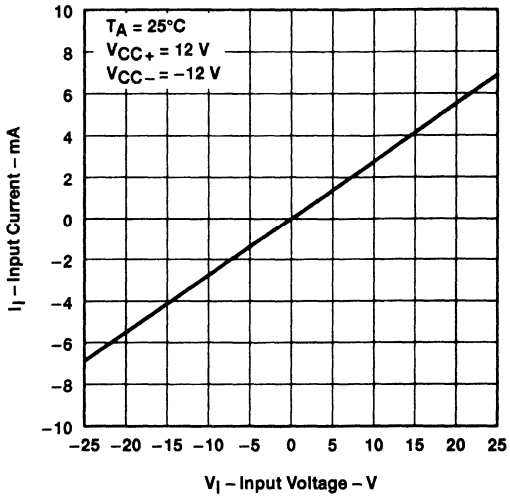


Figure 11

RECEIVER
NOISE REJECTION

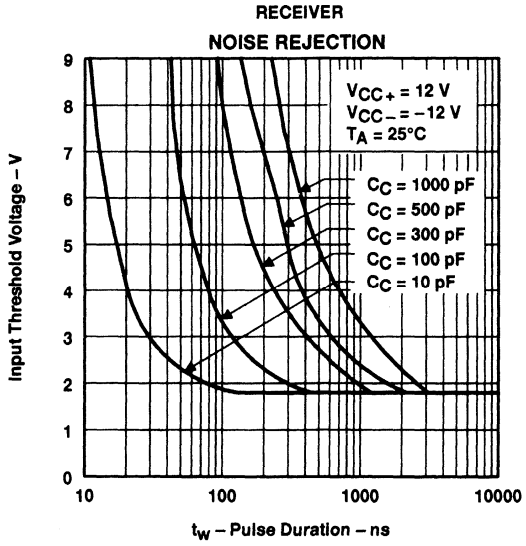
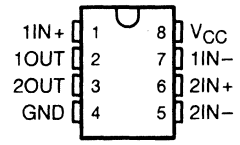


Figure 12

- **Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-422-B and EIA/TIA-423-B and ITU Recommendation V.10 and V.11**
- **Operates From Single 5-V Power Supply**
- **Wide Common-Mode Voltage Range**
- **High Input Impedance**
- **TTL-Compatible Outputs**
- **High-Speed Schottky Circuitry**
- **8-Pin Dual-In-Line Package**

D, P OR PS† PACKAGE
(TOP VIEW)



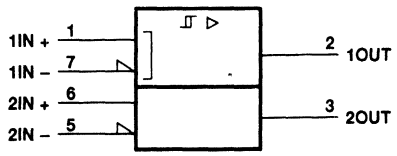
† The PS package is only available left-ended taped and reeled (order SN75157PSLE).

description

The SN75157 is a dual differential line receiver designed to meet Standards EIA/TIA-422-B and -423-B and ITU V.10 and V.11. It utilizes Schottky circuitry and has TTL-compatible outputs. The inputs are compatible with either a single-ended or a differential-line system. The device operates from a single 5-V power supply and is supplied in 8-pin dual-in-line and small-outline packages.

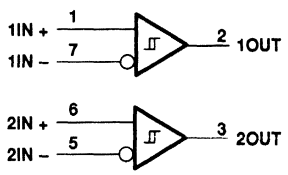
The SN75157 is characterized for operation from 0°C to 70°C.

logic symbol‡



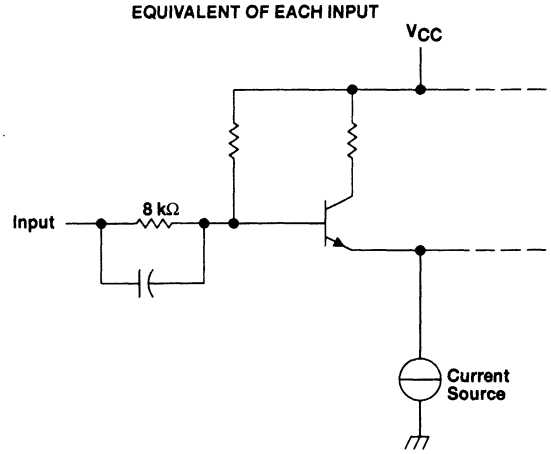
‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

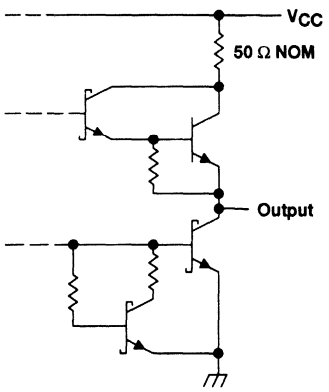


schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Input voltage, V_I ..... ±15 V
Differential input voltage, V_{ID} (see Note 2) ..... ±15 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to 5.5 V
Low-level output current, I_{OL} ..... 50 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW
PS	450 mW	3.6 mW/°C	288 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Operating free-air temperature, T_A	0	25	70	°C

electrical characteristics over recommended ranges of supply voltage, common-mode input voltage, and operating free-air temperature (unless otherwise noted)†

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IT}	Input threshold voltage (V_{IT+} and V_{IT-})			−0.2		0.2	V
		See Note 3		−0.4		0.4	
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)				70		mV
V_{OH}	High-level output voltage	V_{ID} = 0.2 V,	I_O = −1 mA	2.5	3.5		V
V_{OL}	Low-level output voltage	V_{ID} = −0.2 V,	I_O = 20 mA		0.35	0.5	V
I_I	Input current	V_{CC} = 0 to 5.5 V, See Note 4	V_I = 10 V		1.1	3.25	mA
			V_I = −10 V		−1.6	−3.25	
I_{OS}	Short-circuit output current§	V_O = 0,	V_{ID} = 0.2 V	−40	−75	−100	mA
I_{CC}	Supply current	V_{ID} = −0.5 V,	No load		35	50	mA

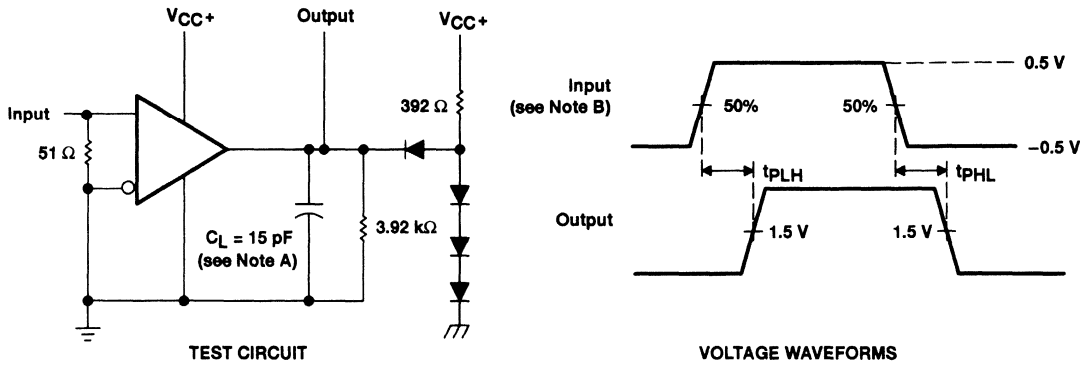
† The algebraic convention, where the less-positive (more-negative) limit is designated as minimum, is used in this data sheet for threshold levels only.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Only one output should be shorted at a time and duration of the short circuit should not exceed one second.

NOTES: 3. The expanded threshold parameter is tested with a 500-Ω resistor in series with each input.
4. The input not under test is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 15 pF, See Figure 1		15	25	ns
t_{PHL}	Propagation delay time, high- to low-level output			13	25	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 5 MHz, duty cycle = 50%.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

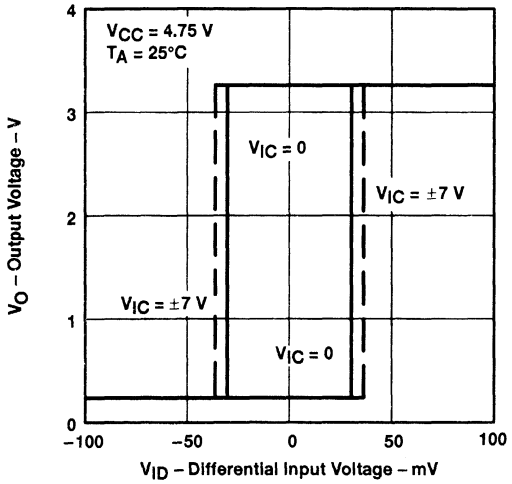


Figure 2

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

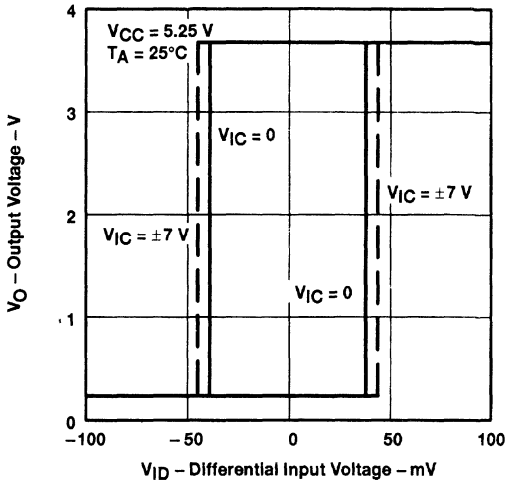


Figure 3

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

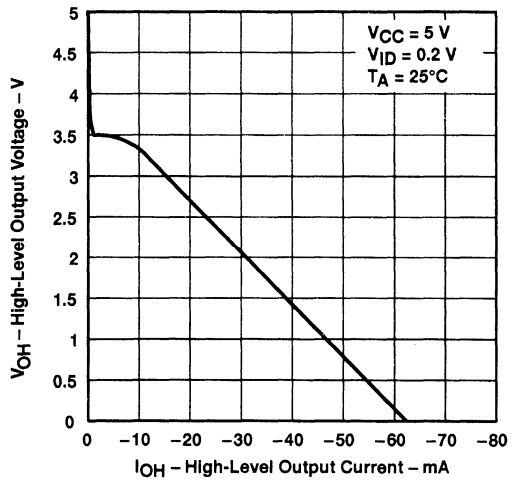


Figure 4

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

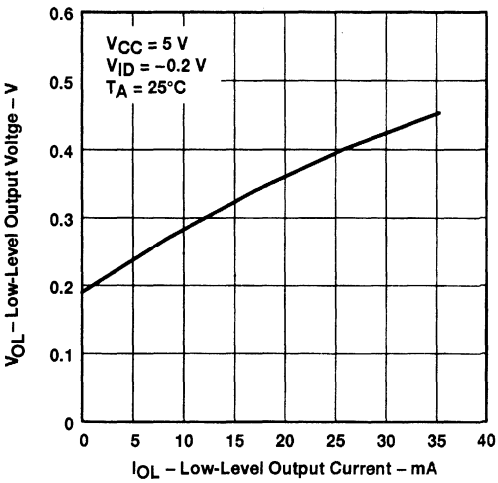


Figure 5

TYPICAL CHARACTERISTICS

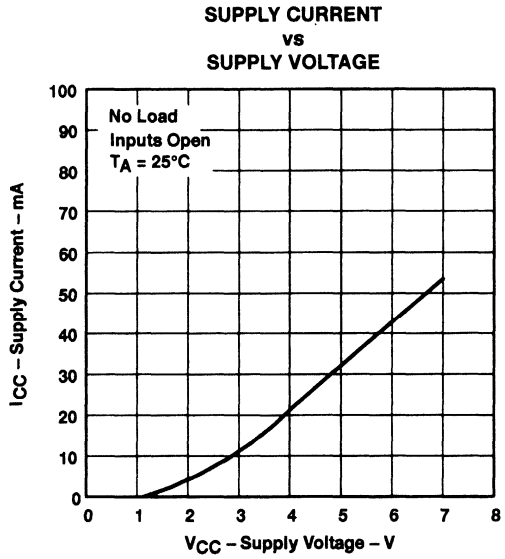


Figure 6

APPLICATION INFORMATION

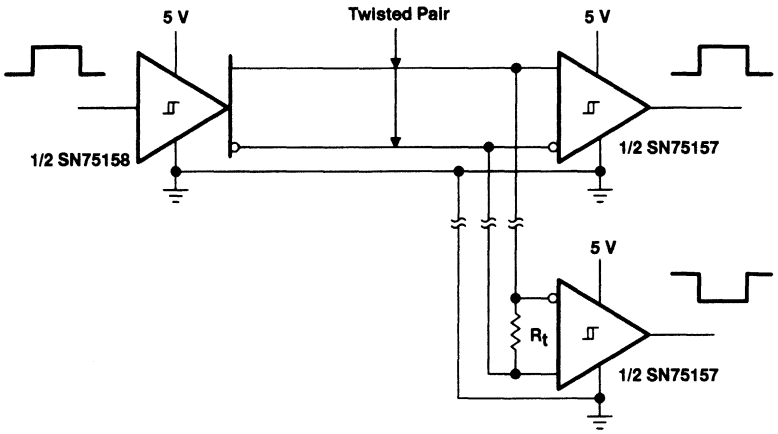
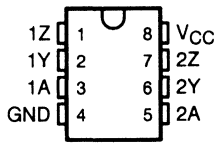


Figure 7. EIA/TIA-422-B System Application

SLLS085B – JANUARY 1977 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of ANSI EIA/TIA-422-B and ITU Recommendation V.11**
- **Single 5-V Supply**
- **Balanced-Line Operation**
- **TTLCompatible**
- **High Output Impedance in Power-Off Condition**
- **High-Current Active-Pullup Outputs**
- **Short-Circuit Protection**
- **Dual Channels**
- **Input Clamp Diodes**

D, P, OR PS† PACKAGE
(TOP VIEW)



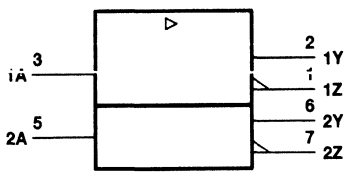
† The PS package is only available left-end taped and reeled, i.e., order SN75158PSLE.

description

The SN75158 is a dual differential line driver designed to satisfy the requirements set by the ANSI EIA/TIA-422-B and ITU V.11 interface specifications. The outputs provide complementary signals with high-current capability for driving balanced lines, such as twisted pair, at normal line impedance without high power dissipation. The output stages are TTL totem-pole outputs providing a high-impedance state in the power-off condition.

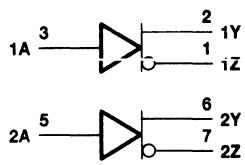
The SN75158 is characterized for operation from 0°C to 70°C.

logic symbol†

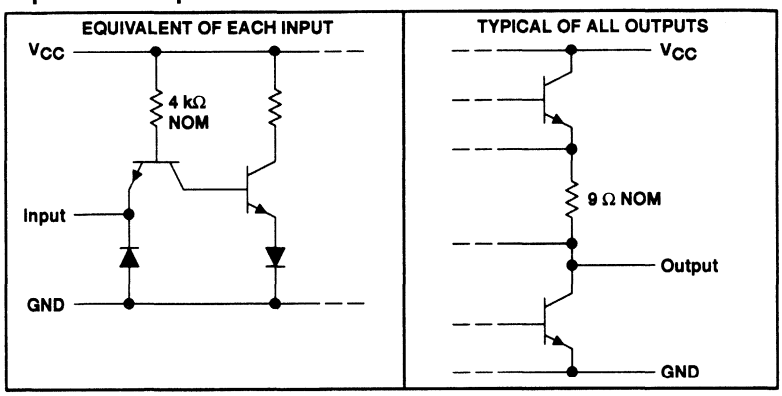


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential output voltage V_{OD}, are with respect to network ground terminal. V_{OD} is at the Y output with respect to the Z output.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW
PS	450 mW	3.6 mW/°C	288 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−40	mA
Low-level output current, I_{OL}			40	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA		−0.9	−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V,	V_{IL} = 0.8 V, I_{OH} = −40 mA	2.4	3		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V,	V_{IL} = 0.8 V, I_{OL} = 40 mA		0.2	0.4	V
$\lvert V_{OD1}\rvert$	Differential output voltage	V_{CC} = MAX,	I_O = 0		3.5	$2\times V_{OD2}$	V
$\lvert V_{OD2}\rvert$	Differential output voltage	V_{CC} = MIN	R_L = 100 Ω, See Figure 1	2	3		V
ΔV_{OD}	Change in magnitude of differential output voltage§	V_{CC} = MIN			±0.02	±0.4	V
V_{OC}	Common-mode output voltage¶	V_{CC} = MAX			1.8	3	V
		V_{CC} = MIN			1.5	3	
ΔV_{OC}	Change in magnitude of common-mode output voltage§	V_{CC} = MIN or MAX			±0.02	±0.4	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V		0.1	100	µA
			V_O = − 0.25 V		−0.1	−100	
			V_O = − 0.25 to 6 V			±100	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40	µA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V		−1	−1.6	mA
I_{OS}	Short-circuit output current#	V_{CC} = MAX		−40	−90	−150	mA
I_{CC}	Supply current (both drivers)	V_{CC} = MAX, T_A = 25°C,	Inputs grounded, No load		37	50	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V and T_A = 25°C except for V_{OC}, for which V_{CC} is as stated under test conditions.
§ ΔV_{OD} and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitudes of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
¶ In ANSI Standard EIA/TIA-422-B, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
# Only one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 2, Termination A		16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			10	20	ns
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 2, Termination B		13	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output			9	15	ns
t_{TLH}	Transition time, low-to-high-level output	See Figure 2, Termination A		4	20	ns
t_{TLH}	Transition time, high-to-low-level output			4	20	ns
	Overshoot factor	See Figure 2, Termination C			10%	

PARAMETER MEASUREMENT INFORMATION

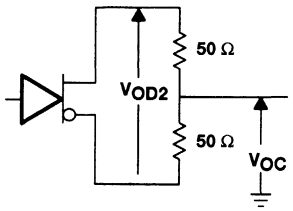
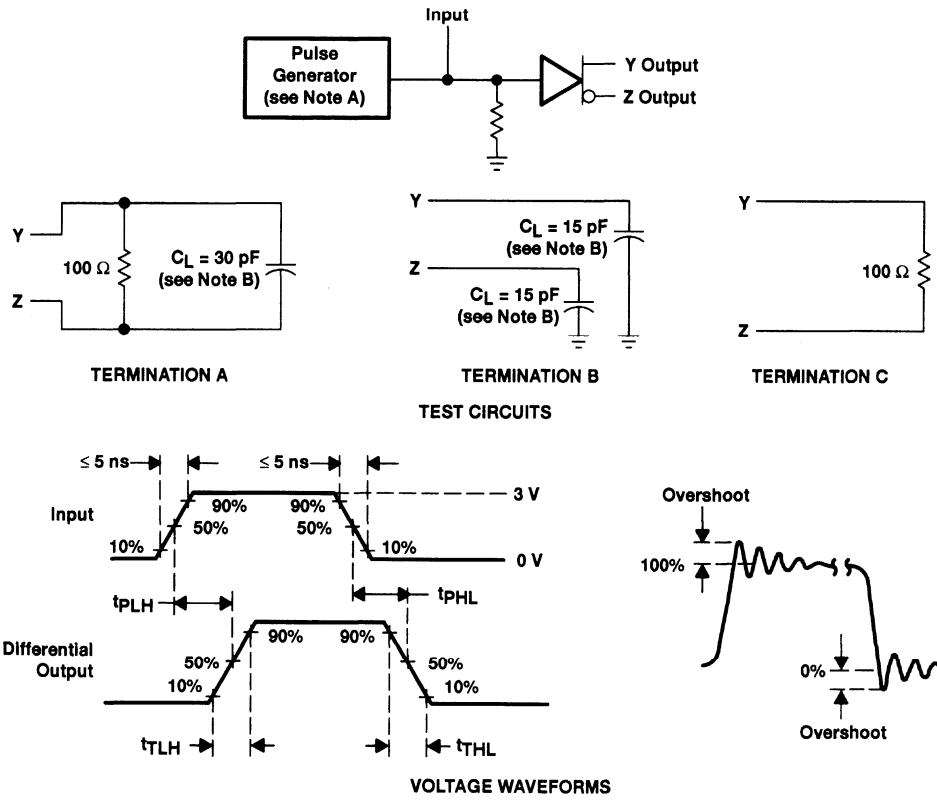


Figure 1. Differential and Common-Mode Output Voltages



NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, t_w = 25 ns, PRR ≤ 10 MHz.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

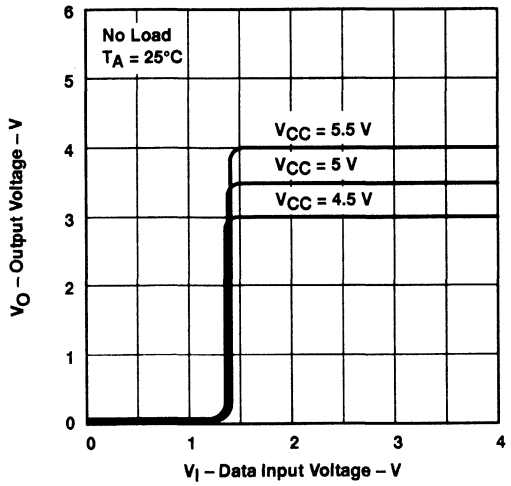


Figure 3

OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

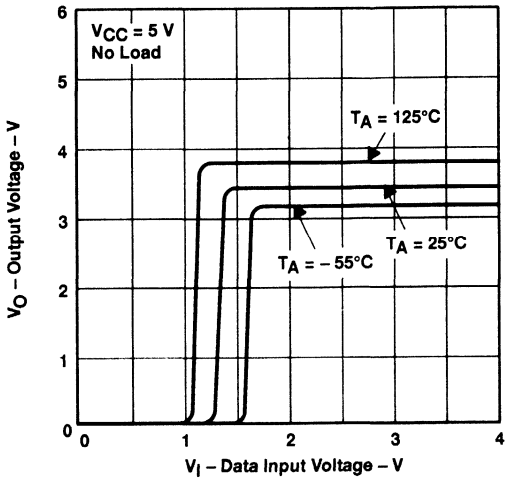


Figure 4

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

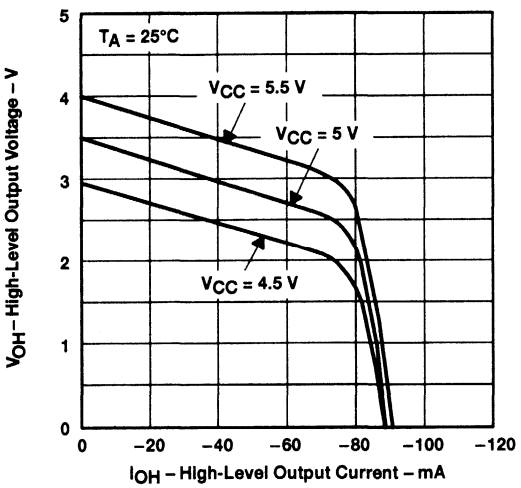


Figure 5

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

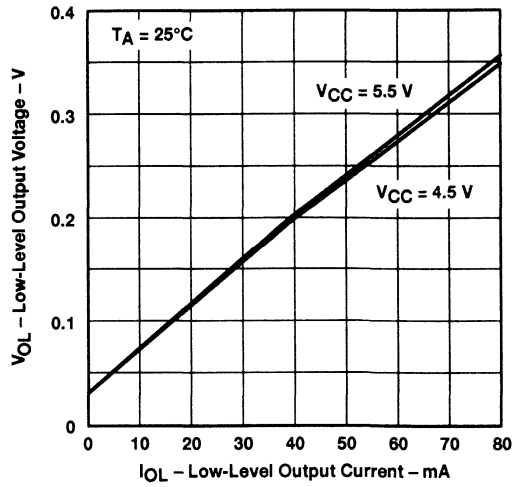


Figure 6

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

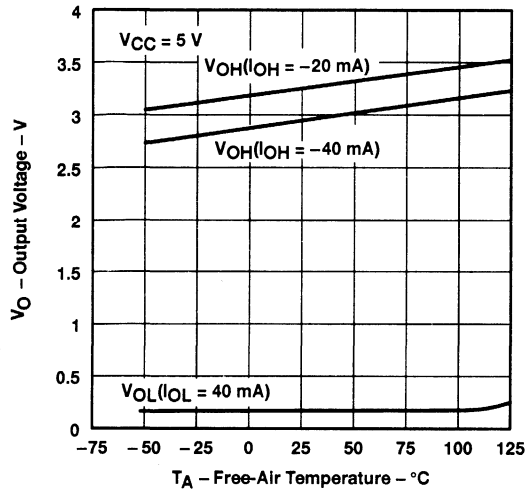


Figure 7

PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

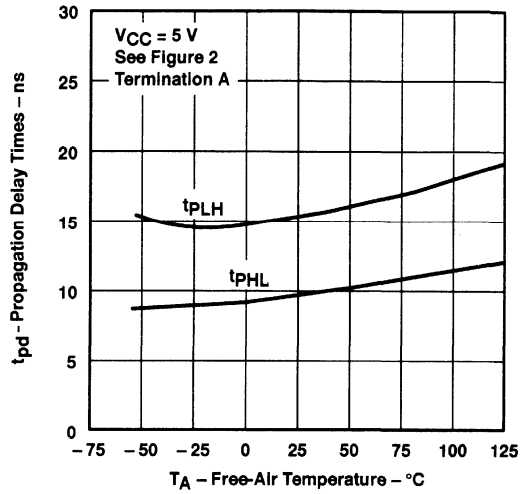


Figure 8

SUPPLY CURRENT
(BOTH DRIVERS)
vs
SUPPLY VOLTAGE

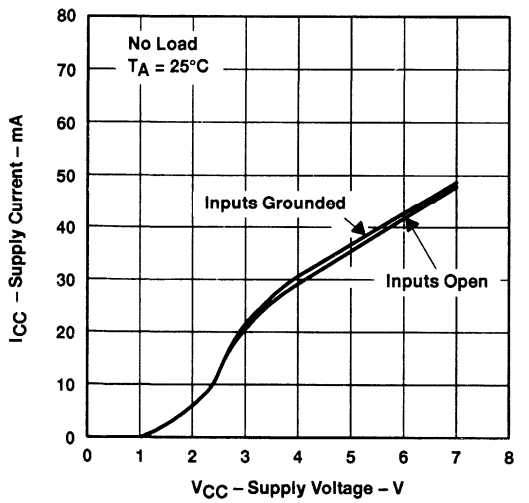


Figure 9

SUPPLY CURRENT
(BOTH DRIVERS)
vs
FREE-AIR TEMPERATURE

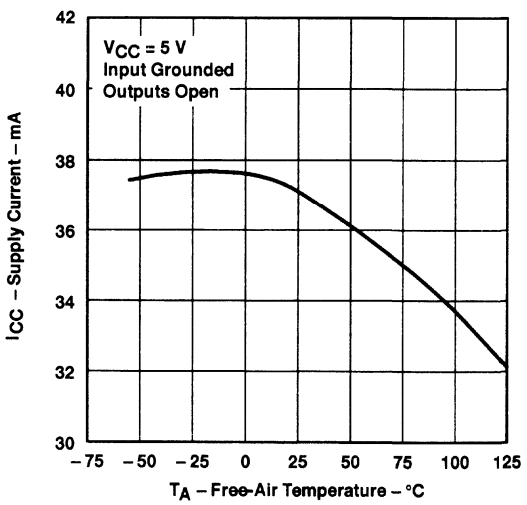


Figure 10

TYPICAL CHARACTERISTICS

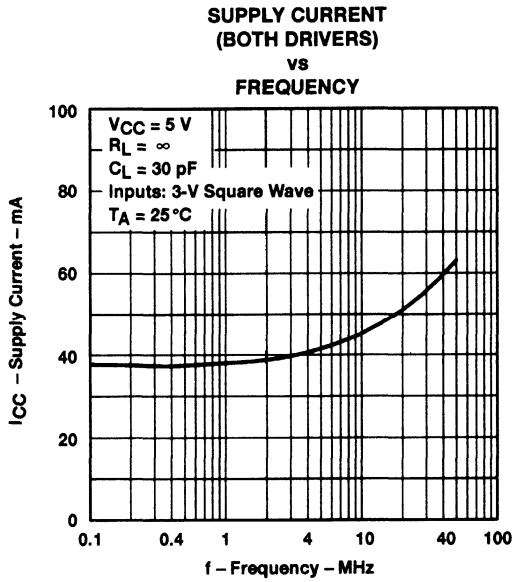


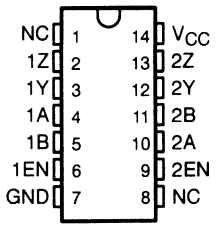
Figure 11

SN75159
DUAL DIFFERENTIAL LINE DRIVER WITH 3-STATE OUTPUTS

SLLS088B – JANUARY 1977 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of ANSI EIA/TIA-422-B and ITU Recommendation V.11**
- **Single 5-V Supply**
- **Balanced Line Operation**
- **TTL Compatible**
- **High-Impedance Output State for Party-Line Applications**
- **High-Current Active-Pullup Outputs**
- **Short-Circuit Protection**
- **Dual Channels**
- **Clamp Diodes at Inputs**

D OR N PACKAGE
(TOP VIEW)



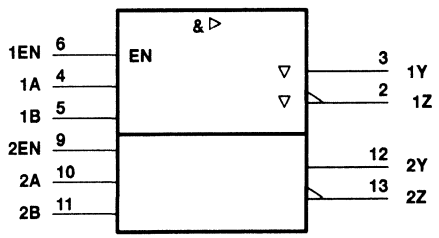
NC – No internal connection

description

The SN75159 dual differential line driver with 3-state outputs is designed to provide all the features of the SN75158 line driver with the added feature of driver output controls. There is an individual control for each driver. When the output control is low, the associated outputs are in a high-impedance state and the outputs can neither drive nor load the bus. This permits many devices to be connected together on the same transmission line for party-line applications.

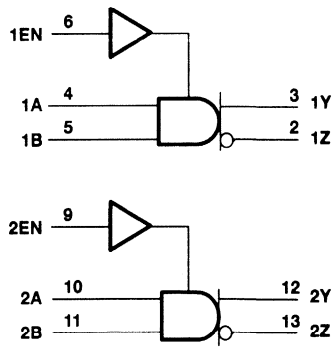
The SN75159 is characterized for operation from 0°C to 70°C.

logic symbol†

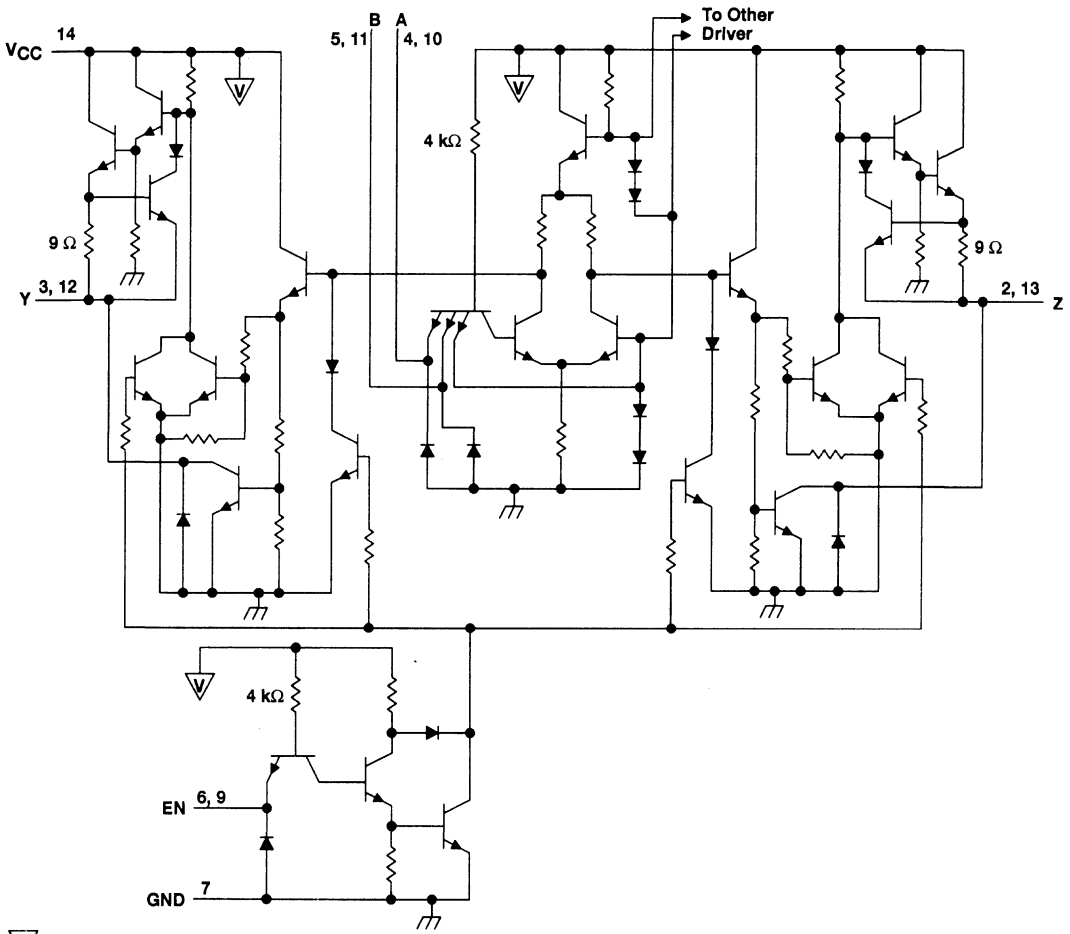


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic (each driver)



▽ . . . V_{CC} bus

Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 5.5 V
Off-state voltage applied to open-collector outputs ..... 12 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values except differential output voltage V_{OD} are with respect to the network ground terminal. V_{OD} is at the Y output with respect to the Z output.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output voltage, I_{OH}			−40	mA
Low-level output current, I_{OL}			40	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V,	I_I = −12 mA			−0.9	−1.5	V
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V,	V_{IL} = 0.8 V, I_{OH} = −40 mA		2.4	3		V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V,	V_{IL} = 0.8 V, I_{OL} = 40 mA			0.25	0.4	V
V_{OK}	Output clamp voltage	V_{CC} = 5.25 V,	I_O = −40 mA			−1.1	−1.5	V
V_O	Output voltage	V_{CC} = 4.75 V to 5.25 V,	I_O = 0		0		6	V
$\lvert V_{OD1}\rvert$	Differential output voltage	V_{CC} = 5.25 V,	I_O = 0			3.5	$2V_{OD2}$	V
$\lvert V_{OD2}\rvert$	Differential output voltage	V_{CC} = 4.75 V			2	3		V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage‡	V_{CC} = 4.75 V	R_L = 100 Ω, See Figure 1			±0.02	±0.4	V
V_{OC}	Common-mode output voltage§	V_{CC} = 5.25 V				1.8	3	V
		V_{CC} = 4.75 V				1.5	3	
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage‡	V_{CC} = 4.75 V to 5.25 V				±0.01	±0.4	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V			0.1	100	µA
			V_O = −0.25 V			−0.1	−100	
			V_O = −0.25 V to 6 V				±100	
I_{OZ}	Off-state (high-impedance state) output current	V_{CC} = 5.25 V, Output controls at 0.8 V	T_A = 25°C	V_O = 0 to V_{CC}			±10	µA
			T_A = 70°C	V_O = 0			−20	
				V_O = 0.4 V			±20	
				V_O = 2.4 V			±20	
				V_O = V_{CC}			20	
I_I	Input current at maximum input voltage	V_{CC} = 5.25 V,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = 5.25 V,	V_I = 2.4 V				40	µA
I_{IL}	Low-level input current	V_{CC} = 5.25 V,	V_I = 0.4 V			−1	−1.6	mA
I_{OS}	Short-circuit output current¶	V_{CC} = 5.25 V			−40	−90	−150	mA
I_{CC}	Supply current (both drivers)	V_{CC} = 5.25 V, T_A = 25°C,	Inputs grounded, No load			47	65	mA

† All typical values are at V_{CC} = 5 V and T_A = 25°C except for V_{OC}, for which V_{CC} is as stated under test conditions.
‡ $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitudes of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
§ In ANSI Standard EIA/TIA-422-B, V_{OC}, which is the average of the two output voltages with respect to GND, is called output offset voltage, V_{OS}.
¶ Only one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics over operating free-air temperature range, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, R_L = 100 Ω, See Figure 2, Termination A		16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			11	20	ns
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, See Figure 2, Termination B		13	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output			9	15	ns
t_{TLH}	Transition time, low-to-high-level output	C_L = 30 pF, R_L = 100 Ω, See Figure 2, Termination A		4	20	ns
t_{THL}	Transition time, high-to-low-level output			4	20	ns
t_{PZH}	Output enable time to high level	C_L = 30 pF, R_L = 180 Ω, See Figure 3		7	20	ns
t_{PZL}	Output enable time to low level	C_L = 30 pF, R_L = 250 Ω, See Figure 4		14	40	ns
t_{PHZ}	Output disable time from high level	C_L = 30 pF, R_L = 180 Ω, See Figure 3		10	30	ns
t_{PLZ}	Output disable time from low level	C_L = 30 pF, R_L = 250 Ω, See Figure 4		17	35	ns
	Overshoot factor	R_L = 100 Ω, See Figure 2, Termination C			10%	

† All typical values are at T_A = 25°C.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	EIA/TIA-422-B
V_O	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o
$\|V_{OD2}\|$	V_t
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$

PARAMETER MEASUREMENT INFORMATION

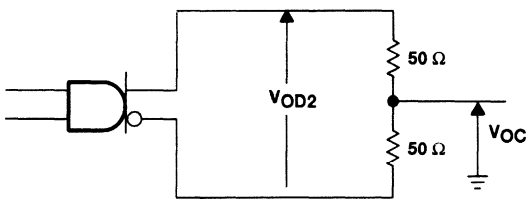
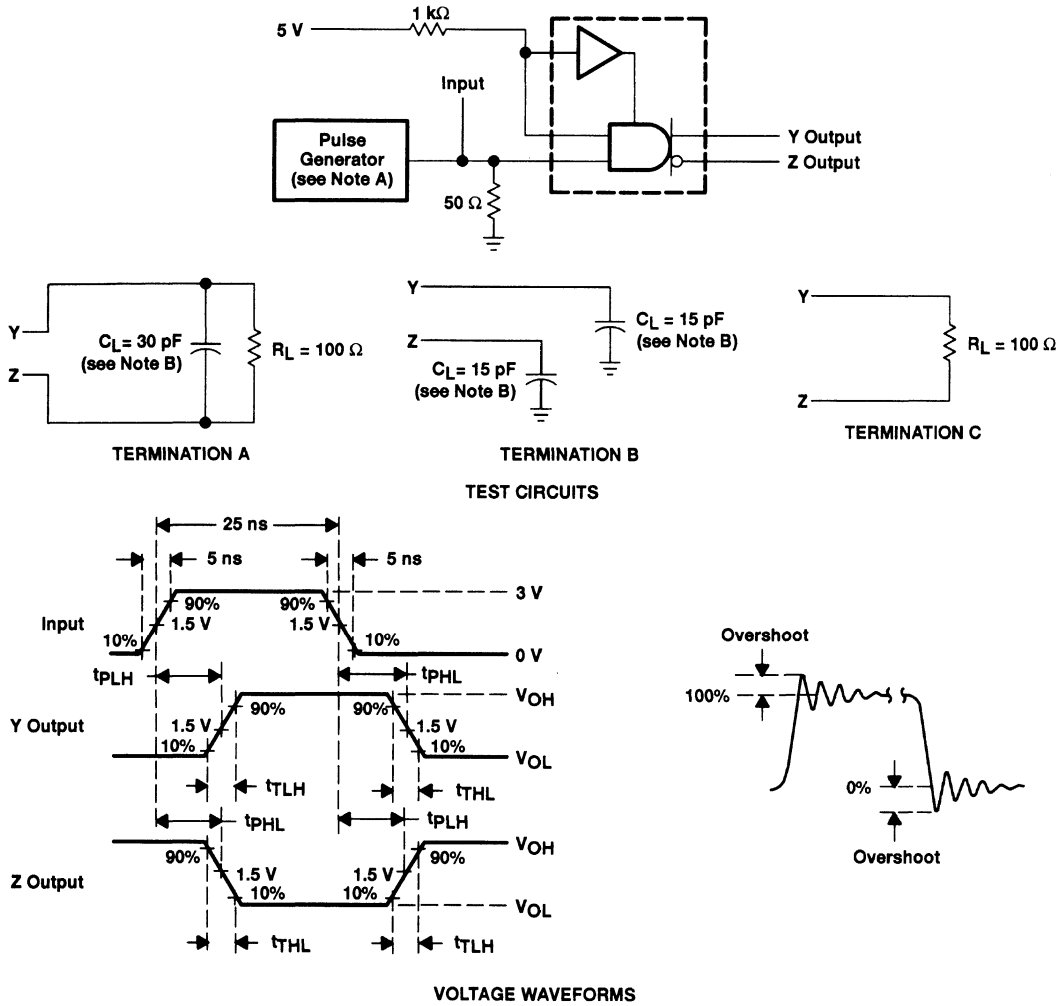


Figure 1. Differential and Common-Mode Output Voltages

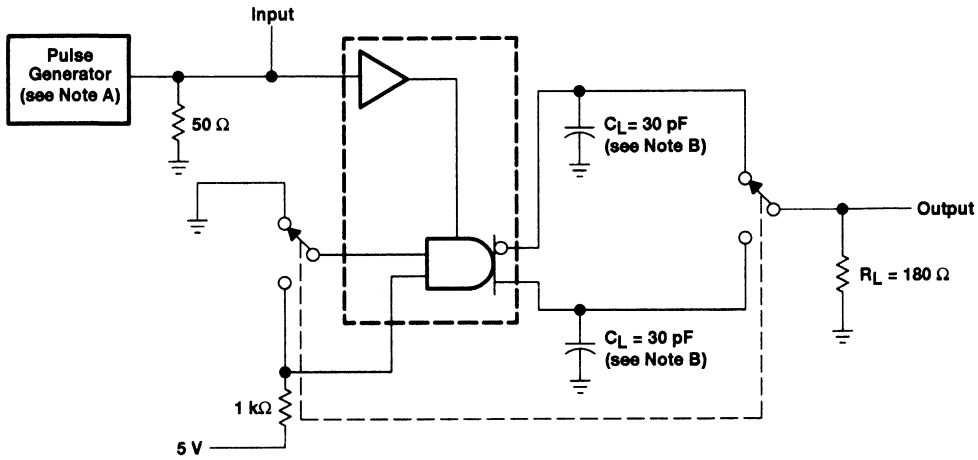
PARAMETER MEASUREMENT INFORMATION



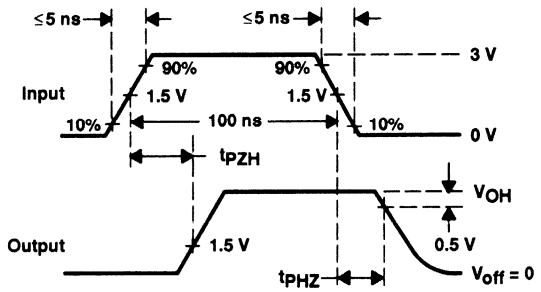
NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, PRR ≤ 10 MHz.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuits, Voltage Waveforms, and Overshoot Factor

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

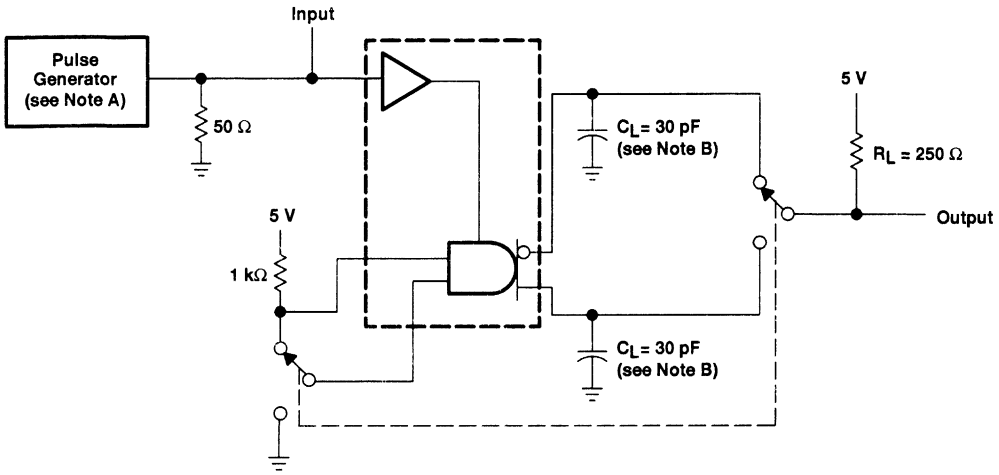


VOLTAGE WAVEFORMS

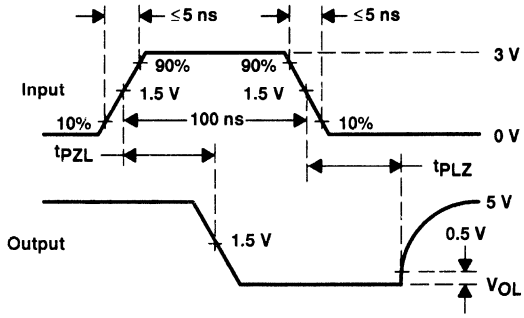
NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, PRR ≤ 500 kHz.
B. C_L includes probe and jig capacitance.

Figure 3. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, PRR ≤ 500 kHz.
B. C_L includes probe and jig capacitance.

Figure 4. Test Circuit and Voltge Waveform

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

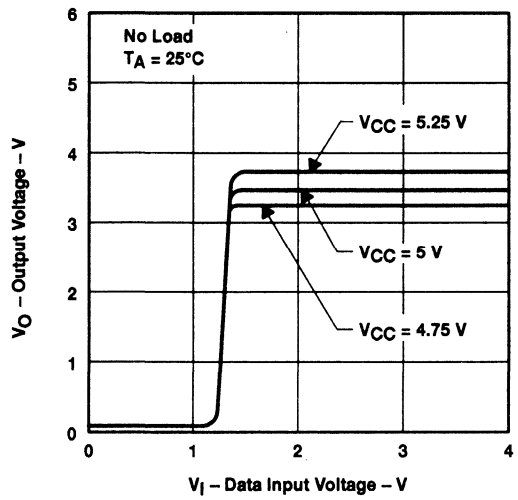


Figure 5

OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

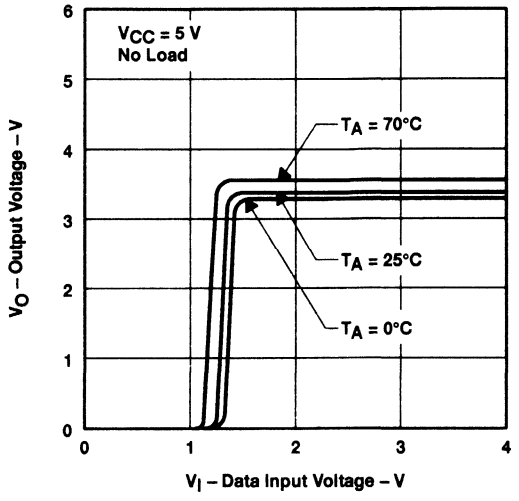


Figure 6

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

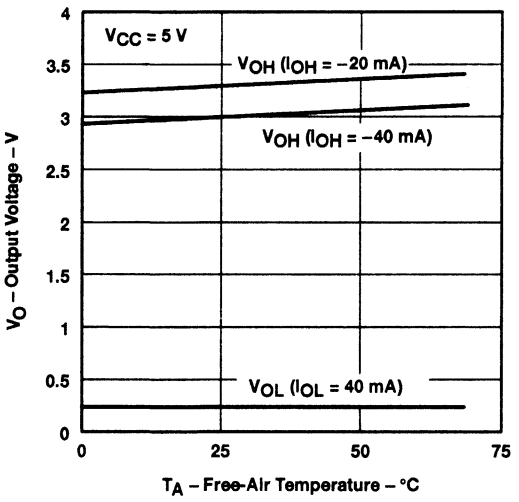


Figure 7

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

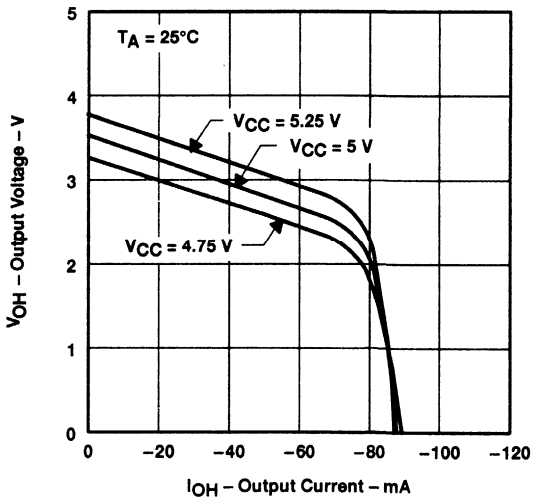


Figure 8

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

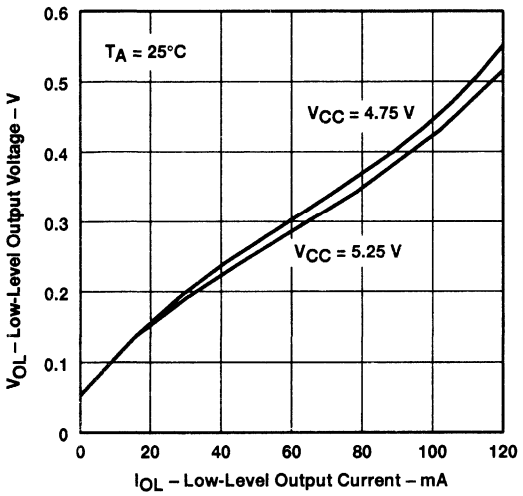


Figure 9

SUPPLY CURRENT
(BOTH DRIVERS)
vs
SUPPLY VOLTAGE

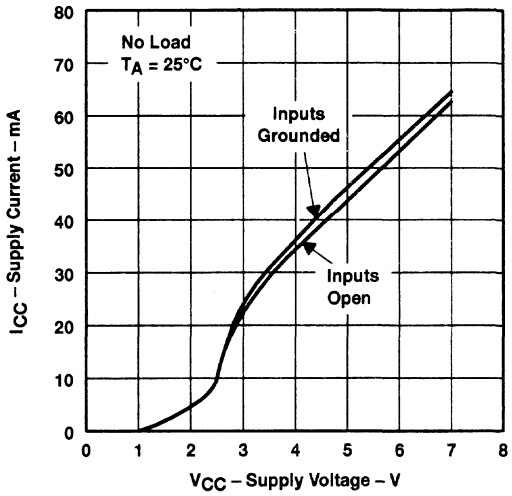


Figure 10

SUPPLY CURRENT
(BOTH DRIVERS)
vs
FREE-AIR TEMPERATURE

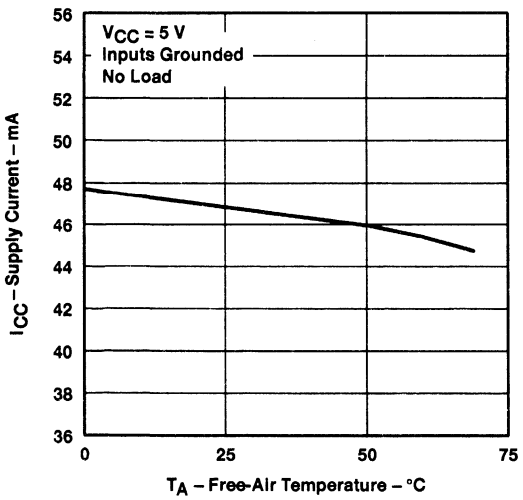


Figure 11

SUPPLY CURRENT
(BOTH DRIVERS)
vs
FREQUENCY

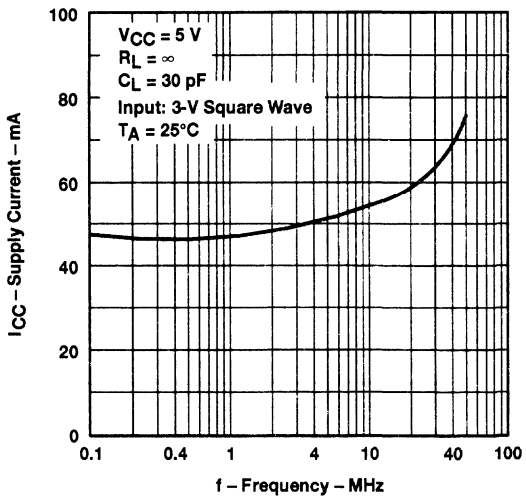


Figure 12

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
FROM DATA INPUTS
vs
FREE-AIR TEMPERATURE

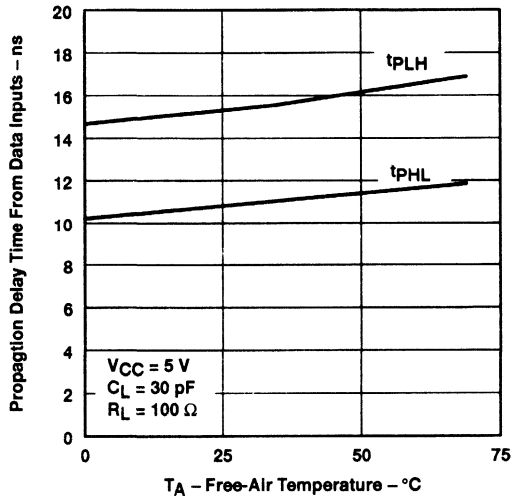


Figure 13

OUTPUT ENABLE AND DISABLE TIME
vs
FREE-AIR TEMPERATURE

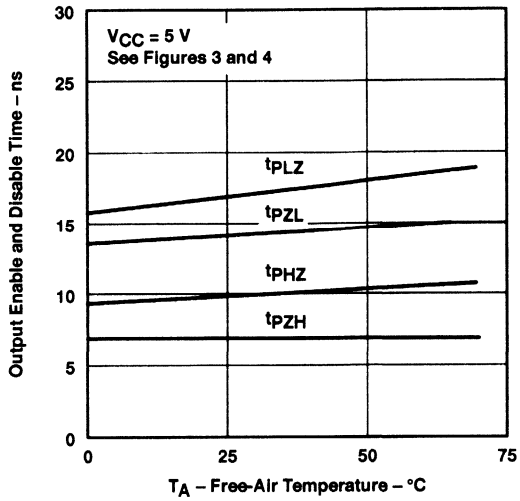


Figure 14

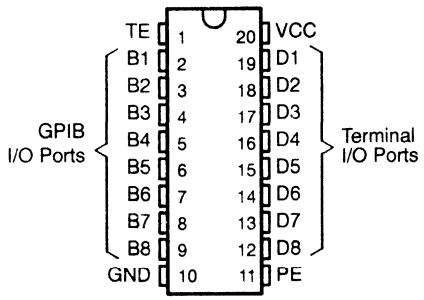
SN75160B
OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

SLLS004B – OCTOBER 1985 – REVISED MAY 1995

MEETS IEEE STANDARD 488-1978 (GPIB)

- **8-Channel Bidirectional Transceiver**
- **Power-Up/Power-Down Protection (Glitch Free)**
- **High-Speed, Low-Power Schottky Circuitry**
- **Low Power Dissipation . . . 72 mW Max Per Channel**
- **Fast Propagation Times . . . 22 ns Max**
- **High-Impedance pnp Inputs**
- **Receiver Hysteresis . . . 650 mV Typ**
- **Open-Collector Driver Output Option**
- **No Loading of Bus When Device Is Powered Down (V_{CC} = 0)**

DW OR N PACKAGE
(TOP VIEW)



description

The SN75160B 8-channel general-purpose interface bus (GPIB) transceiver is a monolithic, high-speed, low-power Schottky device designed for two-way data communications over single-ended transmission lines. It is designed to meet the requirements of IEEE Standard 488-1978. The transceiver features driver outputs that can be operated in either the passive-pullup or 3-state mode. If talk enable (TE) is high, these ports have the characteristics of passive-pullup outputs when pullup enable (PE) is low and of 3-state outputs when PE is high. Taking TE low places these ports in the high-impedance state. The driver outputs are designed to handle loads up to 48 mA of sink current.

Output glitches during power up and power down are eliminated by an internal circuit that disables both the bus and receiver outputs. The outputs do not load the bus when V_{CC} = 0. When combined with the SN75161B or SN75162B management bus transceivers, the pair provides the complete 16-wire interface for the IEEE-488 bus.

The SN75160B is characterized for operation from 0°C to 70°C.

Function Tables

EACH DRIVER

INPUTS			OUTPUT
D	TE	PE	B
H	H	H	H
L	H	X	L
H	X	L	Z†
X	L	X	Z†

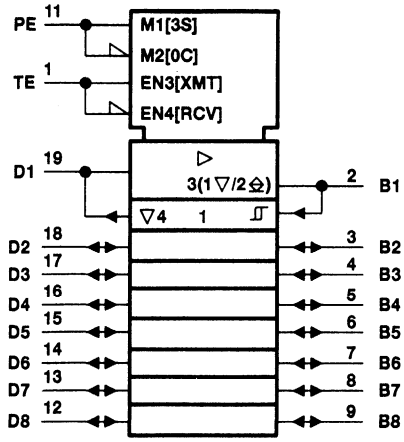
EACH RECEIVER

INPUTS			OUTPUT
B	TE	PE	D
L	L	X	L
H	L	X	H
X	H	X	Z

H = high level, L = low level, X = irrelevant, Z = high-impedance state

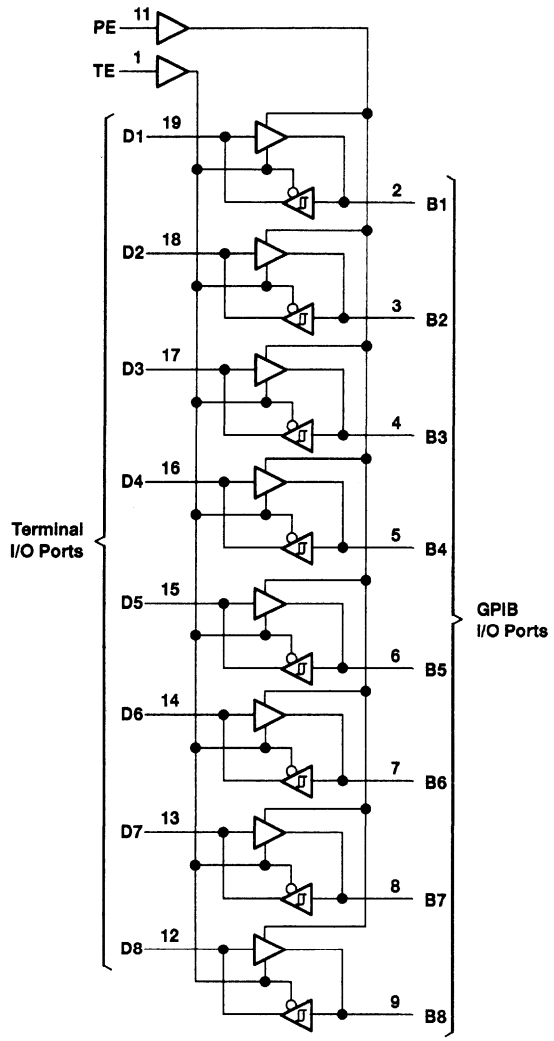
† This is the high-impedance state of a normal 3-state output modified by the internal resistors to V_{CC} and GND.

logic symbol†



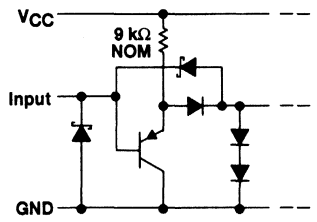
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
▽ Designates 3-state outputs
⏏ Designates passive-pullup outputs

logic diagram (positive logic)

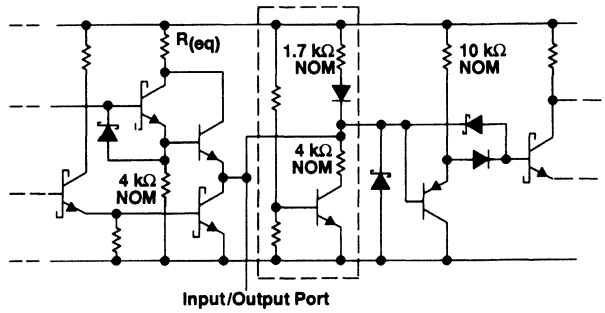


schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS



EQUIVALENT OF ALL INPUT/OUTPUT PORTS



Driver output $R_{(eq)}$ = 30 Ω NOM
Receiver output $R_{(eq)}$ = 110 Ω NOM
Circuit inside dashed lines is on the driver outputs only.
$R_{(eq)}$ = equivalent resistor

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 5.5 V
Low-level driver output current, I_{OL} ..... 100 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with pullups active			−5.2	mA
	Terminal ports			−800	µA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA			−0.8	−1.5	V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)	Bus	See Figure 8		0.4	0.65		V
V_{OH}	High-level output voltage	Terminal	I_{OH} = −800 μA,	TE at 0.8 V	2.7	3.5		V
		Bus	I_{OH} = −5.2 mA,	PE and TE at 2 V	2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA,	TE at 0.8 V		0.3	0.5	V
		Bus	I_{OL} = 48 mA,	TE at 2 V		0.35	0.5	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V			0.2	100	μA
I_{IH}	High-level input current	Terminal	V_I = 2.7 V			0.1	20	μA
I_{IL}	Low-level input current	Terminal	V_I = 0.5 V			−10	−100	μA
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled	$I_{I(bus)}$ = 0	2.5	3.0	3.7	V
				$I_{I(bus)}$ = −12 mA			−1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled	$V_{I(bus)}$ = −1.5 V to 0.4 V	−1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V	0		−3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V			2.5 −3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V	0.7		2.5	
		Power off	V_{CC} = 0,	$V_{I(bus)}$ = 0 to 2.5 V			−40	
I_{OS}	Short-circuit output current	Terminal			−15	−35	−75	mA
		Bus			−25	−50	−125	
I_{CC}	Supply current		No load	Receivers low and enabled		70	90	mA
				Drivers low and enabled		85	110	
$C_{I/O(bus)}$	Bus-port capacitance		V_{CC} = 0 to 5 V, f = 1 MHz	$V_{I/O}$ = 0 to 2 V,		16		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propation delay time, low- to high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		14	20	ns
t_{PHL}	Propagation delay time, high- to low-level output					14	20	
t_{PLH}	Propagation delay time, low- to high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		10	20	ns
t_{PHL}	Propagation delay time, high- to low-level output					15	22	
t_{PZH}	Output enable time to high level	TE	BUS	See Figure 3		25	35	ns
t_{PHZ}	Output disable time from high level					13	22	
t_{PZL}	Output enable time to low level					22	35	
t_{PLZ}	Output disable time from low level					22	32	
t_{PZH}	Output enable time to high level	TE	Terminal	See Figure 4		20	30	ns
t_{PHZ}	Output disable time from high level					12	20	
t_{PZL}	Output enable time to low level					23	32	
t_{PLZ}	Output disable time from low level					19	30	
t_{en}	Output pullup enable time	PE	Bus	See Figure 5		15	22	ns
t_{dis}	Output pullup disable time					13	20	

PARAMETER MEASUREMENT INFORMATION

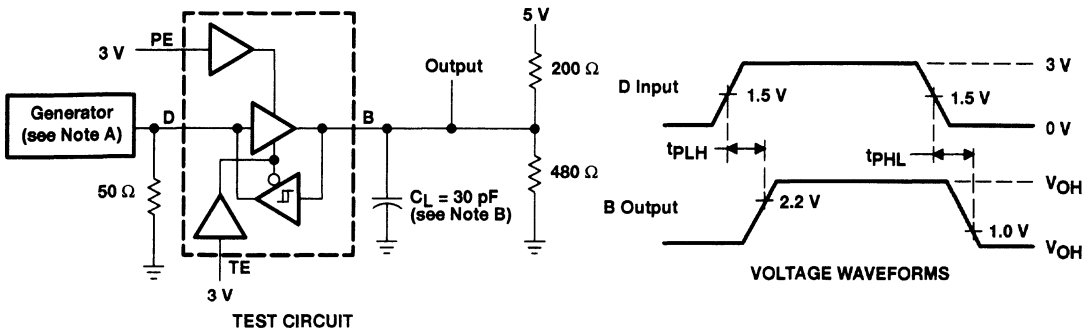


Figure 1. Terminal-to-Bus Test Circuit and Voltage Waveforms

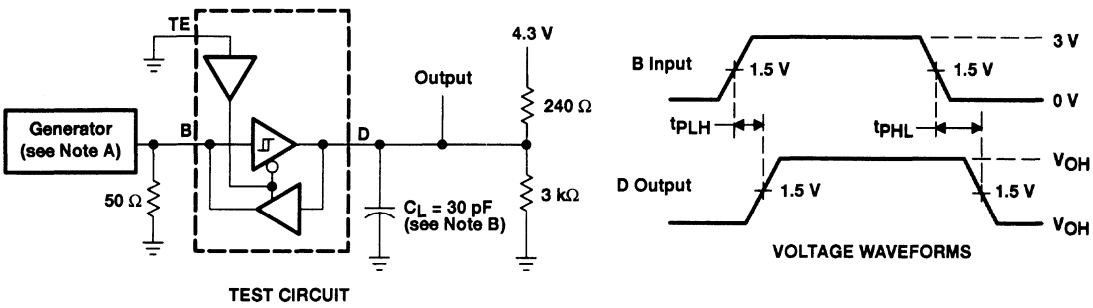


Figure 2. Bus-to-Terminal Test Circuit and Voltage Waveforms

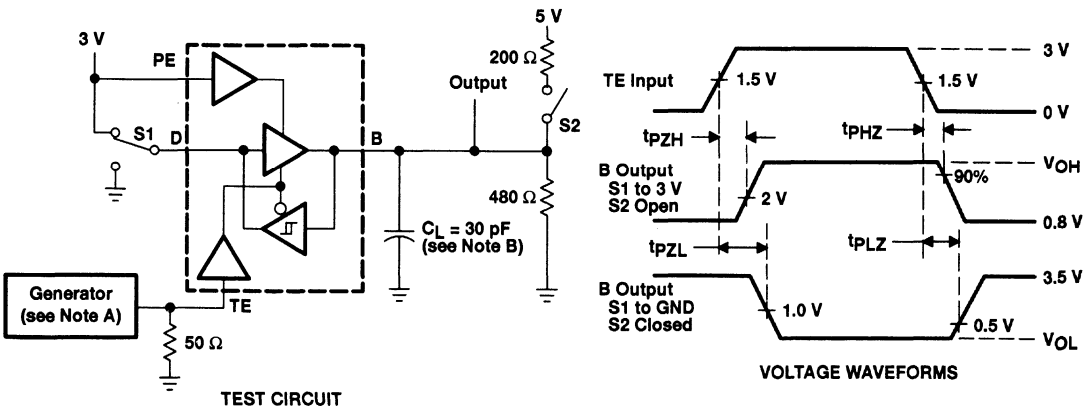


Figure 3. TE-to-Bus Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

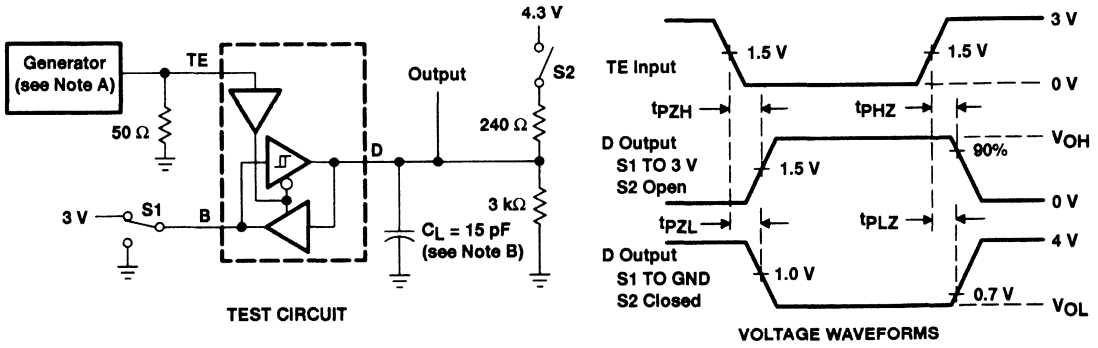


Figure 4. TE-to-Terminal Test Circuit and Voltage Waveforms

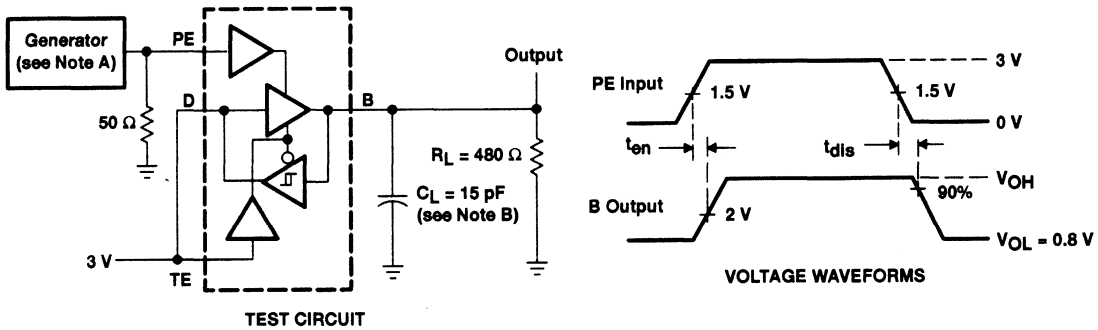


Figure 5. PE-to-Bus Pullup Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

TERMINAL I/O PORTS
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

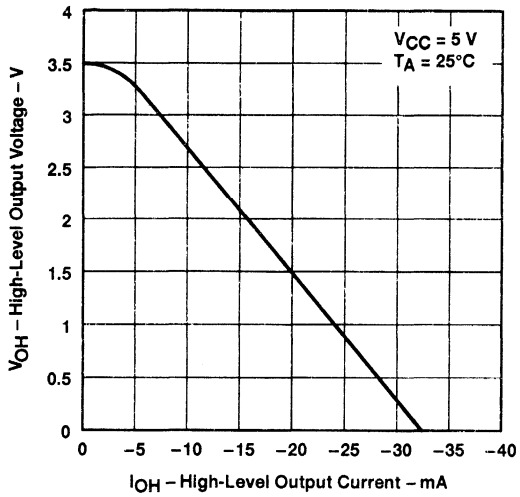


Figure 6

TERMINAL I/O PORTS
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

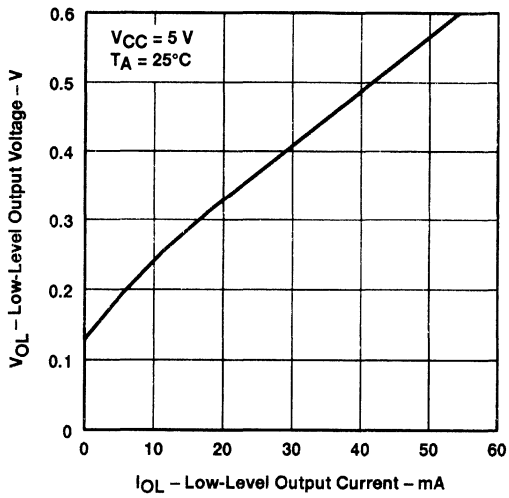


Figure 7

TERMINAL I/O PORTS
OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

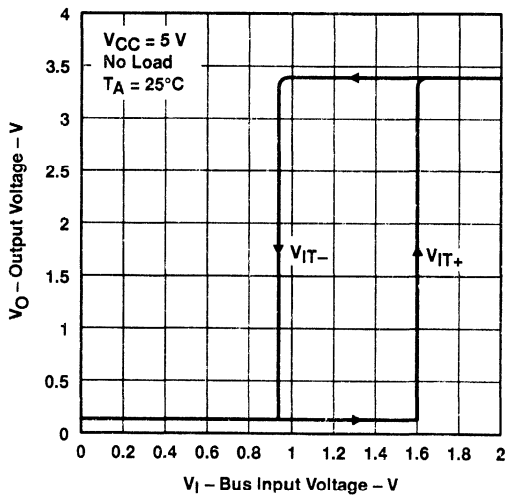


Figure 8

TYPICAL CHARACTERISTICS

GPIB I/O PORTS
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

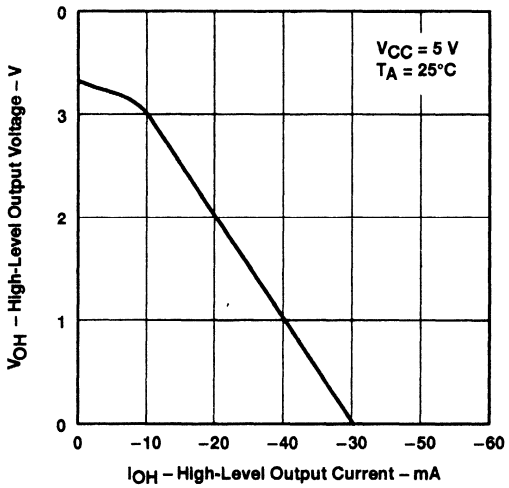


Figure 9

GPIB I/O PORTS
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

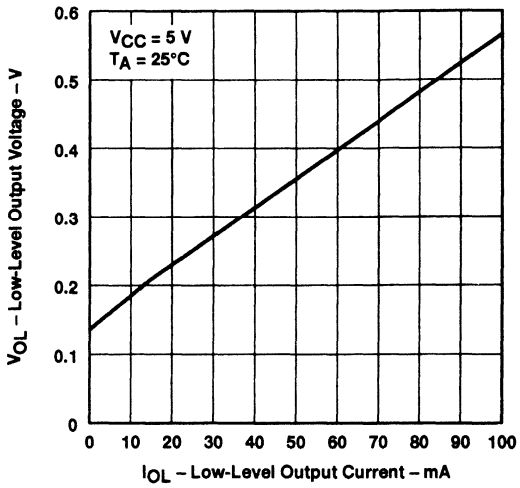


Figure 10

GPIB I/O PORTS
OUTPUT VOLTAGE
vs
THERMAL INPUT VOLTAGE

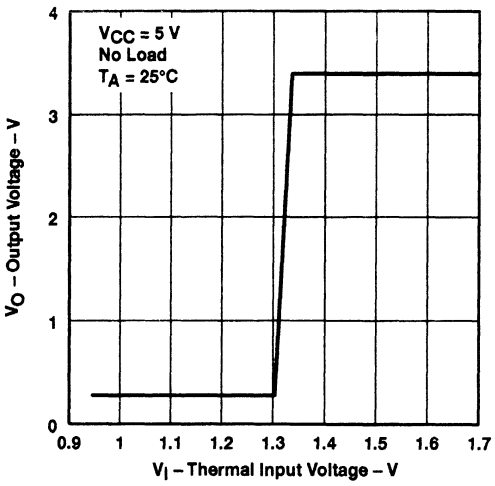


Figure 11

GPIB I/O PORTS
CURRENT
vs
VOLTAGE

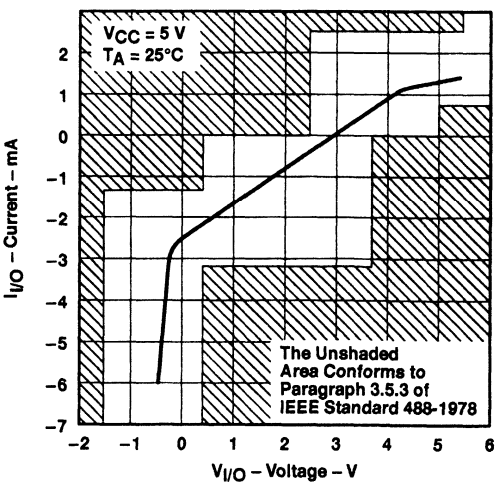


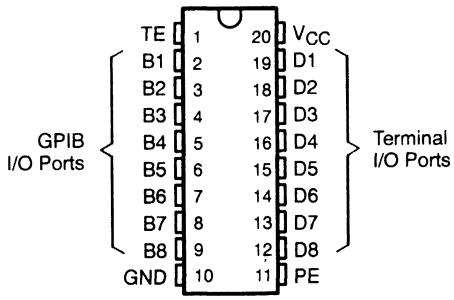
Figure 12

SLLS018D – JUNE 1986 – REVISED MAY 1995

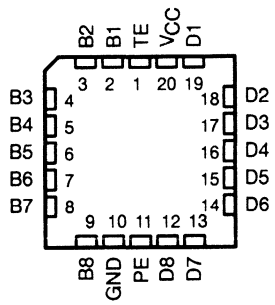
SUITABLE FOR IEEE STANDARD 488-1978 (GPIB)†

- 8-Channel Bidirectional Transceivers
- High-Speed Advanced Low-Power Schottky (ALS) Circuitry
- Low Power Dissipation:
  SN55ALS160 . . . 56 mW Max Per Channel
  SN75ALS160 . . . 46 mW Max Per Channel
- Fast Propagation Times . . . 20 ns Max
- High-Impedance pnp Inputs
- Receiver Hysteresis:
  SN55ALS160 . . . 550 mV Typ
  SN75ALS160 . . . 650 mV Typ
- Open-Collector Driver Output Option
- No Loading of Bus When Device Is Powered Down (V_{CC} = 0)
- Power-Up/Power-Down Protection (Glitch Free)

SN55ALS160 . . . J OR W PACKAGE
SN75ALS160 . . . DW OR N PACKAGE
(TOP VIEW)



SN55ALS160 . . . FK PACKAGE
(TOP VIEW)



description

The SN55ALS160 and SN75ALS160 eight-channel general-purpose interface bus transceivers are monolithic, high-speed, advanced low-power Schottky (ALS) devices designed for two-way data communications over single-ended transmission lines. They are designed to meet the requirements of IEEE Standard 488-1978. The transceivers feature driver outputs that can be operated in either the passive-pullup or 3-state mode. If talk enable (TE) is high, these ports have the characteristics of passive-pullup outputs when pullup enable (PE) is low and of 3-state outputs when PE is high. Taking TE low places these ports in the high-impedance state. The driver outputs are designed to handle loads up to 48 mA of sink current.

An active turn-off feature has been incorporated into the bus-terminating resistors so that the device exhibits a high impedance to the bus when V_{CC} = 0. When combined with the SN55ALS161, SN75ALS161, or SN75ALS162 bus management transceiver, the pair provides the complete 16-wire interface for the IEEE-488 bus.

The SN55ALS160 is characterized for operation from −55°C to 125°C.The SN75ALS160 is characterized for operation from 0°C to 70°C.

Function Tables

EACH DRIVER

INPUTS			OUTPUT
D	TE	PE	B
H	H	H	H
L	H	X	L
H	X	L	Z‡
X	L	X	Z‡

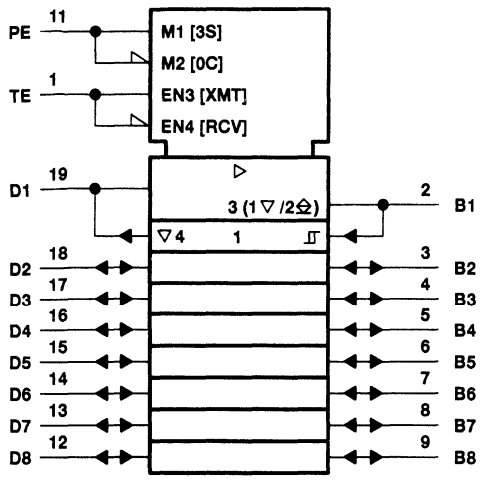
EACH RECEIVER

INPUTS			OUTPUT
B	TE	PE	D
L	L	X	L
H	L	X	H
X	H	X	Z

H = high level, L = low level, X = irrelevant,
Z = high-impedance state
‡ This is the high-impedance state of a normal 3-state output modified by the internal resistors to V_{CC} and GND.

† The transceivers are suitable for IEEE Standard 896 applications to the extent of the operating conditions and characteristics specified in this data sheet. Certain limits contained in the IEEE specification are not met or cannot be tested over the entire military temperature range.

logic symbol†

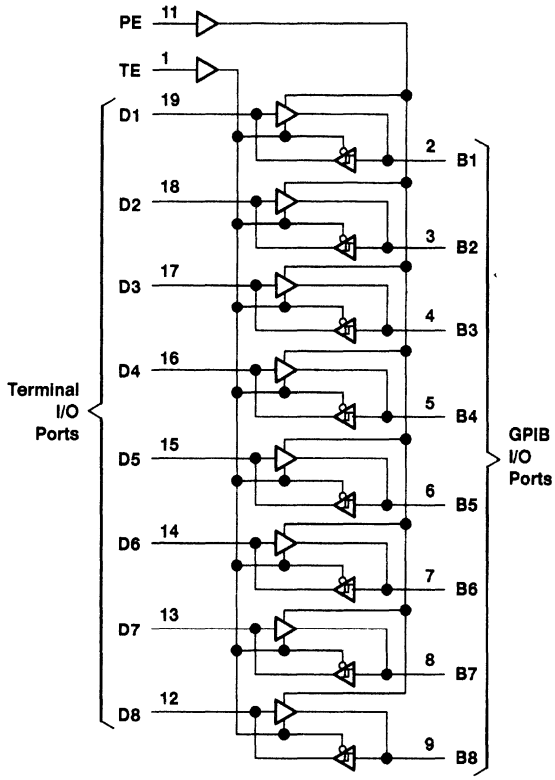


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

▽ Designates 3-state outputs

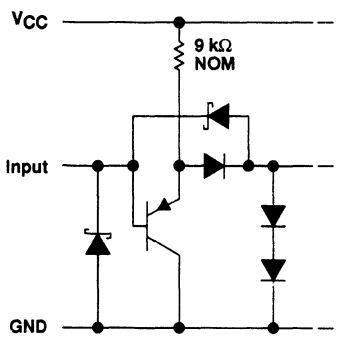
◈ Designates open-collector outputs with passive pullup

logic diagram (positive logic)

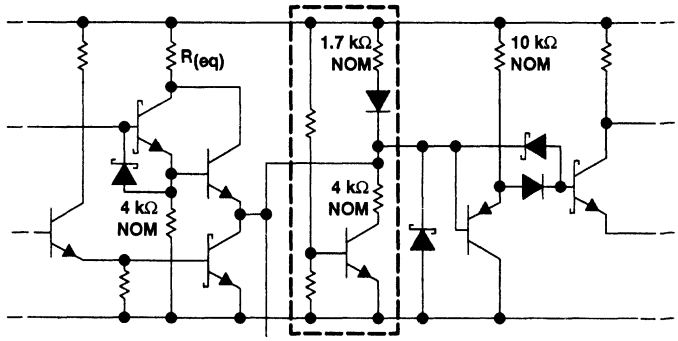


schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS



EQUIVALENT OF ALL INPUT/OUTPUT PORTS



Driver output $R_{(eq)}$ = 30 Ω NOM
Receiver output $R_{(eq)}$ = 110 Ω NOM
$R_{(eq)}$ = equivalent resistor
Circuit inside dashed lines is on the driver outputs only.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 5.5 V
Low-level driver output current, I_{OL} ..... 100 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN55ALS160 ..... −55°C to 125°C
SN75ALS160 ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Case temperature for 60 seconds, T_C: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: DW or N package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J or W package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—
W	1000 mW	8.0 mW/°C	640 mW	200 mW

SN55ALS160 recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	TE and PE at T_A = −55°C to 125°C	2			V
	Bus and terminal at T_A = 25°C to 125°C	2			
	Bus and terminal at T_A = −55°C	2.1			
Low-level input voltage, V_{IL}	TE and PE at T_A = −55°C to 125°C			0.8	V
	Bus and terminal at T_A = 25°C to −55°C			0.8	
	Bus and terminal at T_A = 125°C			0.7	
High-level output current, I_{OH}	Bus ports with pullups active (V_{CC} = 5 V)			−5.2	mA
	Terminal ports			−800	µA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		−55		125	°C

SN75ALS160 recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with pullups active			−5.2	mA
	Terminal ports			−800	µA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN55ALS160			SN75ALS160			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage		I_I = −18 mA,	V_{CC} = MIN		−0.8	−1.5		−0.8	−1.5	V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)	Bus						0.4	0.65		V
		Bus	V_{CC} = 5 V,	T_A = −55°C and 25°C	0.4	0.55					
			V_{CC} = 5 V,	T_A = 125°C	0.25						
V_{OH}§	High-level output voltage	Terminal	I_{OH} = −800 µA,	TE at 0.8 V, V_{CC} = MIN	2.7	3.5		2.7	3.5		V
		Bus	I_{OH} = −5.2 mA,	PE and TE at 2 V, V_{CC} = MIN	2.5	3.3		2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA,	TE at 0.8 V, V_{CC} = MIN		0.3	0.5		0.3	0.5	V
		Bus	I_{OL} = 48 mA,	TE at 2 V, V_{CC} = MIN		0.35	0.5		0.35	0.5	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V,	V_{CC} = MAX		0.2	100		0.2	100	µA
I_{IH}	High-level input current	Terminal, PE, or TE	V_I = 2.7 V,	V_{CC} = MAX		0.1	20		0.1	20	µA
I_{IL}	Low-level input current		V_I = 0.5 V,	V_{CC} = MAX		−30	−100		−10	−100	µA
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled, V_{CC} = 5 V (SN55')	$I_{I(bus)}$ = 0	2.5	3	3.7	2.5	3	3.7	V
				$I_{I(bus)}$ = −12 mA			−1.5			−1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled, V_{CC} = 5 V (SN55')	$V_{I(bus)}$ = −1.5 V to 0.4 V	−1.3			−1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V	0		−3.2	0		−3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V			2.5 −3.2			2.5 −3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V	0		2.5	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V	0.7		2.5	0.7		2.5	
		Power off	V_{CC} = 0	$V_{I(bus)}$ = 0 to 2.5 V			40			40	µA
I_{OS}	Short-circuit output current	Terminal	V_{CC} = MAX		−15	−35	−75	−15	−35	−75	mA
		Bus	V_{CC} = MAX		−25	−50	−125	−25	−50	−125	
I_{CC}	Supply current		No load, V_{CC} = MAX	Terminal outputs low and enabled		42	56		42	65	mA
				Bus outputs low and enabled		52	85		52	80	
$C_{I/O(bus)}$	Bus-port capacitance		V_{CC} = 0 to 5 V,	$V_{I/O}$ = 0 to 2 V, f = 1 MHz		30			30		pF

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ V_{OH} applies to 3-state outputs only.

switching characteristics at V_{CC} = 4.75 V, 5 V, and 5.25 V, C_L = 50 pF (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A†	MIN	TYP‡	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	Terminal	Bus	See Figure 1	25°C		10	17	ns
					Full range			20	
t_{PHL}	Propagation delay time, high- to low-level output				25°C		10	14	
					Full range			16	
t_{PLH}	Propagation delay time, low- to high-level output	Bus	Terminal	See Figure 2	25°C		8	15	ns
					Full range			18	
t_{PHL}	Propagation delay time, high- to low-level output				25°C		8	15	
					Full range			18	
t_{PZH}	Output enable time to high level	TE	Bus	See Figure 3	25°C		24	30	ns
					Full range			41	
t_{PHZ}	Output disable time from high level				25°C		9	14	
					Full range			16	
t_{PZL}	Output enable time to low level				25°C		16	28	
					Full range			34	
t_{PLZ}	Output disable time from low level				25°C		12	19	
					Full range			24	
t_{PZH}	Output enable time to high level	TE	Terminal	See Figure 4	25°C		24	36	ns
					Full range			50	
t_{PHZ}	Output disable time from high level				25°C		10	18	
					Full range			23	
t_{PZL}	Output enable time to low level				25°C		15	26	
					Full range			30	
t_{PLZ}	Output disable time from low level				25°C		15	24	
					Full range			31	
t_{en}	Output pullup enable time	PE	Bus	See Figure 5	25°C		16	24	ns
					Full range			25	
t_{dis}	Output pullup disable time				25°C		9	16	
					Full range			20	

† Full range is −55°C to 125°C.
‡ All typical values are at V_{CC} = 5 V.

switching characteristics over recommended range of operating free-air temperature, V_{CC} = 5 V

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		7	20	ns
t_{PHL}	Propagation delay time, high- to low-level output					8	20	
t_{PLH}	Propagation delay time, low- to high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		7	14	ns
t_{PHL}	Propagation delay time, high- to low-level output					9	14	
t_{PZH}	Output enable time to high level	TE	Bus	C_L = 15 pF, See Figure 3		19	30	ns
t_{PHZ}	Output disable time from high level					5	12	
t_{PZL}	Output enable time to low level					16	35	
t_{PLZ}	Output disable time from low level					9	20	
t_{PZH}	Output enable time to high level	TE	Terminal	C_L = 15 pF, See Figure 4		13	30	ns
t_{PHZ}	Output disable time from high level					12	20	
t_{PZL}	Output enable time to low level					12	20	
t_{PLZ}	Output disable time from low level					11	20	
t_{en}	Output pullup enable time	PE	Bus	C_L = 15 pF, See Figure 5		11	22	ns
t_{dis}	Output pullup disable time					6	12	

† Typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

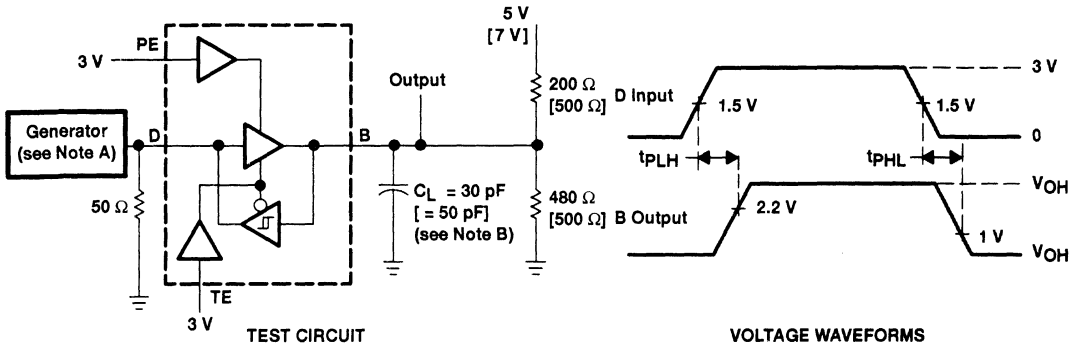


Figure 1. Terminal-to-Bus Test Circuit and Voltage Waveforms

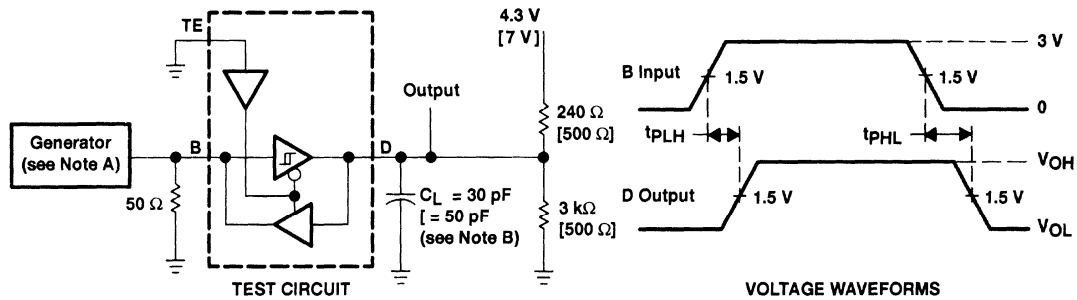


Figure 2. Bus-to-Terminal Test Circuit and Voltage Waveforms

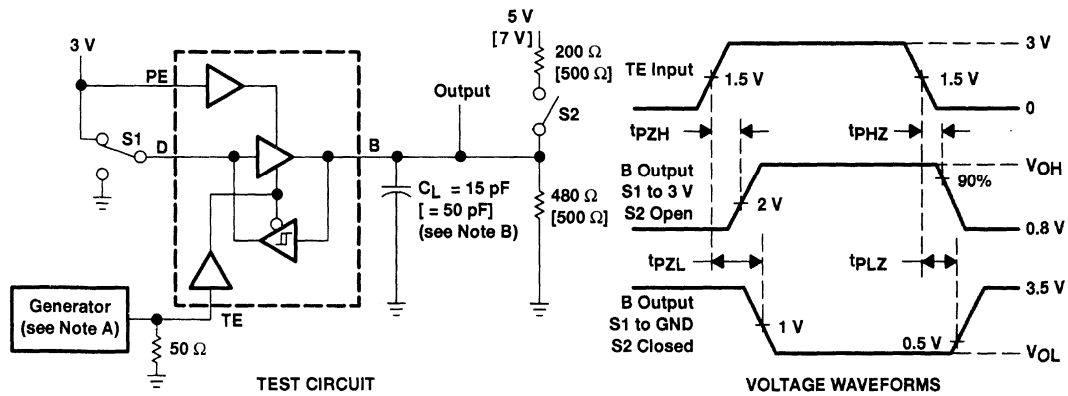


Figure 3. TE-to-Bus Test Circuit and Voltage Waveforms

[ ] denotes the SN55ALS160 military test conditions.

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

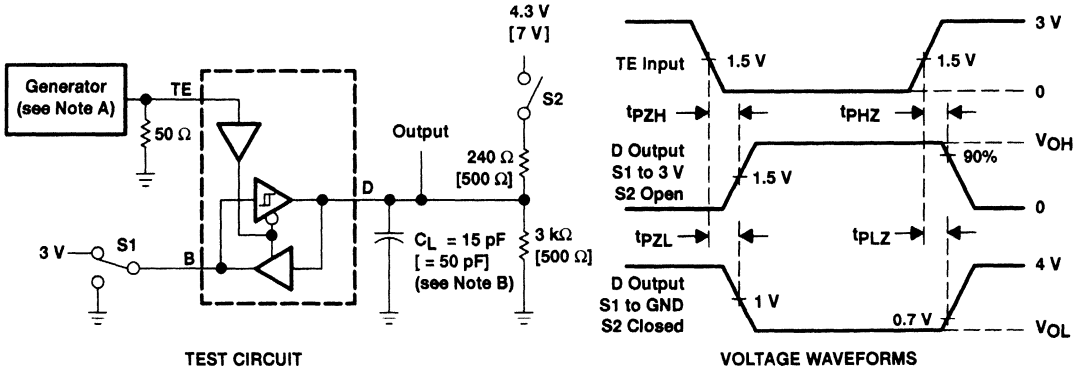


Figure 4. TE-to-Terminal Test Circuit and Voltage Waveforms

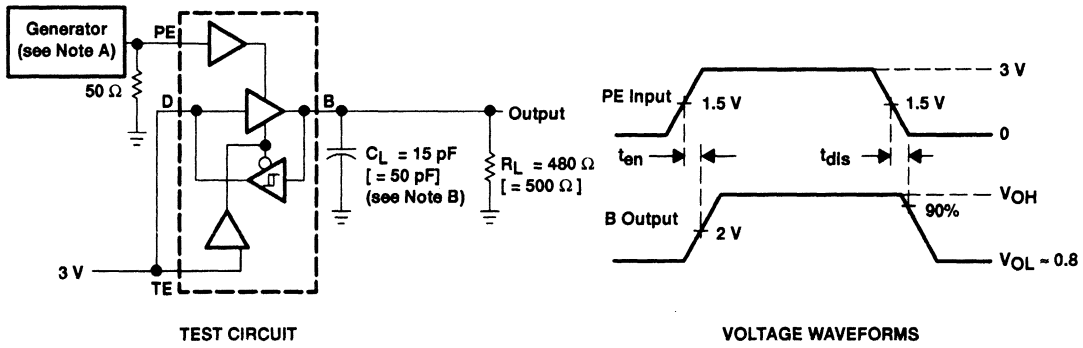


Figure 5. PE-to-Bus Test Circuit and Voltage Waveforms

[ ] denotes the SN55ALS160 military test conditions.

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

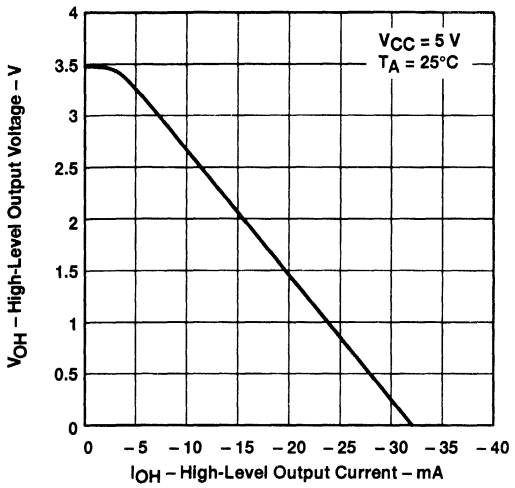


Figure 6

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

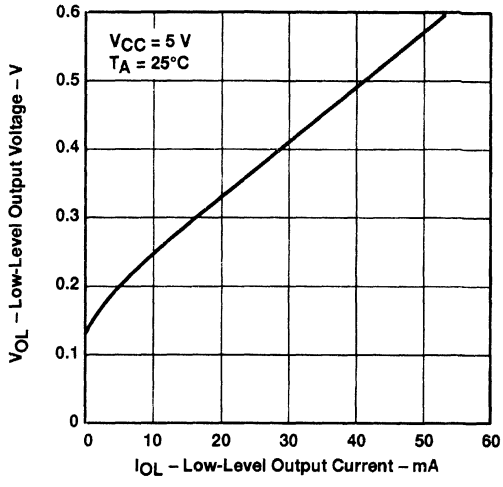


Figure 7

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

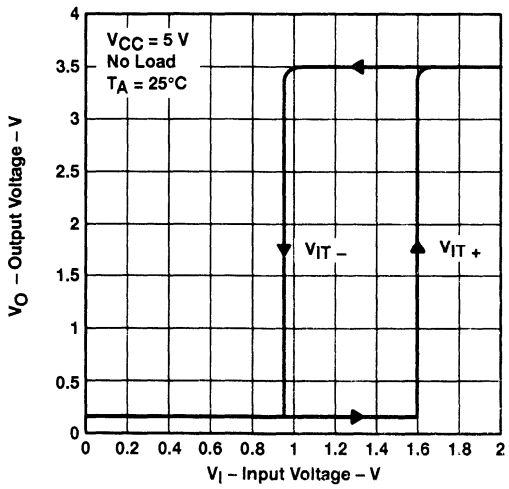


Figure 8

TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
BUS HIGH-LEVEL OUTPUT CURRENT

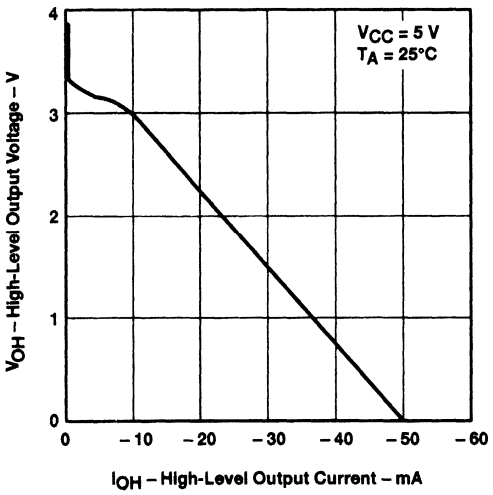


Figure 9

BUS LOW-LEVEL OUTPUT VOLTAGE
vs
BUS LOW-LEVEL OUTPUT CURRENT

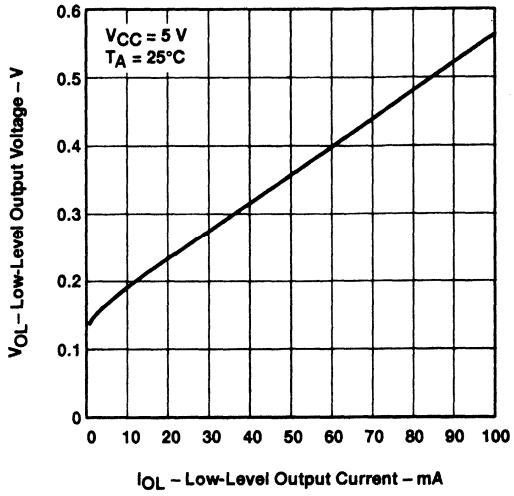


Figure 10

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

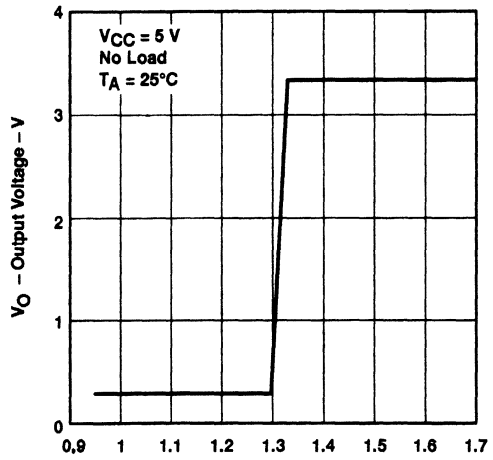


Figure 11

BUS CURRENT
vs
BUS VOLTAGE

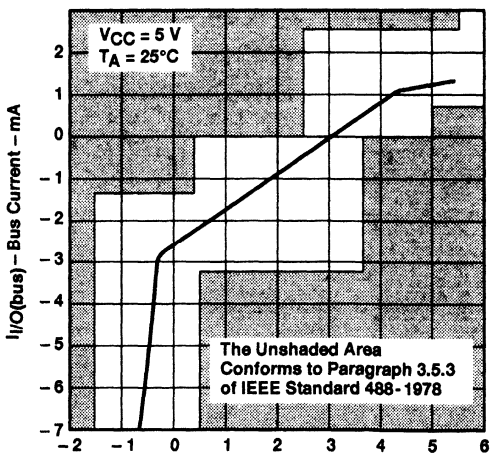


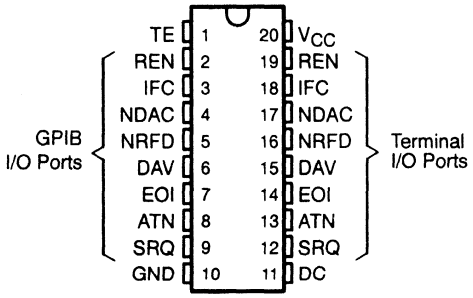
Figure 12

SLLS005B – OCTOBER 1980 – REVISED MAY 1995

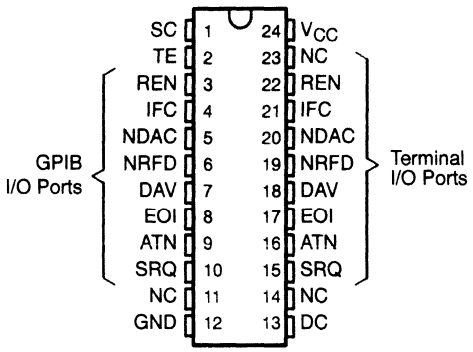
MEETS IEEE STANDARD 488-1978 (GPIB)

- 8-Channel Bidirectional Transceivers
- Power-Up/Power-Down Protection (Glitch Free)
- Designed to Implement Control Bus Interface
- SN75161B Designed for Single Controller
- SN75162B Designed for Multiple Controllers
- High-Speed, Low Power Schottky Circuitry
- Low Power Dissipation . . . 72 mW Max Per Channel
- Fast Propagation Times . . . 22 ns Max
- High-Impedance pnp Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Bus-Terminating Resistors Provided on Driver Outputs
- No Loading of Bus When Device Is Powered Down (V_{CC} = 0)

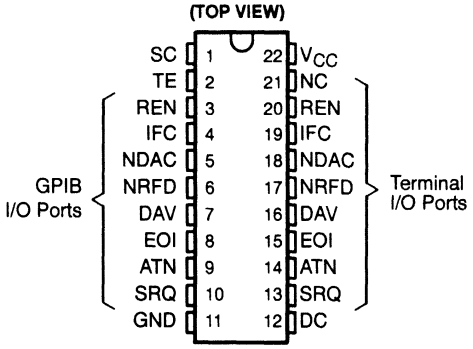
SN75161B . . . DW OR N PACKAGE
(TOP VIEW)



SN75162B . . . DW PACKAGE
(TOP VIEW)



SN75162B . . . N PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN75161B and SN75162B eight-channel, general-purpose interface bus transceivers are monolithic, high-speed, low-power Schottky devices designed to meet the requirements of IEEE Standard 488-1978. Each transceiver is designed to provide the bus-management and data-transfer signals between operating units of a single- or multiple-controller instrumentation system. When combined with the SN75160B octal bus transceiver, the SN75161B or SN75162B provides the complete 16-wire interface for the IEEE-488 bus.

The SN75161B and SN75162B each features eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. A power-up/-down disable circuit is included on all bus and receiver outputs. This provides glitch-free operation during V_{CC} power up and power down. The direction of data through these driver-receiver pairs is determined by the DC, TE, and SC (on SN75162B) enable signals. The SC input on the SN75162B allows the REN and IFC transceivers to be controlled independently.

description (continued)

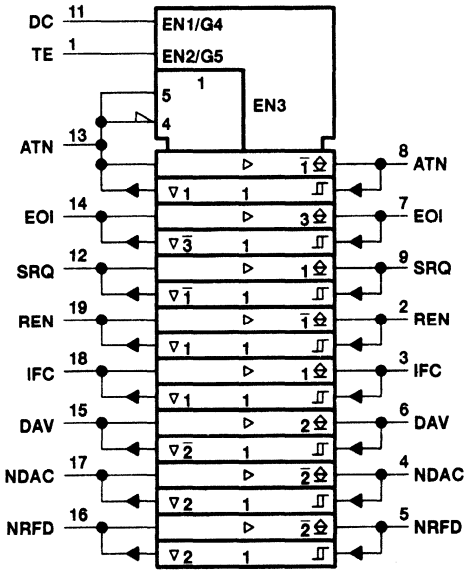
The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when supply voltage V_{CC} is 0. The drivers are designed to handle loads up to 48 mA of sink current. Each receiver features pnp transistor inputs for high input impedance and hysteresis of 400 mV for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

The SN75161B and SN75162B are characterized for operation from 0°C to 70°C.

CHANNEL IDENTIFICATION TABLE

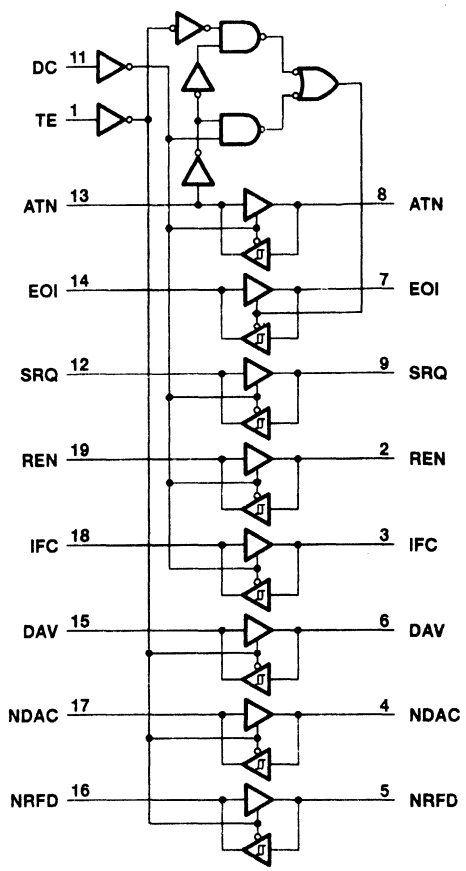
NAME	IDENTITY	CLASS
DC	Direction Control	
TE	Talk Enable	Control
SC	System Control (SN75162B only)	
ATN	Attention	
SRQ	Service Request	
REN	Remote Enable	Bus
IFC	Interface Clear	Management
EOI	End of Identity	
DAV	Data Valid	
NDAC	Not Data Accepted	Data
NRFD	Not Ready for Data	Transfer

SN75161B logic symbol†

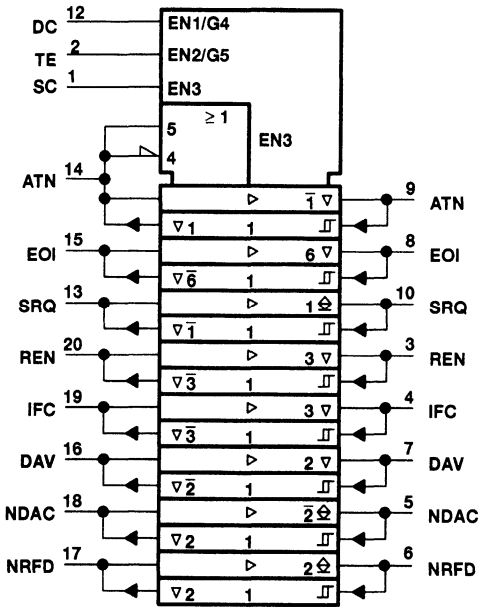


†This symbol is in accordance with IEEE Std 91-1984 and IEC Publication 617-12.
▽ Designates 3-state outputs
⏛ Designates passive-pullup outputs

SN75161B logic diagram (positive logic)

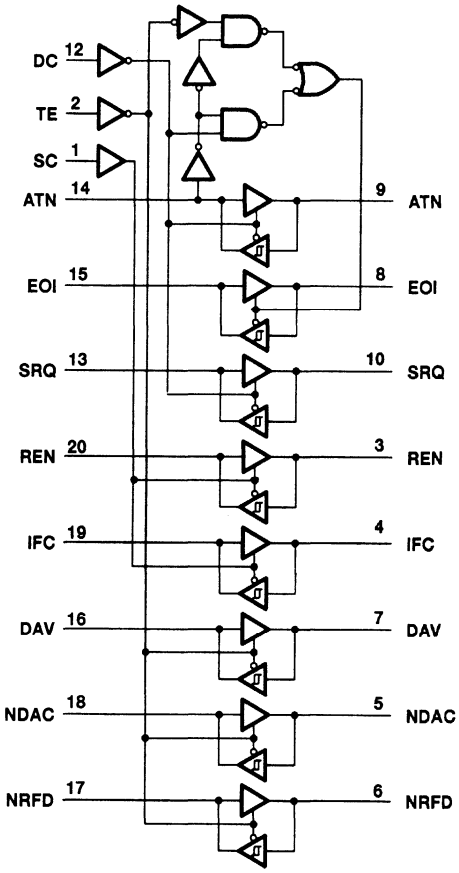


SN75162B logic symbol†



†This symbol is in accordance with IEEE Std 91-1984 and IEC Publication 617-12.
▽ Designates 3-state outputs
⏀ Designates passive-pullup outputs

SN75162B logic diagram (positive logic)



Pin numbers shown are for the N package.

Function Tables

SN75161B RECEIVE/TRANSMIT

CONTROLS			BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
DC	TE	ATN†	ATN†	SRQ	REN	IFC	EOI	DAV	NDAC	NRFD
			(Controlled by DC)					(Controlled by TE)		
H	H	H	R	T	R	R	T	T	R	R
H	H	L					R			
L	L	H	T	R	T	T	R	R	T	T
L	L	L					T			
H	L	X	R	T	R	R	R	R	T	T
L	H	X	T	R	T	T	T	T	R	R

SN75162B RECEIVE/TRANSMIT

CONTROLS				BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
SC	DC	TE	ATN†	ATN†	SRQ	REN	IFC	EOI	DAV	NDAC	NRFD
				(Controlled by DC)		(Controlled by SC)			(Controlled by TE)		
	H	H	H	R	T			T	T	R	R
	H	H	L					R			
	L	L	H	T	R			R	R	T	T
	L	L	L					T			
	H	L	X	R	T			R	R	T	T
	L	H	X	T	R			T	T	R	R
H						T	T				
L						R	R				

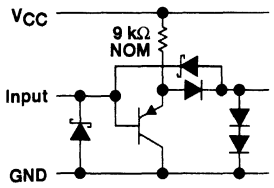
H = high level, L = low level, R = receive, T = transmit, X = irrelevant

Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.

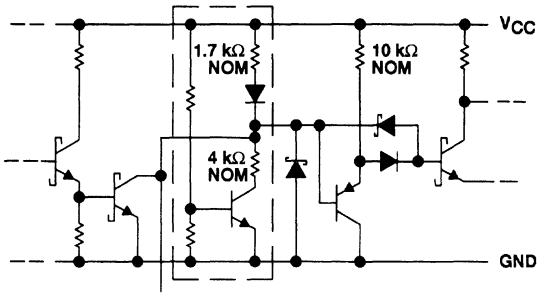
† ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS

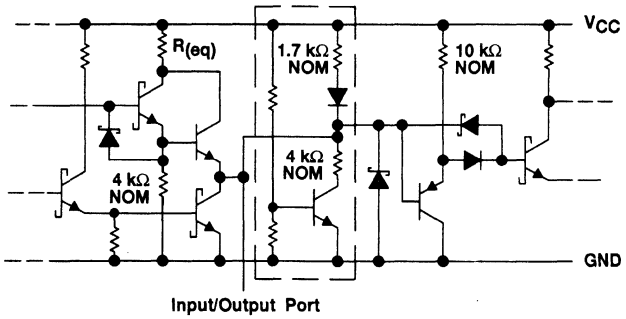


TYPICAL OF SRQ, NDAC, AND NRFD GPIB I/O PORT



Circuit inside dashed lines is on the driver outputs only.

TYPICAL OF ALL I/O PORTS EXCEPT SRQ, NDAC, AND NRFD GPIB I/O PORTS



Driver output $R_{(eq)}$ = 30 Ω NOM
Receiver output $R_{(eq)}$ = 110 Ω NOM
Circuit inside dashed lines is on the driver outputs only.
$R_{(eq)}$ = equivalent resistor

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I	5.5 V
Low-level driver output current, I_{OL}	100 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16) inch from the case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW (20 pin)	1125 mW	9.0 mW/°C	720 mW
DW (24 pin)	1350 mW	10.8 mW/°C	864 mW
N (20 pin)	1150 mW	9.2 mW/°C	736 mW
N (22 pin)	1700 mW	13.6 mW/°C	1088 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with 3-state outputs			−5.2	mA
	Terminal ports			−800	µA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		$I_I = -18$ mA			−0.8	−1.5	V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)	Bus	See Figure 7		0.4	0.65		V
V_{OH}‡	High-level output voltage	Terminal	$I_{OH} = -800$ μA		2.7	3.5		V
		Bus	$I_{OH} = -5.2$ mA		2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	$I_{OL} = 16$ mA			0.3	0.5	V
		Bus	$I_{OL} = 48$ mA			0.35	0.5	
I_I	Input current at maximum input voltage	Terminal	$V_I = 5.5$ V			0.2	100	μA
I_{IH}	High-level input current	Terminal and control inputs	$V_I = 2.7$ V			0.1	20	μA
I_{IL}	Low-level input current		$V_I = 0.5$ V			−10	−100	μA
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled	$I_{I(bus)} = 0$	2.5	3.0	3.7	V
				$I_{I(bus)} = -12$ mA			−1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled	$V_{I(bus)} = -1.5$ V to 0.4 V	−1.3			mA
				$V_{I(bus)} = 0.4$ V to 2.5 V	0		−3.2	
				$V_{I(bus)} = 2.5$ V to 3.7 V			2.5 −3.2	
				$V_{I(bus)} = 3.7$ V to 5 V	0		2.5	
				$V_{I(bus)} = 5$ V to 5.5 V	0.7		2.5	
		Power off	$V_{CC} = 0$,	$V_{I(bus)} = 0$ V to 2.5 V			−40	μA
I_{OS}	Short-circuit output current	Terminal			−15	−35	−75	mA
		Bus			−25	−50	−125	
I_{CC}	Supply current		No load,	TE, DE, and SC low			110	mA
$C_{I/O(bus)}$	Bus-port capacitance		$V_{CC} = 5$ V to 0, $V_{I/O} = 0$ to 2 V,	f = 1 MHz		16		pF

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
‡ V_{OH} applies for 3-state outputs only.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		14	20	ns
t_{PHL}	Propagation delay time, high- to low-level output					14	20	
t_{PLH}	Propagation delay time, low- to high-level output	Terminal	Bus (SRQ, NDAC, NRFD)	C_L = 30 pF, See Figure 1		29	35	ns
t_{PLH}	Propagation delay time, low- to high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		10	20	ns
t_{PHL}	Propagation delay time, high- to low-level output					15	22	
t_{PZH}	Output enable time to high level	TE,DC, or SC	Bus (ATN, EOI, REN, IFC, and DAV)	See Figure 3			60	ns
t_{PHZ}	Output disable time from high level						45	
t_{PZL}	Output enable time to low level						60	
t_{PLZ}	Output disable time from low level						55	
t_{PZH}	Output enable time to high level	TE,DC, or SC	Terminal	See Figure 4			55	ns
t_{PHZ}	Output disable time from high level						50	
t_{PZL}	Output enable time to low level						45	
t_{PLZ}	Output disable time from low level						55	

PARAMETER MEASUREMENT INFORMATION

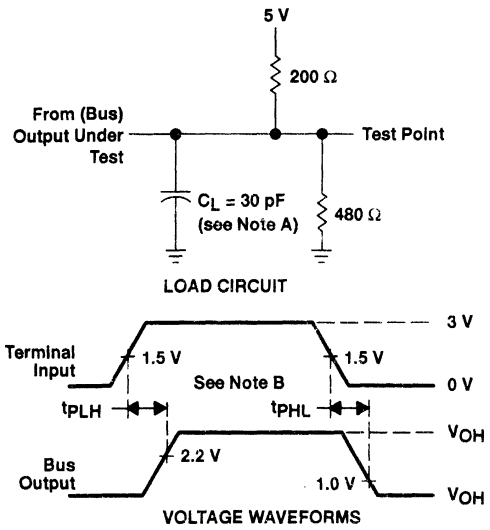


Figure 1. Terminal-to-Bus Load Circuit and Voltage Waveforms

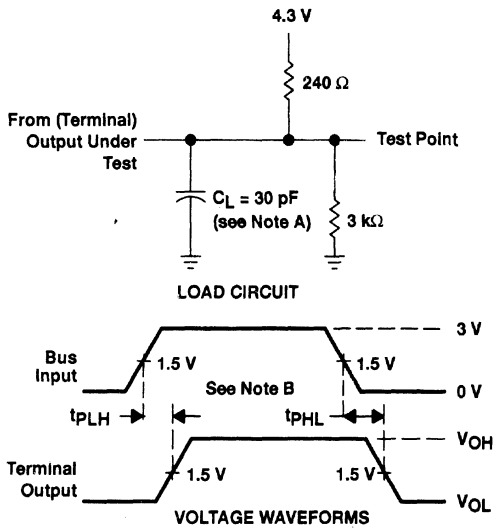


Figure 2. Bus-to-Terminal Load Circuit and Voltage Waveforms

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

PARAMETER MEASUREMENT INFORMATION

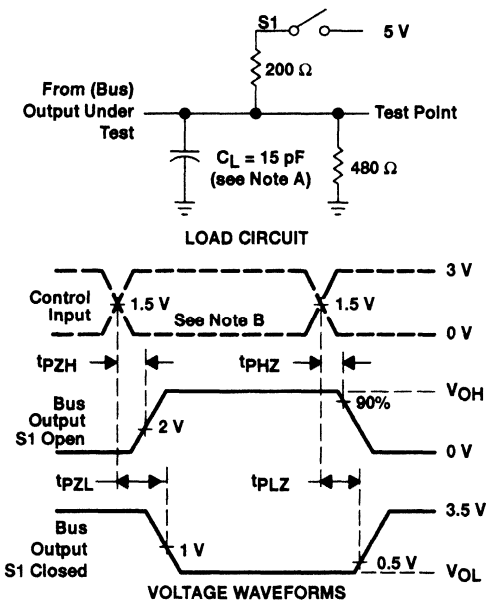


Figure 3. Bus Enable and Disable Times
Load Circuit and Voltage Waveforms

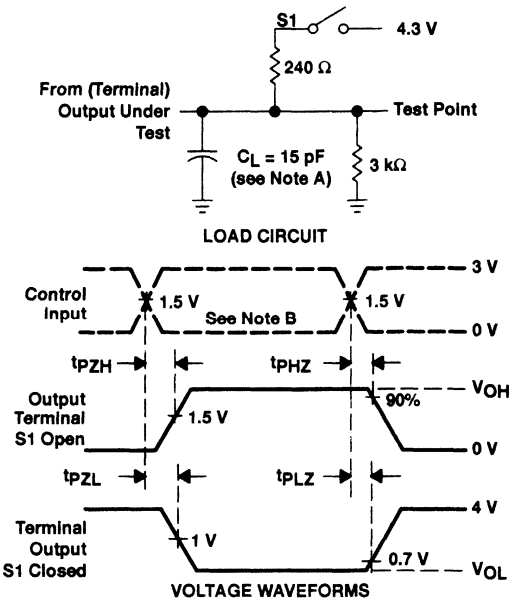


Figure 4. Terminal Enable and Disable Times
Load Circuit and Voltage Waveforms

NOTES: A. C_L includes probe and jig capacitance.
B. The Input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

TYPICAL CHARACTERISTICS

TERMINAL I/O PORTS
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

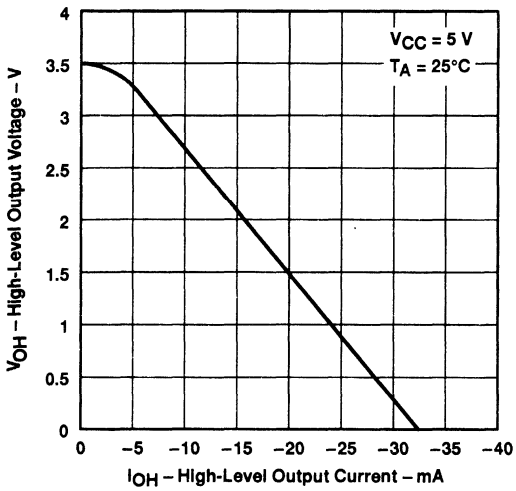


Figure 5

TERMINAL I/O PORTS
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

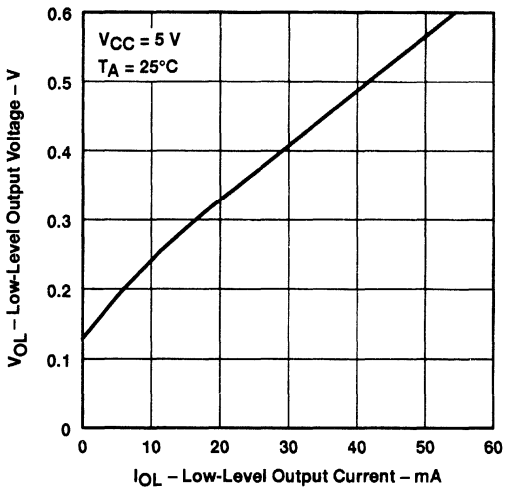


Figure 6

TERMINAL I/O PORTS
OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

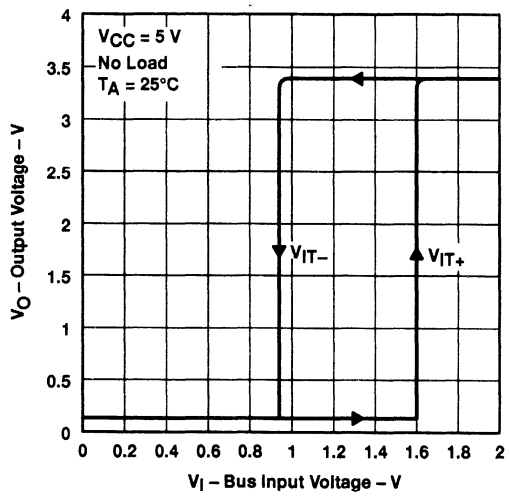


Figure 7

TYPICAL CHARACTERISTICS

GPIB I/O PORTS
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

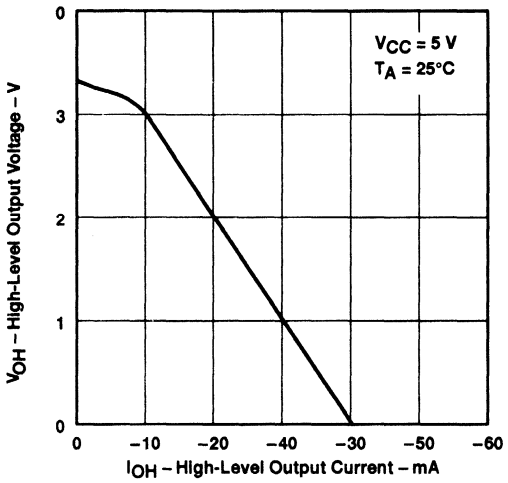


Figure 8

GPIB I/O PORTS
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

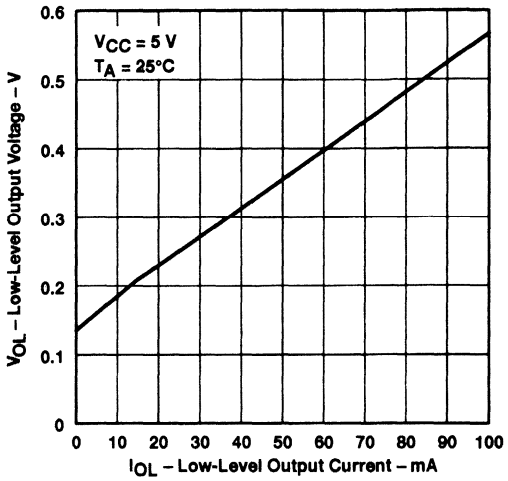


Figure 9

GPIB I/O PORTS
OUTPUT VOLTAGE
vs
THERMAL INPUT VOLTAGE

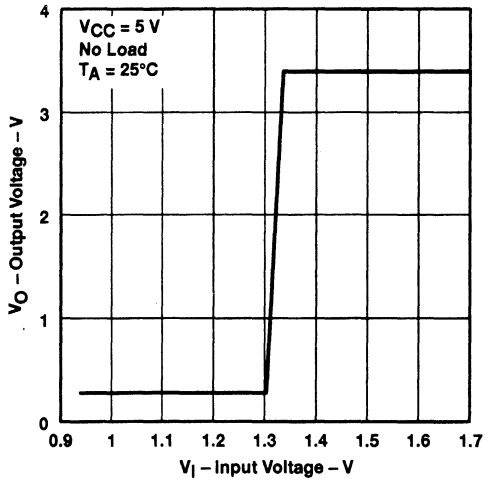


Figure 10

GPIB I/O PORTS
CURRENT
vs
VOLTAGE

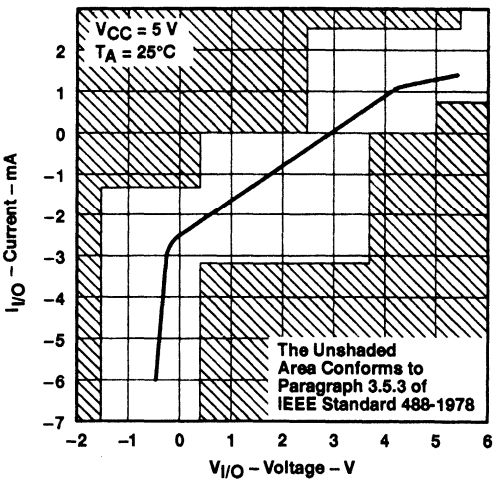


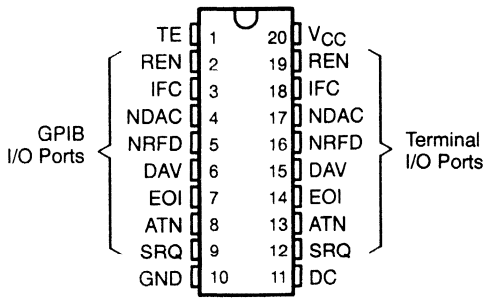
Figure 11

SLLS019D – JUNE 1986 – REVISED MAY 1995

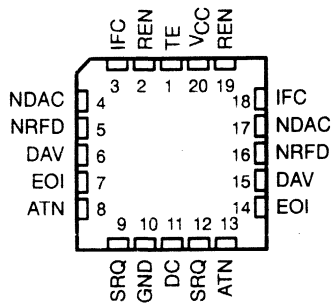
SUITABLE FOR IEEE STANDARD 488-1978 (GPIB)†

- 8-Channel Bidirectional Transceiver
- Designed to Implement Control Bus Interface
- Designed for Single Controller
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Power Dissipation:
  SN55ALS161 . . . 59 mW Max Per Channel
  SN75ALS161 . . . 46 mW Max Per Channel
- Fast Propagation Times:
  SN55ALS161 . . . 25 ns Max
  SN75ALS161 . . . 20 ns Max
- High-Impedance pnp Inputs
- Receiver Hysteresis:
  SN55ALS161 . . . 550 mV Typ
  SN75ALS161 . . . 650 mV Typ
- Bus-Terminating Resistors Provided on Driver Outputs
- No Loading of Bus When Device Is Powered Down (V_{CC} = 0)
- Power-Up/Power-Down Protection (Glitch Free)

SN55ALS161 . . . J OR W PACKAGE
SN75ALS161 . . . DW OR N PACKAGE
(TOP VIEW)



SN55ALS161 . . . FK PACKAGE
(TOP VIEW)



CHANNEL IDENTIFICATION TABLE

NAME	IDENTITY	CLASS
DC	Direction Control	Control
TE	Talk Enable	
ATN	Attention	Bus Management
SRQ	Service Request	
REN	Remote Enable	
IFC	Interface Clear	
EOI	End or Identify	
DAV	Data Valid	Data Transfer
NDAC	Not Data Accepted	
NRFD	Not Ready for Data	

description

The SN55ALS161 and SN75ALS161 eight-channel general-purpose interface bus transceivers are monolithic, high-speed, advanced low-power Schottky process devices designed to provide the bus-management and data-transfer signals between operating units of a single controller instrumentation system. When combined with the SN55ALS160 and SN75ALS160 octal bus transceivers, the 'ALS161 provides the complete 16-wire interface for the IEEE 488 bus.

The SN55ALS161 and SN75ALS161 feature eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. The direction of data through these driver-receiver pairs is determined by the DC and TE enable signals.

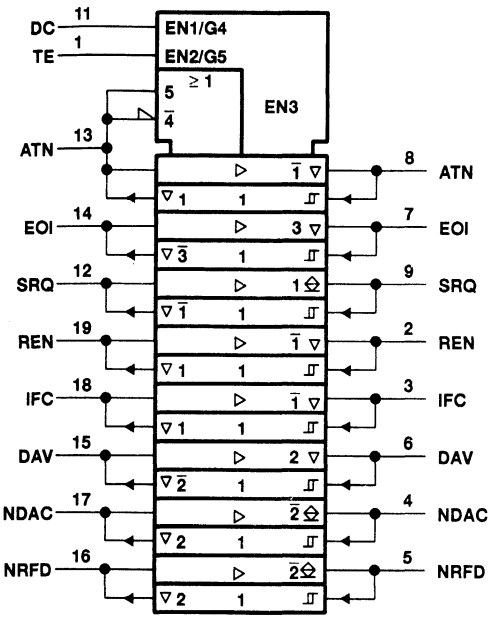
The driver outputs general-purpose interface bus (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when V_{CC} = 0. The drivers are designed to handle loads up to 48 mA of sink current. Each receiver features pnp transistor inputs for high input impedance and hysteresis of 400 mV on the commercial part, 250 mV on the military part minimum for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

† The transceivers are suitable for IEEE Standard 488 applications to the extent of the operating conditions and characteristics specified in this data sheet. Certain limits contained in the IEEE specification are not met or cannot be tested over the entire military temperature range.

description (continued)

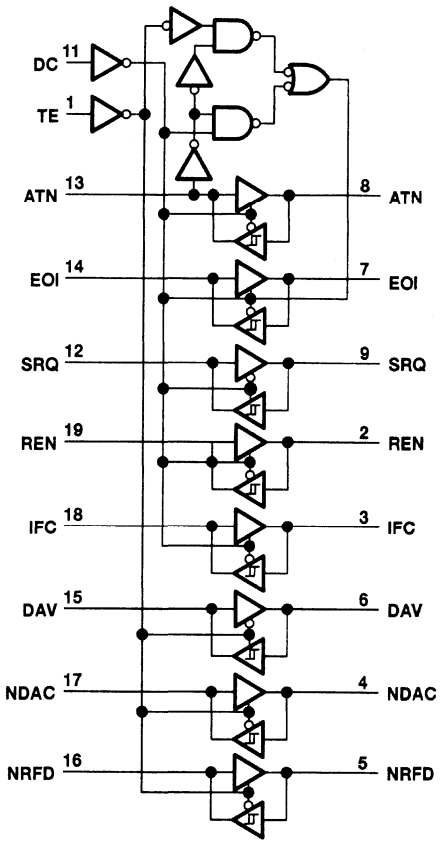
The SN55ALS161 is characterized for operation from −55°C to 125°C. The SN75ALS161 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
▽ Designates 3-state outputs
⏀ Designates passive-pullup outputs

logic diagram (positive logic)



RECEIVE/TRANSMIT FUNCTION TABLE

CONTROLS			BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
DC	TE	ATN†	ATN†	SRQ (controlled by DC)	REN	IFC	EOI	DAV	NDAC (controlled by TE)	NRFD
H	H	H	R	T	R	R	T	T	R	R
H	H	L					R			
L	L	H	T	R	T	T	R	R	T	T
L	L	L					T			
H	L	X	R	T	R	R	R	R	T	T
L	H	X	T	R	T	T	T	T	R	R

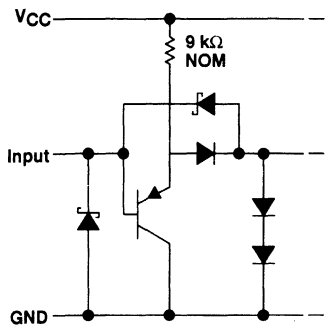
H = high level, L = low level, R = receive, T = transmit, X = irrelevant

Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.

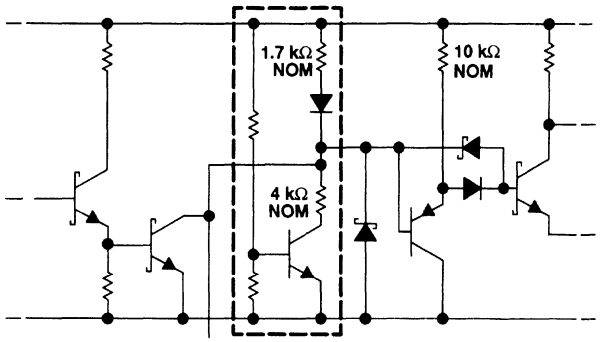
† ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS

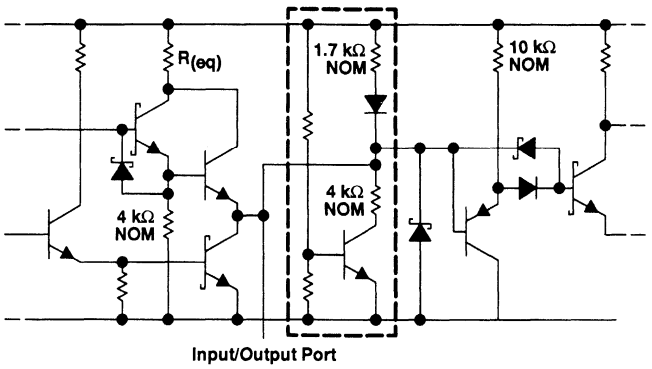


TYPICAL OF SRQ, NDAC, AND NRFD GPIB I/O PORT



Circuit inside dashed lines is on the driver outputs only.

TYPICAL OF ALL I/O PORTS EXCEPT SRQ, NDAC, NRFD GPIB I/O PORTS



Driver output $R_{(eq)}$ = 30 Ω NOM
Receiver output $R_{(eq)}$ = 110 Ω NOM
$R_{(eq)}$ = equivalent resistor
Circuit inside dashed lines is on the driver outputs only.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 5.5 V
Low-level driver output current, I_{OL} ..... 100 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN55ALS161 ..... −55°C to 125°C
SN75ALS161 ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Case temperature for 60 seconds: FK package, T_C ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J or W package ..... 300°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: DW or N package ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—
W	1000 mW	8.0 mW/°C	640 mW	200 mW

SN55ALS161 recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	TE and DC at T_A = −55°C to 125°C	2			V
	Bus and terminal at T_A = 25°C to 125°C	2			
	Bus and terminal at T_A = −55°C	2.1			
Low-level input voltage, V_{IL}	TE and DC at T_A = −55°C to 125°C			0.8	V
	Bus and terminal at T_A = 25°C to −55°C			0.8	
	Bus and terminal at T_A = 125°C			0.7	
High-level output current, I_{OH}	Bus ports with pullups active (V_{CC} = 5 V)			−5.2	mA
	Terminal ports			−800	µA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		−55		125	°C

SN75ALS161 recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with pullups active			– 5.2	mA
	Terminal ports			– 800	µA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			SN55ALS161			SN75ALS161			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage		I_I = –18 mA				–0.8	–1.5		–0.8	–1.5	V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)	Bus							0.4	0.65		V
		Bus	V_{CC} = 5 V,	T_A = –55°C and 25°C		0.4	0.55					
			V_{CC} = 5 V,	T_A = 125°C		0.25						
V_{OH}§	High-level output voltage	Terminal	I_{OH} = –800 µA			2.7	3.5		2.7	3.5		V
		Bus	I_{OH} = –5.2 mA,	V_{CC} = 5 V (SN55')		2.2			2.2			
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA,	V_{CC} = MIN			0.3	0.5		0.3	0.5	V
		Bus	I_{OL} = 48 mA,	V_{CC} = MIN	T_A = –55°C and 25°C (SN55')		0.35	0.5		0.35	0.5	
					T_A = 25°C (SN55')		0.35	0.5		0.35	0.5	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V,	V_{CC} = MAX			0.2	100		0.2	100	µA
I_{IH}	High-level input current	Terminal and control inputs	V_I = 2.7 V,	V_{CC} = MAX			0.1	20		0.1	20	µA
I_{IL}	Low-level input current		V_I = 0.5 V,	V_{CC} = MAX			–30	–100		–10	–100	µA
$V_{I/O}$	Voltage at GPIB I/O port		Driver disabled, V_{CC} = 5 V (SN55')	$I_{I(bus)}$ = 0		2.5	3	3.7	2.5	3	3.7	V
				$I_{I(bus)}$ = –12 mA				–1.5			–1.5	
$I_{I/O}$	Current into GPIB I/O port	Power on	Driver disabled, V_{CC} = 5 V (SN55')	$V_{I(bus)}$ = –1.5 V to 0.4 V		–1.3			–1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V		0		–3.2	0		–3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V				2.5 –3.2			2.5 –3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V		0		2.5	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V		0.7		2.5	0.7		2.5	
		Power off	V_{CC} = 0	$V_{I(bus)}$ = 0 to 2.5 V				40			40	µA
I_{OS}§	Short-circuit output current	Terminal	V_{CC} = MAX			–15	–35	–75	–15	–35	–75	mA
		Bus				–25	–50	–125	–25	–50	–125	
I_{CC}	Supply current		No load,	TE and DC low,	V_{CC} = MAX		55	90		55	75	mA
$C_{I/O}$	GPIB I/O port capacitance		V_{CC} = 0 to 5 V,	$V_{I/O}$ = 0 to 2 V,	f = 1 MHz		30			30		pF

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ V_{OH} and I_{OS} apply to 3-state outputs only.

SN55ALS161 switching characteristics, V_{CC} = 5 V and C_L = 50 pF (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	T_A†	MIN	TYP‡	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	Terminal	Bus (Except SRQ, NDAC, and NRFD)	See Figure 1	25°C		10	17	ns
					Full range			20	
t_{PHL}	Propagation delay time, high- to low-level output				25°C		10	14	
					Full range			16	
t_{PLH}	Propagation delay time, low- to high-level output	Terminal	Bus (NRFD, SRQ, NDAC)	See Figure 2	25°C			25	ns
					Full range			30	
t_{PHL}	Propagation delay time, high- to low-level output				25°C		10	14	
					Full range			16	
t_{PLH}	Propagation delay time, low- to high-level output	Bus	Terminal	See Figure 2	25°C		10	15	ns
					Full range			18	
t_{PHL}	Propagation delay time, high- to low-level output				25°C		10	15	
					Full range			18	
t_{PZH}	Output enable time to high level	TE or DC	Bus (ATN, REN, IFC, and DAV)	See Figure 3	25°C		20	30	ns
					Full range			41	
t_{PHZ}	Output disable time from high level				25°C		8	14	
					Full range			16	
t_{PZL}	Output enable time to low level				25°C		16	28	
					Full range			34	
t_{PLZ}	Output disable time from low level				25°C		10	19	
					Full range			24	
t_{PZH}	Output enable time to high level	TE or DC	Bus (EOI)	See Figure 3	25°C		24	30	ns
					Full range			48	
t_{PHZ}	Output disable time from high level				25°C		13	19	
					Full range			25	
t_{PZL}	Output enable time to low level,				25°C		21	35	
					Full range			43	
t_{PLZ}	Output disable time from low level				25°C		13	20	
					Full range			27	
t_{PZH}	Output enable time to high level	TE or DC	Terminal	See Figure 4	25°C		24	36	ns
					Full range			50	
t_{PHZ}	Output disable time from high level				25°C		12	20	
					Full range			33	
t_{PZL}	Output enable time to low level				25°C		20	34	
					Full range			41	
t_{PLZ}	Output disable time from low level				25°C		13	24	
					Full range			35	

† Full range is −55°C to 125°C.
‡ All typical values are at V_{CC} = 5 V.

SN75ALS161 switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		10	20	ns
t_{PHL}	Propagation delay time, high- to low-level output					12	20	
t_{PLH}	Propagation delay time, low- to high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		5	10	ns
t_{PHL}	Propagation delay time, high- to low-level output					7	14	
t_{PZH}	Output enable time to high level	TE or DC	Bus (ATN, EOI, REN, IFC, and DAV)	C_L = 15 pF, See Figure 3			30	ns
t_{PHZ}	Output disable time from high level						20	
t_{PZL}	Output enable time to low level						45	
t_{PLZ}	Output disable time from low level						20	
t_{PZH}	Output enable time to high level	TE or DC	Terminal	C_L = 15 pF, See Figure 4			30	ns
t_{PHZ}	Output disable time from high level						25	
t_{PZL}	Output enable time to low level						30	
t_{PLZ}	Output disable time from low level						25	

† All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

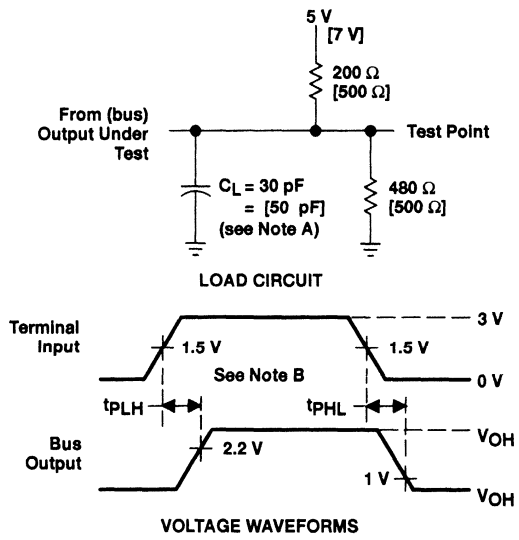


Figure 1. Terminal-to-Bus Load Circuit and Voltage Waveforms

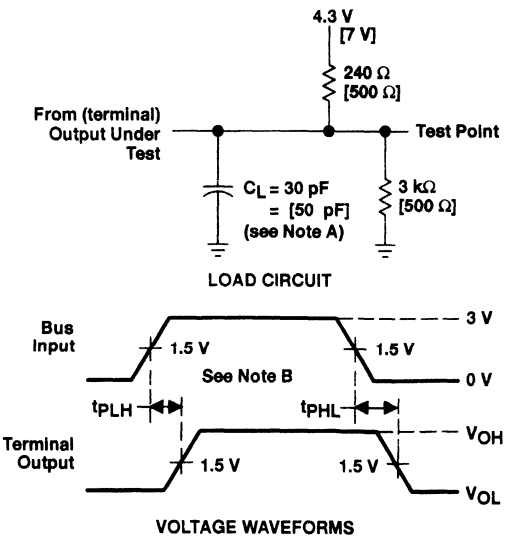


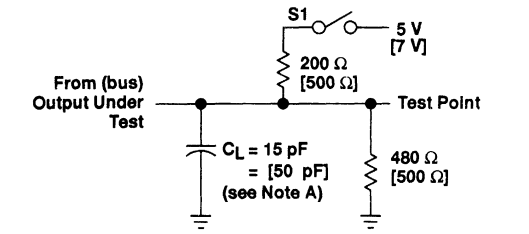
Figure 2. Bus-to-Terminal Load Circuit and Voltage Waveforms

[ ] denotes the SN55ALS161 military test conditions.

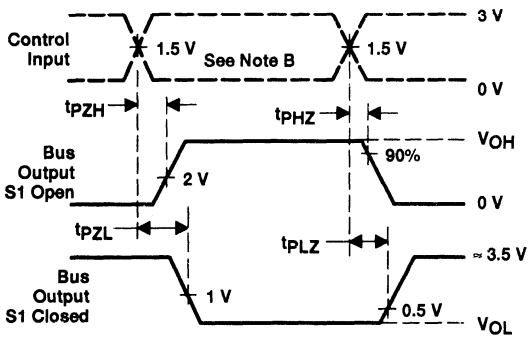
NOTES: A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

PARAMETER MEASUREMENT INFORMATION

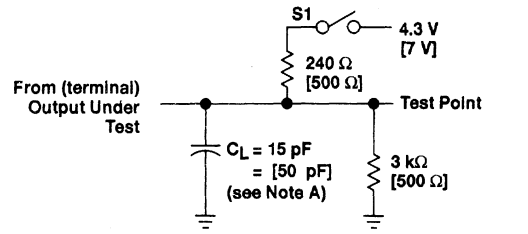


LOAD CIRCUIT

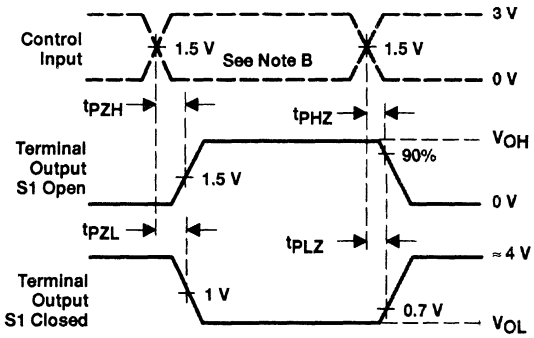


VOLTAGE WAVEFORMS

Figure 3. Bus Load Circuit and Voltage Waveforms



LOAD CIRCUIT



VOLTAGE WAVEFORMS

Figure 4. Terminal Load Circuit and Voltage Waveforms

[ ] denotes the SN55ALS161 military test conditions.

NOTES: A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

TYPICAL CHARACTERISTICS

TERMINAL I/O PORTS
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

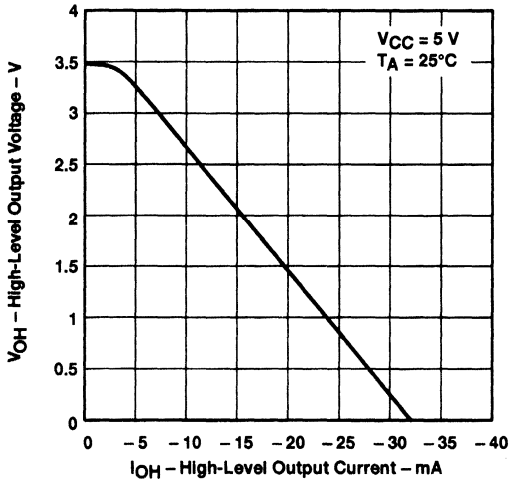


Figure 5

TERMINAL I/O PORTS
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

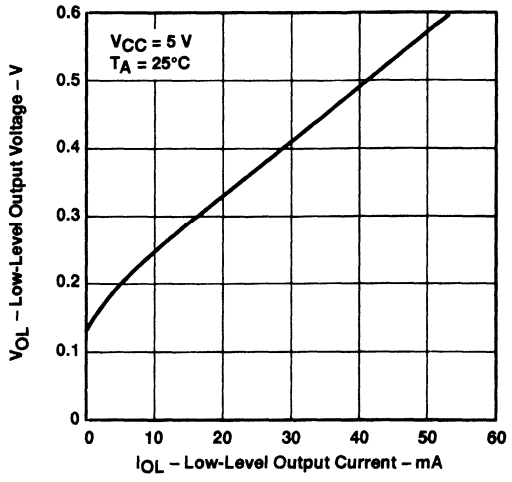


Figure 6

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

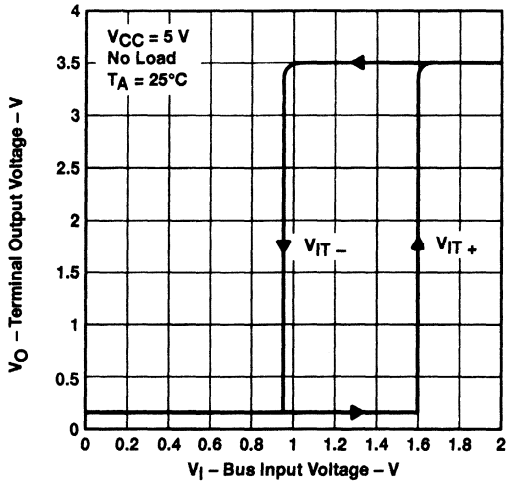


Figure 7

TYPICAL CHARACTERISTICS

GPIB I/O BUS
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

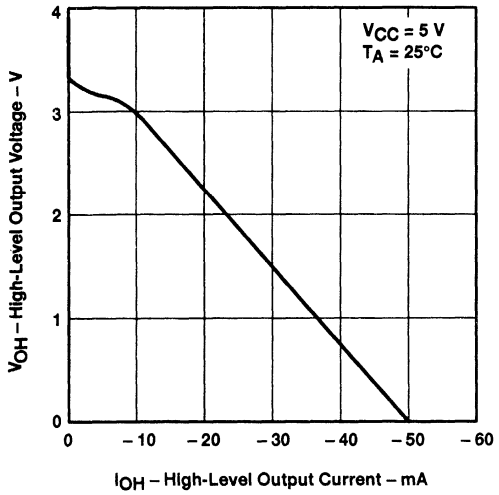


Figure 8

GPIB I/O BUS
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

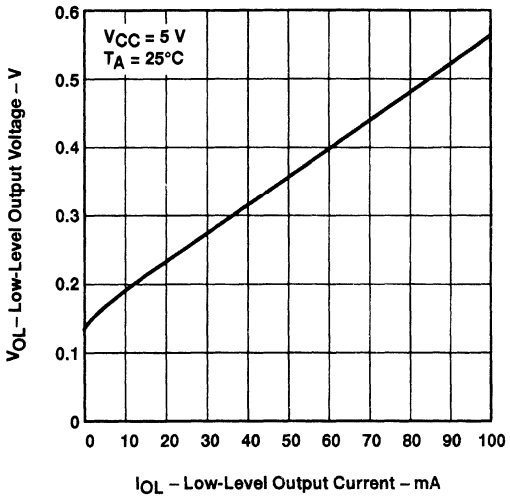


Figure 9

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

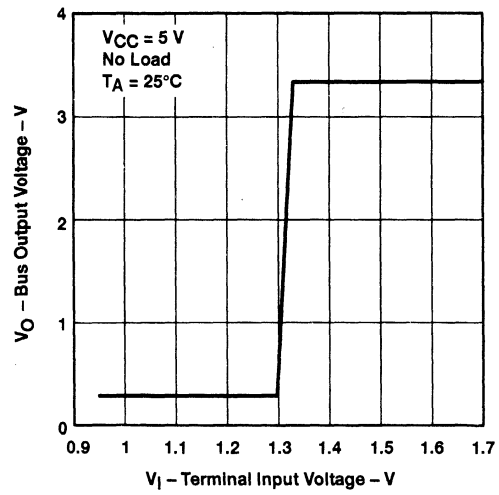


Figure 10

GPIB I/O BUS
CURRENT
vs
VOLTAGE

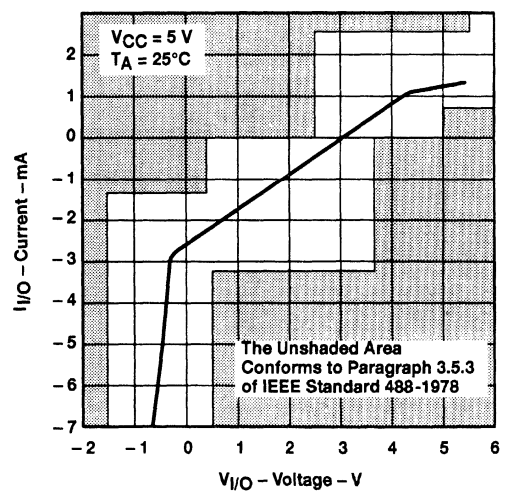


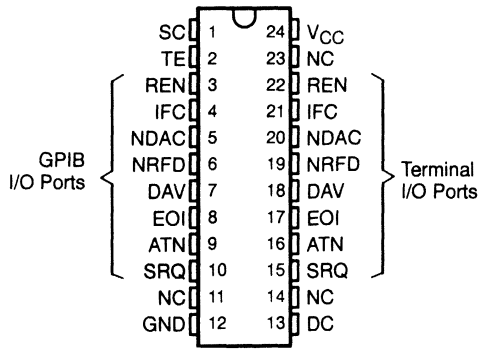
Figure 11

SLLS020C – JUNE 1986 – REVISED MAY 1995

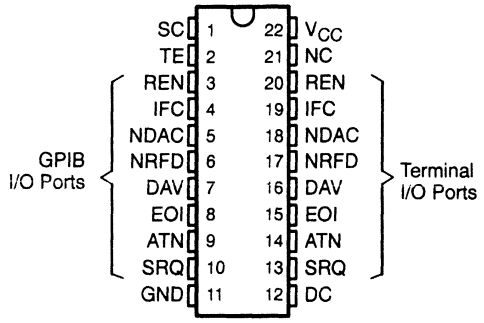
MEETS IEEE STANDARD 488-1978 (GPIB)

- **8-Channel Bidirectional Transceiver**
- **Designed to Implement Control Bus Interface**
- **Designed for Multicontrollers**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Low-Power Dissipation . . . 46 mW Max per Channel**
- **Fast Propagation Times . . . 20 ns Max**
- **High-Impedance PNP Inputs**
- **Receiver Hysteresis . . . 650 mV Typ**
- **Bus-Terminating Resistors Provided on Driver Outputs**
- **No Loading of Bus When Device Is Powered Down (V_{CC} = 0)**
- **Power-Up/Power-Down Protection (Glitch Free)**

DW PACKAGE
(TOP VIEW)



N PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN75ALS162 eight-channel general-purpose interface bus (GPIB) transceiver is a monolithic, high-speed, advanced low-power Schottky process device designed to provide the bus-management and data-transfer signals between operating units of a multiple-controller instrumentation system. When combined with the SN75ALS160 octal bus transceiver, the SN75ALS162 provides the complete 16-wire interface for the IEEE 488 bus.

The SN75ALS162 features eight driver-receiver pairs connected in a front-to-back configuration to form input/output (I/O) ports at both the bus and terminal sides. The direction of data through these driver-receiver pairs is determined by the DC, TE, and SC enable signals. The SC input allows the REN and IFC transceivers to be controlled independently.

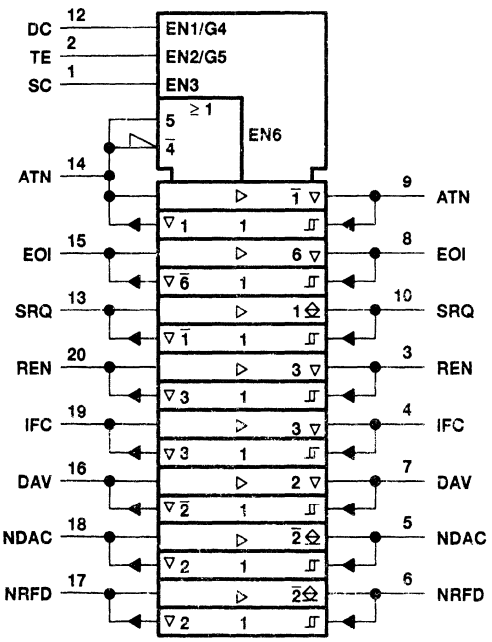
The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high impedance to the bus when V_{CC} = 0. The drivers are designed to handle loads up to 48 mA of sink current. Each receiver features pnp transistor inputs for high input impedance and hysteresis of 400 mV minimum for increased noise immunity. All receivers have 3-state outputs to present a high impedance to the terminal when disabled.

The SN75ALS162 is characterized for operation from 0°C to 70°C.

CHANNEL IDENTIFICATION TABLE

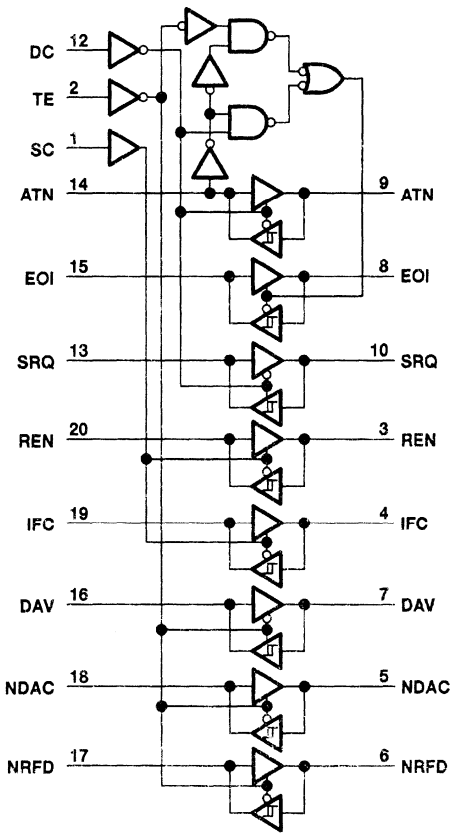
NAME	IDENTITY	CLASS
DC	Direction Control	Control
TE	Talk Enable	
SC	System Control	
ATN	Attention	Bus Management
SRQ	Service Request	
REN	Remote Enable	
IFC	Interface Clear	
EOI	End or Identify	
DAV	Data Valid	Data Transfer
NDAC	No Data Accepted	
NRFD	Not Ready for Data	

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
▽ Designates 3-state outputs
⏀ Designates passive-pullup outputs

logic diagram (positive logic)



Pin numbers shown are for the N package.

RECEIVE/TRANSMIT FUNCTION TABLE

CONTROLS				BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
SC	DC	TE	ATN†	ATN† (controlled by DC)	SRQ (controlled by DC)	REN (controlled by SC)	IFC (controlled by SC)	EOI	DAV (controlled by TE)	NDAC (controlled by TE)	NRFD (controlled by TE)
	H	H	H	R	T			T	T	R	R
	H	H	L					R			
	L	L	H	T	R			R	R	T	T
	L	L	L					T			
	H	L	X	R	T			R	R	T	T
	L	H	X	T	R			T	T	R	R
H						T	T				
L						R	R				

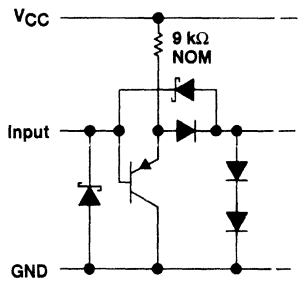
H = high level, L = low level, R = receive, T = transmit, X = irrelevant

Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.

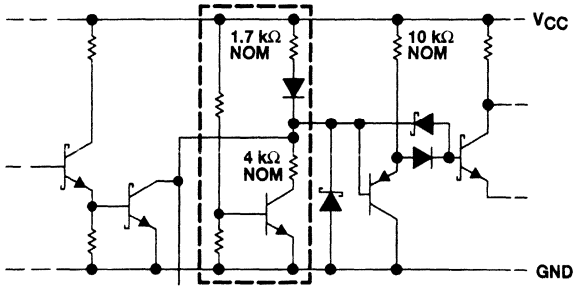
† ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS



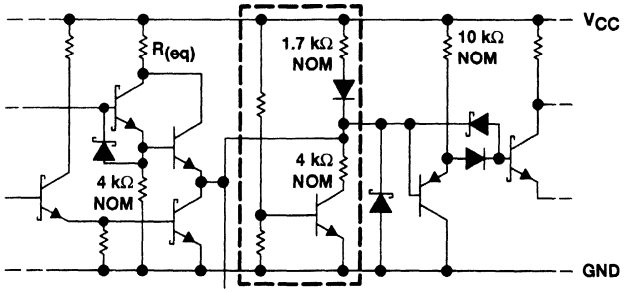
TYPICAL OF SRQ, NDAC, AND NRFD GPIB I/O PORT



Input/Output Port

Circuit inside dashed lines is on the driver outputs only.

TYPICAL OF ALL I/O PORTS EXCEPT SRQ, NDAC, NRFD GPIB I/O PORTS



Input/Output Port

Driver output $R_{(eq)}$ = 30 Ω NOM

Receiver output $R_{(eq)}$ = 110 Ω NOM

Circuit inside dashed lines is on the driver outputs only.

$R_{(eq)}$ = equivalent resistor

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 5.5 V
Low-level driver output current, I_{OL} ..... 100 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING
DW	1350 mW	10.8 mW/°C	864 mW
N	1700 mW	13.6 mW/°C	1088 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with 3-state outputs			– 5.2	mA
	Terminal ports			– 800	µA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = –18 mA			–0.8	–1.5	V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)	Bus			0.4	0.65		V
V_{OH}‡	High-level output voltage	Terminal	I_{OH} = –800 µA		2.7	3.5		V
		Bus	I_{OH} = –5.2 mA		2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA			0.3	0.5	V
		Bus	I_{OL} = 48 mA			0.35	0.5	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V			0.2	100	µA
I_{IH}	High-level input current	Terminal and control inputs	V_I = 2.7 V			0.1	20	µA
I_{IL}	Low-level input current		V_I = 0.5 V			–10	–100	µA
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled	$I_{I(bus)}$ = 0	2.5	3.0	3.7	V
				$I_{I(bus)}$ = –12 mA			–1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled	$V_{I(bus)}$ = –1.5 V to 0.4 V	–1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V	0		–3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V			+2.5 –3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V	0.7		2.5	
		Power off	V_{CC} = 0,	$V_{I(bus)}$ = 0 to 2.5 V			–40	µA
I_{OS}	Short-circuit output current	Terminal			–15	–35	–75	mA
		Bus			–25	–50	–125	
I_{CC}	Supply current		No load,	TE, DC, and SC low		55	75	mA
$C_{I/O(bus)}$	Bus-port capacitance		V_{CC} = 0 to 5 V,	$V_{I/O}$ = 0 to 2 V, f = 1 MHz		30		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ V_{OH} applies to 3-state outputs only.

switching characteristics over recommended range of operating free-air temperature, V_{CC} = 5 V

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		10	20	ns
t_{PHL}	Propagation delay time, high- to low-level output					12	20	
t_{PLH}	Propagation delay time, low- to high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		5	10	ns
t_{PHL}	Propagation delay time, high- to low-level output					7	14	
t_{PZH}	Output enable time to high level	TE, DC, or SC	Bus (ATN, EOI, REN, IFC, and DAV)	C_L = 15 pF, See Figure 3			30	ns
t_{PHZ}	Output disable time from high level						20	
t_{PZL}	Output enable time to low level						45	
t_{PLZ}	Output disable time from low level						20	
t_{PZH}	Output enable time to high level	TE, DC, or SC	Terminal	C_L = 15 pF, See Figure 4			30	ns
t_{PHZ}	Output disable time from high level						25	
t_{PZL}	Output enable time to low level						30	
t_{PLZ}	Output disable time from low level						25	

† All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

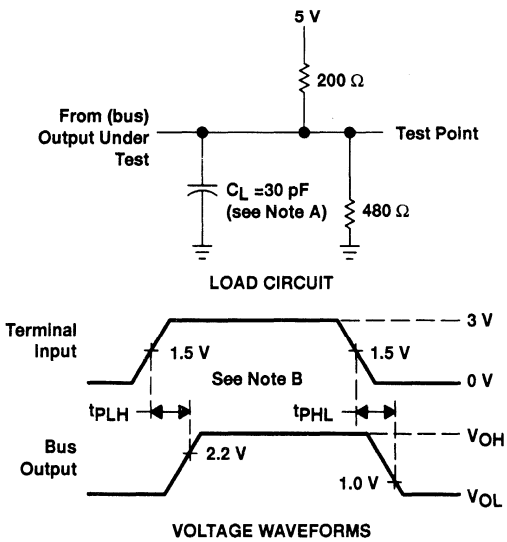


Figure 1. Terminal-to-Bus Load Circuit and Voltage Waveforms

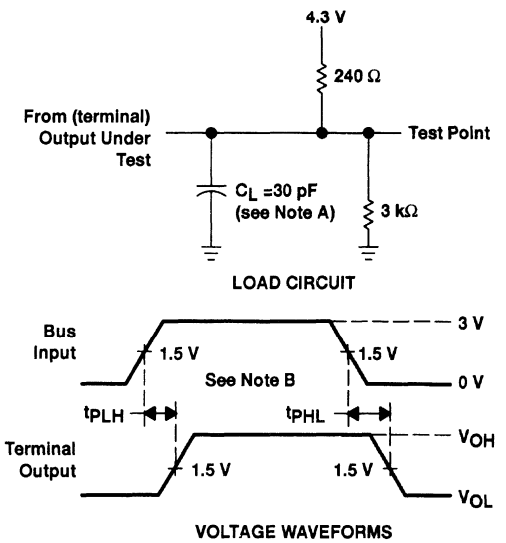
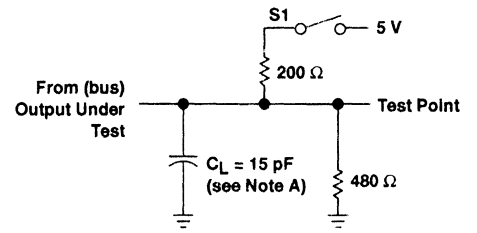


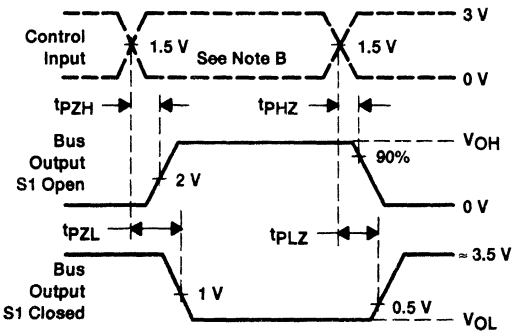
Figure 2. Bus-to-Terminal Load Circuit and Voltage Waveforms

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

PARAMETER MEASUREMENT INFORMATION

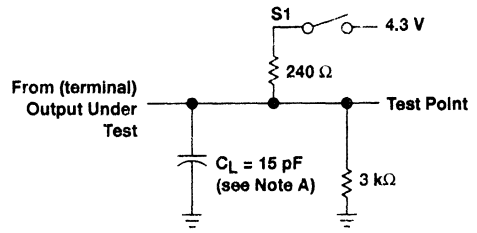


LOAD CIRCUIT

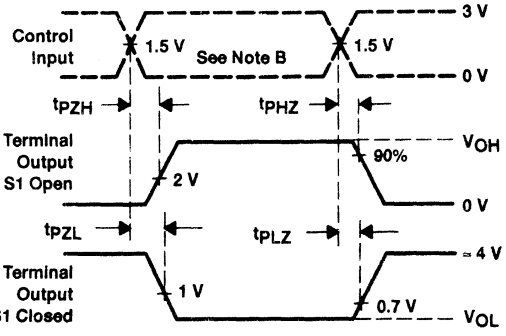


VOLTAGE WAVEFORMS

Figure 3. Bus Load Circuit and Voltage Waveforms



LOAD CIRCUIT



VOLTAGE WAVEFORMS

Figure 4. Terminal Load Circuit and Voltage Waveforms

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

TYPICAL CHARACTERISTICS

TERMINAL
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

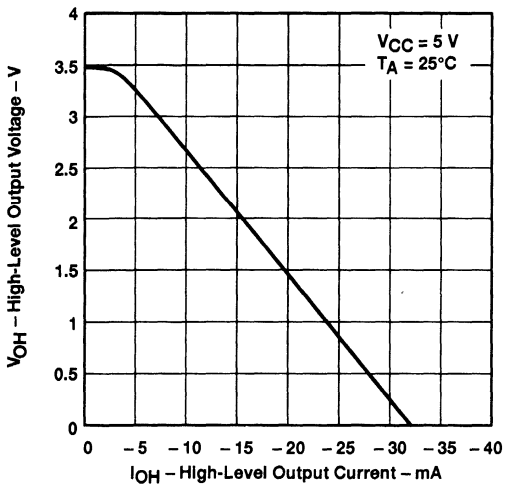


Figure 5

TERMINAL
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

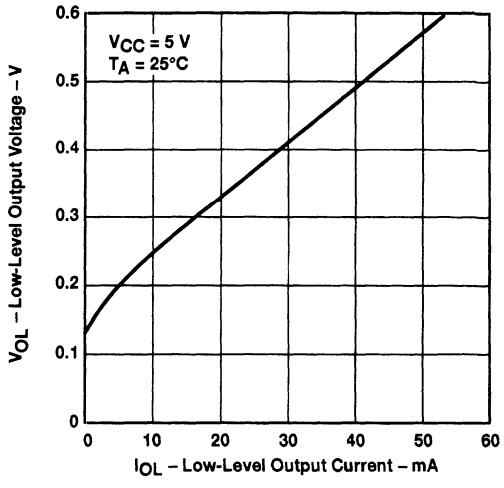


Figure 6

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

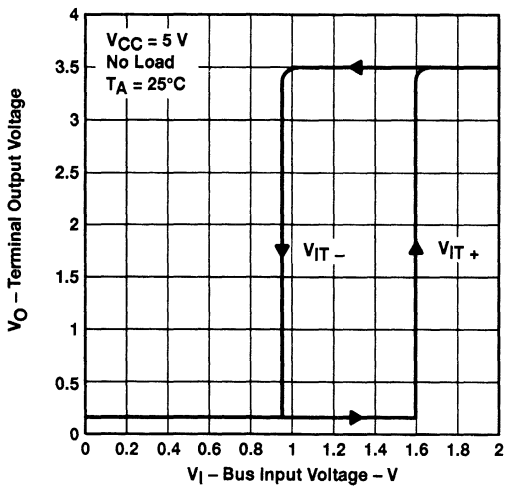


Figure 7

TYPICAL CHARACTERISTICS

BUS
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

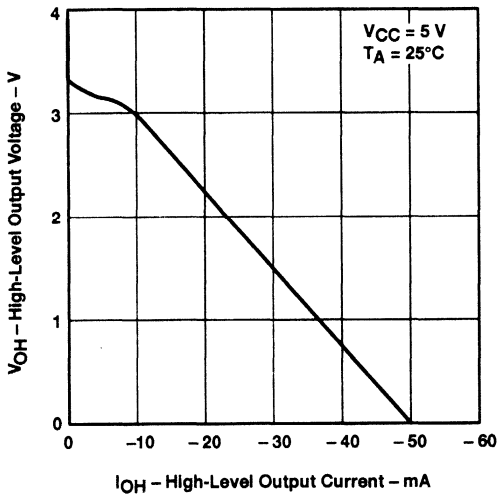


Figure 8

BUS
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

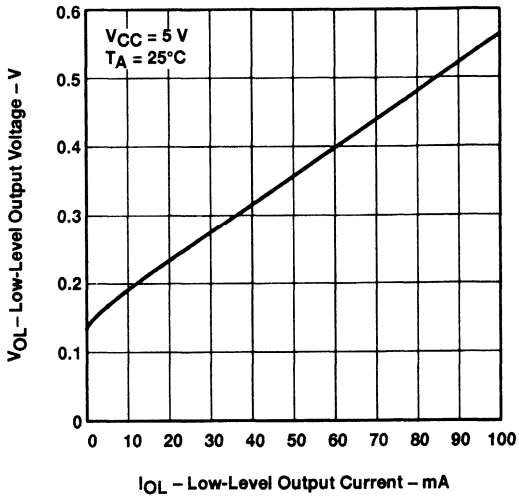


Figure 9

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

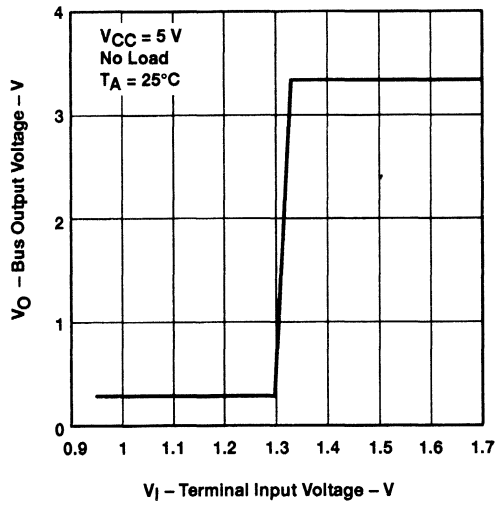


Figure 10

BUS
CURRENT
vs
VOLTAGE

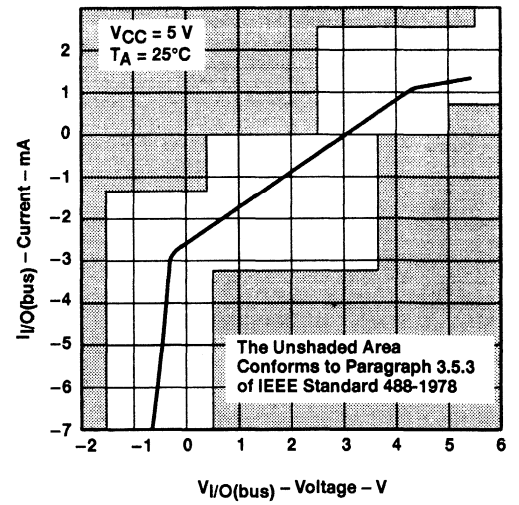


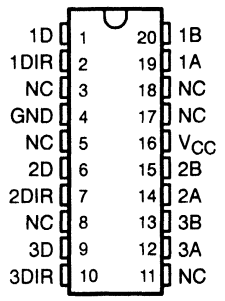
Figure 11

SN75ALS170, SN75ALS170A
TRIPLE DIFFERENTIAL BUS TRANSCEIVER

SLLS055D – AUGUST 1987 – REVISED SEPTEMBER 1995

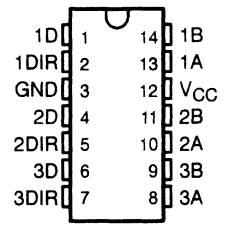
- **Three Bidirectional Transceivers**
- **Driver Meets or Exceeds ANSI Standard EIA/TIA-422-B and RS-485 and ITU Recommendation V.11**
- **Two Skew Limits Available**
- **Designed to Operate Up to 20 Million Data Transfers per Second (FAST-20 SCSI)**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Designed for Multipoint Transmission on Long Bus Lines In Noisy Environments**
- **Wide Positive and Negative Input/Output Bus Voltage Ranges**
- **Driver Output Capacity . . . ±60 mA**
- **Thermal Shutdown Protection**
- **Driver Positive- and Negative-Current Limiting**
- **Receiver Input Impedances . . . 12 kΩ Min**
- **Receiver Input Sensitivity . . . ±300 mV Max**
- **Receiver Input Hysteresis . . . 60 mV Typ**
- **Operates From a Single 5-V Supply**
- **Glitch-Free Power-Up and Power-Down Protection**
- **Features Independent Direction Controls for Each Channel**

DW PACKAGE
(TOP VIEW)



NC – No internal connection

J PACKAGE
(TOP VIEW)



description

The SN75ALS170 and SN75ALS170A triple differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and the driver meets ANSI Standards EIA/TIA-422-B and RS-485 and both the driver and receiver meet ITU Recommendation V.11. The SN75ALS170A is designed for FAST-20 SCSI and can transmit or receive data pulses as short as 30 ns with a maximum skew of 5 ns.

AVAILABLE OPTIONS

SKEW LIMIT	PART NUMBER	
10 ns	SN75ALS170DW	SN75ALS170J
5 ns	SN75ALS170ADW	

Function Tables

EACH DRIVER

INPUT D	DIR	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

EACH RECEIVER

DIFFERENTIAL INPUTS A – B	DIR	OUTPUT R
$V_{ID} \geq 0.3$ V	L	H
-0.3 V $< V_{ID} < 0.3$ V	L	?
$V_{ID} \leq -0.3$ V	L	L
X	H	Z
Open	L	H

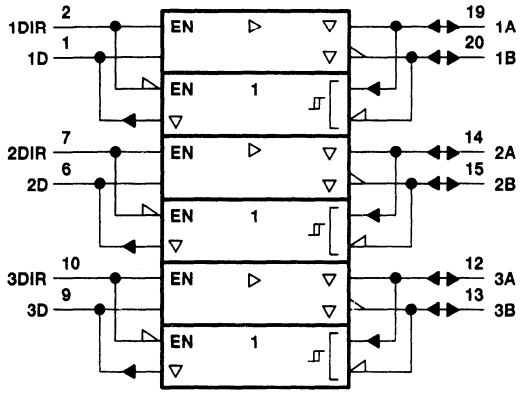
H = high level, L = low level, ? = indeterminate;
X = irrelevant, Z = high impedance (off)

description (continued)

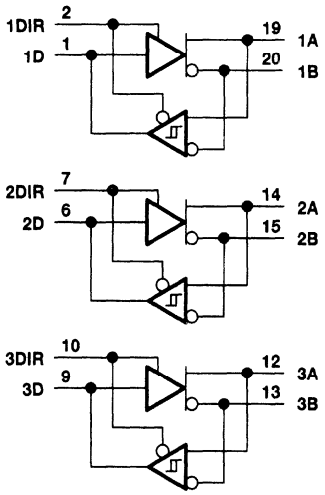
The SN75ALS170 and SN75ALS170A operate from a single 5-V power supply. The drivers and receivers have active-high and active-low enables, respectively, which are internally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The SN75ALS170 and the SN75ALS170A are characterized for operation from 0°C to 70°C.

logic symbol†

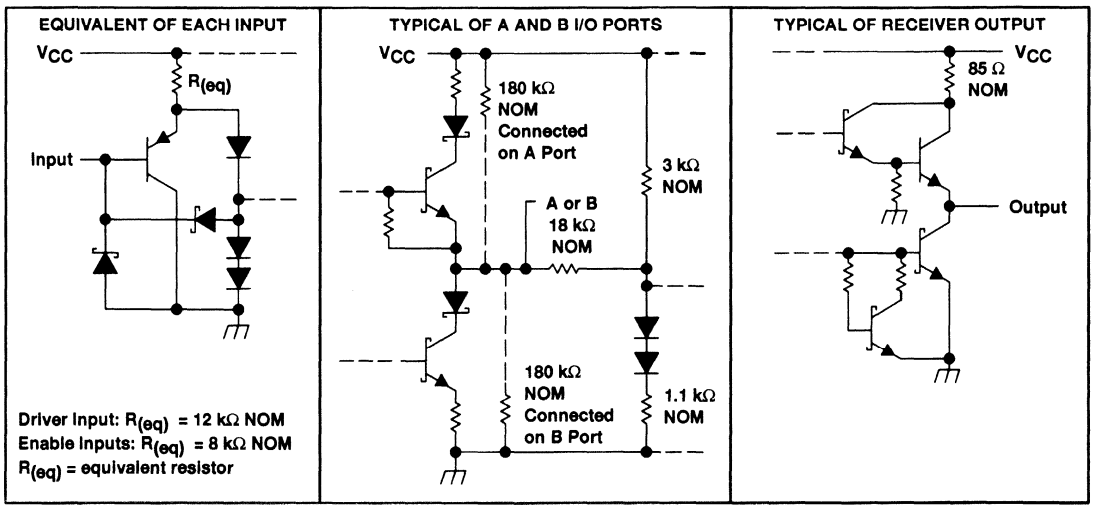


logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW package.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Voltage range at any bus terminal ..... −7 V to 12 V
Enable input voltage, V_I ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
J	1025 mW	8.2 mW/°C	656 mW

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12	V
				−7	
High-level input voltage, V_{IH}	D, DIR	2			V
Low-level input voltage, V_{IL}	D, DIR			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	µA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -19$ mA				−1.5	V
V_O	Output voltage	$I_O = 0$		0		6	V
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −55 mA	2.7			V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 55 mA			1.7	V
$\lvert V_{OD1} \rvert$	Differential output voltage	$I_O = 0$		1.5		6	V
$\lvert V_{OD2} \rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 1	1/2 V_{OD1} or 2§			V
		R_L = 54 Ω,	See Figure 1	1.5	2.5	5	V
V_{OD3}	Differential output voltage	V_{test} = −7 V to 12 V,	See Figure 2	1.5		5	V
$\Delta \lvert V_{OD} \rvert$	Change in magnitude of differential output voltage¶	R_L = 540 Ω or 100 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage					3	V
						−1	
$\Delta \lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage¶					±0.2	V
I_O	Output current	Output disabled, See Note 3	V_O = 12 V			1	mA
			V_O = −7 V			−0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−400	μA
I_{OS}	Short-circuit output current	V_O = −6 V				−250	mA
		V_O = 0				−150	
		$V_O = V_{CC}$				250	
		V_O = 8 V				250	
I_{CC}	Supply current	No load	Outputs enabled		69	90	mA
			Outputs disabled		57	78	

† The power-off measurement in ANSI Standard EIA/TIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.
§ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
¶ $\Delta \lvert V_{OD} \rvert$ and $\Delta \lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.

NOTE 3: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The EIA/TIA-422-B limit does not apply for a combined driver and receiver terminal.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	ALS170	R_L = 54 Ω,	C_L = 50 pF,	3	8	13	ns
		ALS170A	T_A = 25°C,	See Figure 3	5.5	8	10.5	
		ALS170	$R_{L1} = R_{L3}$ = 165 Ω,	R_{L2} = 75 Ω,	3	8	13	
		ALS170A	C_L = 60 pF, See Figure 4	T_A = 25°C,	5.5	8	10.5	
$t_{sk(p)}$	Pulse skew‡		R_L = 54 Ω, See Figure 3	C_L = 50 pF,		1	5	ns
			$R_{L1} = R_{L3}$ = 165 Ω, C_L = 60 pF,	R_{L2} = 75 Ω, See Figure 4		1	5	ns
$t_{sk(lim)}$	Skew limit§	ALS170	R_L = 54 Ω, See Figure 3	C_L = 50 pF,			10	ns
		ALS170A					5	
		ALS170	$R_{L1} = R_{L3}$ = 165 Ω, C_L = 60 pF,	R_{L2} = 75 Ω, See Figure 4			10	
		ALS170A					5	
$t_{t(OD)}$	Differential-output transition time		R_L = 54 Ω, See Figure 3	C_L = 50 pF,	3	8	13	ns
			$R_{L1} = R_{L3}$ = 165 Ω, C_L = 60 pF,	R_{L2} = 75 Ω, See Figure 4	3	8	13	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ Pulse skew is defined as the $|t_{d(ODH)} - t_{d(ODL)}|$ of each channel.
§ Skew limit is the maximum difference in propagation delay times between any two channels of one device and between any two devices. This parameter is applicable at one V_{CC} and operating temperature within the recommended operating conditions.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	EIA/TIA-422-B	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_O	V_O
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\|V_{OD3}\|$		V_t (Test Termination Measurement 2)
V_{test}		V_{tst}
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V}_{os}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.3	V
V_{IT-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.3‡			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)				60		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 300 mV, See Figure 5	I_{OH} = −400 µA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −300 mV, See Figure 5	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 2.4 V				20	µA
		V_O = 0.4 V				−400	
I_I	Line input current	Other input = 0, See Note 4	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	µA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	µA
r_I	Input resistance			12			kΩ
I_{OS}	Short-circuit output current	V_{ID} = 300 mV,	V_O = 0	−15		−85	mA
I_{CC}	Supply current	No load	Outputs enabled		69	90	mA
			Outputs disabled		57	78	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
NOTE 4: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	ALS170	V_{ID} = −1.5 V to 1.5 V, C_L = 15 pF, T_A = 25°C, See Figure 6	9		19	ns
		ALS170A		11.5		16.5	
t_{PHL}	Propagation delay time, high-to-low-level output	ALS170		9		19	ns
		ALS170A		11.5		16.5	
$t_{sk(p)}$	Pulse skew§	ALS170	V_{ID} = −1.5 V to 1.5 V, C_L = 15 pF, See Figure 6		2	6	ns
		ALS170A				5	
$t_{sk(lim)}$	Skew limit¶	ALS170				10	ns
		ALS170A				5	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
§ Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel.
¶ Skew limit is the maximum difference in propagation delay times between any two channels of one device and between any two devices. This parameter is applicable at one V_{CC} and operating temperature within the recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION

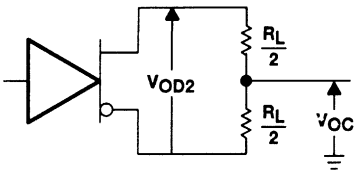


Figure 1. Driver V_{OD} and V_{OC}

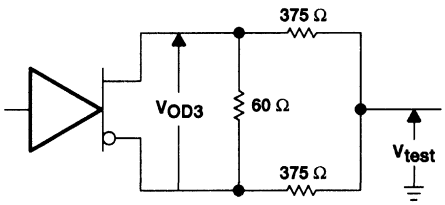
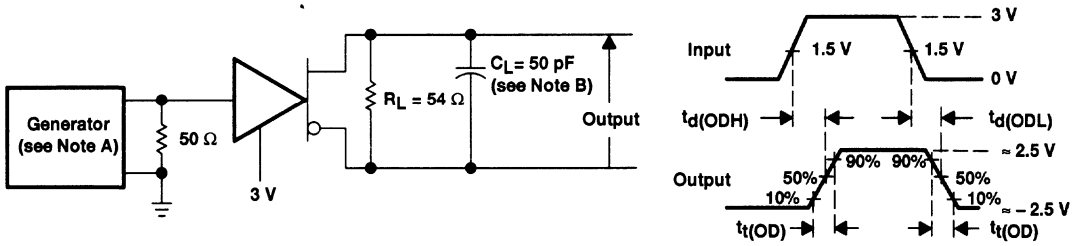


Figure 2. Driver V_{OD3}

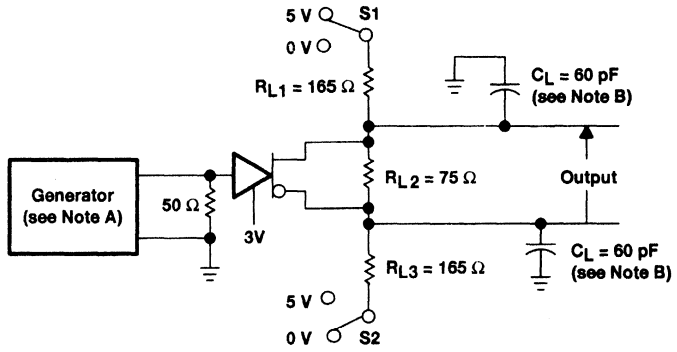


TEST CIRCUIT VOLTAGE WAVEFORMS

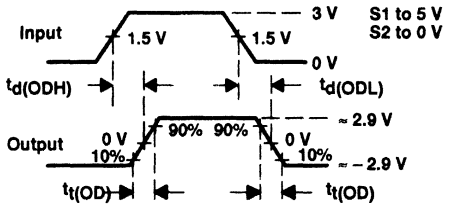
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

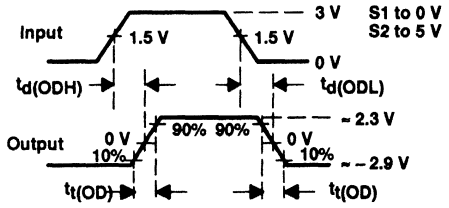
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 4. Driver Test Circuit and Voltage Waveforms With Double-Differential-SCSI Termination for the Load

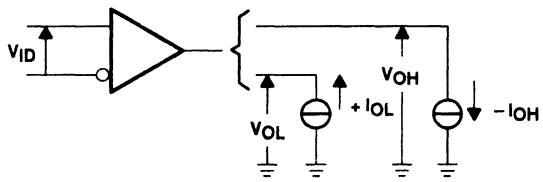
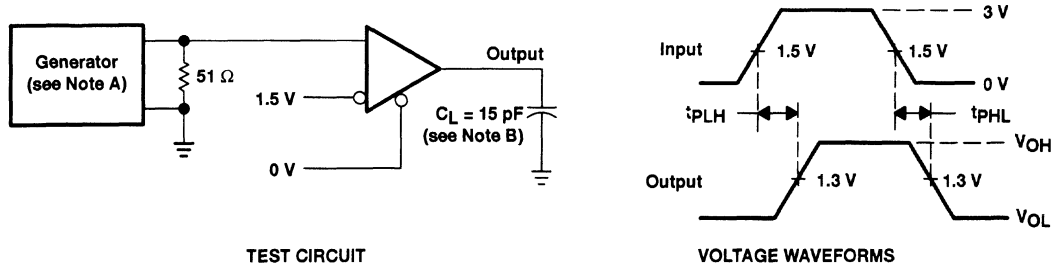


Figure 5. Receiver V_{OH} and V_{OL}

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 6. Receiver Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

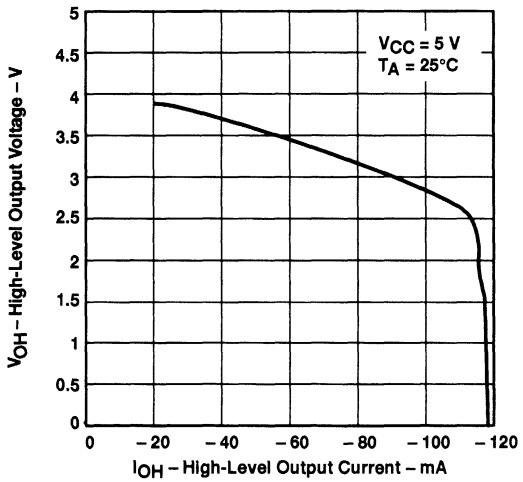


Figure 7

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

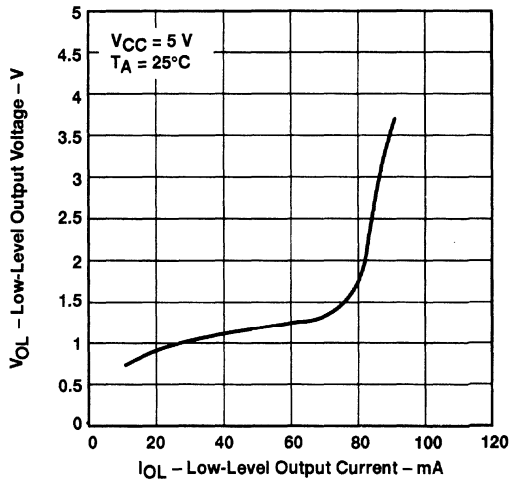


Figure 8

TYPICAL CHARACTERISTICS

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

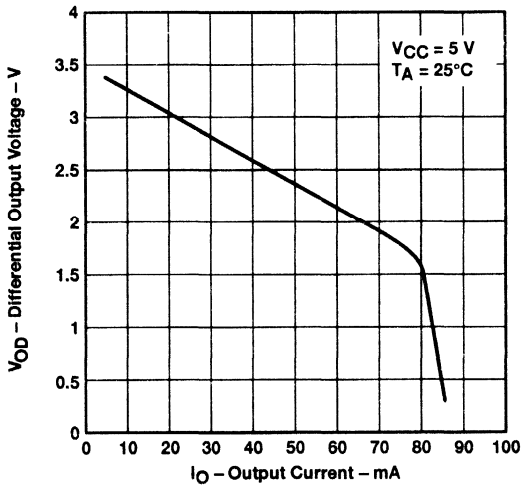


Figure 9

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

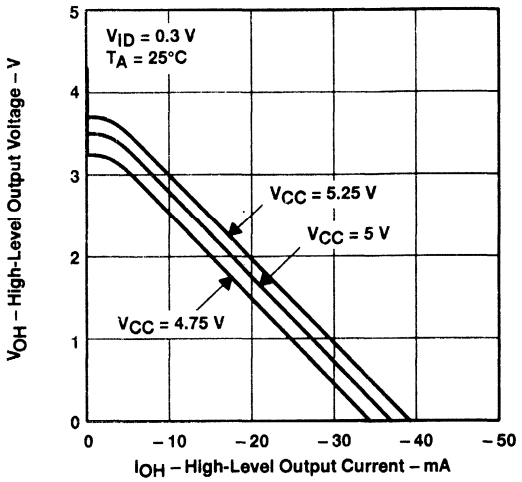


Figure 10

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

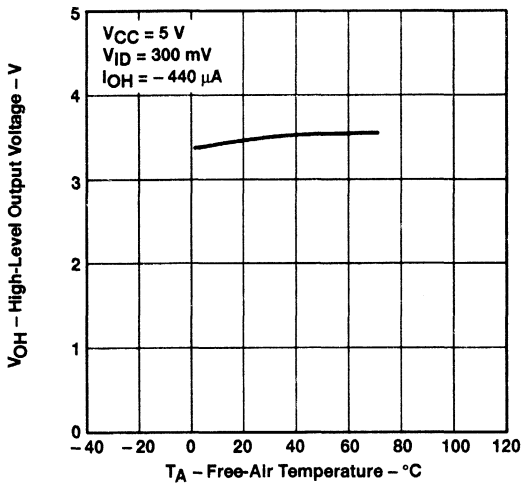


Figure 11

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

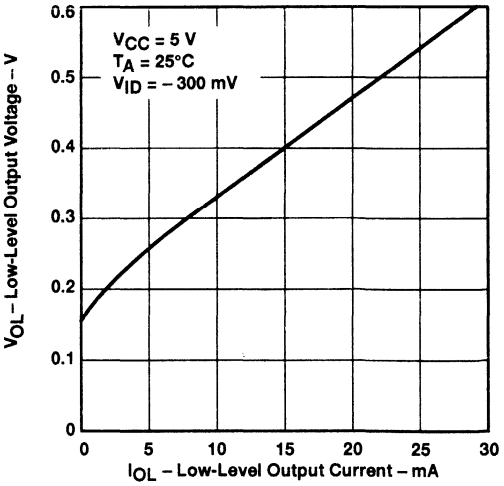


Figure 12

TYPICAL CHARACTERISTICS

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

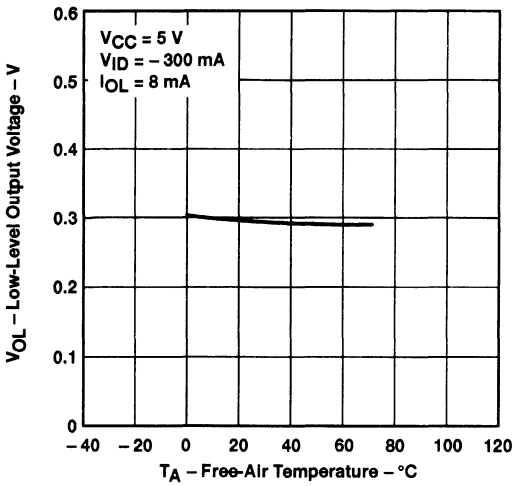


Figure 13

RECEIVER
OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

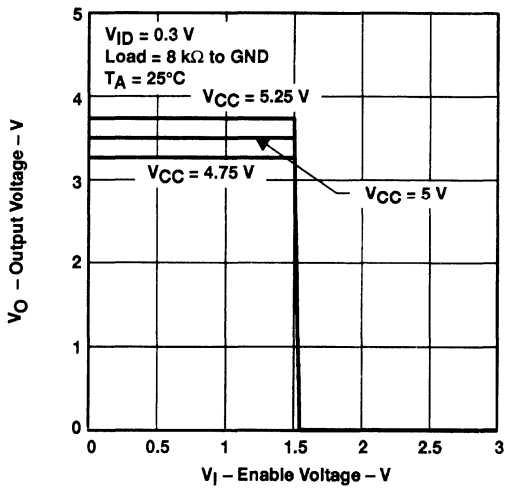


Figure 14

RECEIVER
OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

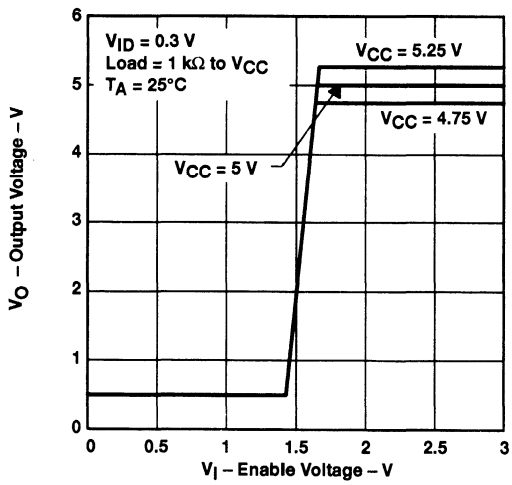
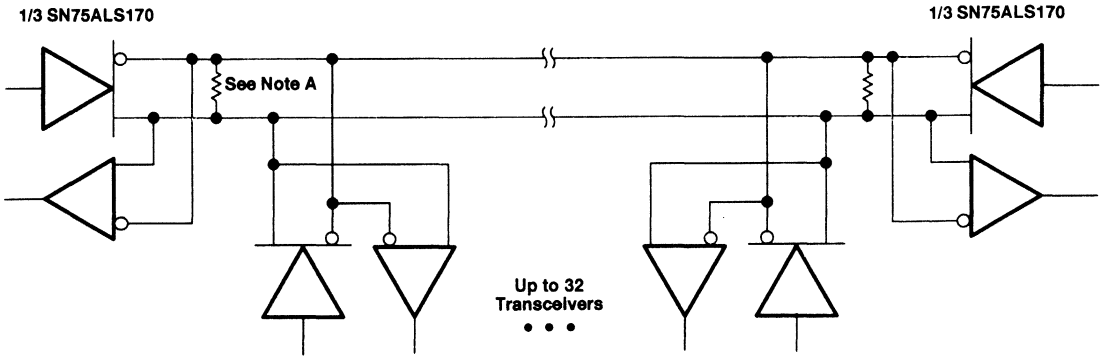


Figure 15

APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

Figure 16. Typical Application Circuit

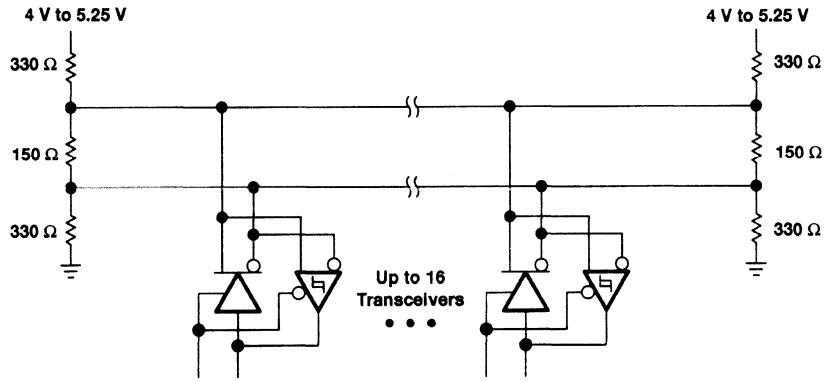


Figure 17. Typical Differential SCSI Application Circuit

APPLICATION INFORMATION

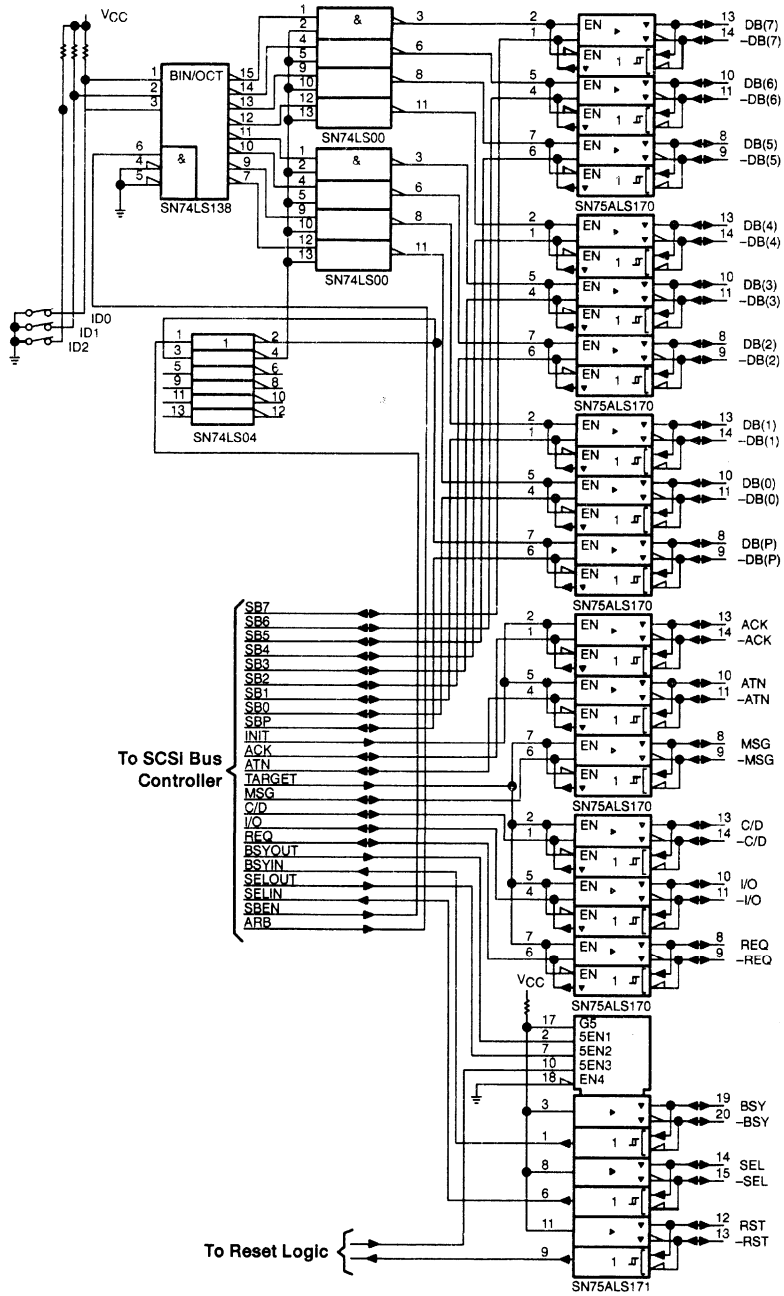
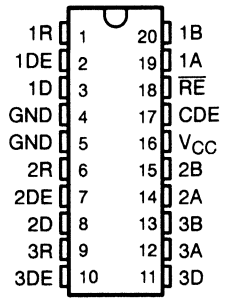


Figure 18. Typical Differential SCSI Bus Interface Implementation

SLLS056D – AUGUST 1987 – REVISED SEPTEMBER 1995

- Three Bidirectional Transceivers
- Driver Meets or Exceeds the Requirements of ANSI EIA/TIA-422-B and RS-485 and ITU Recommendation V.11
- Two Skew Limits Available
- Designed to Operate Up to 20 Million Data Transfers per Second (FAST-20 SCSI)
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Pulse Skew . . . 5 ns Max
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Features Independent Driver Enables and Combined Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltages Ranges
- Driver Output Capacity . . . ±60 mA
- Thermal Shutdown Protection
- Driver Positive- and Negative-Current Limiting
- Receiver Input Impedances . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±300 mV Max
- Receiver Input Hysteresis . . . 60 mV Typ
- Operates From a Single 5-V Supply
- Glitch-Free Power-Up and Power-Down Protection

DW OR J PACKAGE
(TOP VIEW)



Function Tables

EACH DRIVER

INPUT	ENABLE		OUTPUTS	
D	DE	CDE	A	B
H	H	H	H	L
L	H	H	L	H
X	L	X	Z	Z
X	X	L	Z	Z

EACH RECEIVER

DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.3$ V	L	H
-0.3 V $< V_{ID} < 0.3$ V	L	?
$V_{ID} \leq -0.3$ V	L	L
X	H	Z
Open	L	H

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

description

The SN75ALS171 and the SN75ALS171A triple differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines, and each driver meets ANSI Standards EIA/TIA-422-B and RS-485 and both the drivers and receivers meet ITU Recommendation V.11. The SN75ALS171A is designed for FAST-20 SCSI and can transmit or receive data pulses as short as 30 ns with a maximum skew of 5 ns.

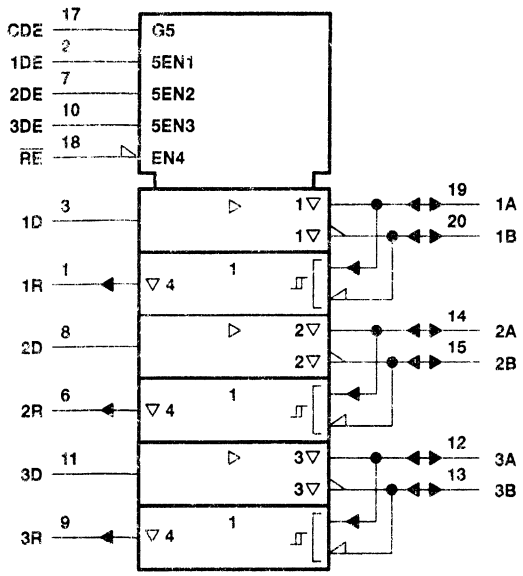
The SN75ALS171 and the SN75ALS171A operate from a single 5-V power supply. The drivers and receivers have individual active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver differential output and the receiver differential input pairs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or V_{CC} is at 0 V. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The SN75ALS171 and the SN75ALS171A are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

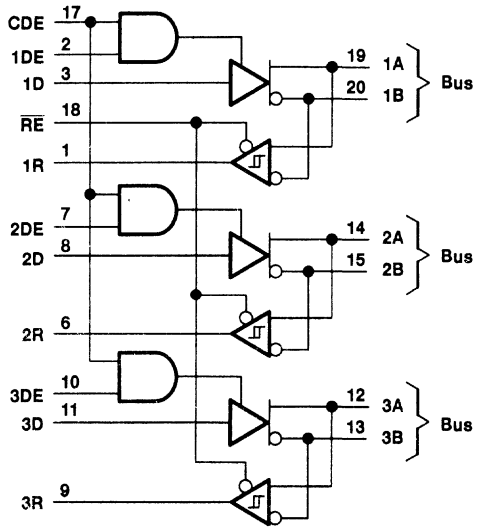
SKEW LIMIT	PART NUMBER	
10 ns	SN75ALS171DW	SN75ALS171J
5 ns	SN75ALS171ADW	

logic symbol†

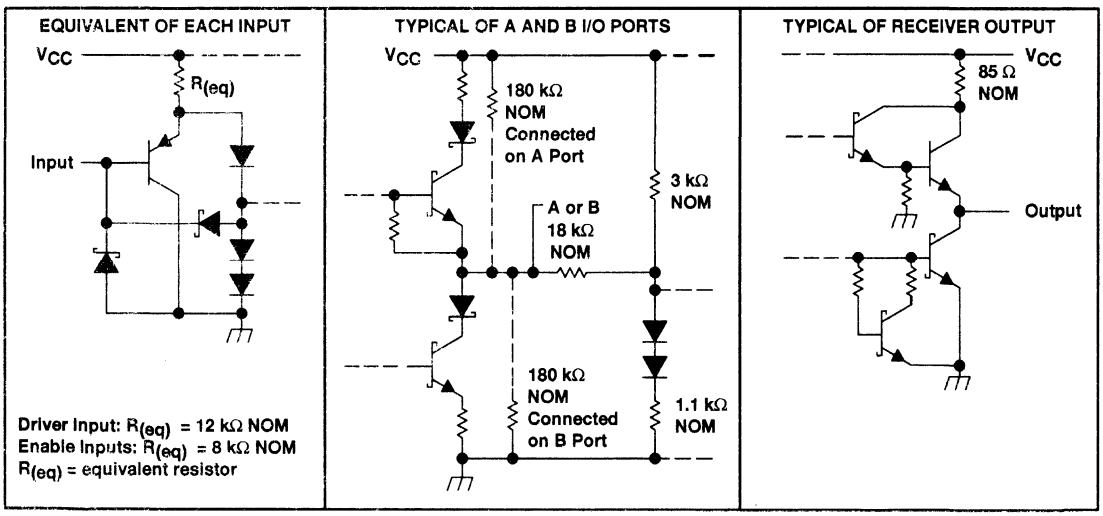


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Voltage range at any bus terminal ..... −7 V to 12 V
Enable input voltage, V_I ..... 7 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
J	1025 mW	8.2 mW/°C	656 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}		−7		12	V
High-level input voltage, V_{IH}	D, CDE, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, CDE, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	µA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_O	Output voltage	$I_O = 0$		0		6	V
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −55 mA	2.7			V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 55 mA			1.7	V
$\lvert V_{OD1} \rvert$	Differential output voltage	$I_O = 0$		1.5		6	V
$\lvert V_{OD2} \rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 1	$1/2 V_{OD1}$ or 2§	2.5	5	V
		R_L = 54 Ω,	See Figure 1	1.5	2.5	5	
V_{OD3}	Differential output voltage	V_{test} = −7 V to 12 V,	See Figure 2	1.5		5	V
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of differential output voltage¶	R_L = 54 Ω or 100 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage					3	V
						−1	
$\Delta\lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage¶					±0.2	V
I_O	Output current	Output disabled, See Note 3	V_O = 12 V			1	mA
			V_O = −7 V			−0.8	
I_{IH}	High-level enable-input current	D and DE	V_{IH} = 2.7 V			20	μA
		CDE				60	
I_{IL}	Low-level enable-input current	D and DE	V_{IL} = 0.4 V			−100	μA
		CDE				−900	
I_{OS}	Short-circuit output current	V_O = −6 V				−250	mA
		$V_O = 0$				−150	
		$V_O = V_{CC}$				250	
		V_O = 8 V				250	
I_{CC}	Supply current	No load	Outputs enabled		69	90	mA
			Outputs disabled		57	78	

† The power-off measurement in ANSI Standard EIA/TIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.
§ The minimum V_{OD2} with 100-W load is either 1/2 V_{OD2} or 2 V, whichever is greater.
¶ $\Delta\lvert V_{OD} \rvert$ and $\Delta\lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

NOTE 3: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The EIA/TIA-422-B limit does not apply for a combined driver and receiver terminal.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	ALS171	R_L = 54 Ω, C_L = 50 pF	See Figure 3,	3		13	ns
		ALS171A			6		11	
		ALS171	$R_{L1} = R_{L3}$ = 165 Ω, C_L = 60 pF, R_{L2} = 75 Ω,	V_{TERM} = 5 V, See Figure 6	3		13	
		ALS171A			6		11	
$t_{sk(p)}$	Pulse skew‡		R_L = 54 Ω, See Figure 3	C_L = 50 pF,		1	5	ns
			$R_{L1} = R_{L3}$ = 165 Ω, C_L = 60 pF,	R_{L2} = 75 Ω, See Figure 6		1	5	ns
$t_{sk(lim)}$	Skew limit§	ALS171	R_L = 54 Ω, See Figure 3	C_L = 50 pF,			10	ns
		ALS171A					5	
		ALS171	$R_{L1} = R_{L3}$ = 165 Ω, C_L = 60 pF,	R_{L2} = 75 Ω, See Figure 6			10	
		ALS171A					5	
$t_{t(OD)}$	Differential-output transition time		R_L = 54 Ω, See Figure 3	C_L = 50 pF,	3	8	13	ns
			$R_{L1} = R_{L3}$ = 165 Ω, C_L = 60 pF, See Figure 6	R_{L2} = 75 Ω, V_{TERM} = 5 V,	3	8	13	
t_{PZH}	Output enable time to high level		R_L = 110 Ω,	See Figure 4		30	50	ns
t_{PZL}	Output enable time to low level		R_L = 110 Ω,	See Figure 5		30	50	ns
t_{PHZ}	Output disable time from high level		R_L = 110 Ω,	See Figure 4	3	8	13	ns
t_{PLZ}	Output disable time from low level		R_L = 110 Ω,	See Figure 5	3	8	13	ns
t_{PDE}	Differential-output enable time		$R_{L1} = R_{L3}$ = 165 Ω, C_L = 60 pF,	R_{L2} = 75 Ω, See Figure 7	8	30	45	ns
t_{PDZ}	Differential-output disable time				5	10	45	ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ Pulse skew is defined as the $|t_{d(ODH)} - t_{d(ODL)}|$ of each channel.
§ Skew limit is the maximum difference in propagation delay times between any two channels of one device and between any two devices. This parameter is applicable at one V_{CC} and operating temperature within the recommended operating conditions.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	EIA/TIA-422-B	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\|V_{OD3}\|$		V_t (Test Termination Measurement 2)
V_{test}		V_{tst}
$\Delta\|V_{OD}\|$	$\|\|V_t\|-\|\overline{V}_t\|\|$	$\|\|V_t\|-\|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V}_{os}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.3	V
V_{IT-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.3‡			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)				60		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 300 mV, See Figure 8	I_{OH} = −400 μA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −300 mV, See Figure 8	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input = 0 V, See Note 4	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				60	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−300	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current	V_{ID} = 300 mV,	V_O = 0	−15		−85	mA
I_{CC}	Supply current	No load	Outputs enabled		69	90	mA
			Outputs disabled		57	78	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
NOTE 4: This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	ALS171	V_{ID} = −1.5 V to 1.5 V, C_L = 15 pF, T_A = 25°C, See Figure 9	9		19	ns
		ALS171A		11		16	
t_{PHL}	Propagation delay time, high- to low-level output	ALS171		9		19	ns
		ALS171A		11		16	
$t_{sk(p)}$	Pulse skew§		V_{ID} = −1.5 V to 1.5 V, C_L = 15 pF, See Figure 9		2	5	ns
$t_{sk(lim)}$	Skew limit¶	ALS171				10	ns
		ALS171A				5	
t_{PZH}	Output enable time to high level		C_L = 15 pF, See Figure 10		7	14	ns
t_{PZL}	Output enable time to low level				7	14	ns
t_{PHZ}	Output disable time from high level		C_L = 15 pF, See Figure 10		20	35	ns
t_{PLZ}	Output disable time from low level				8	17	ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
§ Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel.
¶ Skew limit is the maximum difference in propagation delay times between any two channels of one device and between any two devices. This parameter is applicable at one V_{CC} and operating temperature within the recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION

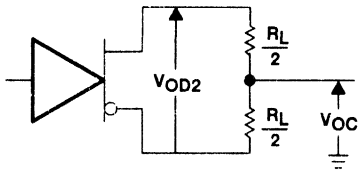


Figure 1. Driver V_{OD} and V_{OC}

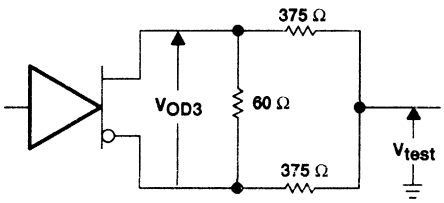
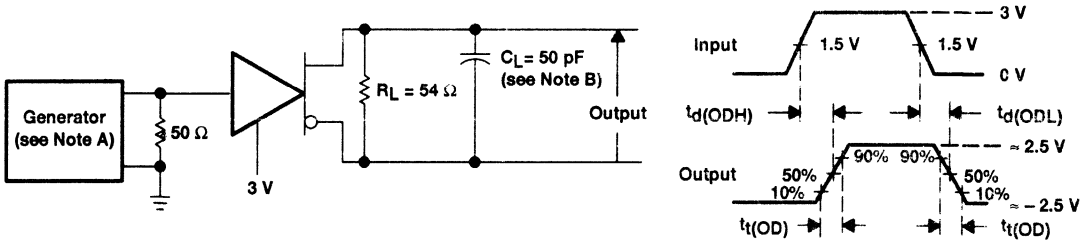


Figure 2. Driver V_{OD3}



TEST CIRCUIT VOLTAGE WAVEFORMS

Figure 3. Driver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

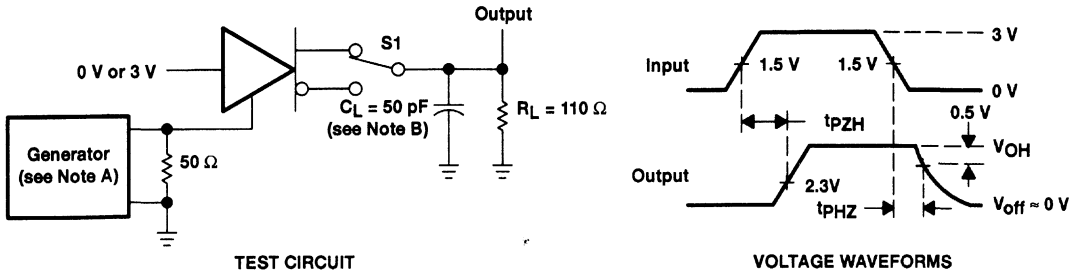


Figure 4. Driver Test Circuit and Voltage Waveforms

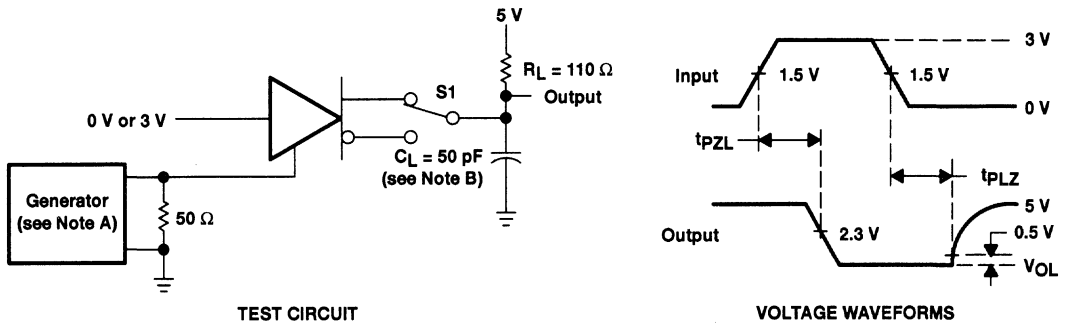
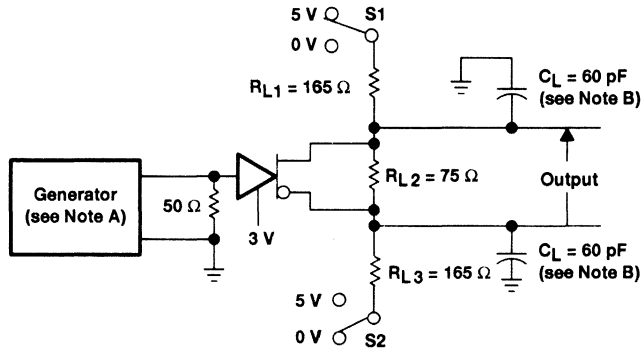


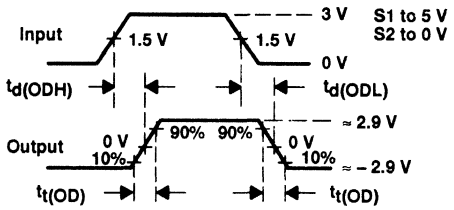
Figure 5. Driver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

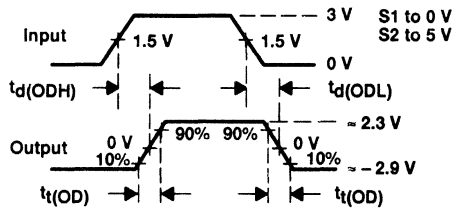
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

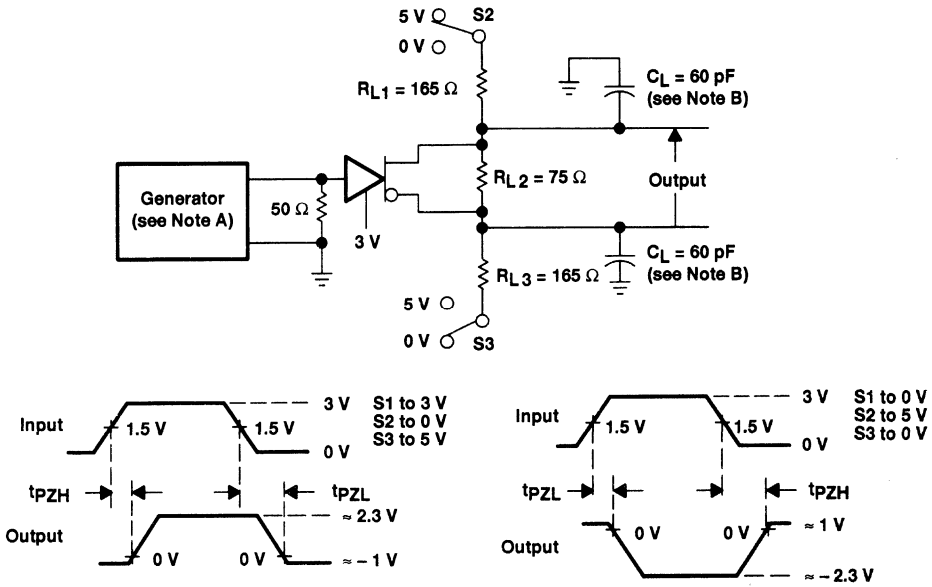


VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 6. Driver Test Circuit and Voltage Waveforms With Double-Differential-SCSI Termination for the Load

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 7. Driver Differential-Enable and Disable Times With a Double-SCSI Termination

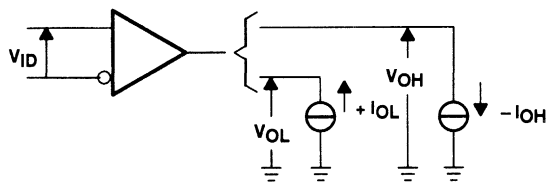


Figure 8. Receiver V_{OH} and V_{OL}

PARAMETER MEASUREMENT INFORMATION

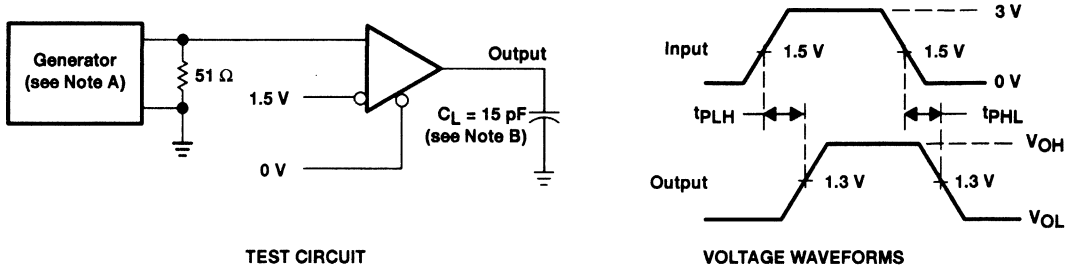


Figure 9. Receiver Test Circuit and Voltage Waveforms

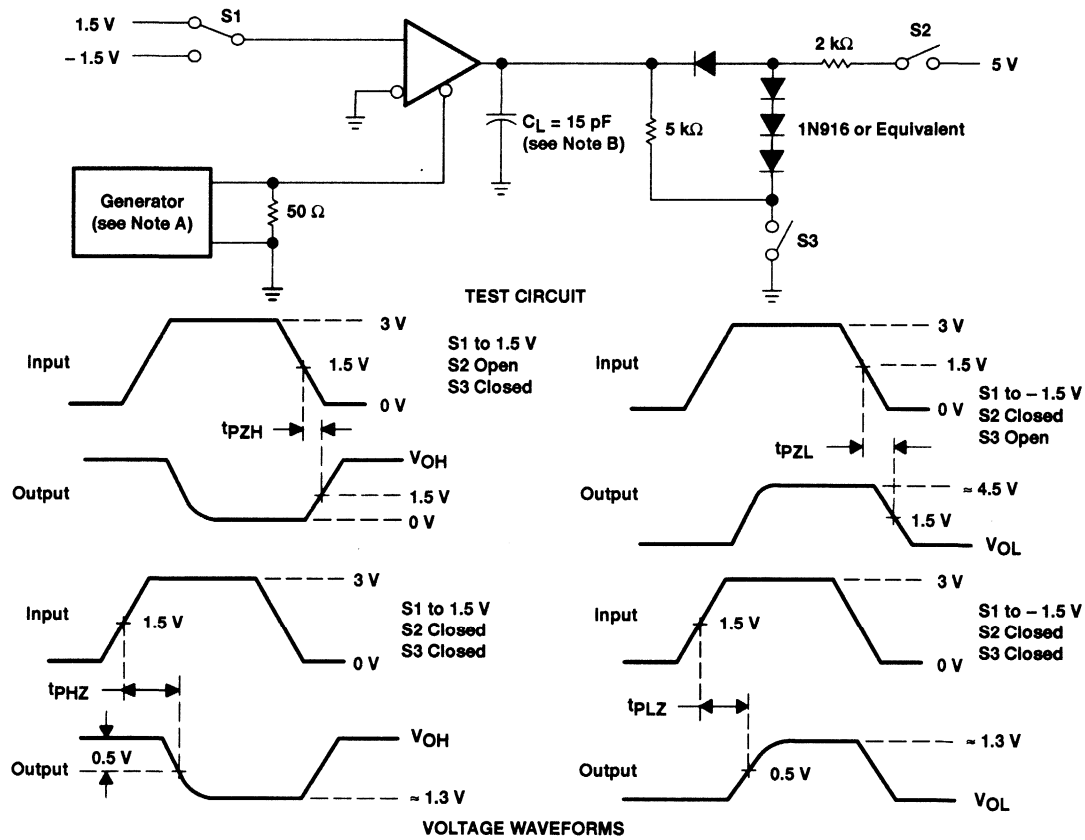


Figure 10. Receiver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

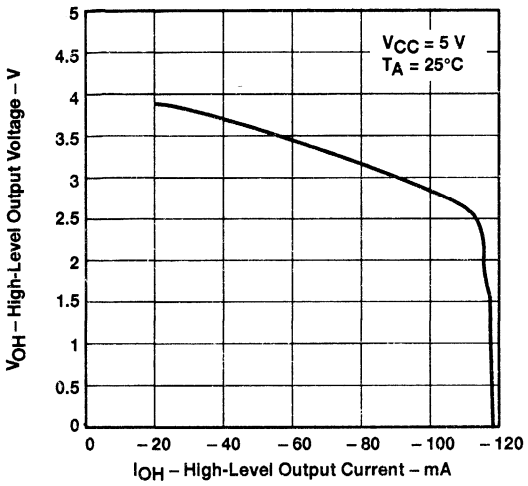


Figure 11

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

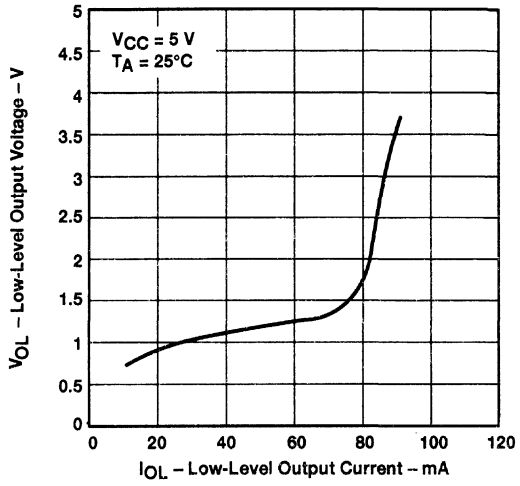


Figure 12

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

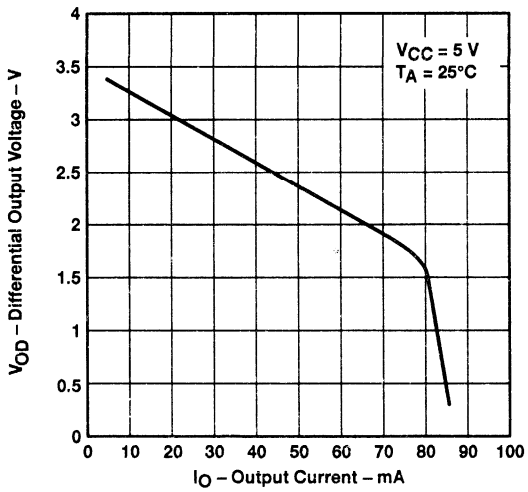


Figure 13

TYPICAL CHARACTERISTICS

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

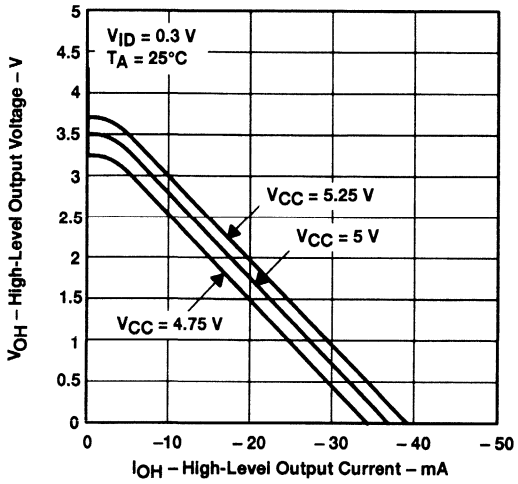


Figure 14

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

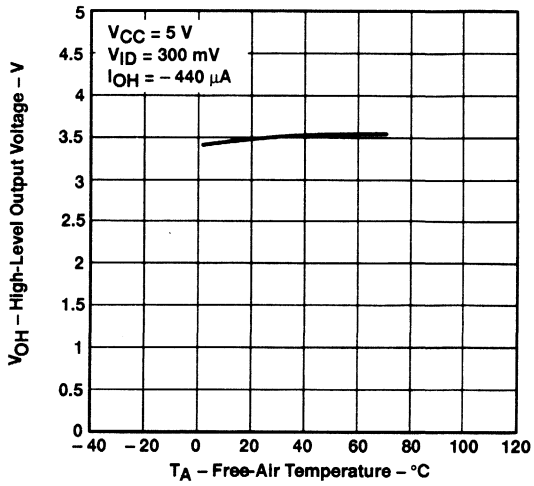


Figure 15

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

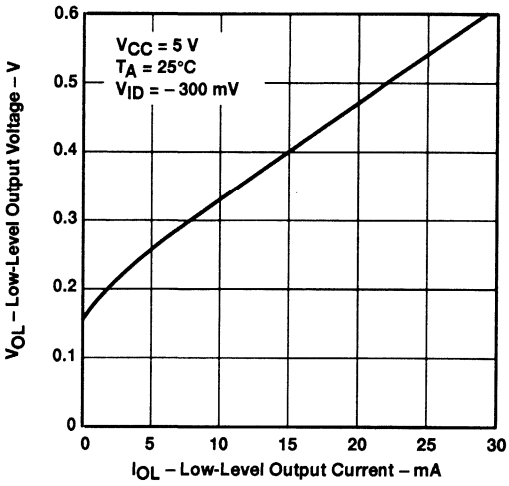


Figure 16

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

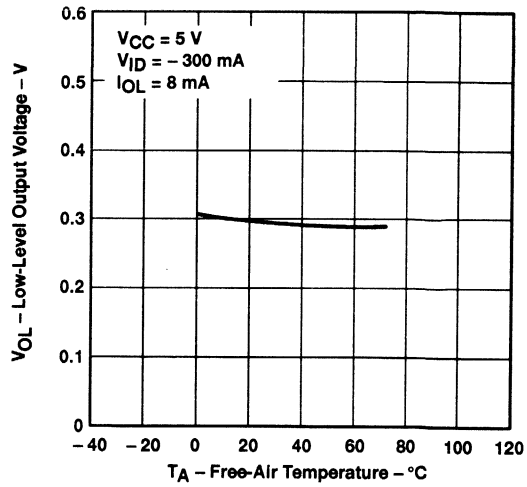


Figure 17

TYPICAL CHARACTERISTICS

RECEIVER
OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

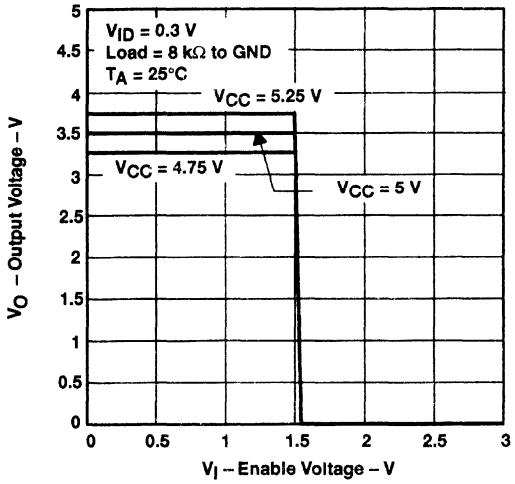


Figure 18

RECEIVER
OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

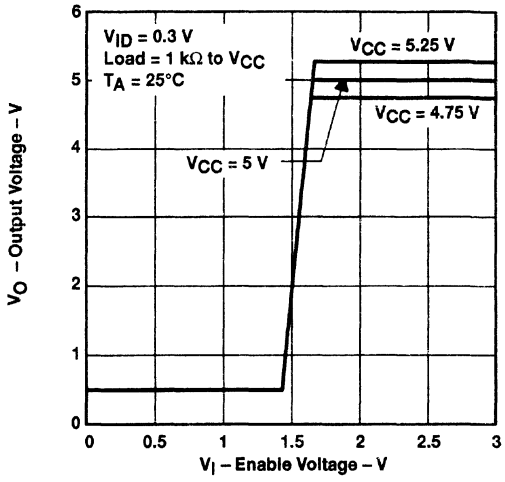
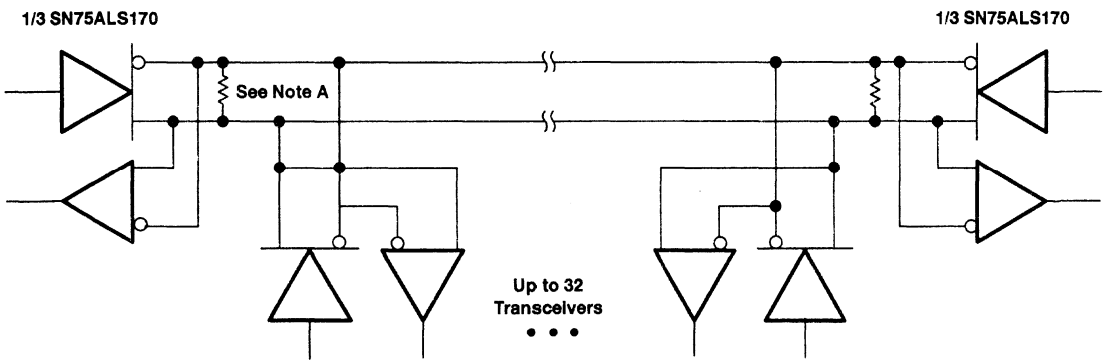


Figure 19

APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

Figure 20. Typical Application Circuit

APPLICATION INFORMATION

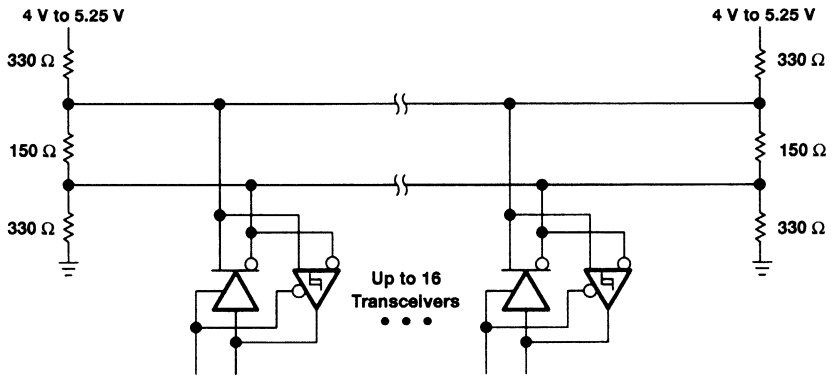


Figure 21. Typical Differential SCSI Application Circuit

APPLICATION INFORMATION

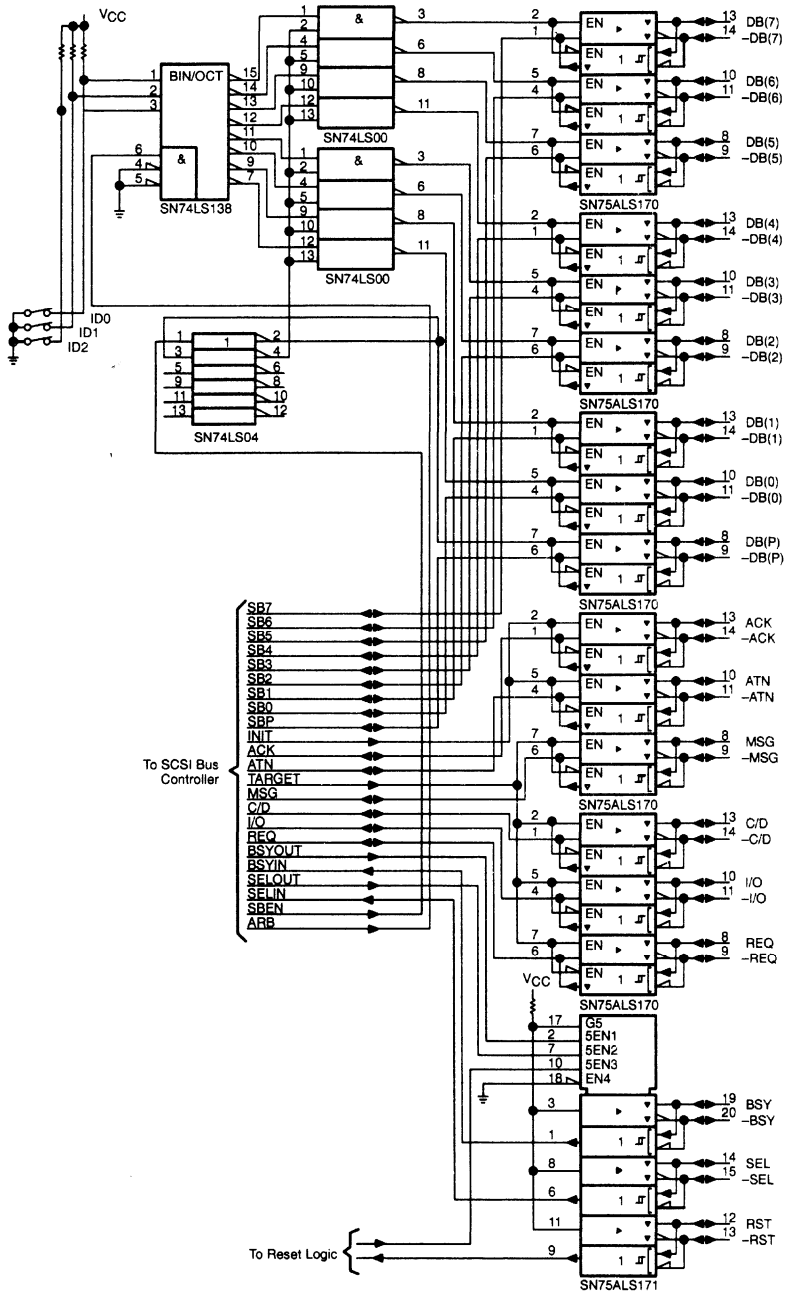
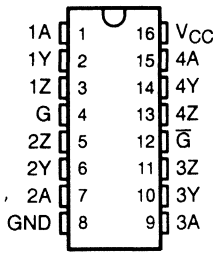


Figure 22. Typical Differential SCSI Bus Interface Implementation

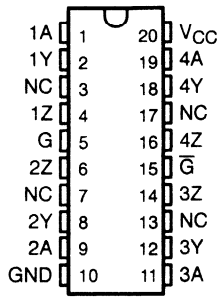
SLLS038B – OCTOBER 1980 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendation V.11**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **3-State Outputs**
- **Common-Mode Output Voltage Range of –7 V to 12 V**
- **Active-High and Active-Low Enables**
- **Thermal Shutdown Protection**
- **Positive- and Negative-Current Limiting**
- **Operates From Single 5-V Supply**
- **Logically Interchangeable With AM26LS31**

N PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN75172 is a monolithic quadruple differential line driver with 3-state outputs. It is designed to meet the requirements of ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendation V.11. The device is optimized for balanced multipoint bus transmission at rates of up to 4 megabaud. Each driver features wide positive and negative common-mode output voltage ranges, making it suitable for party-line applications in noisy environments.

The SN75172 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C. This device offers optimum performance when used with the SN75173 or SN75175 quadruple differential line receivers.

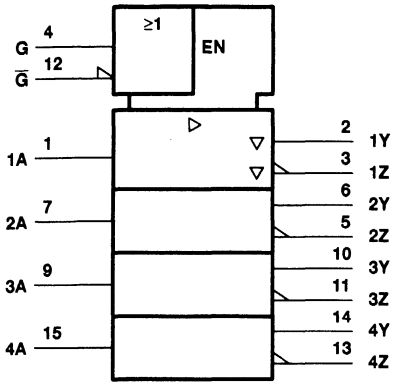
The SN75172 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each driver)

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

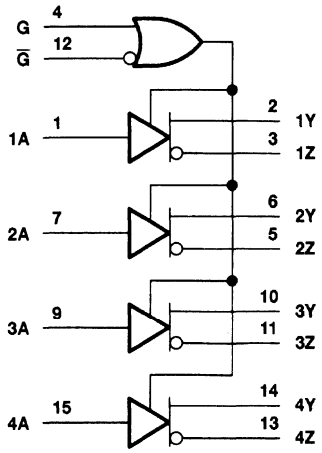
H = high level, L = low level,
X = irrelevant, Z = high impedance (off)

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Terminal numbers shown are for the N package.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Voltage range at any bus terminal ..... −10 V to 15 V
Input voltage, V_I ..... 5.5 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Common-mode output voltage, V_{OC}			−7 to 12	V
High-level output current, I_{OH}			−60	mA
Low-level output current, I_{OL}			60	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA					−1.5	V
V_O	Output voltage	$I_O = 0$			0		6	V
V_{OH}	High-level output voltage	$V_{IH} = 2$ V,	$V_{IL} = 0.8$ V,	$I_{OH} = -33$ mA		3.7		V
V_{OL}	Low-level output voltage	$V_{IH} = 2$ V,	$V_{IL} = 0.8$ V,	$I_{OH} = 33$ mA		1.1		V
$\lvert V_{OD1}\rvert$	Differential output voltage	$I_O = 0$			1.5		6	V
$\lvert V_{OD2}\rvert$	Differential output voltage	$R_L = 100\ \Omega$,	See Figure 1		1/2 V_{OD1} or 2‡			V
		$R_L = 54\ \Omega$,	See Figure 1		1.5	2.5	5	V
V_{OD3}	Differential output voltage	See Note 2			1.5		5	V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage§	$R_L = 54\ \Omega$ or $100\ \Omega$,		See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage¶						+3 −1	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage§						±0.2	V
I_O	Output current with power off	$V_{CC} = 0$,	$V_O = -7$ V to 12 V				±100	μA
I_{OZ}	High-impedance-state output current	$V_O = -7$ V to 12 V					±100	μA
I_{IH}	High-level input current	$V_I = 2.7$ V					20	μA
I_{IL}	Low-level input current	$V_I = 0.5$ V					−360	μA
I_{OS}	Short-circuit output current	$V_O = -7$ V					−180	mA
		$V_O = V_{CC}$					180	
		$V_O = 12$ V					500	
I_{CC}	Supply current (all drivers)	No load	Outputs enabled			38	60	mA
			Outputs disabled			18	40	

† All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.

‡ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.

§ $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

¶ In ANSI Standard EIA/TIA-422-B, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

NOTE 2: See Figure 3-5 of EIA Standard RS-485.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	EIA/TIA-422-B	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\lvert V_{OD1}\rvert$	V_o	V_o
$\lvert V_{OD2}\rvert$	V_t ($R_L = 100\ \Omega$)	V_t ($R_L = 54\ \Omega$)
$\lvert V_{OD2}\rvert$		V_t (Test Termination) Measurement 2)
$\Delta\lvert V_{OD}\rvert$	$\lvert\lvert V_t\rvert - \lvert\overline{V}_t\rvert\rvert$	$\lvert\lvert V_t\rvert - \lvert\overline{V}_t\rvert\rvert$
V_{OC}	$\lvert V_{os}\rvert$	$\lvert V_{os}\rvert$
$\Delta\lvert V_{OC}\rvert$	$\lvert V_{os} - \overline{V}_{os}\rvert$	$\lvert V_{os} - \overline{V}_{os}\rvert$
I_{OS}	$\lvert I_{sa}\rvert, \lvert I_{sb}\rvert$	
I_O	$\lvert I_{xa}\rvert, \lvert I_{xb}\rvert$	I_{ia}, I_{ib}

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	R_L = 54 Ω,	See Figure 2		45	65	ns
$t_{t(OD)}$	Differential-output transition time				80	120	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 3		80	120	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 4		45	80	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 3		78	115	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 4		18	30	ns

PARAMETER MEASUREMENT INFORMATION

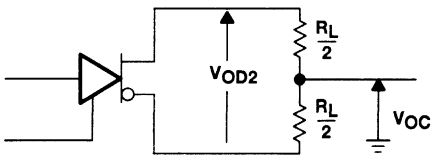


Figure 1. Differential and Common-Mode Output Voltages

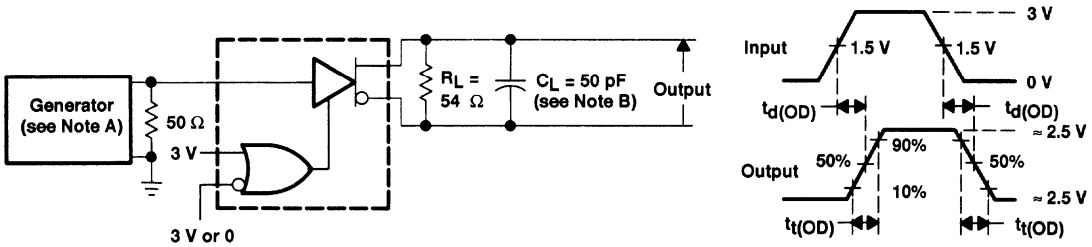


Figure 2. Differential-Output Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.

PARAMETER MEASUREMENT INFORMATION

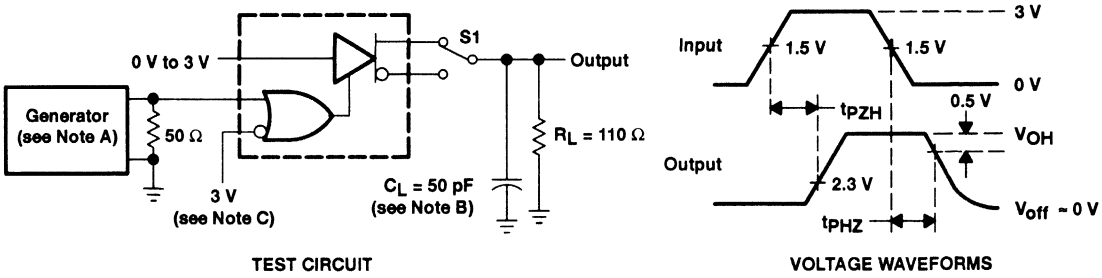


Figure 3. Test Circuit and Voltage Waveforms

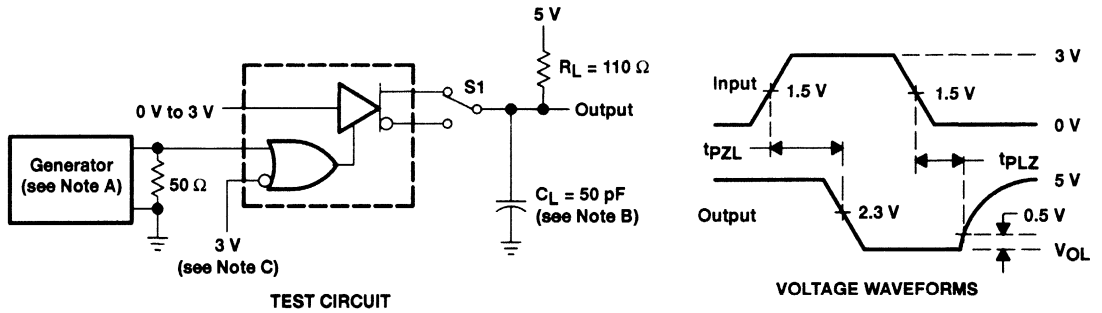


Figure 4. Test Circuit and Voltage Waveforms

NOTES. A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, $t_r \leq 5$ ns, $t_f \leq 5$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and stray capacitance.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$.

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

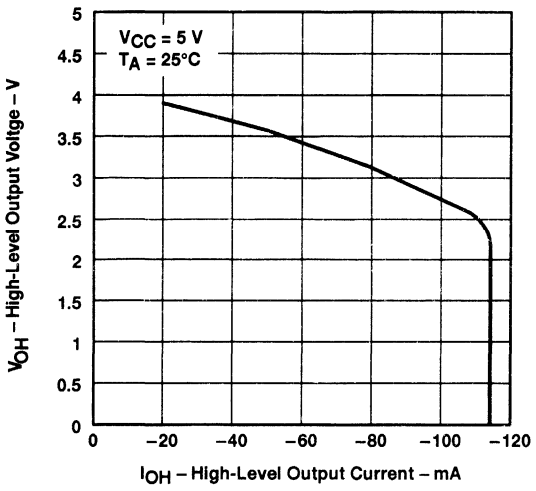


Figure 5

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

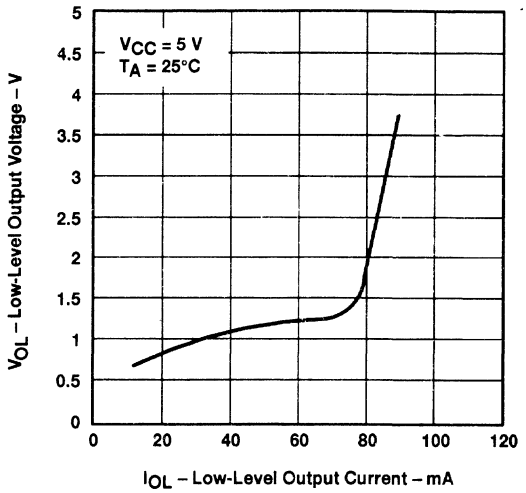


Figure 6

DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

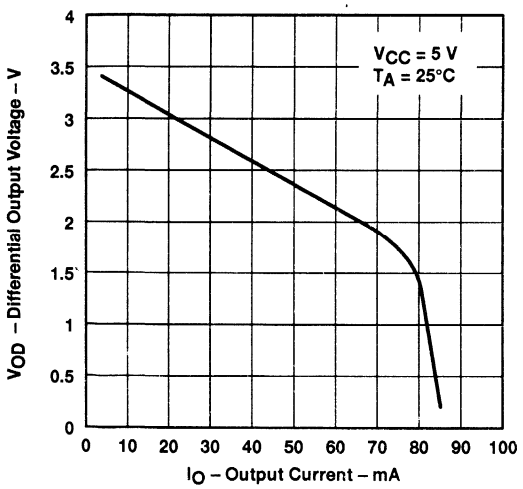


Figure 7

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

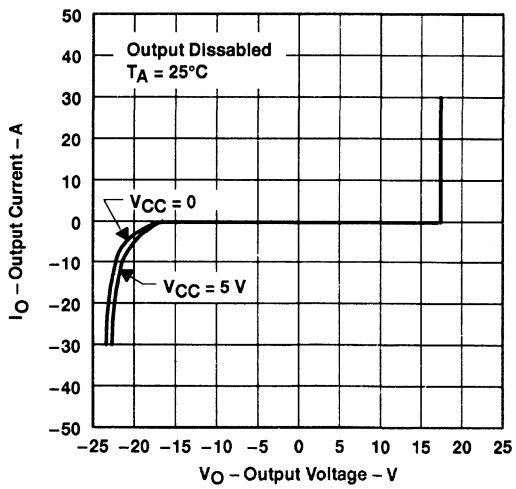


Figure 8

TYPICAL CHARACTERISTICS

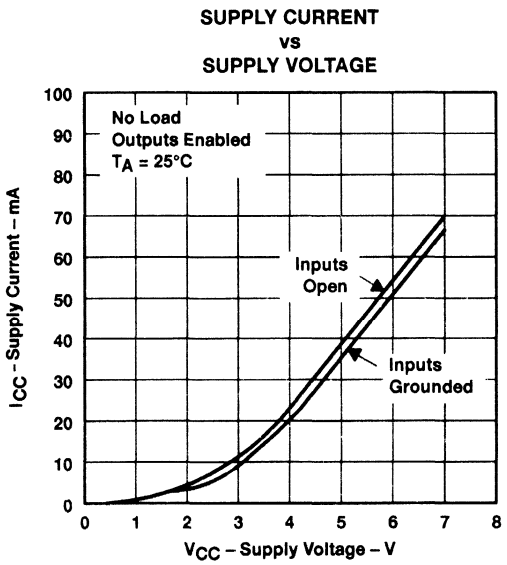


Figure 9

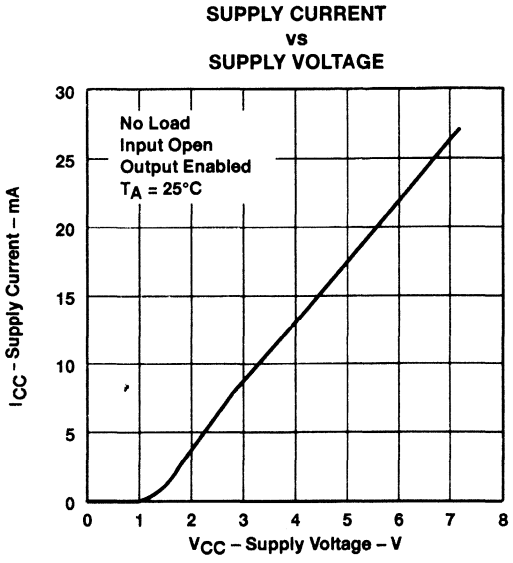
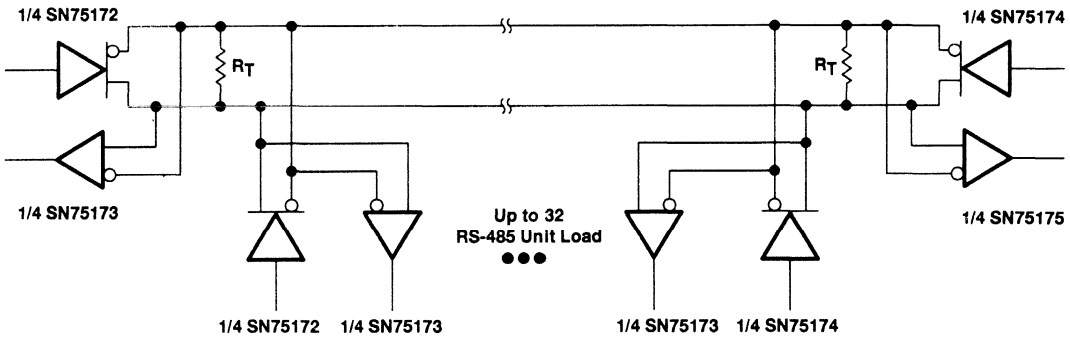


Figure 10

APPLICATION INFORMATION



NOTE A: The line length should be terminated at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

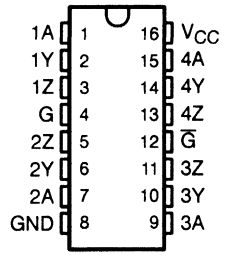
Figure 11

SN65ALS172A, SN75ALS172A
QUADRUPLE DIFFERENTIAL LINE DRIVERS

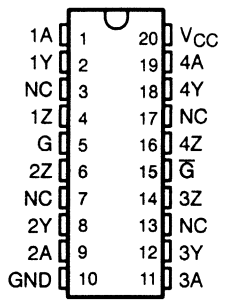
SLLS121C – AUGUST 1990 – REVISED MAY 1995

- **Meets or Exceeds ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendation V.11**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Designed for 20-MBaud Operation in Both Serial and Parallel Applications**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Low Supply Current Requirements 55 mA Max**
- **Wide Positive and Negative Input/Output Bus Voltages Ranges**
- **Driver Output Capacity . . . ±60 mA**
- **Thermal Shutdown Protection**
- **Driver Positive and Negative Current Limiting**
- **Logically Interchangeable With SN75172**

SN75ALS172A . . . N PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN65ALS172A and SN75ALS172A are comprised of four line drivers with 3-state differential outputs. They are designed to meet the requirements of ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendation V.11. These devices are optimized for balanced multipoint bus transmission at rates of up to 20 Mbaud. Each driver features wide positive and negative common-mode output voltage ranges making them suitable for party-line applications in noisy environments.

The SN65ALS172A and SN75ALS172A provide positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C.

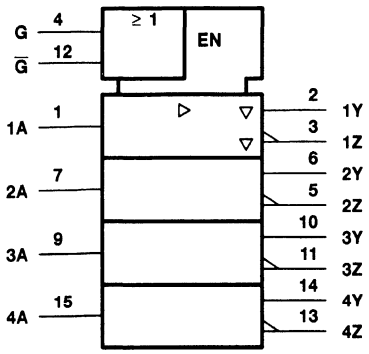
The SN65ALS172A is characterized for operation from −40°C to 85°C and the SN75ALS172A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each driver)

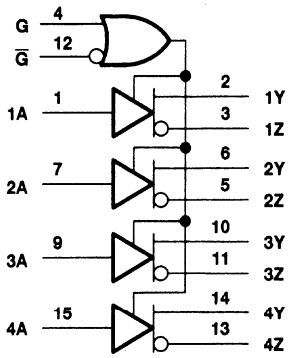
INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H = high level, L = low level, X = irrelevant,
Z = high impedance (off)

logic symbol†

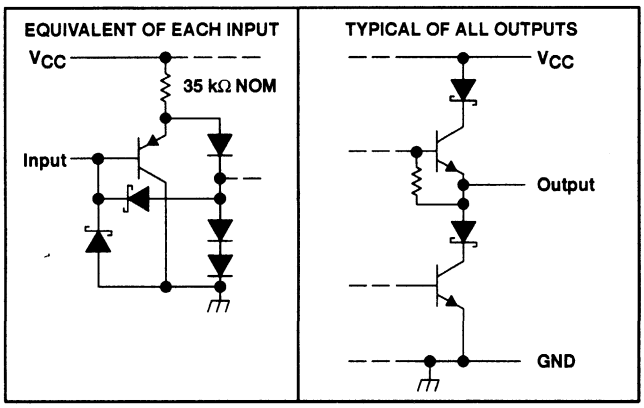


logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Terminal numbers shown are for the N package.

schematics of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 7 V
Output voltage range, V_O ..... −9 V to 14 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65ALS172A ..... −40°C to 85°C
SN75ALS172A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1125 mW	9 mW/°C	720 mW	585 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Common-mode output voltage, V_{OC}				+12 −7	V
High-level output current, I_{OH}				−60	mA
Low-level output current, I_{OL}				60	mA
Operating free-air temperature, T_A	SN65ALS172A	−40		85	°C
	SN75ALS172A	0		70	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_O	Output voltage	$I_O = 0$		0		6	V
$\lvert V_{OD1} \rvert$	Differential output voltage	$I_O = 0$		1.5		6	V
$\lvert V_{OD2} \rvert$	Differential output voltage	V_{CC} = 5 V, R_L = 100 Ω	See Figure 1	1/2 V_{OD1} or 2‡			V
		R_L = 54 Ω		1.5	2.5	5	
$\lvert V_{OD3} \rvert$	Differential output voltage	See Note 2		1.5		5	V
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of differential output voltage§	R_L = 54 Ω or 100 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage¶					+3 −1	V
$\Delta\lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current with power off	V_{CC} = 0,	V_O = −7 V to 12 V			±100	μA
I_{OZ}	High-impedance-state output current	V_O = −7 V to 12 V				±100	μA
I_{IH}	High-level input current	V_I = 2.7 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−100	μA
I_{OS}	Short-circuit output current	V_O = −7 V to 12 V				±250	mA
I_{CC}	Supply current (all drivers)	No load	Outputs enabled		36	55	mA
			Outputs disabled		15	30	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
§ $\Delta\lvert V_{OD} \rvert$ and $\Delta\lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
¶ In ANSI Standard EIA/TIA-422-B, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
NOTE 2: See EIA Standard RS-485, Figure 3-5, Test Termination Measurement 2.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	R_L = 54 Ω,	See Figure 2	9	15	22	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 3	30	45	70	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 4	25	40	65	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 3	10	20	35	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 4	10	30	45	ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

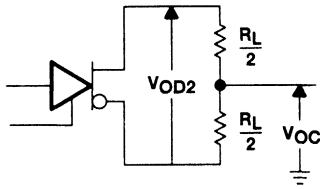
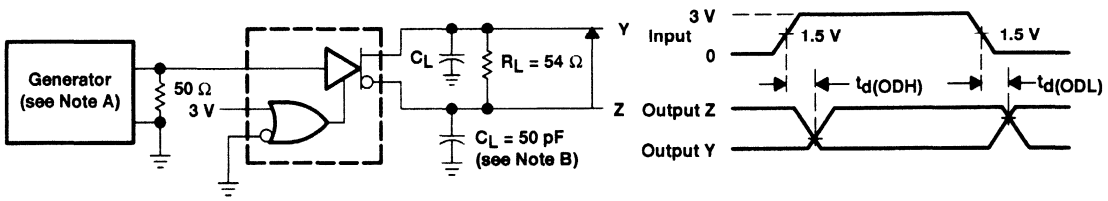


Figure 1. Differential and Common-Mode Output Voltages



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, duty cycle = 50%, $t_f \leq 5$ ns, $t_r \leq 5$ ns.
B. C_L includes probe and stray capacitance.

Figure 2. Differential Output Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

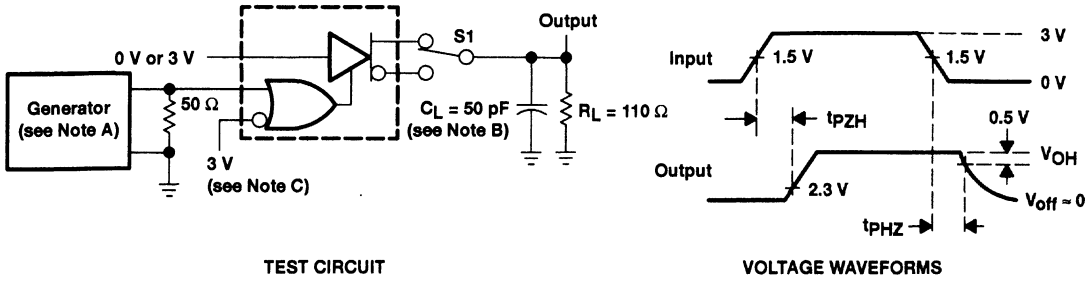


Figure 3. Test Circuit and Voltage Waveforms, t_{PZH} and t_{PHZ}

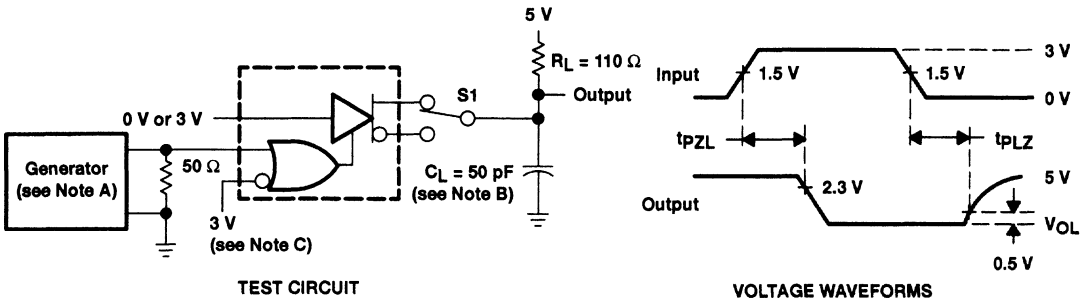


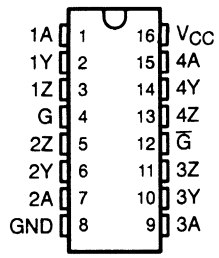
Figure 4. Test Circuit and Voltage Waveforms, t_{PZL} and t_{PLZ}

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, duty cycle = 50%, $t_f \leq 5$ ns, $t_r \leq 5$ ns.
B. C_L includes probe and stray capacitance.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

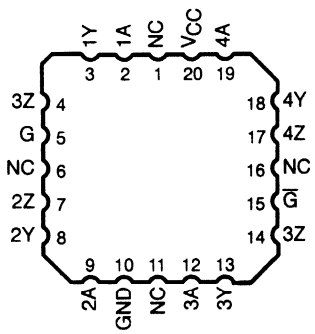
SN55LBC172
QUADRUPLE LOW-POWER DIFFERENTIAL LINE DRIVER

- **Meets Standard EIA-485**
- **Designed for High-Speed Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Supports Data Rates up to and Exceeding Ten Million Transfers Per Second**
- **Common-Mode Output Voltage Range of –7 V to 12 V**
- **Positive- and Negative-Current Limiting**
- **Low Power Consumption . . . 1.5 mA Max (Output Disabled)**

J OR W PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN55LBC172 is a monolithic quadruple differential line driver with 3-state outputs. This device is designed to meet the requirements of the Electronics Industry Association (EIA) standard RS-485. The SN55LBC172 is optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. The driver features wide positive and negative common-mode output voltage ranges, current limiting, and thermal-shutdown circuitry, making it suitable for party-line applications in noisy environments. The device is designed using the LinBiCMOS™ process, facilitating ultralow power consumption and inherent robustness.

The SN55LBC172 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. This device offers optimum performance when used with the SN55LBC173M quadruple line receiver. The SN55LBC172 is available in the 16-pin CDIP package (J), the 16-pin CPAK package (W), or the 20-pin LCCC package (FK).

The SN55LBC172 is characterized for operation over a military temperature range of –55°C to 125°C.

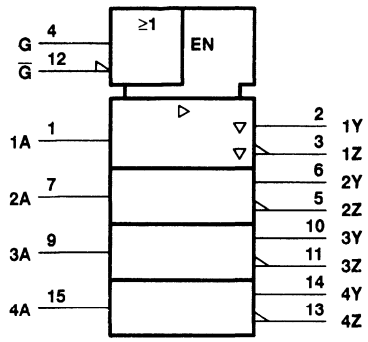
FUNCTION TABLE
(each driver)

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H = high level, L = low level,
X = irrelevant, Z = high impedance (off)

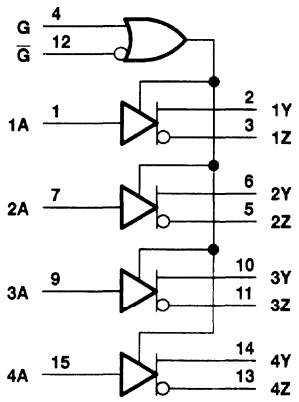
LinBiCMOS is a trademark of Texas Instruments Incorporated.

logic symbol†

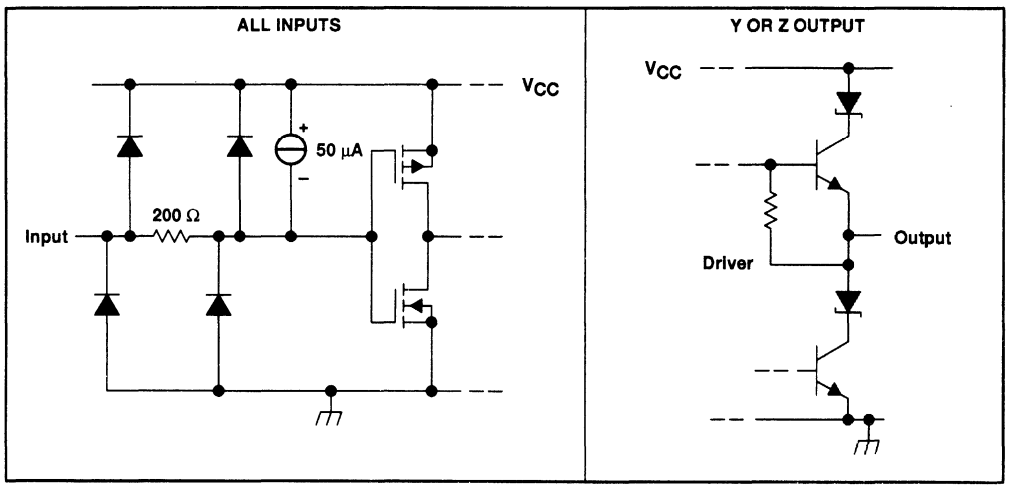


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the J or W package.

logic diagram (positive logic)



schematic diagrams of inputs and outputs



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.3 V to 7 V
Output voltage range, V_O ..... −10 V to 15 V
Input voltage range, V_I ..... −0.3 V to 7 V
Continuous power dissipation ..... internally limited‡
Operating free-air temperature range, T_A ..... −55°C to 125°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.
NOTE 1: All voltage values are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 125°C$ POWER RATING
FK	1375 mW	11.0 mW/°C	275 mW
J	1375 mW	11.0 mW/°C	275 mW
W	1000 mW	8.0 mW/°C	200 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Output voltage at any bus terminal (separately or common mode), V_O	Y or Z			12	V
				−7	
High-level output current, I_{OH}	Y or Z			−60	mA
Low-level output current, I_{OL}	Y or Z			60	mA
Continuous total power dissipation		See Dissipation Rating Table			
Operating free-air temperature, T_A		−55		125	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
$\|V_{OD}\|$	Differential output voltage‡	R_L = 54 Ω, See Figure 1		1.1	1.8	5	V
		R_L = 60 Ω, See Figure 2		1.1	1.7	5	
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage§	R_L = 54 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage					3 −1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current with power off	V_{CC} = 0, V_O = −7 V to 12 V				±100	µA
I_{OZ}	High-impedance-state output current	V_O = −7 V to 12 V				±100	µA
I_{IH}	High-level input current	V_I = 2.4 V				−100	µA
I_{IL}	Low-level input current	V_I = 0.4 V				−100	µA
I_{OS}	Short-circuit output current	V_O = −7 V to 12 V				±250	mA
I_{CC}	Supply current (all drivers)	No load	Outputs enabled			7	mA
			Outputs disabled			1.5	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

‡ The minimum V_{OD} specification does not fully comply with EIA-485 at operating temperatures below 0°C. The lower output signal should be used to determine the maximum signal transmission distance.

§ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

switching characteristics, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω, See Figure 3	25°C	2	11	20	ns
			−55°C to 125°C	2		40	
$t_{t(OD)}$	Differential output transition time	R_L = 54 Ω, See Figure 3	25°C	10	15	25	ns
			−55°C to 125°C	4		40	
t_{PZH}	Output enable time to high level	R_L = 110 Ω, See Figure 4	25°C			30	ns
			−55°C to 125°C			40	
t_{PZL}	Output enable time to low level	R_L = 110 Ω, See Figure 5	25°C			30	ns
			−55°C to 125°C			40	
t_{PHZ}	Output disable time from high level	R_L = 110 Ω, See Figure 4	25°C			50	ns
			−55°C to 125°C			90	
t_{PLZ}	Output disable time from low level	R_L = 110 Ω, See Figure 5	25°C			30	ns
			−55°C to 125°C			45	

PARAMETER MEASUREMENT INFORMATION

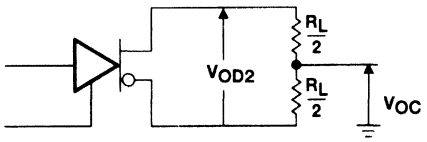


Figure 1. Differential and Common-Mode Output Voltages

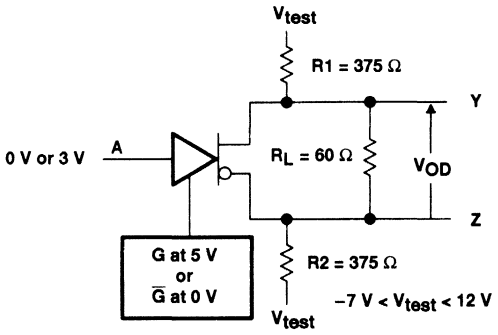
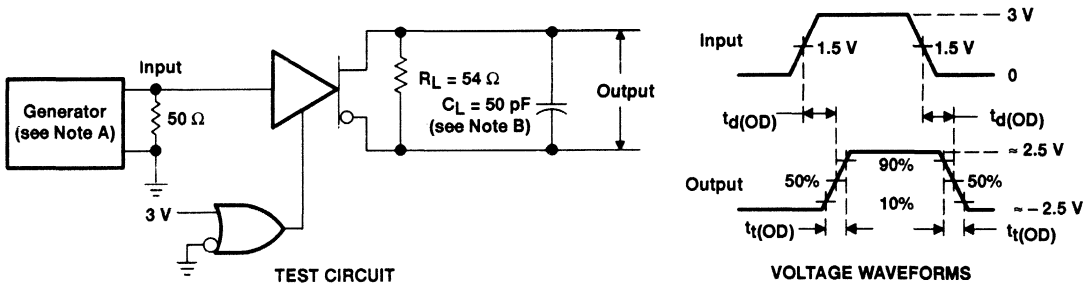


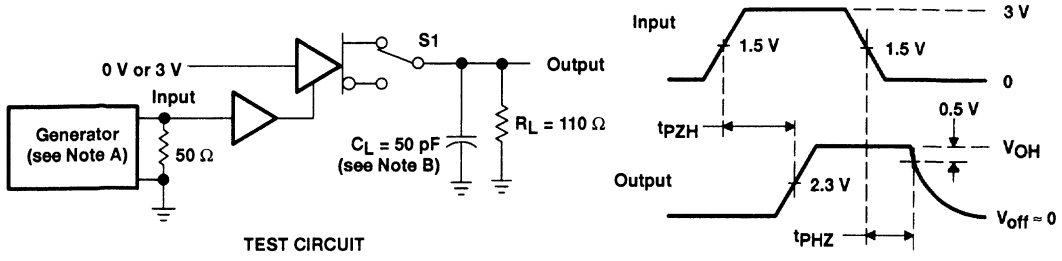
Figure 2. Driver V_{OD} Test Circuit



NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 5 ns, t_f ≤ 5 ns, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.

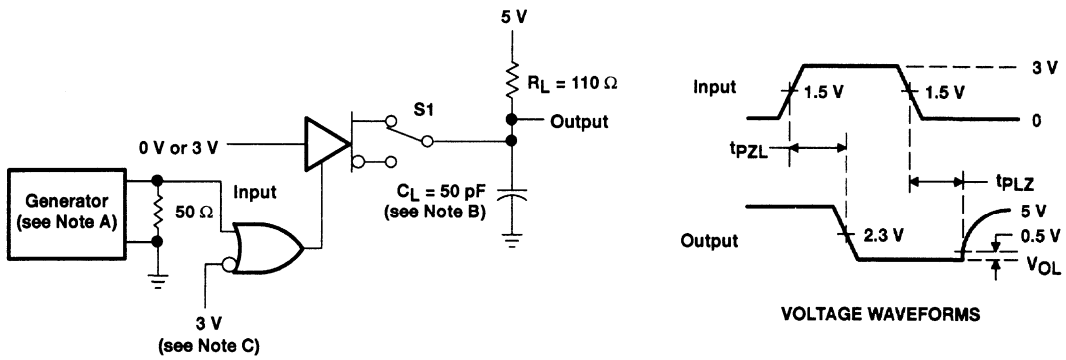
Figure 3. Driver Differential-Output Test Circuit and Delay and Transition-Time Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 5 ns, t_f ≤ 5 ns, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.

Figure 4. t_{PZH} and t_{PHZ} Test Circuit and Voltage Waveforms



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 5 ns, t_f ≤ 5 ns, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$.

Figure 5. t_{PZL} and t_{PLZ} Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

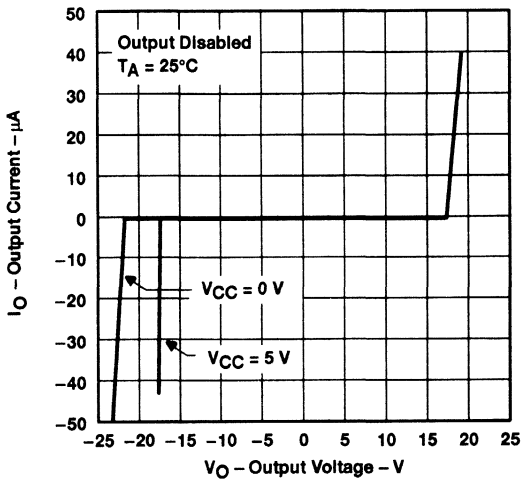


Figure 6

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

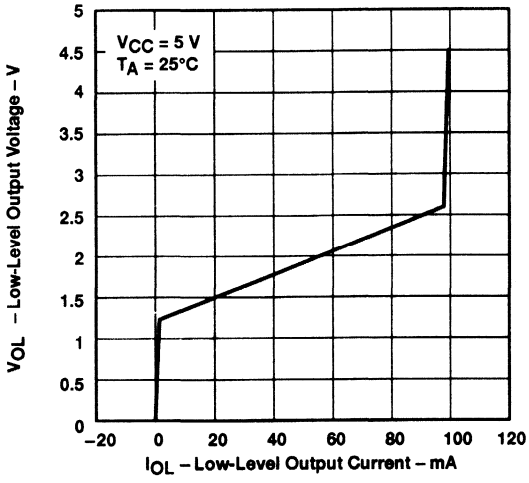


Figure 7

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

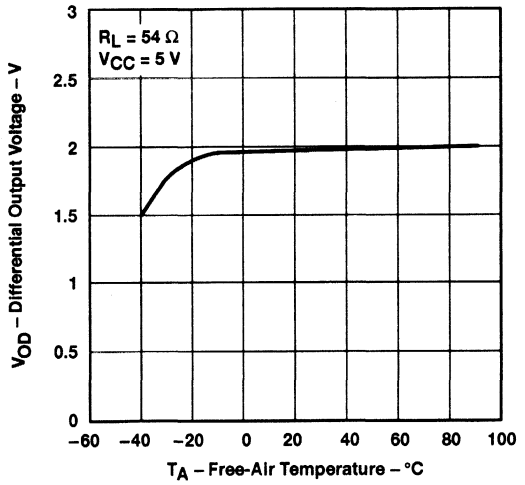


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

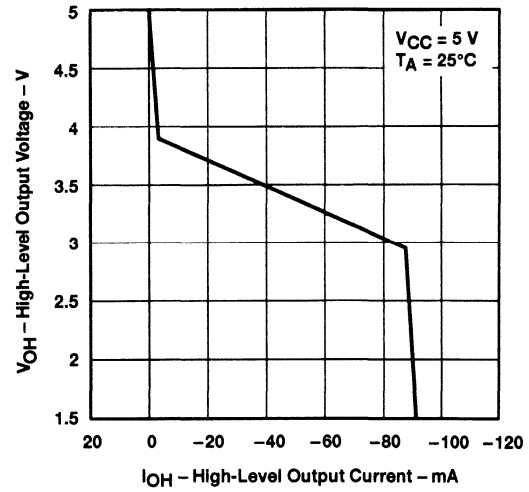


Figure 9

TYPICAL CHARACTERISTICS

DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

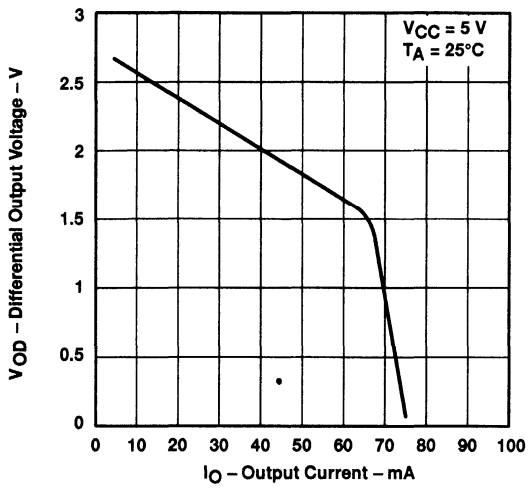


Figure 10

PROPAGATION DELAY TIME,
DIFFERENTIAL OUTPUT
vs
FREE-AIR TEMPERATURE

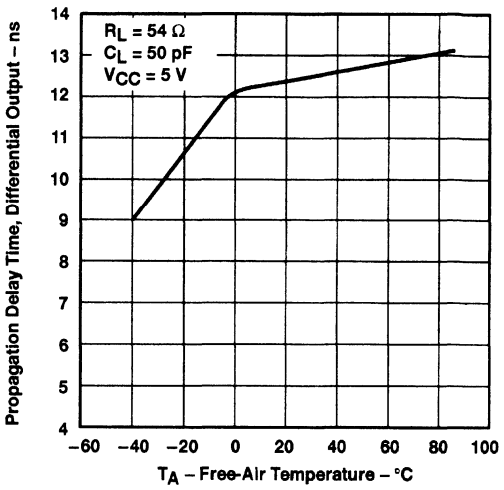
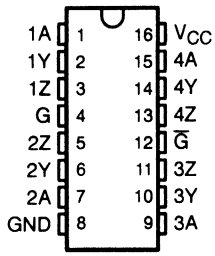


Figure 11

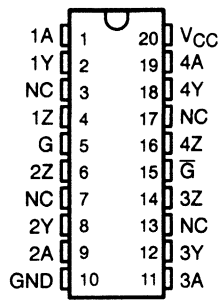
SLLS163 – JULY 1993

- **Meet or Exceed EIA Standard RS-485**
- **Designed for High-Speed Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Support Data Rates up to and Exceeding Ten Million Transfers Per Second**
- **Common-Mode Output Voltage Range of –7 V to 12 V**
- **Positive- and Negative-Current Limiting**
- **Low Power Consumption . . . 1.5 mA Max (Output Disabled)**
- **Functionally Interchangeable With SN75172**

N PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each driver)

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H = high level, L = low level,
X = irrelevant, Z = high impedance (off)

description

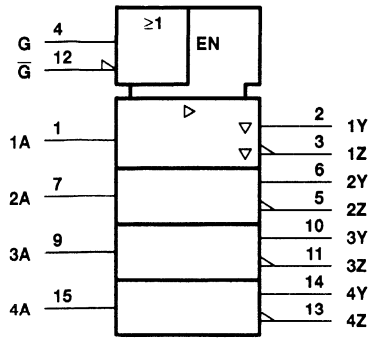
The SN65LBC172 and SN75LBC172 are monolithic quadruple differential line drivers with 3-state outputs. Both devices are designed to meet the requirements of EIA Standard RS-485. These devices are optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. Each driver features wide positive and negative common-mode output voltage ranges, current limiting, and thermal-shutdown circuitry making it suitable for party-line applications in noisy environments. Both devices are designed using LinBiCMOS™, facilitating ultra-low power consumption and inherent robustness.

Both the SN65LBC172 and SN75LBC172 provide positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. These devices offer optimum performance when used with the SN75LBC173 or SN75LBC175 quadruple line receivers. The SN65LBC172 and SN75LBC172 are available in the 16-pin DIP package (N) and the 20-pin wide-body small-outline inline-circuit (SOIC) package (DW).

The SN75LBC172 is characterized for operation over the commercial temperature range of 0°C to 70°C. The SN65LBC172 is characterized over the industrial temperature range of –40°C to 85°C.

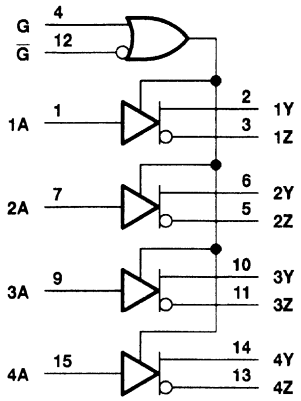
LinBiCMOS is a trademark of Texas Instruments Incorporated.

logic symbol†

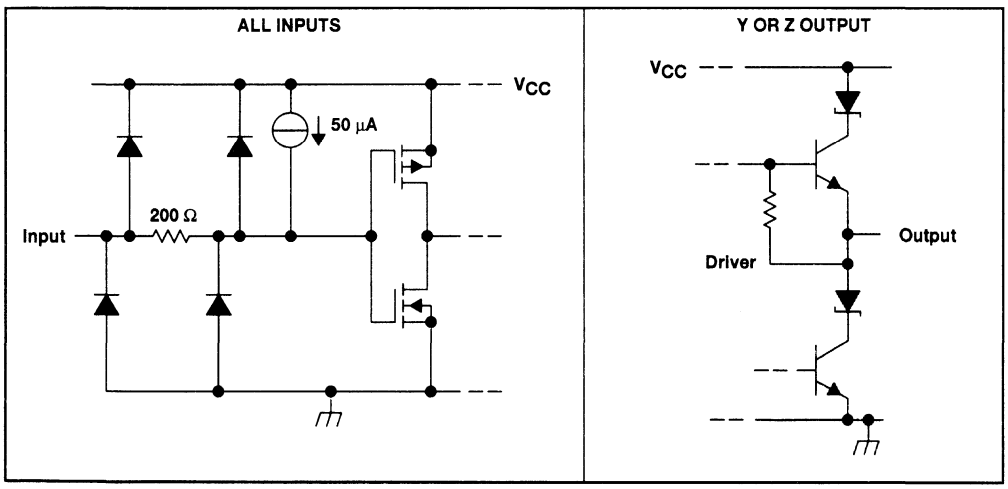


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

logic diagram (positive logic)



schematic diagrams of inputs and outputs



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.3 V to 7 V
Output voltage range, V_O ..... −10 V to 15 V
Input voltage range, V_I ..... −0.3 V to 7 V
Continuous power dissipation ..... internally limited‡
Operating free-air temperature range, T_A: SN65LBC172 ..... −40°C to 85°C
SN75LBC172 ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.
NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Voltage at any bus terminal (separately or common mode), V_O	Y or Z			12	V
				−7	
High-level output current, I_{OH}	Y or Z			−60	mA
Low-level output current, I_{OL}	Y or Z			60	mA
Continuous total power dissipation		See Dissipation Rating Table			
Operating free-air temperature, T_A	SN65LBC172	−40		85	°C
	SN75LBC172	0		70	

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW	585 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
$\lvert V_{OD}\rvert$	Differential output voltage‡	R_L = 54 Ω, See Figure 1	SN65LBC172	1.1	1.8	5	V
			SN75LBC172	1.5	1.8	5	
		R_L = 60 Ω, See Figure 2	SN65LBC172	1.1	1.7	5	
			SN75LBC172	1.5	1.7	5	
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of common-mode output voltage§	R_L = 54 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage					3 −1	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current with power off	V_{CC} = 0, V_O = −7 V to 12 V				±100	µA
I_{OZ}	High-impedance-state output current	V_O = −7 V to 12 V				±100	µA
I_{IH}	High-level input current	V_I = 2.4 V				−100	µA
I_{IL}	Low-level input current	V_I = 0.4 V				−100	µA
I_{OS}	Short-circuit output current	V_O = −7 V to 12 V				±250	mA
I_{CC}	Supply current (all drivers)	No load	Outputs enabled			7	mA
			Outputs disabled			1.5	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

‡ The minimum V_{OD} specification does not fully comply with EIA-485 at operating temperatures below 0°C. The lower output signal should be used to determine the maximum signal-transmission distance.

§ $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input changes from a high level to a low level.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω,	See Figure 3	2	11	20	ns
$t_{t(OD)}$	Differential output transition time			10	15	25	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 4			30	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 5			30	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 4			50	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 5			30	ns

PARAMETER MEASUREMENT INFORMATION

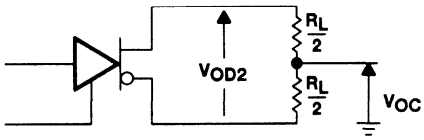


Figure 1. Differential and Common-Mode Output Voltages

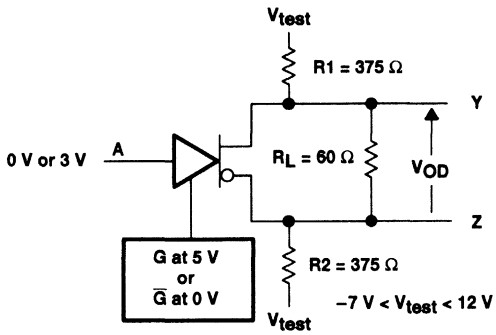
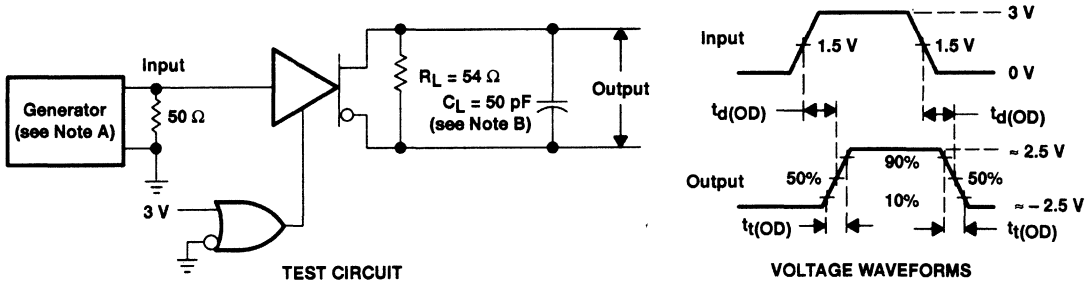


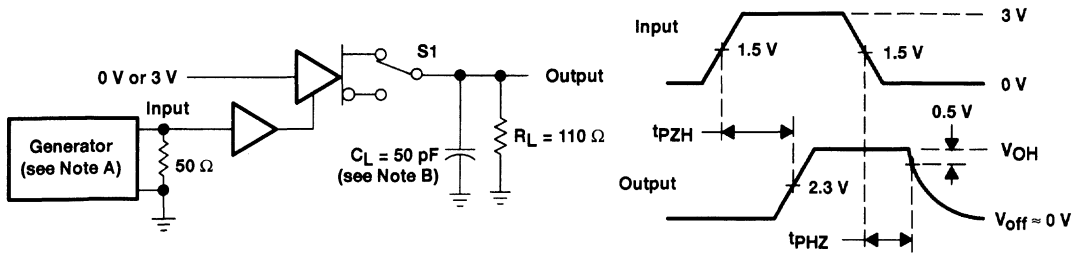
Figure 2. Driver V_{OD} Test Circuit



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 5 ns, t_f ≤ 5 ns, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.

Figure 3. Driver Differential-Output Test Circuit and Delay and Transition-Time Waveforms

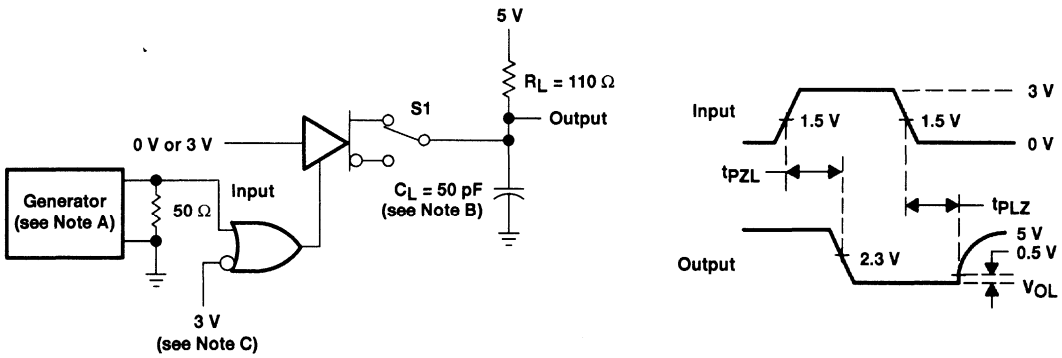
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 5 ns, t_f ≤ 5 ns, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.

Figure 4. t_{PZH} and t_{PHZ} Test Circuit and Voltage Waveforms



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 5 ns, t_f ≤ 5 ns, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$.

Figure 5. t_{PZL} and t_{PLZ} Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

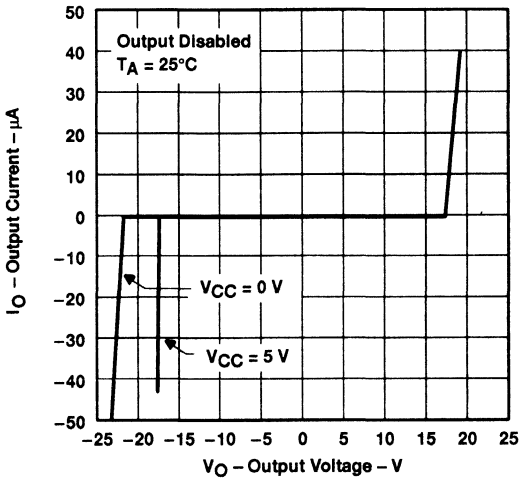


Figure 6

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

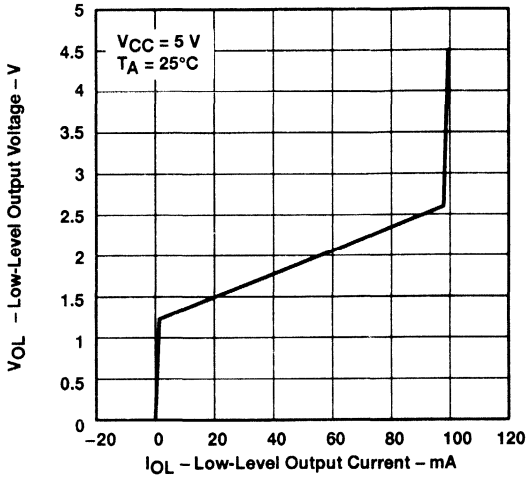


Figure 7

DIFFERENTIAL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

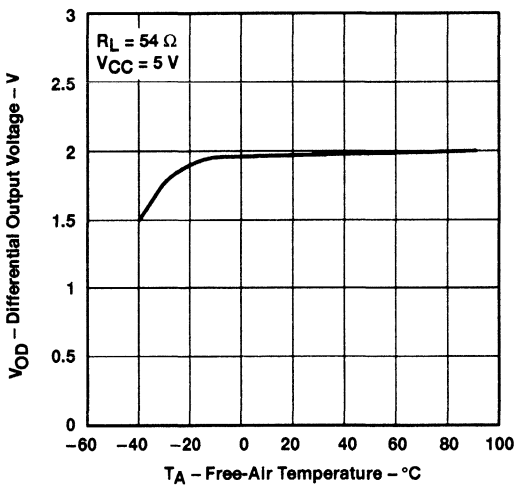


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

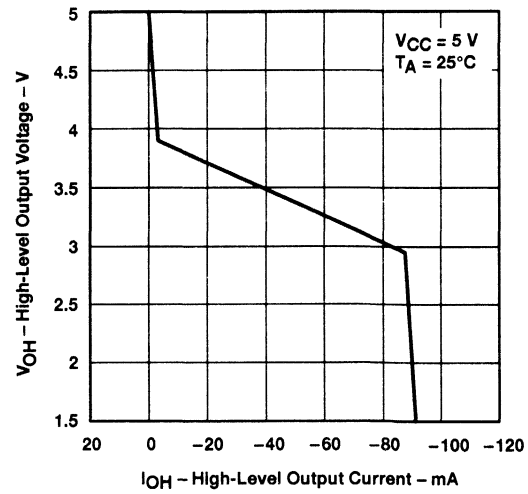


Figure 9

TYPICAL CHARACTERISTICS

DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

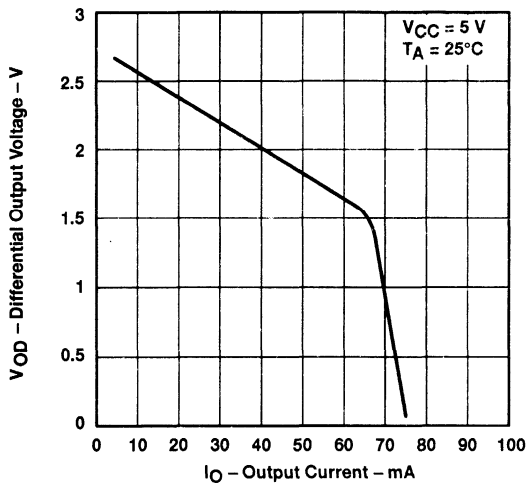


Figure 10

PROPAGATION DELAY TIME,
DIFFERENTIAL OUTPUT
vs
FREE-AIR TEMPERATURE

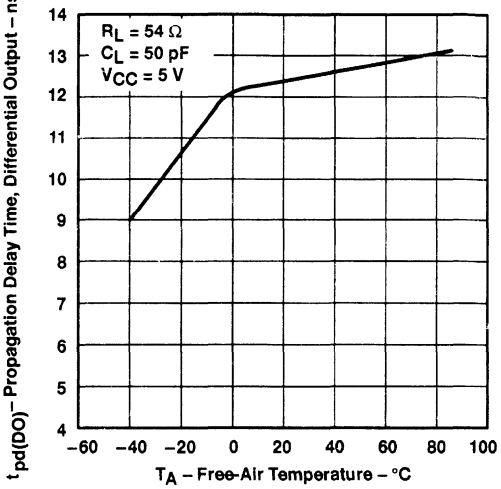


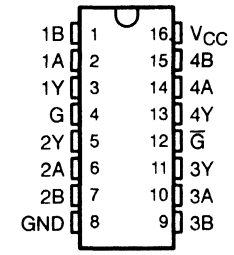
Figure 11

SN55173, SN65173, SN75173
QUADRUPLE DIFFERENTIAL LINE RECEIVERS

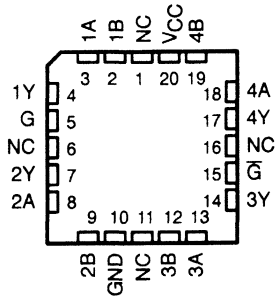
SLLS144B – OCTOBER 1980 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of ANSI EIA/TIA-422-B, EIA/TIA-423-B, and RS-485 and ITU Recommendations V.10, V.11, X.26, and X.27**
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments**
- **3-State Outputs**
- **Common-Mode Input Voltage Range of −12 V to 12 V**
- **Input Sensitivity . . . ±200 mV**
- **Input Hysteresis . . . 50 mV Typ**
- **High Input Impedance . . . 12 kΩ Min**
- **Operates From Single 5-V Supply**
- **Low Power Requirements**
- **Plug In Replacement for AM26LS32**

SN75173 . . . D OR N PACKAGE
SN55173 . . . J PACKAGE
(TOP VIEW)



SN55173 . . . FK PACKAGE
(TOP VIEW)



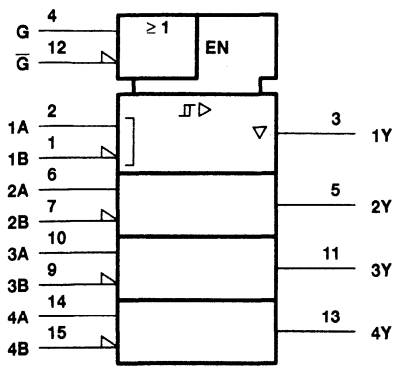
NC – No internal connection

description

The SN55173, SN65173, and SN75173 are monolithic quadruple differential line receivers with 3-state outputs. They are designed to meet the requirements of ANSI Standards EIA/TIA-422-B, EIA/TIA-423-B, RS-485, and several ITU recommendations. The standards are for balanced multipoint bus transmission at rates up to 10 megabits per second. The four receivers share two OR enable inputs, one active when high, the other active when low. The '173 devices feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of −12 to 12 V. Fail-safe design ensures that if the inputs are open circuited, the outputs are always high. The SN65173 and SN75173 are designed for optimum performance when used with the SN75172 or SN75174 quad differential line drivers.

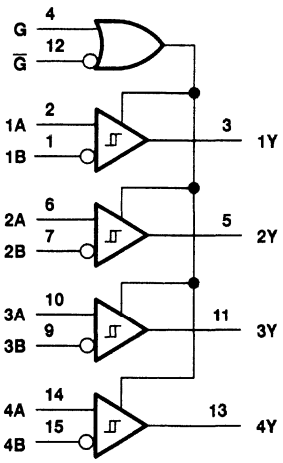
The SN55173 is characterized over the full military temperature range of −55°C to 125°C. The SN65173 is characterized for operation from −40°C to 85°C. The SN75173 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

logic diagram (positive logic)

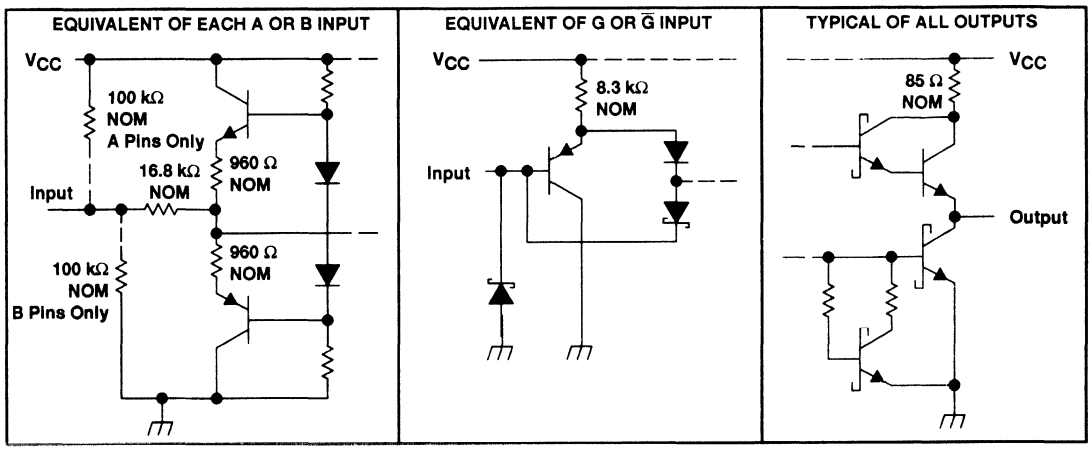


FUNCTION TABLE
(each receiver)

DIFFERENTIAL A – B	ENABLES G	ENABLES $\overline{G}$	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
-0.2 V $< V_{ID} < 0.2$ V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
X	L	H	Z
Open circuit	X	L	H
	H	X	H

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage (V_I or B inputs) ..... ±25 V
Differential input voltage, V_{ID} (see Note 2) ..... ±25 V
Enable input voltage, V_I ..... 7 V
Low-level output current, I_{OL} ..... 50 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN55173 ..... −55°C to 125°C
SN65173 ..... −40°C to 85°C
SN75173 ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Case temperature for 60 seconds, T_C: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	—

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	SN55173	4.5	5	5.5	V
	SN65173, SN75173	4.75	5	5.25	
Common-mode input voltage, V_{IC}				±12	V
Differential input voltage, V_{ID}				±12	V
High-level enable-input voltage, V_{IH}		2			V
Low-level enable-input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}				−400	μA
Low-level output current, I_{OL}				16	mA
Operating free-air temperature, T_A	SN55173	−55		125	°C
	SN65173	−40		85	
	SN75173	0		70	

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V, I_O = −0.4 mA				0.2	V
V_{IT-}	Negative-going input threshold voltage	V_O = 0.5 V, I_O = 16 mA		−0.2‡			V
V_{hys}	Hysteresis ($V_{IT+} - V_{IT-}$)	See Figure 4			50		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = −400 μA	SN55173	2.5			V
			SN65173, SN75173	2.7			
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 1	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input at 0 V, See Note 3	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current			−15		−85	mA
I_{CC}	Supply current	Outputs disabled				70	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltage levels only.
NOTE 3: Refer to ANSI Standards EIA/TIA-422-B and EIA/TIA423-B for exact conditions.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = –1.5 V to 1.5 V, C_L = 15 pF, See Figure 1			20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output				22	35	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 2		17	22	ns
t_{PZL}	Output enable time to low level	C_L = 15 pF,	See Figure 3		20	25	ns
t_{PHZ}	Output disable time from high level	C_L = 5 pF,	See Figure 2		21	30	ns
t_{PLZ}	Output disable time from low level	C_L = 5 pF,	See Figure 3		30	40	ns

PARAMETER MEASUREMENT INFORMATION

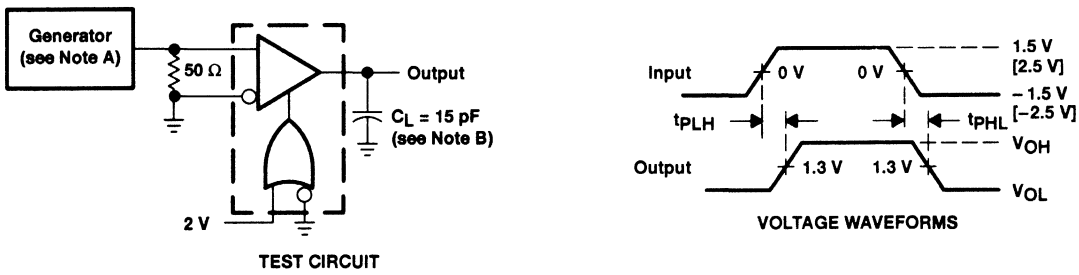


Figure 1. t_{PLH}, t_{PHL} Test Circuit and Voltage Waveforms

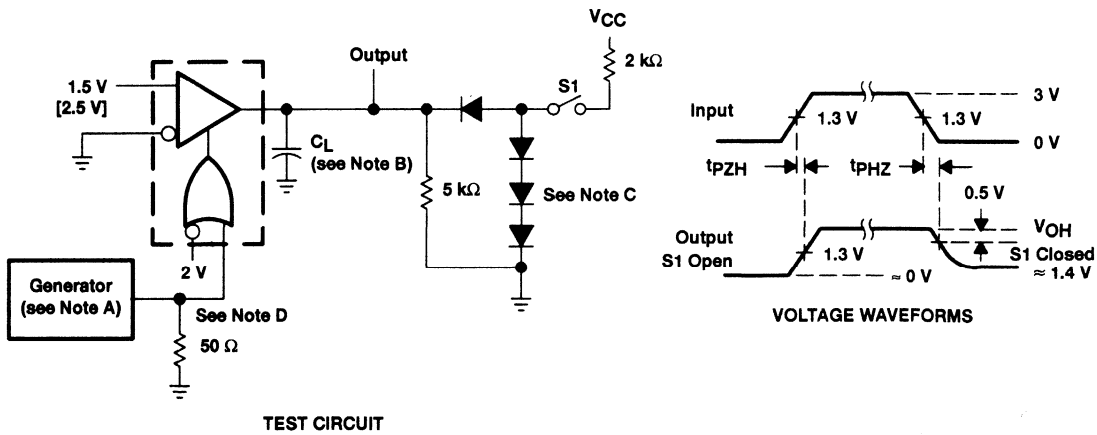


Figure 2. t_{PHZ}, t_{PZH} Test Circuit and Voltage Waveforms

[ ] represent voltages on the SN55173 only.

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

C. All diodes are 1N916 or equivalent.

D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

PARAMETER MEASUREMENT INFORMATION

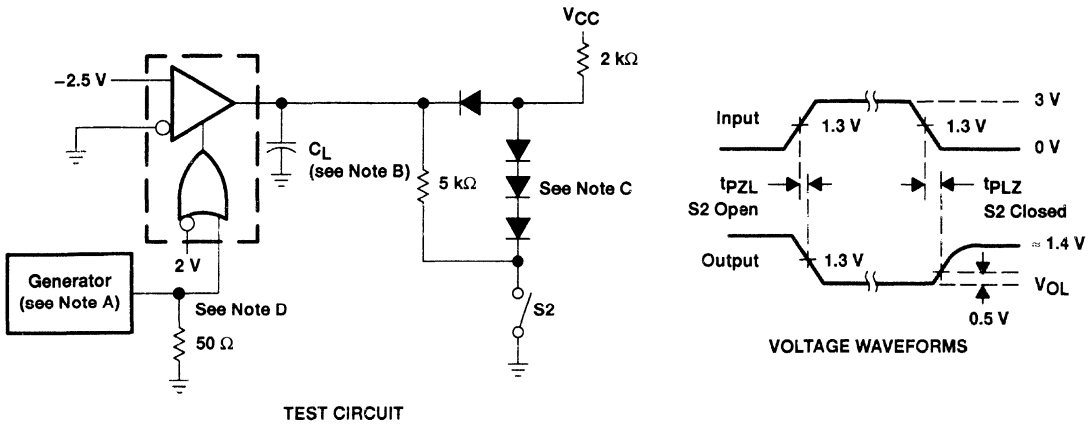


Figure 3. t_{PZL}, t_{PLZ} Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \le 6$ ns, $t_f \le 6$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.
D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

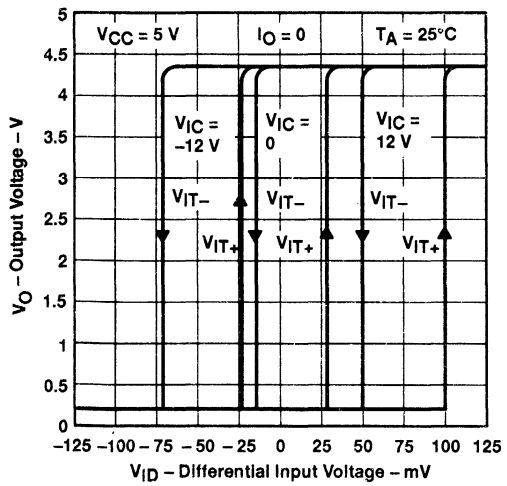


Figure 4

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

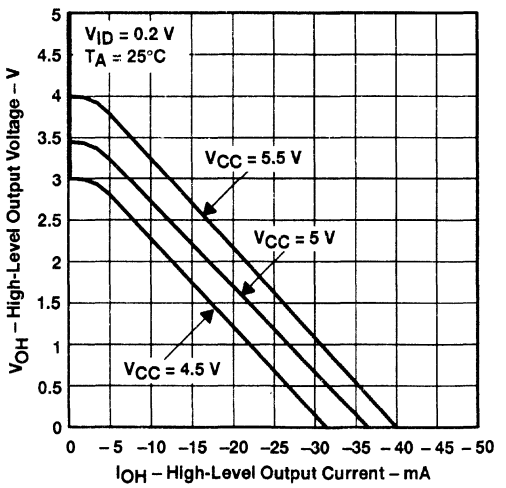


Figure 5

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

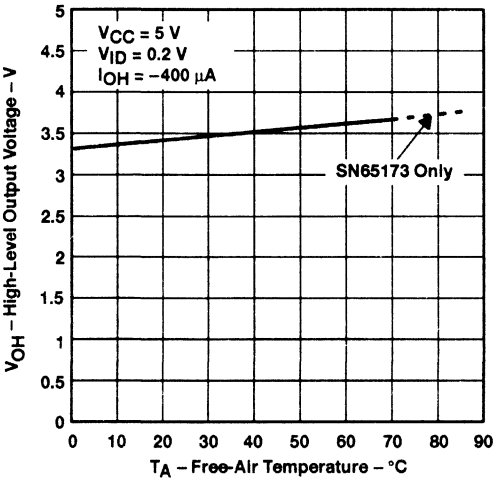


Figure 6

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

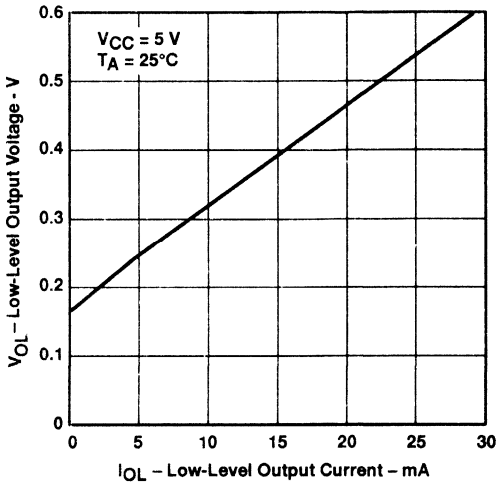


Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

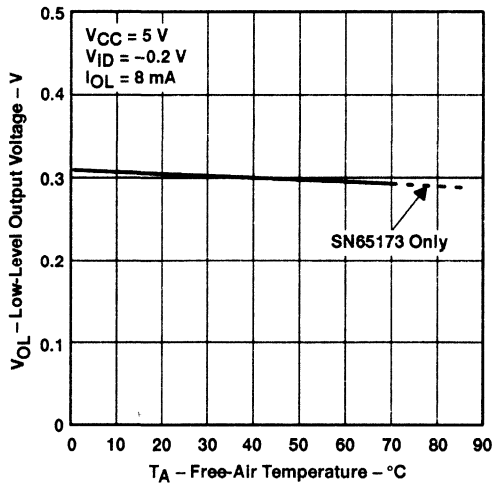


Figure 8

OUTPUT VOLTAGE
vs
ENABLE G VOLTAGE

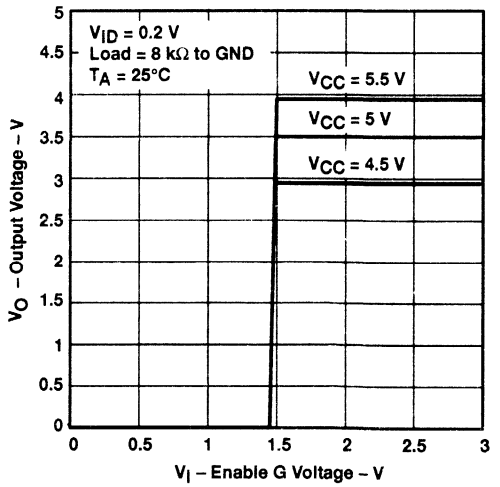


Figure 9

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
ENABLE G VOLTAGE

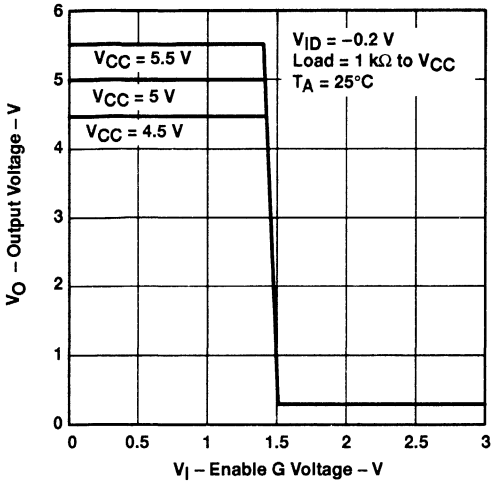


Figure 10

INPUT CURRENT
vs
INPUT VOLTAGE

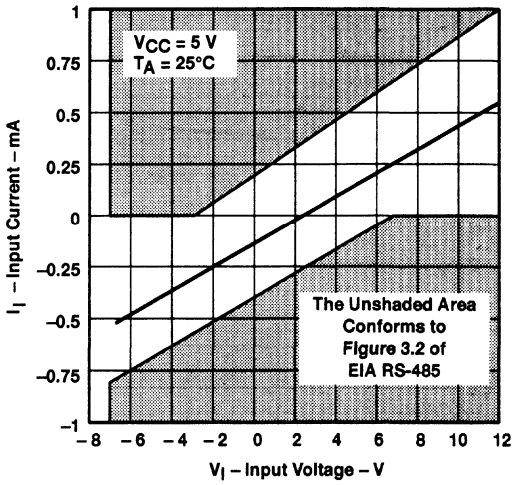
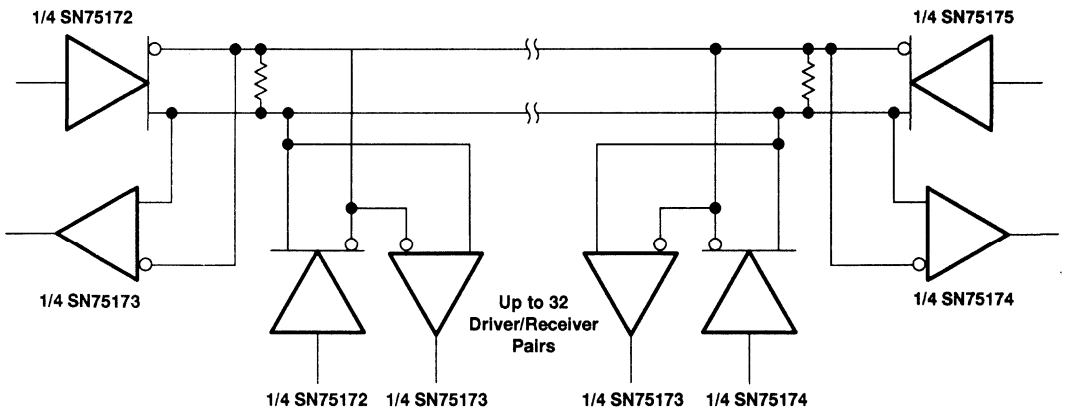


Figure 11

APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

Figure 12. Typical Application Circuit

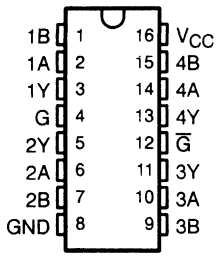
- **Meets or Exceeds the Requirements of ANSI EIA/TIA-422-B, EIA/TIA-423-B, and RS-485**
- **Meets or Exceeds the Requirements of ITU Recommendations V.10, V.11, X.26, and X.27**
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments**
- **3-State Outputs**
- **Common-Mode Input Voltage Range of −12 V to 12 V**
- **Input Sensitivity . . . ±200 mV**
- **Input Hysteresis . . . 50 mV Typ**
- **High Input Impedance . . . 12 kΩ Min**
- **Operates From Single 5-V Supply**
- **Low Supply Current Requirement 27 mA Max**

description

The SN75ALS173 is a monolithic quadruple differential line receiver with 3-state outputs. It is designed to meet the requirements of ANSI Standards EIA/TIA-422-B, EIA/TIA-423-B, RS-485, and several ITU recommendations. Advanced low-power Schottky technology provides high speed without the usual power penalty. The four receivers have an ORed pair of enables in common. Either G high or $\overline{G}$ low enables all of the receivers. The device features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of −12 V to 12 V.

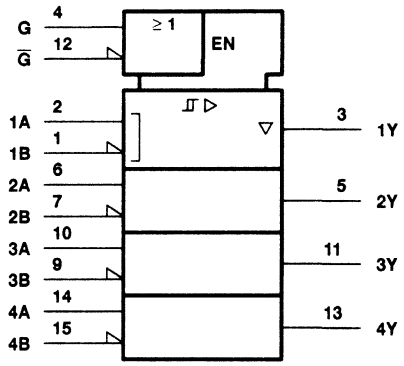
The SN75ALS173 is characterized for operation from 0°C to 70°C.

N OR NS† PACKAGE
(TOP VIEW)



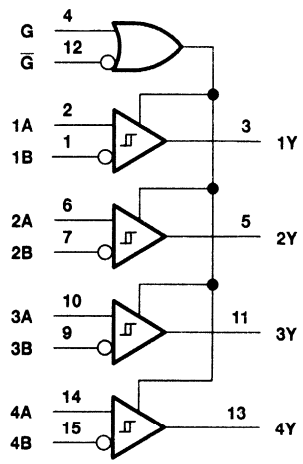
† The NS package is only available left-end taped and reeled (order device SN75ALS173 NSLE).

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

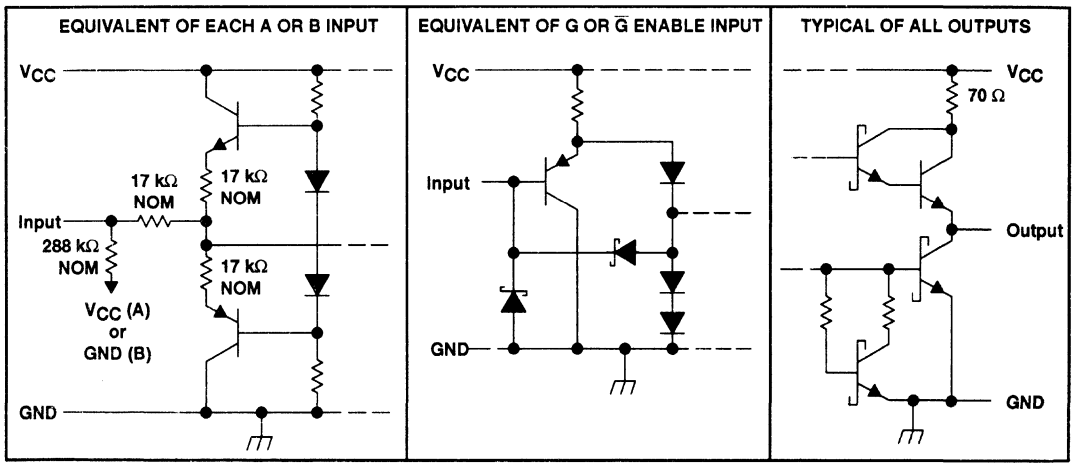


FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A – B	ENABLES G	ENABLES $\overline{G}$	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
-0.2 V $< V_{ID} < 0.2$ V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
X	L	H	Z
Open Circuit	H	X	H
	X	L	H

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I (A or B inputs) ..... ±14 V
Differential input voltage, V_{ID} (see Note 2) ..... ±14 V
Enable input voltage, V_I ..... 7 V
Low-level output current, I_{OL} ..... 50 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
N	1150 mW	9.2 mW/°C	736 mW
NS	625 mW	5.0 mW/°C	400 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Common-mode input voltage, V_{IC}				±12	V
Differential input voltage, V_{ID}				±12	V
High-level input voltage, V_{IH}	G, $\overline{G}$	2			V
Low-level input voltage, V_{IL}	G, $\overline{G}$			0.8	V
High-level output current, I_{OH}				−400	μA
Low-level output current, I_{OL}				8	mA
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted) (see Note 3)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage						200	mV
V_{IT-}	Negative-going input threshold voltage				−200‡			mV
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)					50		mV
V_{IK}	Input clamp voltage	G, $\overline{G}$	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage		V_{ID} = 200 mV, I_{OH} = −400 μA, See Figure 1		2.7			V
V_{OL}	Low-level output voltage		V_{ID} = −200 mV, I_{OL} = 8 mA, See Figure 1				0.45	V
I_{OZ}	High-impedance-state output current		V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current		Other input at 0 V	V_I = 12 V			1	mA
				V_I = −7 V			−0.8	
I_{IH}	High-level input current	G, $\overline{G}$	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level input current	G, $\overline{G}$	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance				12			kΩ
I_{OS}	Short-circuit output current		See Note 4		−15		−85	mA
I_{CC}	Supply current (total package)		No load,	Outputs enabled		16	24	mA
			No load,	Outputs disabled		18	27	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltage levels only.

NOTES: 3. Refer to ANSI Standard RS-485 for exact conditions.

4. The duration of the short circuit should not cause the maximum package power dissipation to be exceeded.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	V_{ID} = −2.5 V to 2.5 V, See Figure 2	9	18	27	ns
t_{PLH}	Propagation delay time, low- to high-level output		9	18	27	ns
t_{PZH}	Output enable time to high level	See Figure 3	4	12	18	ns
t_{PZL}	Output enable time to low level	See Figure 4	6	13	21	ns
t_{PHZ}	Output disable time from high level	See Figure 3	10	21	27	ns
t_{PLZ}	Output disable time from low level	See Figure 4	8	15	25	ns

PARAMETER MEASUREMENT INFORMATION

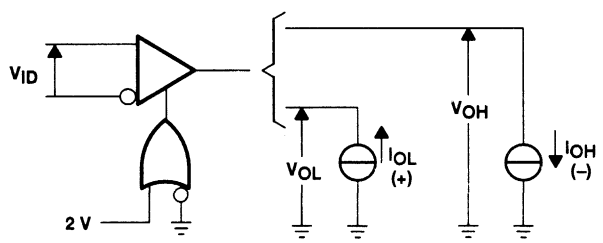


Figure 1. V_{OH}, V_{OL}

PARAMETER MEASUREMENT INFORMATION

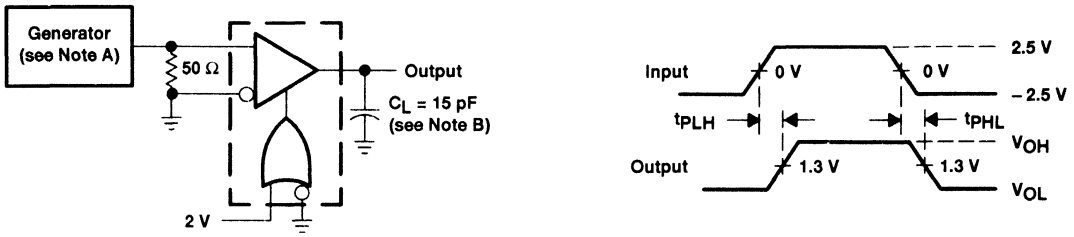


Figure 2. Test Circuit and Voltage Waveforms

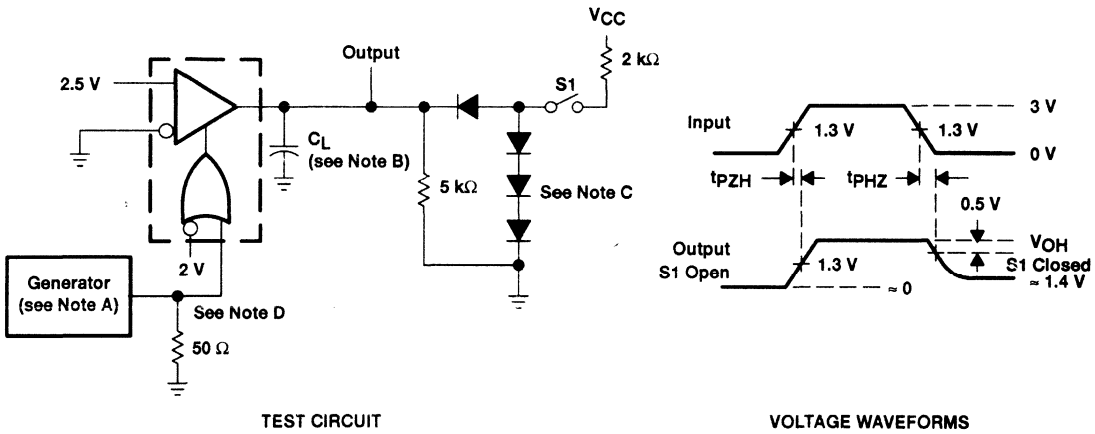


Figure 3. Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.
D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

PARAMETER MEASUREMENT INFORMATION

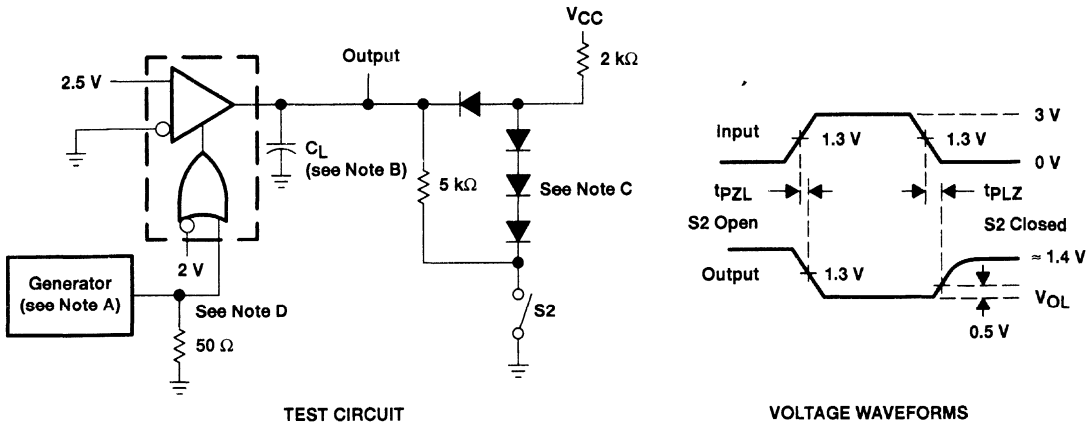


Figure 4. Test Circuit and Voltage Waveforms

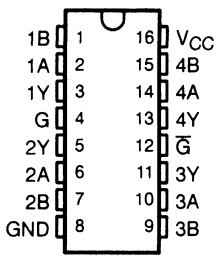
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.
D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

SN55LBC173
QUADRUPLE LOW-POWER DIFFERENTIAL LINE DRIVER

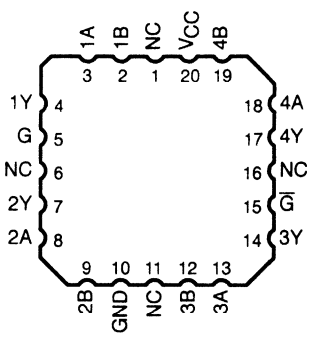
SGLS081 – MARCH 1995

- **Meets EIA Standards RS-422-A, RS-423-A, RS-485, and CCITT V.11**
- **Designed to Operate With Pulse Durations as Short as 20 ns**
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments**
- **Input Sensitivity . . . ±200 mV**
- **Low-Power Consumption . . . 20 mA Max**
- **Open-Circuit Fail-Safe Design**
- **Pin Compatible With SN75173 and AM26LS32**

J OR W PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN55LBC173 is a monolithic quadruple differential line receiver with 3-state outputs and is designed to meet the requirements of the EIA standards RS-422-A, RS-423-A, RS-485, and CCITT V.11. This device is optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. The four receivers share two ORed enable inputs, one active when high, the other active when low. Each receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of 12 V to –7 V. Fail-safe design ensures that if the inputs are open circuited, the output is always high. The SN55LBC173 is designed using the Texas Instruments proprietary LinBiCMOS™ technology that provides low power consumption, high switching speeds, and robustness.

This device offers optimum performance when used with the SN55LBC172M quadruple line driver. The SN55LBC173 is available in the 16-pin CDIP (J), the 16-pin CPAK (W), or the 20-pin LCCC (FK) packages.

The SN55LBC173 is characterized over the military temperature range of –55°C to 125°C.

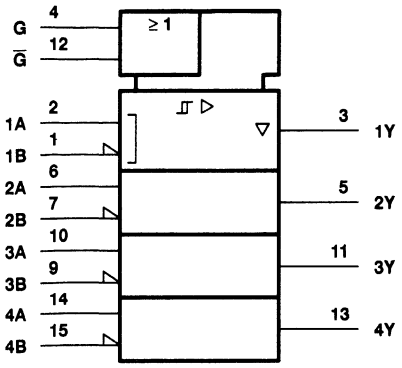
FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A–B	ENABLES G	ENABLES $\overline{G}$	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
-0.2 V $< V_{ID} < 0.2$ V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
X	L	H	Z
Open circuit	H	X	H
	X	L	H

H = high level, L = low level, X = irrelevant,
Z = high impedance (off), ? = indeterminate

LinBiCMOS is a trademark of Texas Instruments Incorporated.

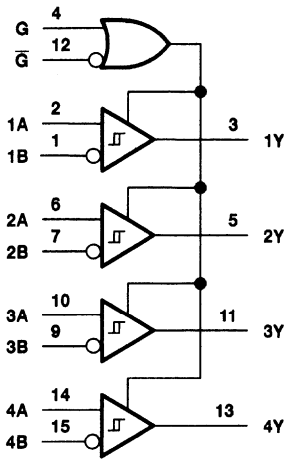
logic symbol†



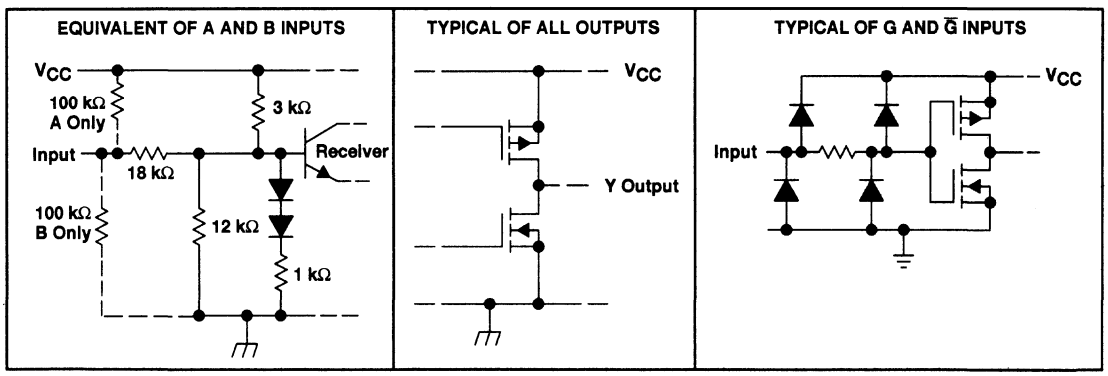
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the J or W package.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.3 V to 7 V
Input voltage, V_I (A or B inputs) ..... ±25 V
Differential input voltage, V_{ID} (see Note 2) ..... ±25 V
Data and control voltage range ..... −0.3 V to 7 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −55°C to 125°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 125°C$ POWER RATING
FK	1375 mW	11.0 mW/°C	275 mW
J	1375 mW	11.0 mW/°C	275 mW
W	1000 mW	8.0 mW/°C	200 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Common-mode input voltage, V_{IC}		−7		12	V
Differential input voltage, V_{ID}				±6	V
High-level input voltage, V_{IH}	G inputs	2			V
Low-level input voltage, V_{IL}	G inputs			0.8	V
High-level output current, I_{OH}				−8	mA
Low-level output current, I_{OL}				16	mA
Operating free-air temperature, T_A		−55		125	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		I_O = −8 mA					0.2	V
V_{IT-}	Negative-going input threshold voltage		I_O =16 mA			−0.2			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)						45		mV
V_{IK}	Enable input clamp voltage		I_I = −18 mA				−0.9	−1.5	V
V_{OH}	High-level output voltage		V_{ID} = 200 mV,	I_{OH} = −8 mA		3.5	4.5		V
V_{OL}	Low-level output voltage		V_{ID} = −200 mV,	I_{OL} = 16 mA			0.3	0.5	V
			V_{ID} = −200 mV,	I_{OL} = 16 mA,	T_A = 125°C			0.7	
I_{OZ}	High-impedance-state output current		V_O = 0 V to V_{CC}					±20	µA
I_I	Bus input current	A or B inputs	V_{IH} = 12 V,	V_{CC} = 5 V,	Other inputs at 0 V		0.7	1	mA
			V_{IH} = 12 V,	V_{CC} = 0 V,	Other inputs at 0 V		0.8	1	
			V_{IH} = −7 V,	V_{CC} = 5 V,	Other inputs at 0 V		−0.5	−0.8	
			V_{IH} = −7 V,	V_{CC} = 0 V,	Other inputs at 0 V		−0.4	−0.8	
I_{IH}	High-level input current		V_{IH} = 5 V					±20	µA
I_{IL}	Low-level input current		V_{IL} = 0 V					−20	µA
I_{OS}	Short-circuit output current		V_O = 0				−80	−120	mA
I_{CC}	Supply current		Outputs enabled,	I_O = 0,	V_{ID} = 5 V		11	20	mA
			Outputs disabled				0.9	1.4	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output	V_{ID} = −1.5 V to 1.5 V, See Figure 1	25°C	11	22	30	ns
			−55°C to 125°C	11		35	
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5 V to 1.5 V, See Figure 1	25°C	11	22	35	ns
			−55°C to 125°C	11		35	
t_{PZH}	Output enable time to high level	See Figure 2	25°C		17	40	ns
			−55°C to 125°C			45	
t_{PZL}	Output enable time to low level	See Figure 3	25°C		18	30	ns
			−55°C to 125°C			35	
t_{PHZ}	Output disable time from high level	See Figure 2	25°C		30	40	ns
			−55°C to 125°C			55	
t_{PLZ}	Output disable time from low level	See Figure 3	25°C		25	40	ns
			−55°C to 125°C			45	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	See Figure 1	25°C		0.5	6	ns
			−55°C to 125°C			7	
t_t	Transition time	See Figure 1	25°C		5	10	ns
			−55°C to 125°C			16	

PARAMETER MEASUREMENT INFORMATION

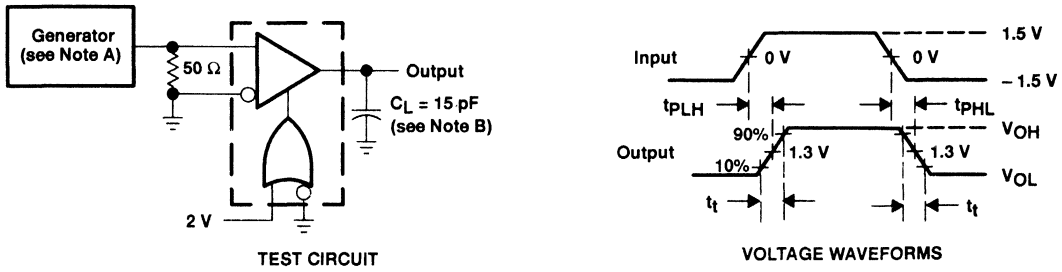


Figure 1. t_{pd} and t_t Test Circuit and Voltage Waveforms

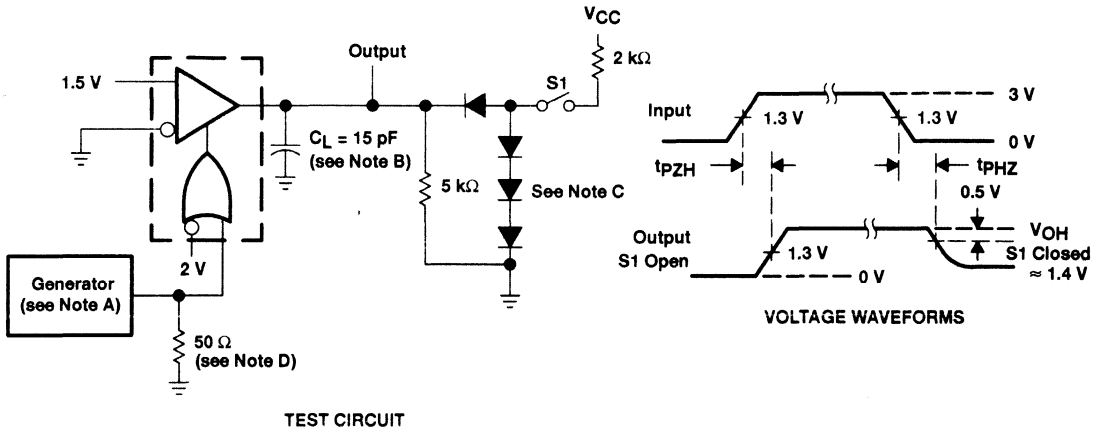


Figure 2. t_{PHZ} and t_{PZH} Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.
D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

PARAMETER MEASUREMENT INFORMATION

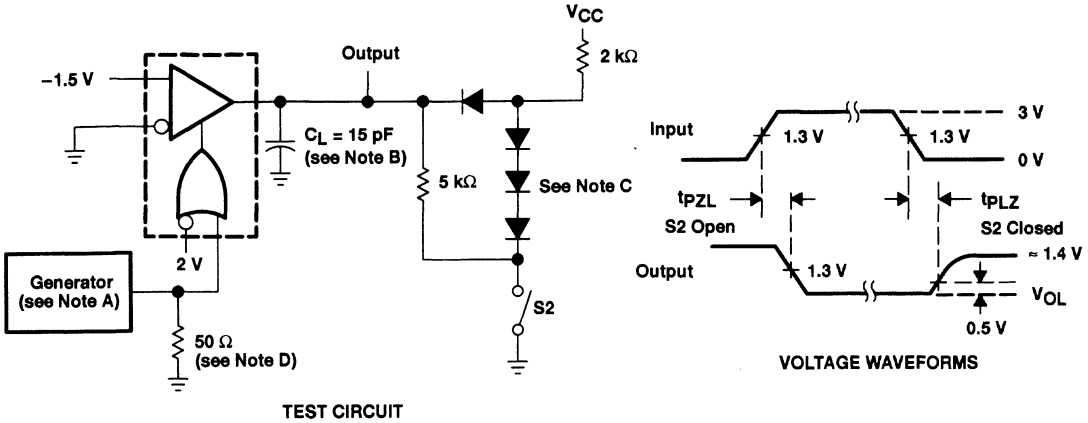


Figure 3. t_{PZL} and t_{PLZ} Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.
D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

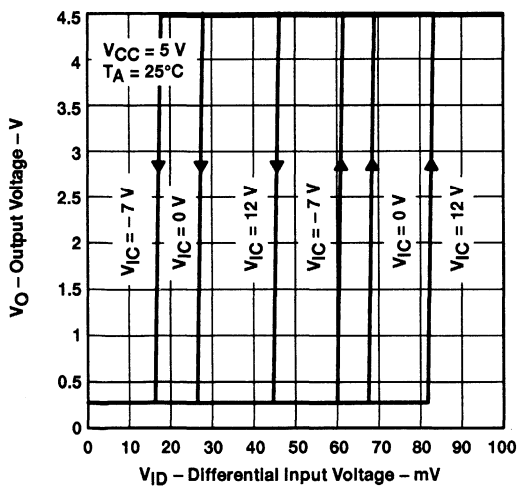


Figure 4

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

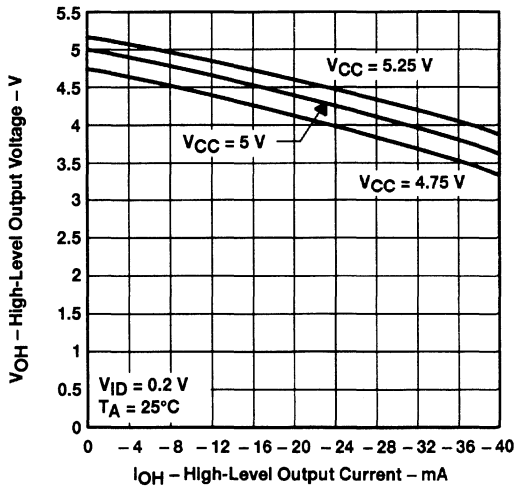


Figure 5

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

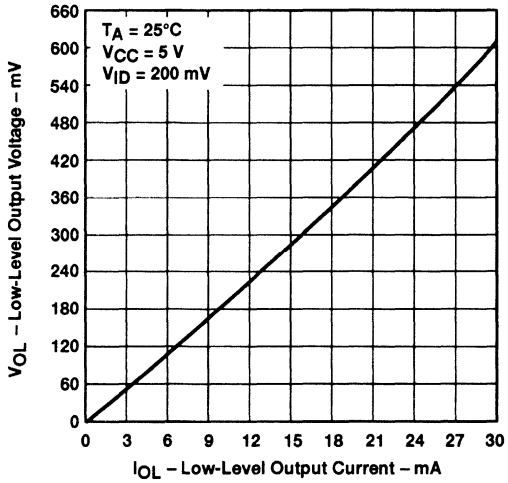


Figure 6

AVERAGE SUPPLY CURRENT
vs
FREQUENCY

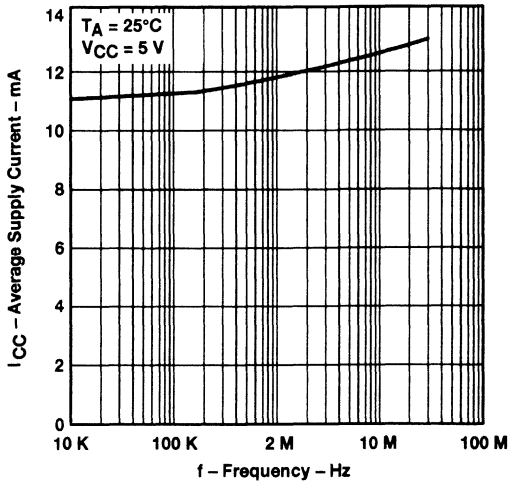


Figure 7

BUS INPUT CURRENT
vs
INPUT VOLTAGE
(COMPLEMENTARY INPUT AT 0 V)

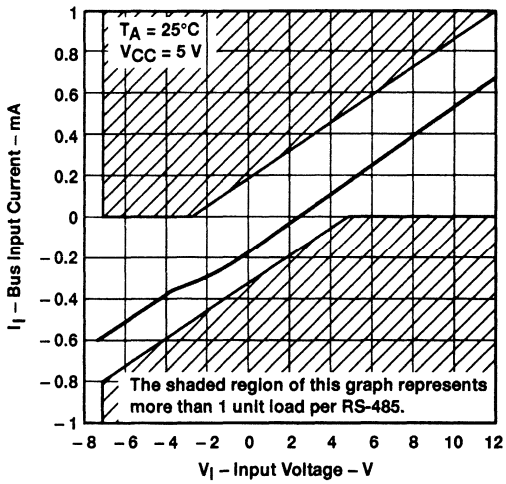


Figure 8

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

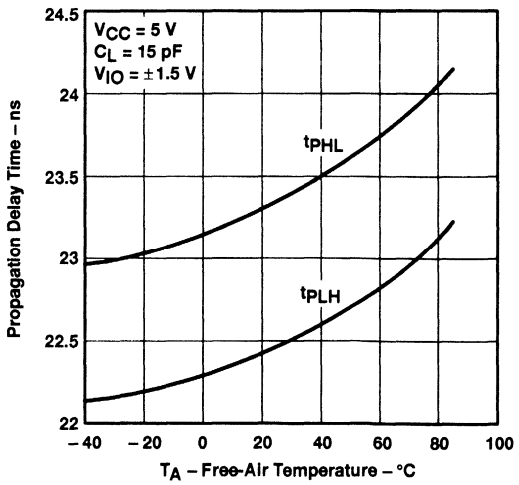
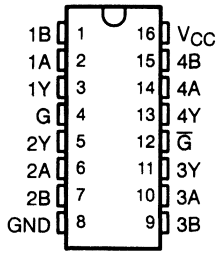


Figure 9

- **Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-422-B, EIA/TIA-423-B, RS-485, and ITU Recommendations V.10 and V.11.**
- **Designed to Operate With Pulse Durations as Short as 20 ns**
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments**
- **Input Sensitivity . . . ±200 mV**
- **Low-Power Consumption . . . 20 mA Max**
- **Open-Circuit Fail-Safe Design**
- **Pin Compatible With SN75173 and AM26LS32**

D OR N PACKAGE
(TOP VIEW)



description

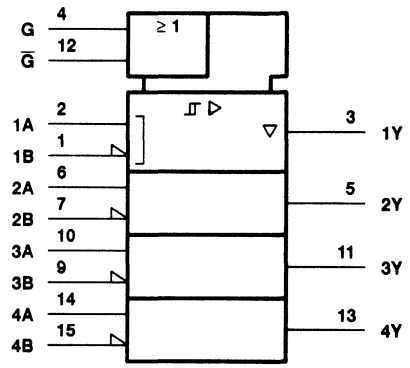
The SN65LBC173 and SN75LBC173 are monolithic quadruple differential line receivers with 3-state outputs and are designed to meet the requirements of the ANSI standards EIA/TIA-422-B, EIA/TIA-423-B, RS-485, and ITU Recommendations V.10 and V.11. The devices are optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. The four receivers share two ORed enable inputs, one active when high, the other active when low.

Each receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of 12 V to −7 V. Fail-safe design ensures that if the inputs are open circuited, the output is always high. Both devices are designed using the Texas Instruments proprietary LinBiCMOS™ technology that provides low power consumption, high switching speeds, and robustness.

These devices offer optimum performance when used with the SN75LBC172 or SN75LBC174 quadruple line drivers. The SN65LBC173 and SN75LBC173 are available in the 16-pin DIP (N) and SOIC (D) packages.

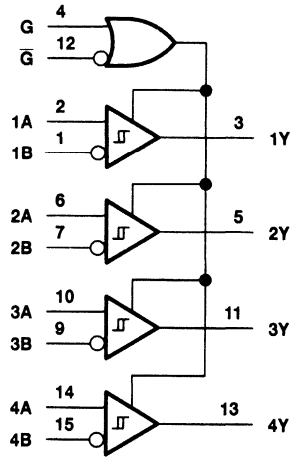
The SN65LBC173 is characterized over the industrial temperature range of −40°C to 85°C. The SN75LBC173 is characterized for operation over the commercial temperature range of 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



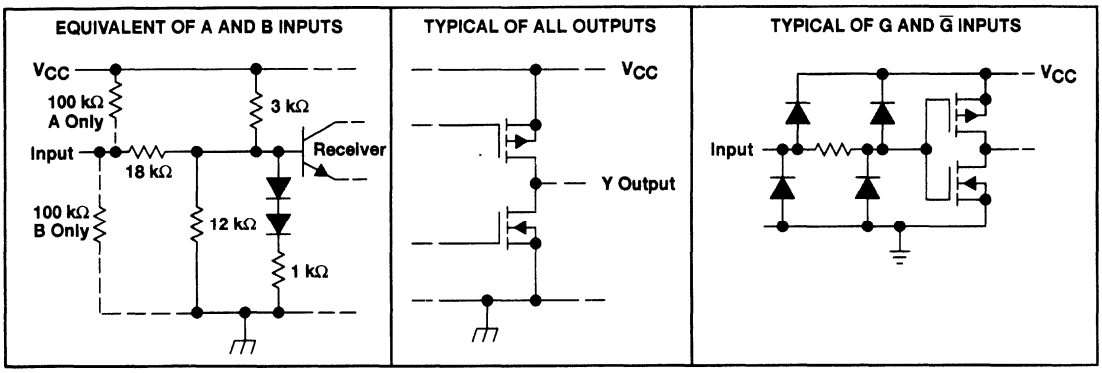
LinBiCMOS is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A–B	ENABLES G	ENABLES $\overline{G}$	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
-0.2 V $< V_{ID} < 0.2$ V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
X	L	H	Z
Open Circuit	H	X	H
	X	L	H

H = high level, L = low level, X = irrelevant,
Z = high impedance (off), ? = indeterminate

schematics of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.3 V to 7 V
Input voltage, V_I (A or B inputs) ..... ±25 V
Differential input voltage, V_{ID} (see Note 2) ..... ±25 V
Data and control voltage range ..... −0.3 V to 7 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65LBC173 ..... −40°C to 85°C
SN75LBC173 ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	1100 mW	8.7 mW/°C	708 mW	578 mW
N	1510 mW	12.1 mW/°C	965 mW	784 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Common-mode input voltage, V_{IC}		−7		12	V
Differential input voltage, V_{ID}				±6	V
High-level input voltage, V_{IH}	G inputs	2			V
Low-level input voltage, V_{IL}	G inputs			0.8	V
High-level output current, I_{OH}				−8	mA
Low-level output current, I_{OL}				16	mA
Operating free-air temperature, T_A	SN65LBC173	−40		85	°C
	SN75LBC173	0		70	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		I_O = −8 mA					0.2	V
V_{IT-}	Negative-going input threshold voltage		I_O =16 mA			−0.2			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)						45		mV
V_{IK}	Enable input clamp voltage		I_I = −18 mA				−0.9	−1.5	V
V_{OH}	High-level output voltage		V_{ID} = 200 mV,	I_{OH} = −8 mA		3.5	4.5		V
V_{OL}	Low-level output voltage		V_{ID} = −200 mV,	I_{OL} = 16 mA			0.3	0.5	V
I_{OZ}	High-impedance-state output current		V_O = 0 V to V_{CC}					±20	µA
I_I	Bus input current	A or B inputs	V_{IH} = 12 V,	V_{CC} = 5 V,	Other inputs at 0 V		0.7	1	mA
			V_{IH} = 12 V,	V_{CC} = 0 V,	Other inputs at 0 V		0.8	1	mA
			V_{IH} = −7 V,	V_{CC} = 5 V,	Other inputs at 0 V		−0.5	−0.8	mA
			V_{IH} = −7 V,	V_{CC} = 0 V,	Other inputs at 0 V		−0.4	−0.8	mA
I_{IH}	High-level input current		V_{IH} = 5 V					±20	µA
I_{IL}	Low-level input current		V_{IL} = 0 V					−20	µA
I_{OS}	Short-circuit output current		V_O = 0				−80	−120	mA
I_{CC}	Supply current		Outputs enabled,	I_O = 0,	V_{ID} = 5 V		11	20	mA
			Outputs disabled				0.9	1.4	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	V_{ID} = −1.5 V to 1.5 V, See Figure 1	11	22	30	ns
t_{PLH}	Propagation delay time, low- to high-level output		11	22	30	ns
t_{PZH}	Output enable time to high level	See Figure 2		17	30	ns
t_{PZL}	Output enable time to low level	See Figure 3		18	30	ns
t_{PHZ}	Output disable time from high level	See Figure 2		35	45	ns
t_{PLZ}	Output disable time from low level	See Figure 3		25	40	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	See Figure 2		0.5	6	ns
t_t	Transition time	See Figure 1		5	10	ns

PARAMETER MEASUREMENT INFORMATION

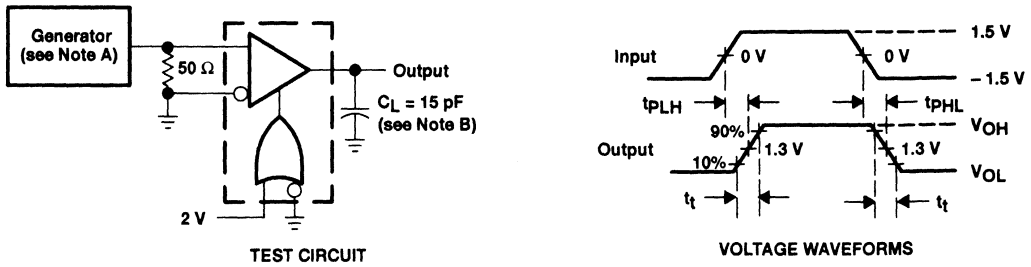


Figure 1. t_{pd} and t_t Test Circuit and Voltage Waveforms

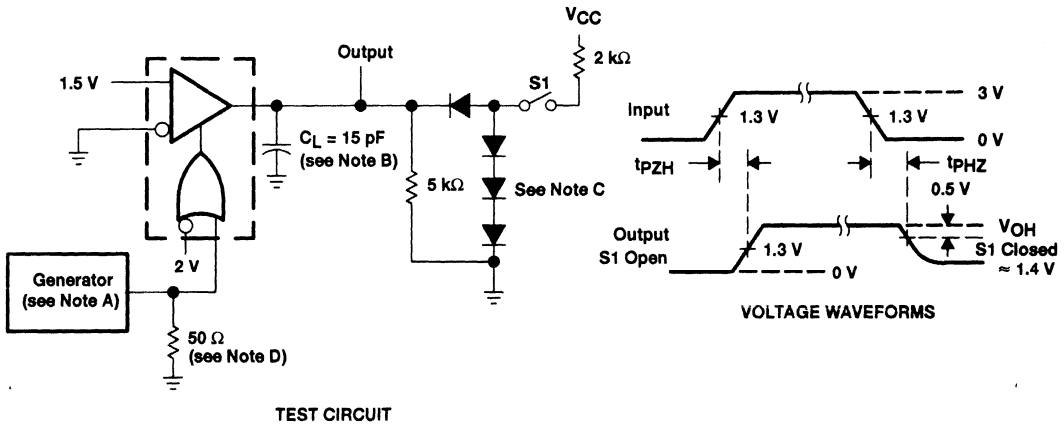


Figure 2. t_{PHZ} and t_{PZH} Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.
D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

PARAMETER MEASUREMENT INFORMATION

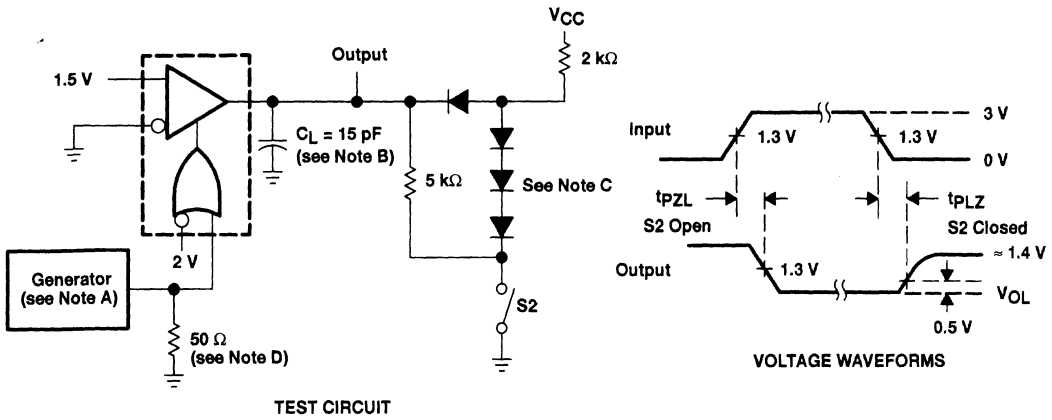


Figure 3. t_{PZL} and t_{PLZ} Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \le 6$ ns, $t_f \le 6$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.
D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

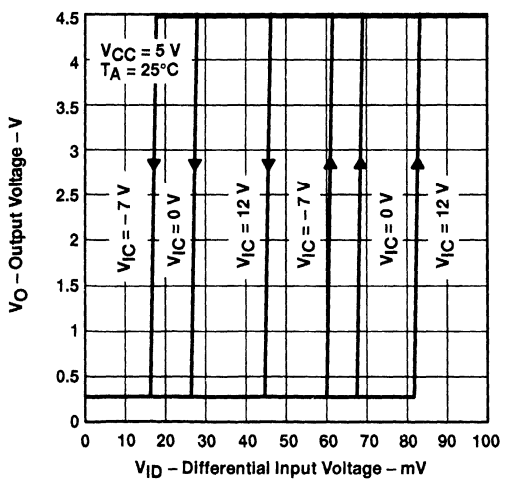


Figure 4

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

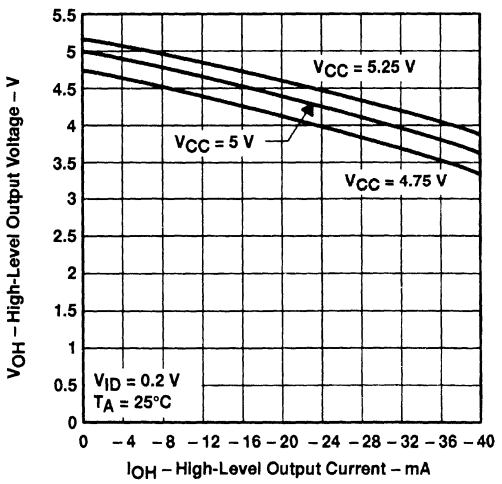


Figure 5

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

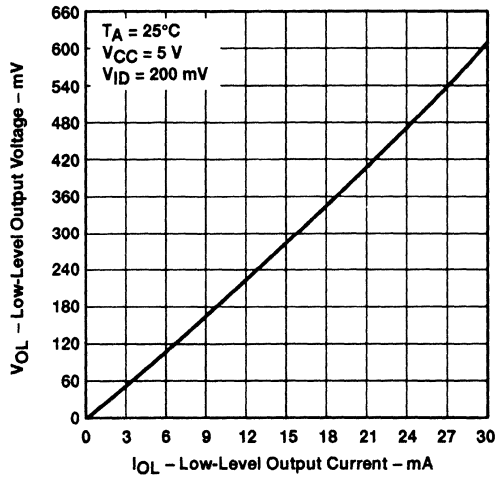


Figure 6

AVERAGE SUPPLY CURRENT
vs
FREQUENCY

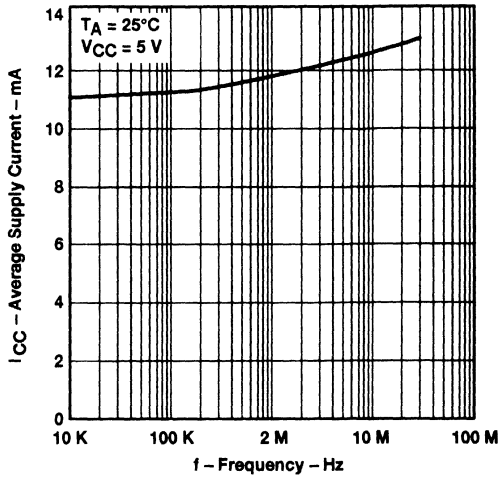


Figure 7

BUS
INPUT CURRENT
vs
INPUT VOLTAGE
(COMPLEMENTARY INPUT AT 0 V)

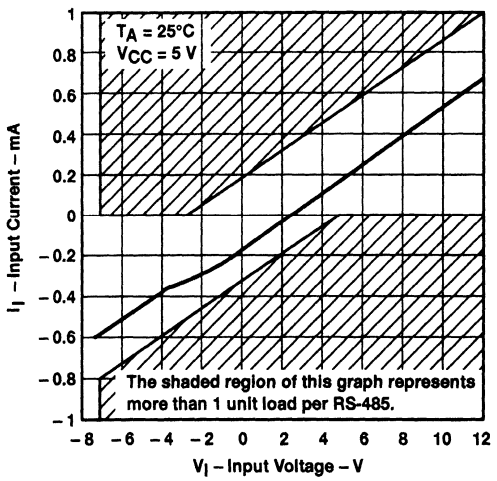


Figure 8

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

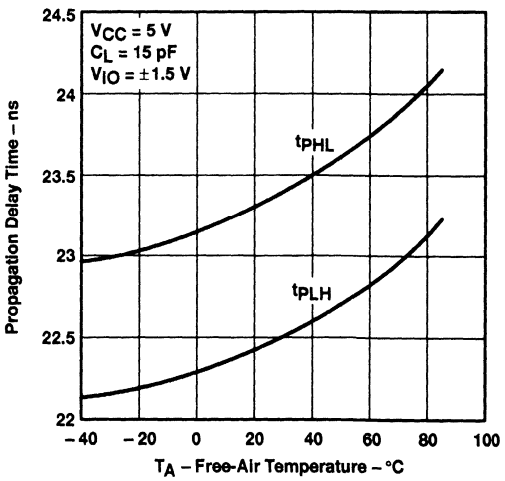


Figure 9

- **Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendation V.11.**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **3-State Outputs**
- **Common-Mode Output Voltage Range of –7 V to 12 V**
- **Active-High Enable**
- **Thermal Shutdown Protection**
- **Positive- and Negative-Current Limiting**
- **Operates From Single 5-V Supply**
- **Low Power Requirements**
- **Functionally Interchangeable With MC3487**

description

The SN75174 is a monolithic quadruple differential line driver with 3-state outputs. It is designed to meet the requirements of ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendation V.11. The device is optimized for balanced multipoint bus transmission at rates up to 4 megabaud. Each driver features wide positive and negative common-mode output voltage ranges making it suitable for party-line applications in noisy environments.

The SN75174 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C. This device offers optimum performance when used with the SN75173 or SN75175 quadruple differential line receivers.

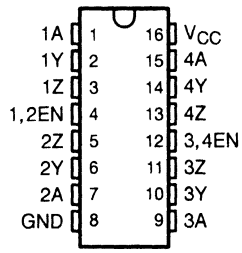
The SN75174 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each driver)

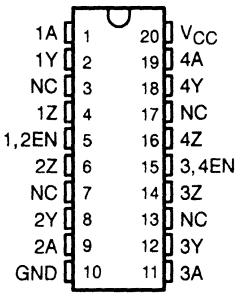
INPUT	ENABLE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = TTL high level, X = irrelevant,
L = TTL low level,
Z = high impedance (off)

N PACKAGE
(TOP VIEW)

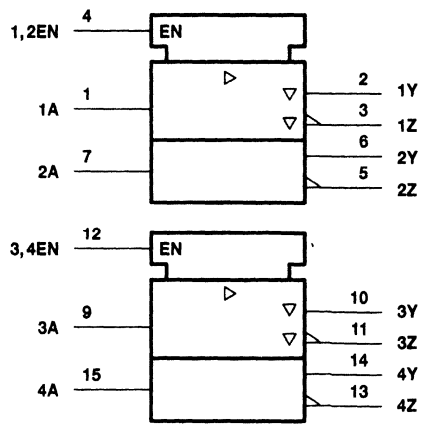


DW PACKAGE
(TOP VIEW)



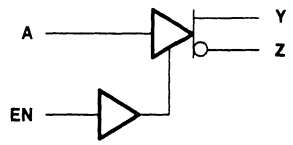
NC – No internal connection

logic symbol†

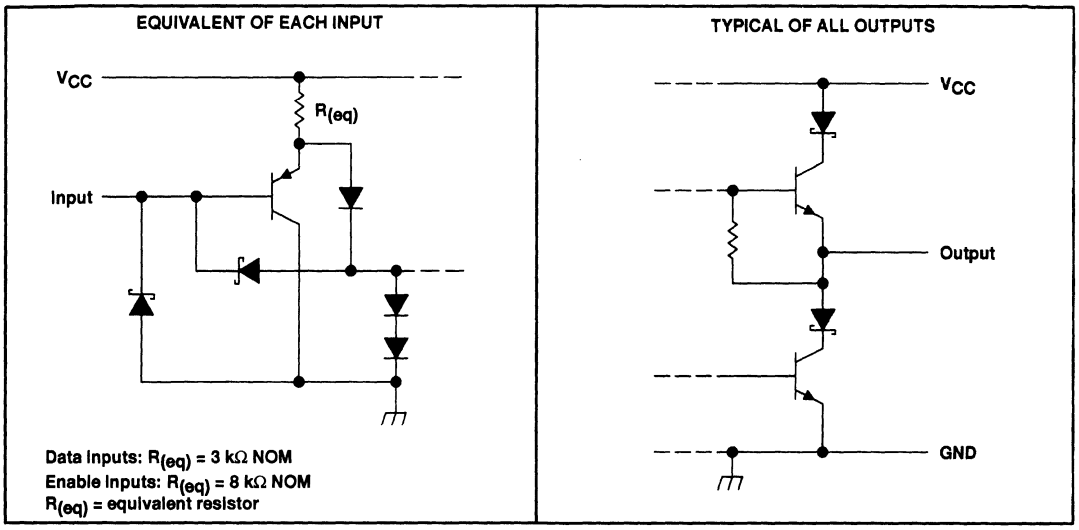


† This symbol is in accordance with ANSI/IEEE Std 91-984 and IEC Publication 617-12.

logic diagram, each driver (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Output voltage range, V_O ..... −10 V to 15 V
Input voltage, V_I ..... 5.5 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended, operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Common-mode output voltage, V_{OC}			−7 to 12	V
High-level output current, I_{OH}			−60	mA
Low-level output current, I_{OL}			60	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −33 mA			3.7		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 33 mA			1.1		V
V_O	Output voltage	I_O = 0		0		6	V
$\lvert V_{OD1}\rvert$	Differential output voltage	I_O = 0		1.5	6	6	V
$\lvert V_{OD2}\rvert$	Differential output voltage	R_L = 100 Ω, See Figure 1		1/2 V_{OD1} or 2‡			V
		R_L = 54 Ω, See Figure 1		1.5	2.5	5	V
V_{OD3}	Differential output voltage	See Note 2		1.5		5	V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage§	R_L = 54 Ω or 100 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage¶					+3 −1	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current with power off	V_{CC} = 0, V_O = −7 V to 12 V				±100	μA
I_{OZ}	High-impedance-state output current	V_O = −7 V to 12 V				±100	μA
I_{IH}	High-level input current	V_I = 2.7 V				20	μA
I_{IL}	Low-level input current	V_I = 0.5 V				−360	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−180	mA
		V_O = V_{CC}				180	
		V_O = 12 V				500	
I_{CC}	Supply current (all drivers)	No load	Outputs enabled		38	60	mA
			Outputs disabled		18	40	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
§ $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
¶ In ANSI Standard EIA/TIA-422-B, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
NOTE 2: See EIA Standard RS-485.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	R_L = 54 Ω,	See Figure 2		45	65	ns
$t_{t(OD)}$	Differential-output transition time				80	120	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 3		80	120	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 4		55	80	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 3		75	115	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 3		18	30	ns

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	EIA/TIA-422-B	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\|V_{OD3}\|$		V_t (Test Termination) Measurement 2)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V}_{os}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|,\|I_{sb}\|$	
I_O	$\|I_{xa}\|,\|I_{xb}\|$	I_{ia},I_{ib}

PARAMETER MEASUREMENT INFORMATION

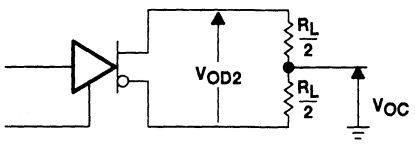
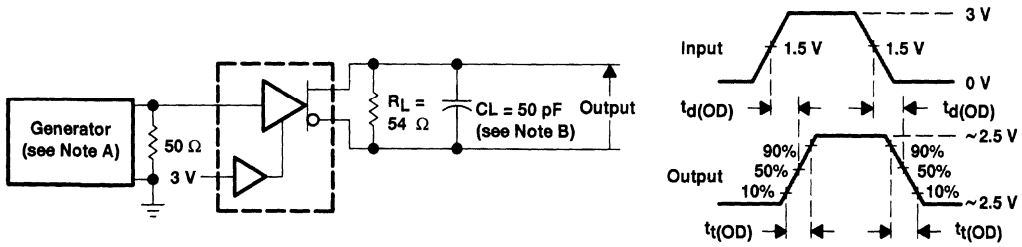


Figure 1. Differential and Common-Mode Output Voltages



NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \le 5$ ns, $t_f \le 5$ ns, PRR ≤ 1 MHz, duty cycle = 50%, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.

Figure 2. Differential-Output Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

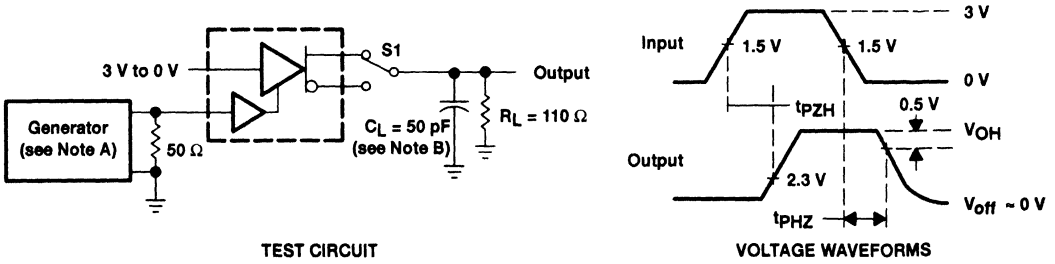


Figure 3. Test Circuit and Voltage Waveforms

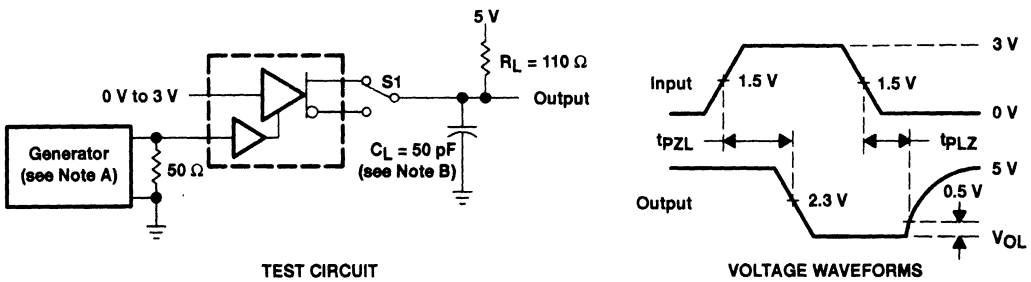


Figure 4. Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, $t_r \leq 5$ ns, $t_f \leq 5$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and stray capacitance.

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

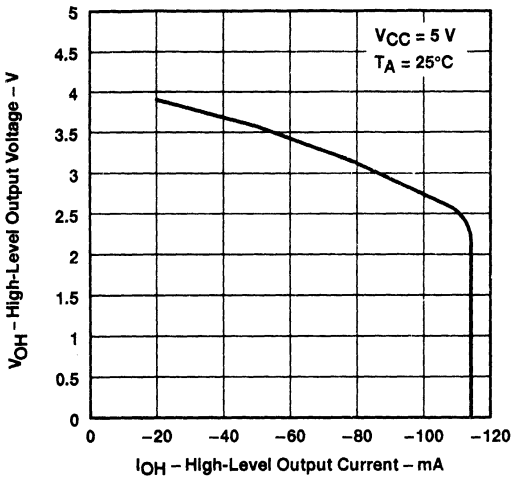


Figure 5

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

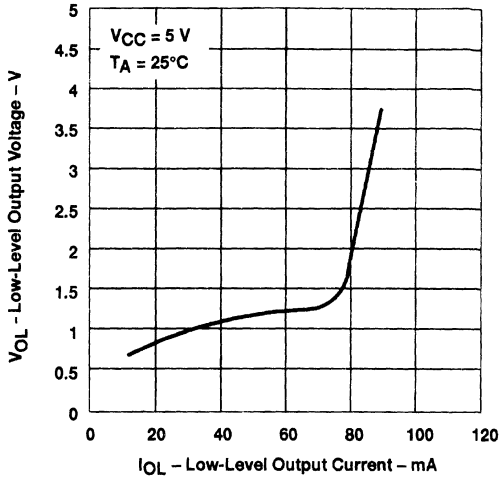


Figure 6

DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

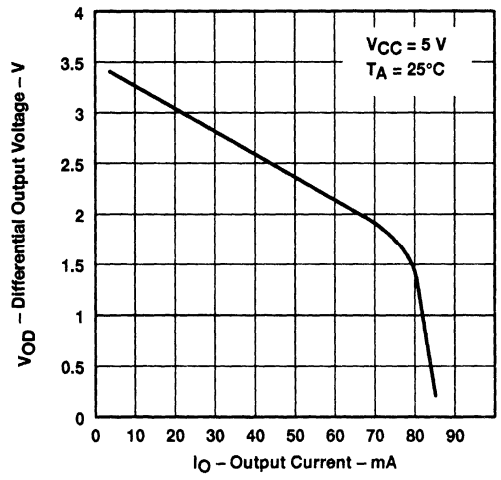


Figure 7

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

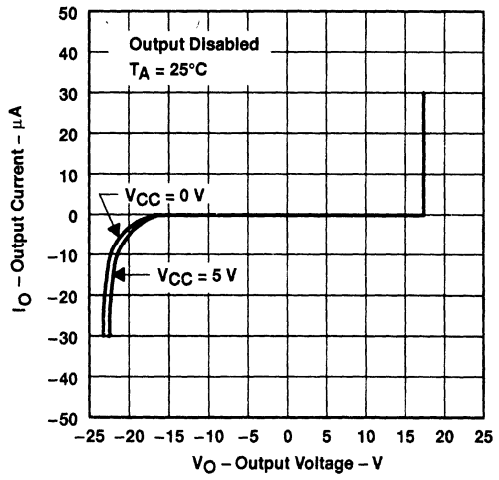


Figure 8

TYPICAL CHARACTERISTICS

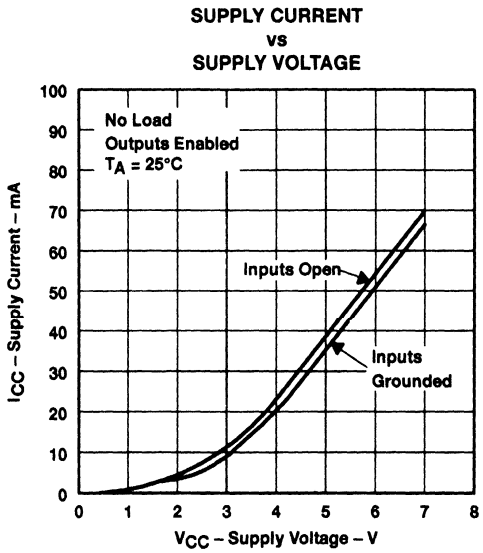


Figure 9

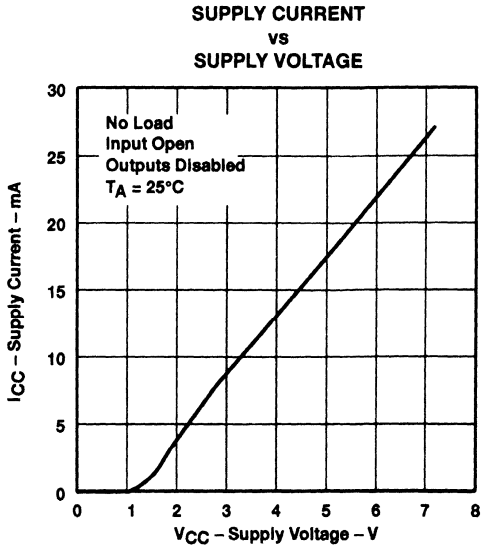
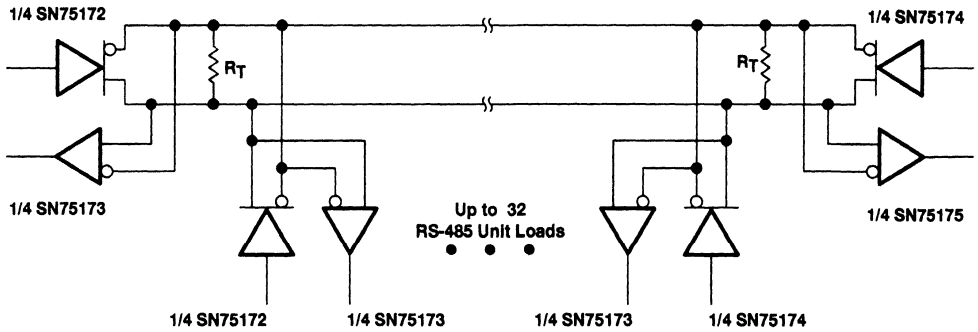


Figure 10

APPLICATION INFORMATION



NOTE: The line length should be terminated at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

Figure 11. Typical Application Circuit

SLLS122D – JULY 1991 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of ANSI EIA/TIA-422-B and RS-485**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Designed for up to 20-Mbps Operation in Both Serial and Parallel Applications**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Low Supply Current Requirements 55 mA Max**
- **Wide Positive and Negative Input/Output Bus Voltage Ranges**
- **Driver Output Capacity . . . ±60 mA**
- **Thermal-Shutdown Protection**
- **Driver Positive- and Negative-Current Limiting**
- **Functionally Interchangeable With SN75174**

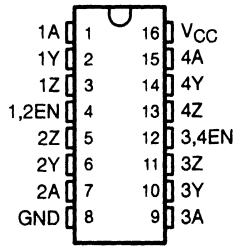
description

The SN65ALS174A and SN75ALS174A are quadruple line drivers with 3-state differential outputs. They are designed to meet the requirements of ANSI Standards EIA/TIA-422-B and RS-485. These devices are optimized for balanced multipoint bus transmission at rates of up to 20 Mbps. Each driver features wide positive and negative common-mode output voltage ranges that make them suitable for party-line applications in noisy environments.

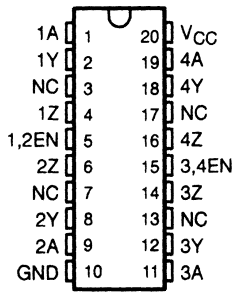
The SN65ALS174A and SN75ALS174A provide positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C.

The SN65ALS174A is characterized for operation from −40°C to 85°C and the SN75ALS174A is characterized for operation from 0°C to 70°C.

SN75ALS174A . . . N PACKAGE
(TOP VIEW)



SN65ALS174A, SN75ALS174A . . . DW PACKAGE
(TOP VIEW)



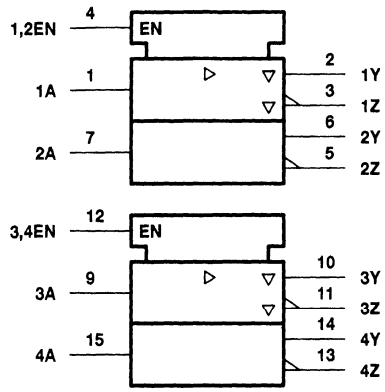
NC – No internal connection

FUNCTION TABLE
(each driver)

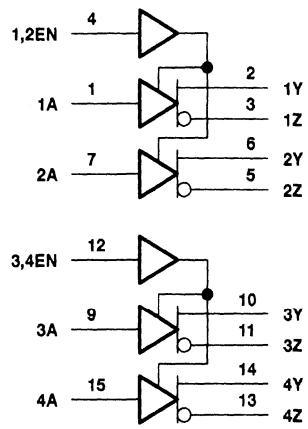
INPUT A	ENABLES	OUTPUTS Y	OUTPUTS Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = high level, L = low level, X = irrelevant,
Z = high impedance (off)

logic symbol†

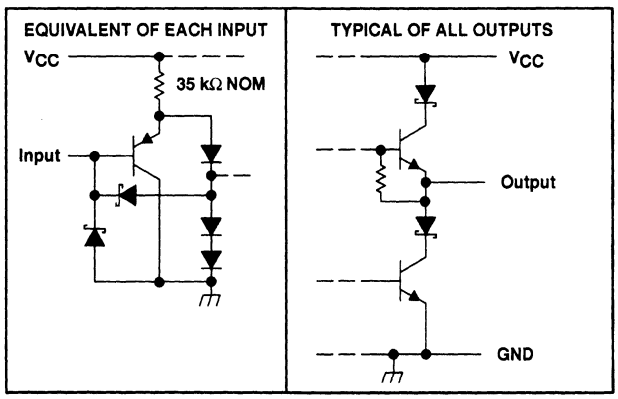


logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

schematics of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 7 V
Output voltage range, V_O ..... −9 V to 14 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65ALS174A ..... −40°C to 85°C
SN75ALS174A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW	585 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Common-mode output voltage, V_{OC}				12 −7	V
High-level output current, I_{OH}				−60	mA
Low-level output current, I_{OL}				60	mA
Operating free-air temperature, T_A	SN65ALS174A	−40		85	°C
	SN75ALS174A	0		70	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA				–1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω	See Figure 1	1/2 V_{OD1} or 2‡			V
		R_L = 54 Ω		1.5	2.5	5	
$\|V_{OD3}\|$	Differential output voltage	See Note 2		1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage§	R_L = 54 Ω or 100 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage¶					3 –1	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current with power off	V_{CC} = 0,	V_O = –7 V to 12 V			±100	µA
I_{OZ}	High-impedance-state output current	V_O = –7 V to 12 V				±100	µA
I_{IH}	High-level input current	V_I = 2.7 V				20	µA
I_{IL}	Low-level input current	V_I = 0.4 V				–100	µA
I_{OS}	Short-circuit output current	V_O = –7 V to 12 V				±250	mA
I_{CC}	Supply current (all drivers)	No load	Outputs enabled		36	55	mA
			Outputs disabled		16	30	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
§ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
¶ In ANSI Standard EIA/TIA-422-B, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
NOTE 2: See EIA Standard RS-485, Figure 3-5, Test Termination Measurement 2.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω,	See Figure 2	9	15	22	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 3	30	45	70	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 4	25	40	65	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 3	10	20	35	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 4	10	30	45	ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

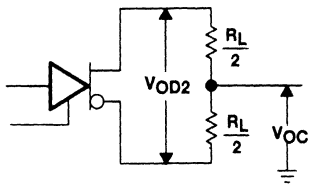
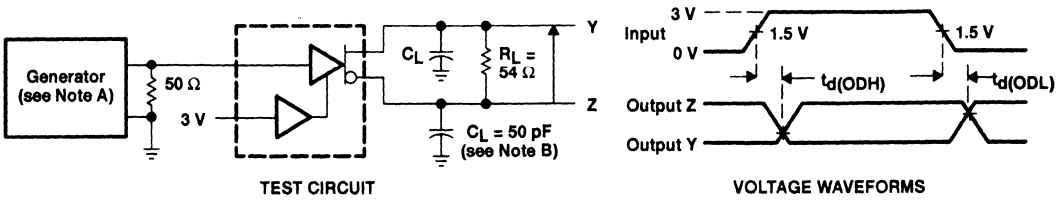
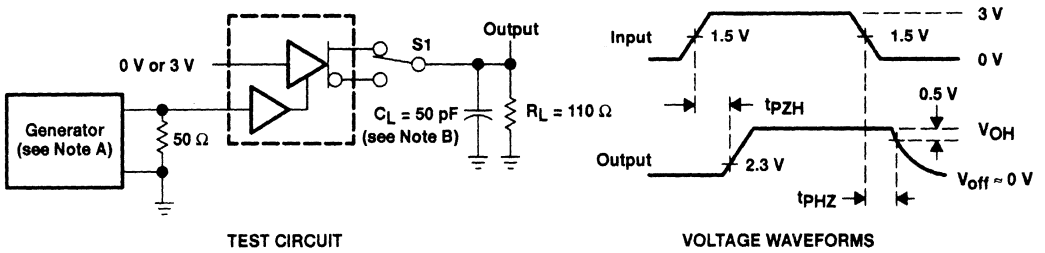


Figure 1. Differential and Common-Mode Output Voltages



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, duty cycle = 50%, $t_f \leq 5$ ns, $t_r \leq 5$ ns.
B. C_L includes probe and stray capacitance.

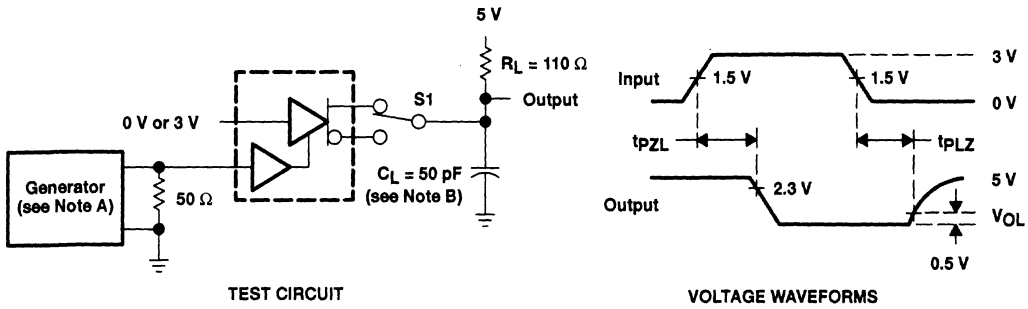
Figure 2. Differential-Output Test Circuit and Delay and Transition Times Voltage Waveforms



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, duty cycle = 50%, $t_f \leq 5$ ns, $t_r \leq 5$ ns.
B. C_L includes probe and stray capacitance.

Figure 3. Test Circuit and Voltage Waveforms, t_{PZH} and t_{PHZ}

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, duty cycle = 50%, $t_f \leq 5$ ns, $t_r \leq 5$ ns.
B. C_L includes probe and stray capacitance.

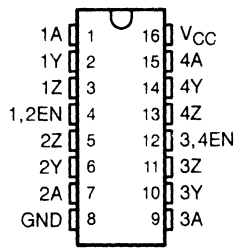
Figure 4. Test Circuit and Voltage Waveforms, t_{PZL} and t_{PLZ}

SN55LBC174
QUADRUPLE LOW-POWER DIFFERENTIAL LINE DRIVER

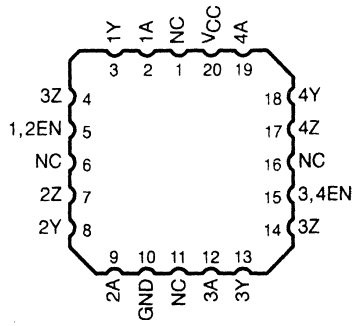
SGLS082 – MARCH 1995

- **Meets EIA Standard RS-485**
- **Designed for High-Speed Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Supports Data Rates up to and Exceeding Ten Million Transfers Per Second**
- **Common-Mode Output Voltage Range of –7 V to 12 V**
- **Positive- and Negative-Current Limiting**
- **Low Power Consumption . . . 1.5 mA Max (Output Disabled)**

J OR W PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN55LBC174 is composed of monolithic quadruple differential line drivers with 3-state outputs. This device is designed to meet the requirements of the Electronics Industry Association (EIA) Standard RS-485 and is optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. Each driver features wide positive and negative common-mode output voltage ranges, current limiting, and thermal-shutdown protection making it suitable for party-line applications in noisy environments. This device is designed using LinBiCMOS™, facilitating ultra-low power consumption and inherent robustness.

The SN55LBC174 provides positive and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. This device offers optimum performance when used with the SN55LBC173 quadruple line receiver. The SN55LBC174 is available in the 16-pin CDIP package (J), the 16-pin CPAK (W), or the 20-pin LCCC package (FK).

The SN55LBC174 is characterized for operation over the military temperature range of –55°C to 125°C.

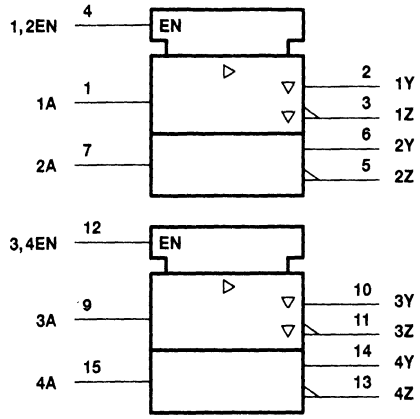
FUNCTION TABLE
(each driver)

INPUT	ENABLE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = high level, L = low level,
X = irrelevant, Z = high impedance (off)

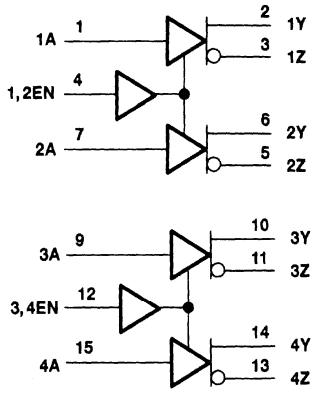
LinBiCMOS is a trademark of Texas Instruments Incorporated.

logic symbol†

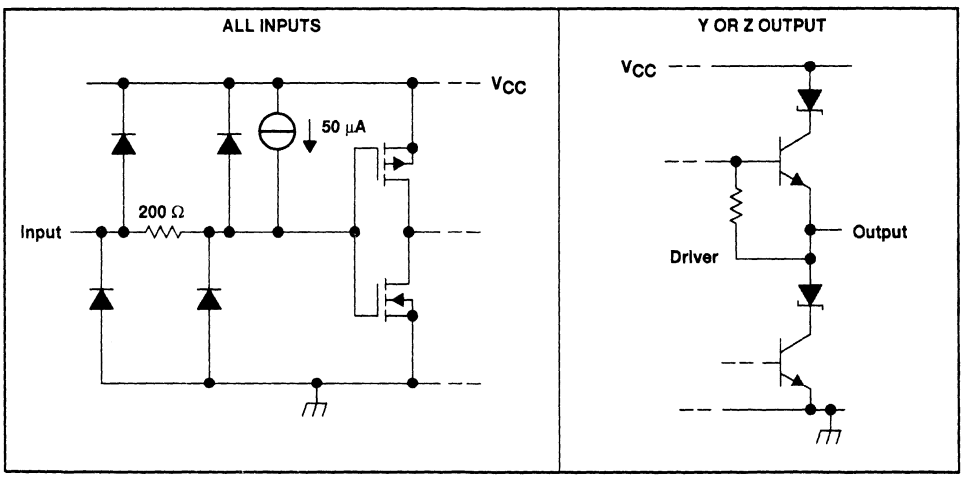


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the J or W package.

logic diagram (positive logic)



schematic of inputs and outputs



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.3 V to 7 V
Output voltage range, V_O ..... −10 V to 15 V
Input voltage range, V_I ..... −0.3 V to 7 V
Continuous power dissipation ..... internally limited‡
Operating free-air temperature range, T_A ..... −55°C to 125°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.

NOTE 1: All voltage values are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 125°C$ POWER RATING
FK	1375 mW	11.0 mW/°C	275 mW
J	1375 mW	11.0 mW/°C	275 mW
W	1000 mW	8.0 mW/°C	200 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Voltage at any bus terminal (separately or common mode), V_O	Y or Z			12	V
				−7	
High-level output current, I_{OH}	Y or Z			−60	mA
Low-level output current, I_{OL}	Y or Z			60	mA
Operating free-air temperature, T_A		−55		125	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
$\lvert V_{OD}\rvert$	Differential output voltage‡	R_L = 54 Ω, See Figure 1		1.1	1.8	5	V
		R_L = 60 Ω, See Figure 2		1.1	1.7	5	
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage§	R_L = 54 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage					3 −1	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current with power off	V_{CC} = 0, V_O = −7 V to 12 V				±100	µA
I_{OZ}	High-impedance-state output current	V_O = −7 V to 12 V				±100	µA
I_{IH}	High-level input current	V_I = 2.4 V				−100	µA
I_{IL}	Low-level input current	V_I = 0.4 V				−100	µA
I_{OS}	Short-circuit output current	V_O = −7 V to 12 V				±250	mA
I_{CC}	Supply current (all drivers)	No load	Outputs enabled			7	mA
			Outputs disabled			1.5	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The minimum V_{OD} specification does not fully comply with EIA Standard RS-485 at operating temperatures below 0°C. The lower output signal should be used to determine the maximum signal transmission distance.
§ $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

switching characteristics, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω, See Figure 3	25°C	2	11	20	ns
			−55°C to 125°C	2		40	
$t_{t(OD)}$	Differential output transition time	R_L = 54 Ω, See Figure 3	25°C	4	15	25	ns
			−55°C to 125°C	4		40	
t_{PZH}	Output enable time to high level	R_L = 110 Ω, See Figure 4	25°C			30	ns
			−55°C to 125°C			40	
t_{PZL}	Output enable time to low level	R_L = 110 Ω, See Figure 5	25°C			30	ns
			−55°C to 125°C			40	
t_{PHZ}	Output disable time from high level	R_L = 110 Ω, See Figure 4	25°C			50	ns
			−55°C to 125°C			90	
t_{PLZ}	Output disable time from low level	R_L = 110 Ω, See Figure 5	25°C			30	ns
			−55°C to 125°C			45	

PARAMETER MEASUREMENT INFORMATION

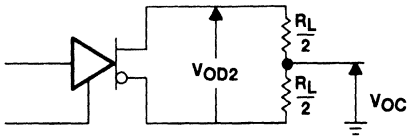


Figure 1. Differential and Common-Mode Output Voltages

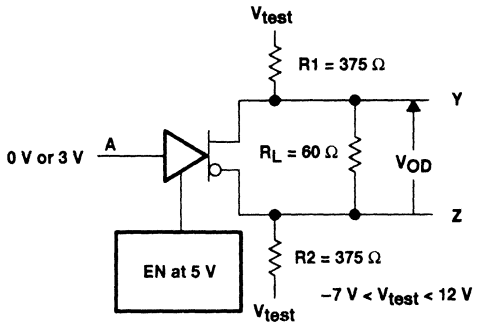
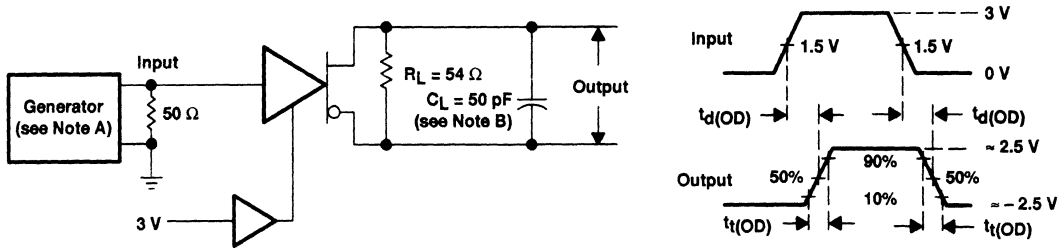


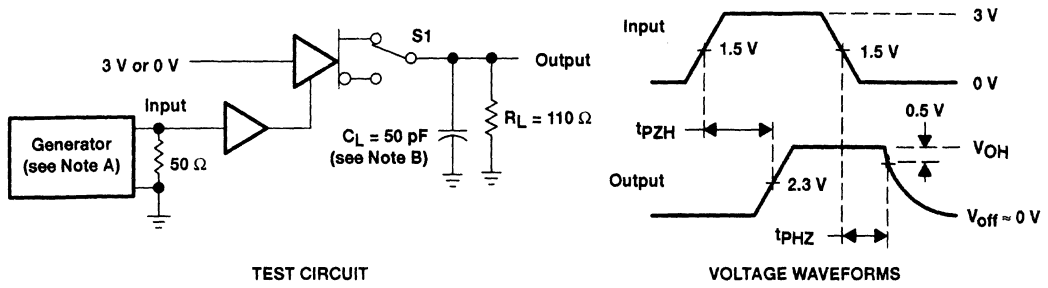
Figure 2. Driver V_{OD} Test Circuit



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 5 ns, t_f ≤ 5 ns, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.

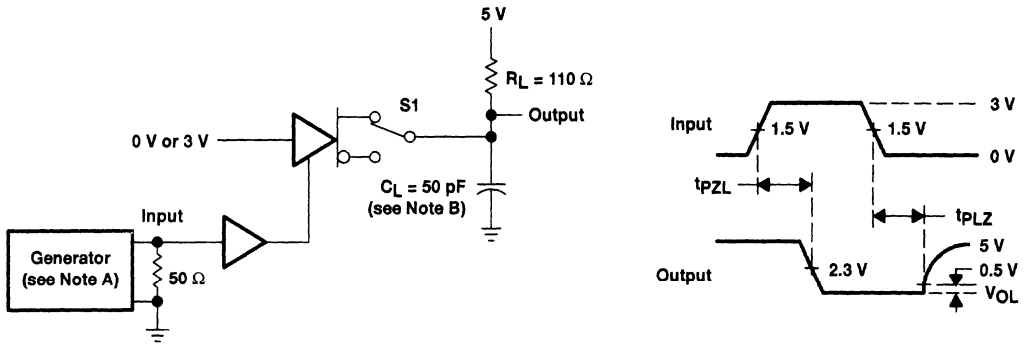
Figure 3. Driver Differential-Output Test Circuit Delay and Transition-Time Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

Figure 4. t_{PZH} and t_{PHZ} Test Circuit and Waveforms



TEST CIRCUIT VOLTAGE WAVEFORMS

Figure 5. t_{PZL} and t_{PLZ} Test Circuit and Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r ≤ 5 ns, t_f ≤ 5 ns, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.

TYPICAL CHARACTERISTICS

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

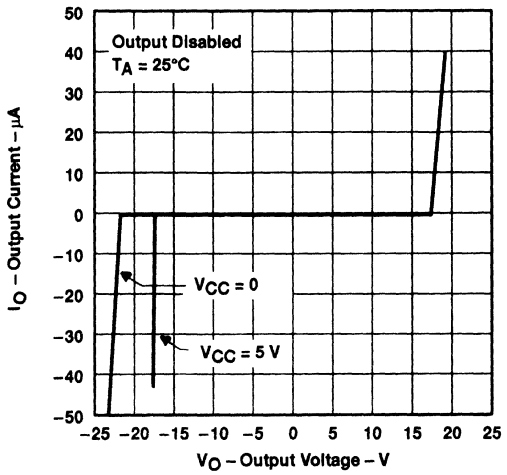


Figure 6

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

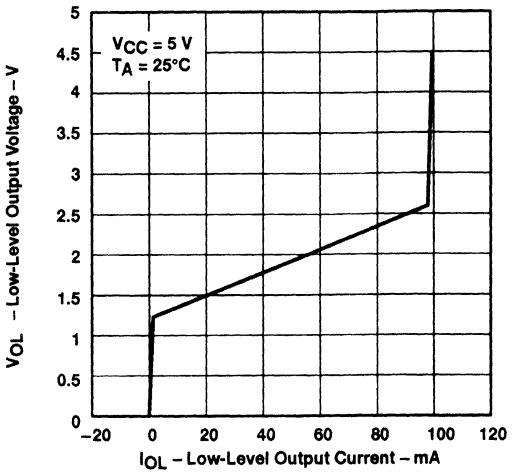


Figure 7

DIFFERENTIAL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

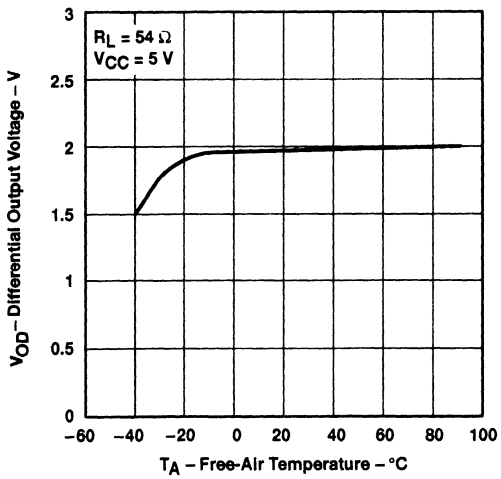


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

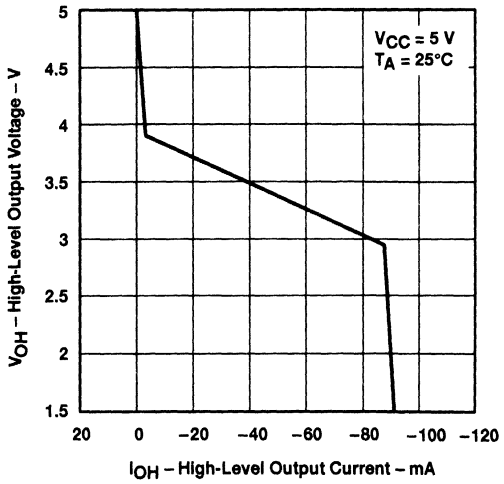


Figure 9

TYPICAL CHARACTERISTICS

DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

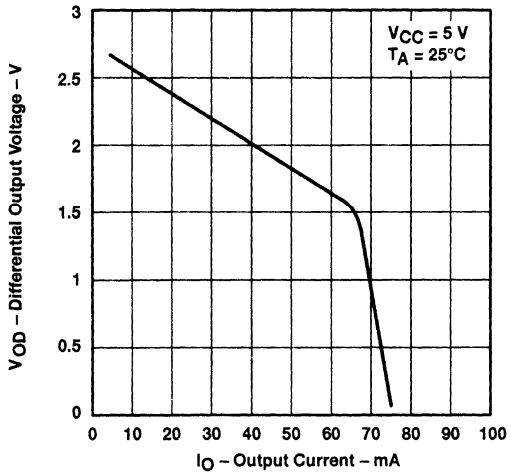


Figure 10

PROPAGATION DELAY TIME,
DIFFERENTIAL OUTPUT
vs
FREE-AIR TEMPERATURE

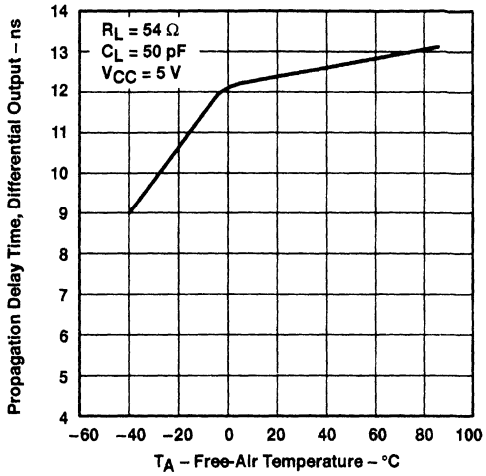


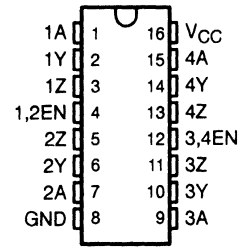
Figure 11

SN65LBC174, SN75LBC174
QUADRUPLE LOW-POWER DIFFERENTIAL LINE DRIVERS

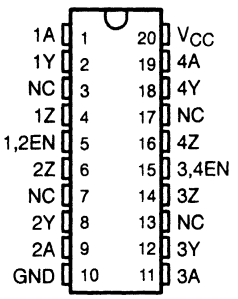
SLLS162 – JULY 1993

- **Meets or Exceeds the Standard EIA-485**
- **Designed for High-Speed Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Supports Data Rates up to and Exceeding Ten Million Transfers Per Second**
- **Common-Mode Output Voltage Range of –7 V to 12 V**
- **Positive- and Negative-Current Limiting**
- **Low Power Consumption . . . 1.5 mA Max (Output Disabled)**
- **Functionally Interchangeable With SN75174**

N PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN65LBC174 and SN75LBC174 are monolithic, quadruple, differential line drivers with 3-state outputs. Both devices are designed to meet the requirements of the Electronics Industry Association Standard EIA-485. These devices are optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. Each driver features wide positive and negative common-mode output voltage ranges, current limiting, and thermal-shutdown protection, making it suitable for party-line applications in noisy environments. Both devices are designed using LinBiCMOS™, facilitating ultra-low power consumption and inherent robustness.

Both the SN65LBC174 and SN75LBC174 provide positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. These devices offer optimum performance when used with the SN75LBC173 or SN75LBC175 quadruple line receivers. The SN65LBC174 and SN75LBC174 are available in the 16-terminal DIP package (N) and the 20-terminal wide-body small outline intergrated circuit (SOIC) package (DW).

FUNCTION TABLE
(each driver)

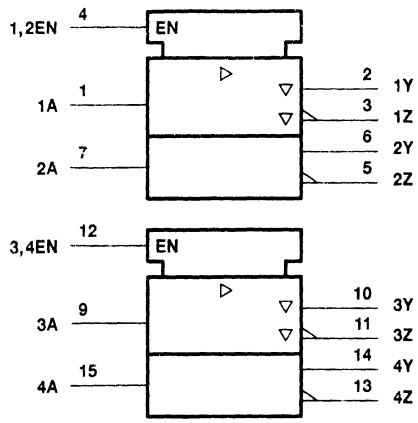
INPUT	ENABLE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = high level, L = low level,
X = irrelevant, Z = high impedance (off)

The SN75LBC174 is characterized for operation over the commercial temperature range of 0°C to 70°C. The SN65LBC174 is characterized over the industrial temperature range of –40°C to 85°C.

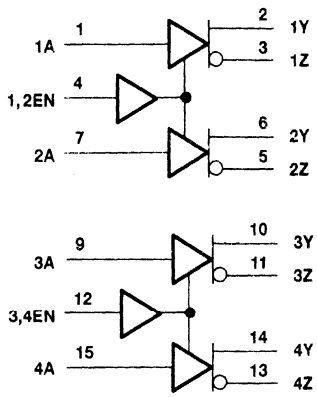
LinBiCMOS is a trademark of Texas Instruments Incorporated.

logic symbol†

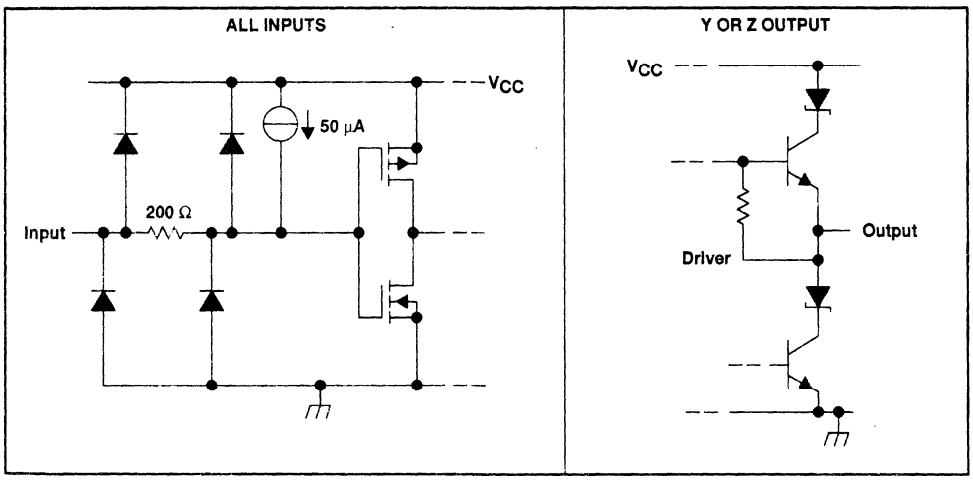


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Terminal numbers shown are for the N package.

logic diagram (positive logic)



schematic of inputs and outputs



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.3 V to 7 V
Output voltage range, V_O ..... −10 V to 15 V
Input voltage range, V_I ..... −0.3 V to 7 V
Continuous total power dissipation ..... internally limited‡
Operating free-air temperature range, T_A: SN65LBC174 ..... −40°C to 85°C
SN75LBC174 ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Voltage at any bus terminal (separately or common-mode), V_O	Y or Z			12	V
				−7	
High-level output current, I_{OH}	Y or Z			−60	mA
Low-level output current, I_{OL}	Y or Z			60	mA
Continuous total power dissipation		See Dissipation Rating Table			
Operating free-air temperature, T_A	SN65LBC174	−40		85	°C
	SN75LBC174	0		70	

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW	585 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
$\lvert V_{OD}\rvert$	Differential output voltage‡	R_L = 54 Ω, See Figure 1	SN65LBC174	1.1	1.8	5	V
			SN75LBC174	1.5	1.8	5	
		R_L = 60 Ω, See Figure 2	SN65LBC174	1.1	1.7	5	
			SN75LBC174	1.5	1.7	5	
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of common-mode output voltage§	R_L = 54 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage					3 −1	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current with power off	V_{CC} = 0,	V_O = −7 V to 12 V			±100	µA
I_{OZ}	High-impedance-state output current	V_O = −7 V to 12 V				±100	µA
I_{IH}	High-level input current	V_I = 2.4 V				−100	µA
I_{IL}	Low-level input current	V_I = 0.4 V				−100	µA
I_{OS}	Short-circuit output current	V_O = −7 V to 12 V				±250	mA
I_{CC}	Supply current (all drivers)	No load	Outputs enabled			7	mA
			Outputs disabled			1.5	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The minimum V_{OD} specification does not fully comply with EIA-485 at operating temperatures below 0°C. The lower output signal should be used to determine the maximum signal transmission distance.
§ $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω,	See Figure 3	2	11	20	ns
$t_{t(OD)}$	Differential output transition time			10	15	25	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 3			30	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 5			30	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 4			50	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 5			30	ns

PARAMETER MEASUREMENT INFORMATION

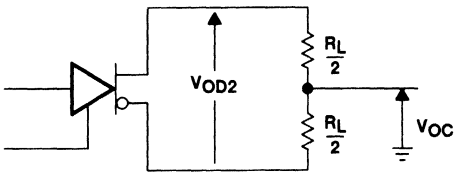


Figure 1. Differential and Common-Mode Output Voltages

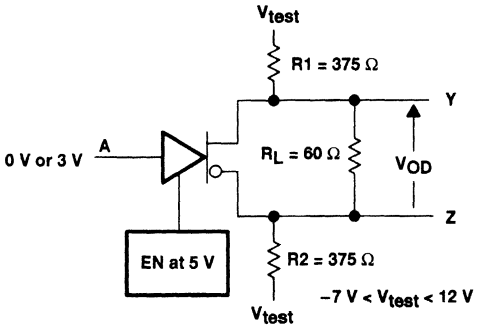
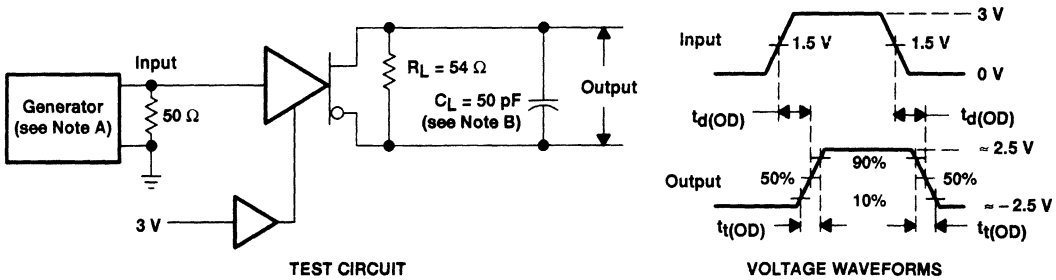


Figure 2. Driver V_{OD} Test Circuit



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, $t_r \leq 5$ ns, $t_f \leq 5$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and stray capacitance.

Figure 3. Time Waveforms for Driver Differential Output Test Circuit Delay and Transition

PARAMETER MEASUREMENT INFORMATION

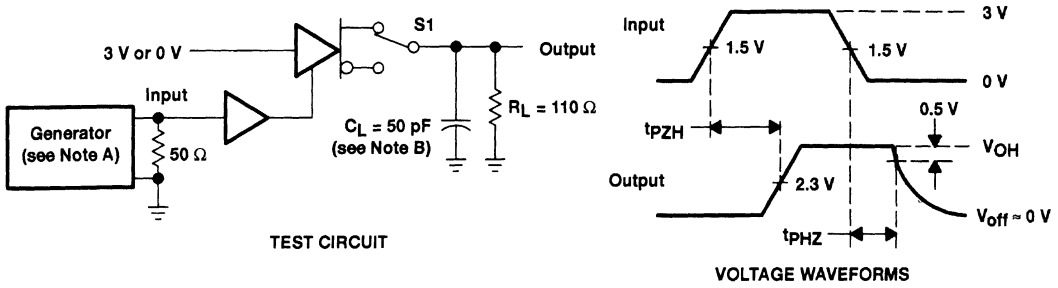


Figure 4. t_{PZH} and t_{PHZ} Test Circuit and Waveforms

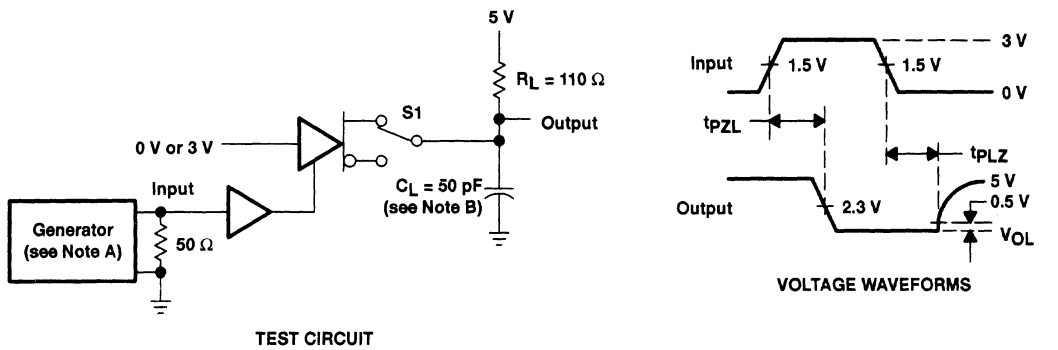


Figure 5. t_{PZL} and t_{PLZ} Test Circuit and Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 5 ns, t_f ≤ 5 ns, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.

TYPICAL CHARACTERISTICS

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

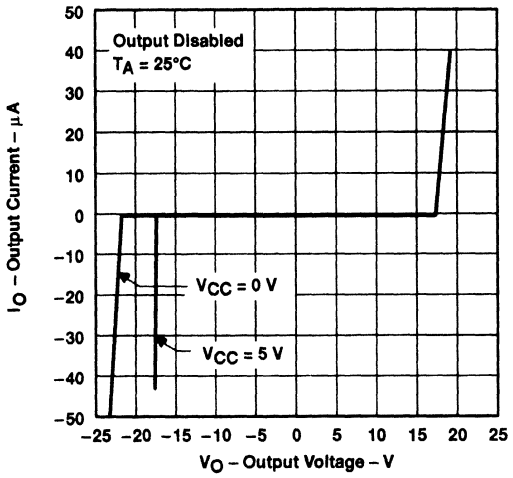


Figure 6

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

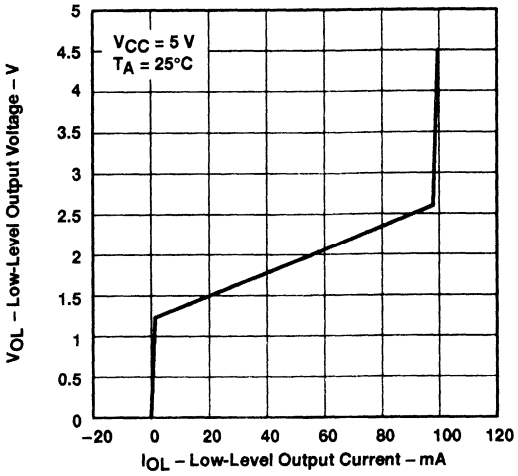


Figure 7

DIFFERENTIAL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

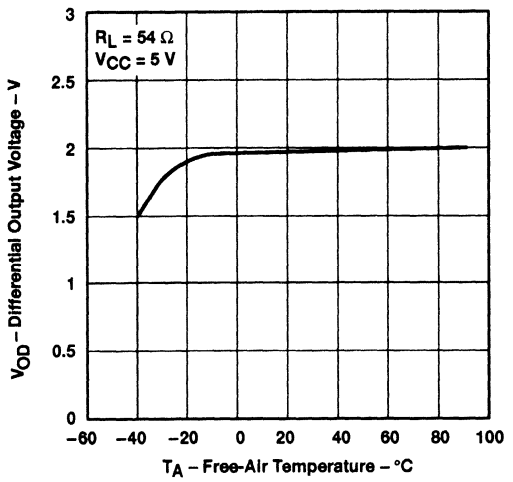


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

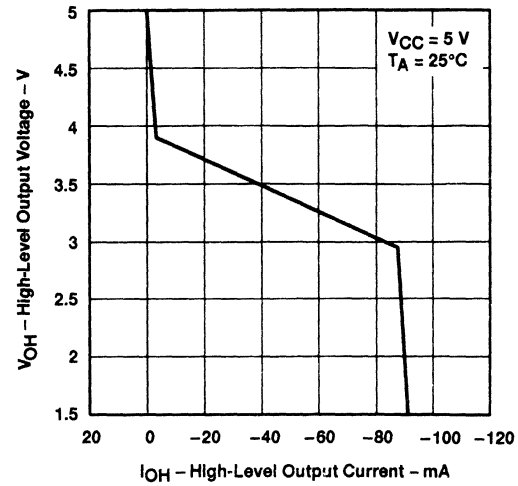


Figure 9

TYPICAL CHARACTERISTICS

DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

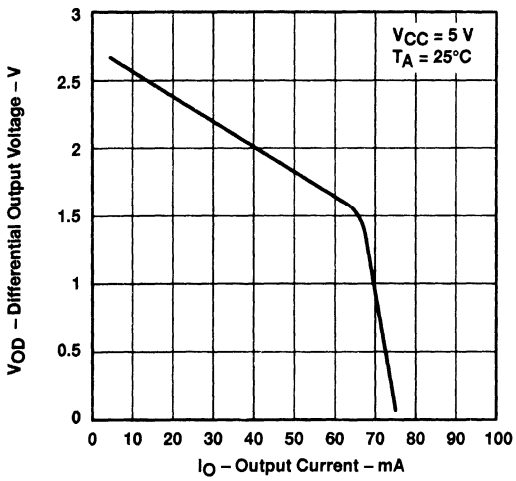


Figure 10

PROPAGATION DELAY TIME,
DIFFERENTIAL OUTPUT
vs
FREE-AIR TEMPERATURE

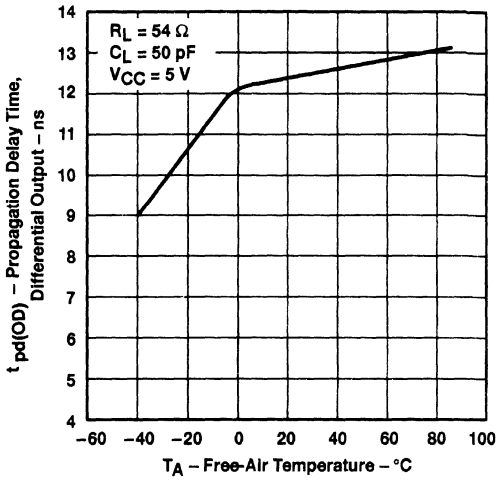


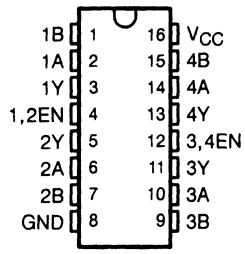
Figure 11

SN65175, SN75175
QUADRUPLE DIFFERENTIAL LINE RECEIVER

SLLS145B – OCTOBER 1990 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of ANSI Standard EIA/TIA-422-B, RS-423-B, and RS-485**
- **Meets ITU Recommendations V.10, V.11, X.26, and X.27**
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments**
- **3-State Outputs**
- **Common-Mode Input Voltage Range −12 V to 12 V**
- **Input Sensitivity . . . ±200 mV**
- **Input Hysteresis . . . 50 mV Typ**
- **High Input Impedance . . . 12 kΩ Min**
- **Operates From Single 5-V Supply**
- **Low-Power Requirements**
- **Plug-In Replacement for MC3486**

D OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A – B	ENABLE	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	H
-0.2 V $< V_{ID} < 0.2$ V	H	?
$V_{ID} \leq -0.2$ V	H	L
X	L	Z
Open circuit	H	?

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

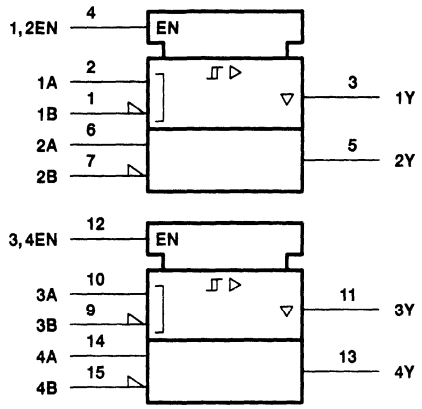
description

The SN65175 and SN75175 are monolithic quadruple differential line receivers with 3-state outputs. They are designed to meet the requirements of ANSI Standards EIA/TIA-422-B, RS-423-B, RS-485, and several ITU recommendations. These standards are for balanced multipoint bus transmission at rates up to 10 megabits per second. Each of the two pairs of receivers has a common active-high enable.

The receivers feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of ±12 V. The SN65175 and SN75175 are designed for optimum performance when used with the SN75172 or SN75174 quadruple differential line drivers.

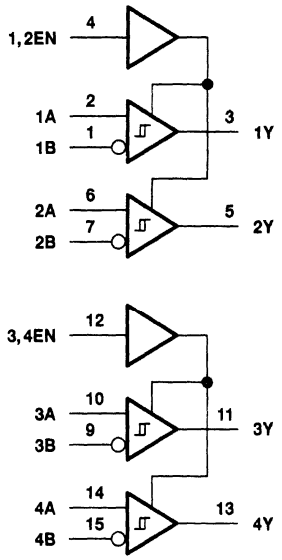
The SN65175 is characterized for operation from −40°C to 85°C. The SN75175 is characterized for operation from 0°C to 70°C.

logic symbol†

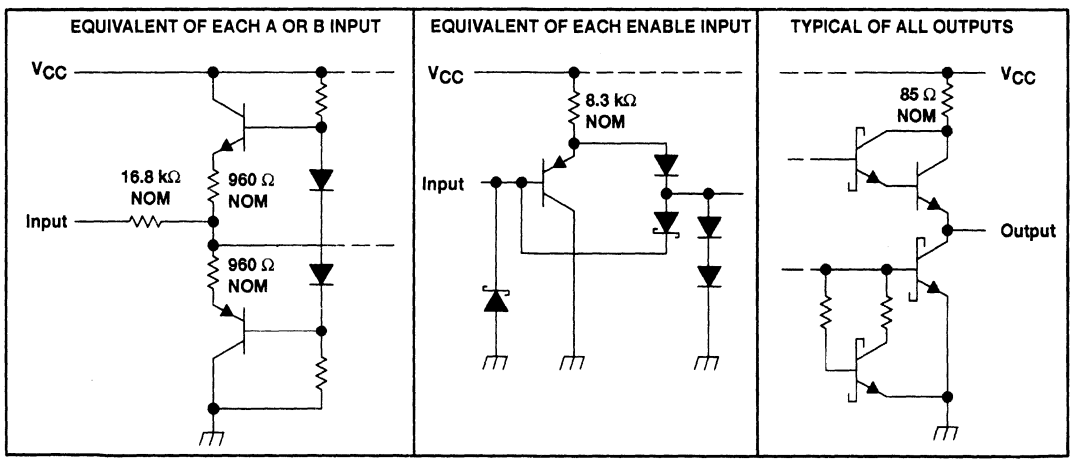


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage V_I, (A or B inputs) ..... ±25 V
Differential input voltage, V_{ID} (see Note 2) ..... ±25 V
Enable input voltage, V_I, EN ..... 7 V
Low-level output current, I_{OL} ..... 50 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65175 ..... −40°C to 85°C
SN75175 ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Common-mode input voltage, V_{IC}				+12	V
Differential input voltage, V_{ID}				±12	V
High-level enable-input voltage, V_{IH}		2			V
Low-level enable-input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}				−400	μA
Low-level output current, I_{OL}				16	mA
Operating free-air temperature, T_A	SN65175	−40		85	°C
	SN75175	0		70	

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA				0.2	V
V_{IT-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 16 mA		−0.2‡			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)	See Figure 4				50		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA					−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = −400 µA,	See Figure 1	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV,	See Figure 1	I_{OL} = 8 mA			0.45	V
				I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V					±20	µA
I_I	Line input current	Other input at 0 V,	See Note 3	V_I = 12 V			1	mA
				V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V					20	µA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V					−100	µA
r_i	Input resistance				12			kΩ
I_{OS}	Short-circuit output current§				−15		−85	mA
I_{CC}	Supply current	Outputs disabled					70	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltage levels only.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 3: Refer to ANSI Standards EIA/TIA-422-B, RS-423-B, and RS-485 for exact conditions.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 2		22	35	ns
t_{PHL}	Propagation delay time, high- to low-level output			25	35	ns
t_{PZH}	Output enable time to high level	See Figure 3		13	30	ns
t_{PZL}	Output enable time to low level			19	30	ns
t_{PHZ}	Output disable time from high level	See Figure 3		26	35	ns
t_{PLZ}	Output disable time from low level			25	35	ns

PARAMETER MEASUREMENT INFORMATION

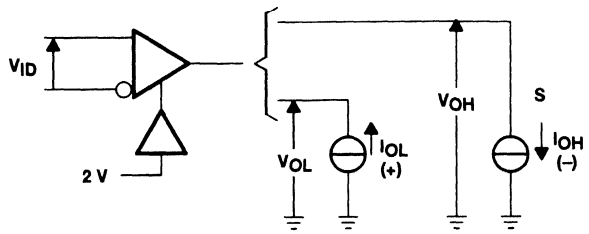


Figure 1. V_{OH}, V_{OL}

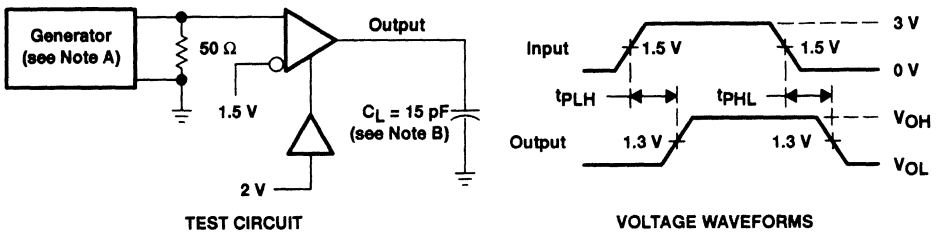


Figure 2. Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.

PARAMETER MEASUREMENT INFORMATION

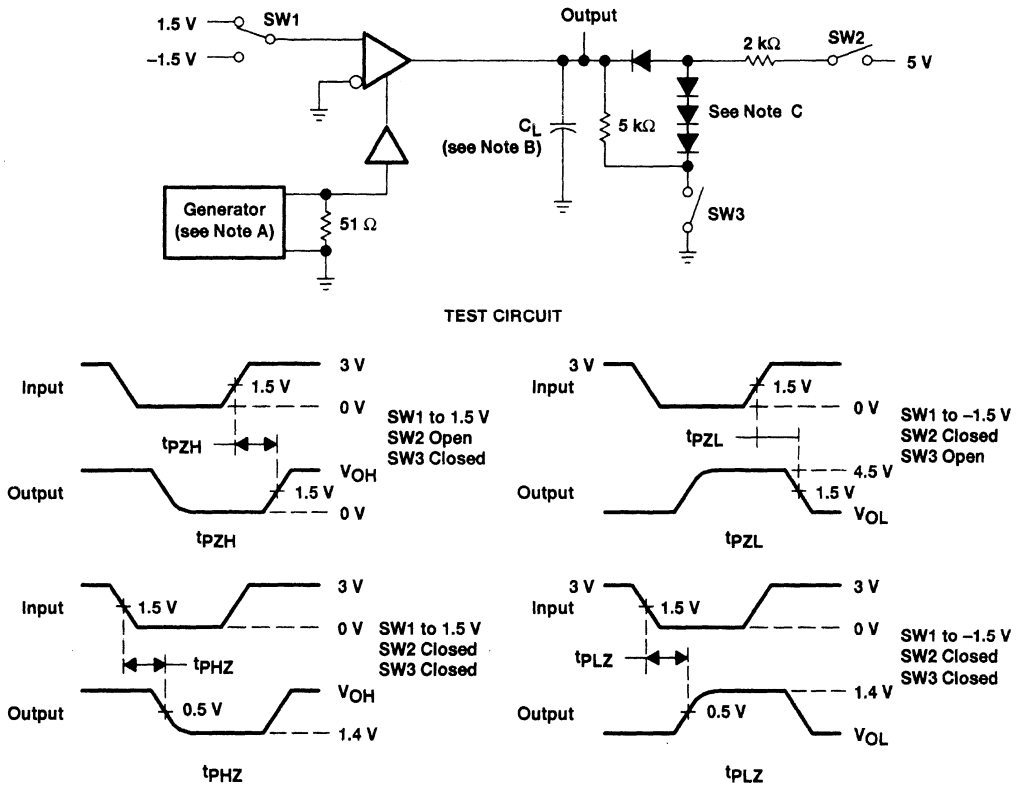


Figure 3. Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, $t_f \leq 6$ ns, $t_r \leq 6$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and stray capacitance.
C. All diodes are 1N916 or equivalent.

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

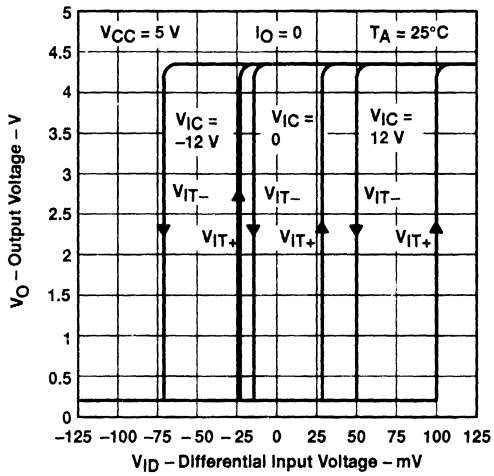


Figure 4

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

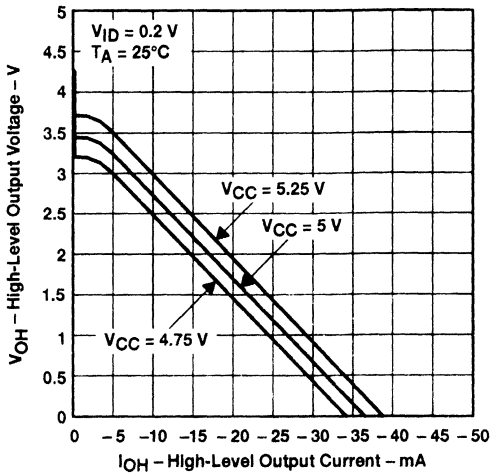


Figure 5

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

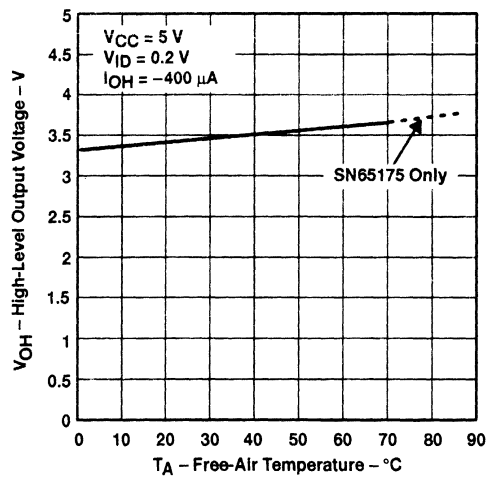


Figure 6

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

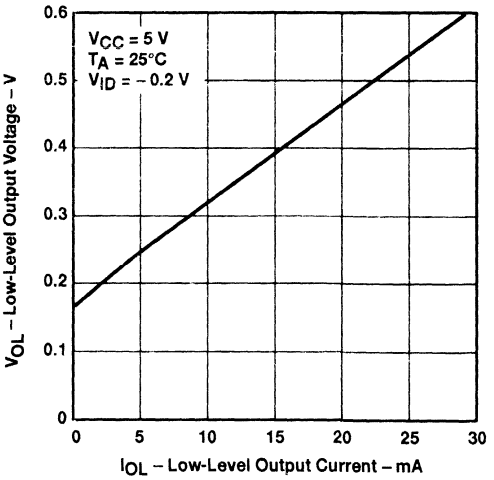


Figure 7

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

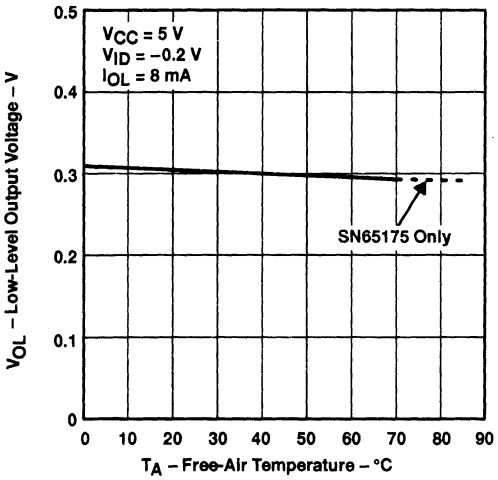


Figure 8

OUTPUT VOLTAGE
vs
ENABLE G VOLTAGE

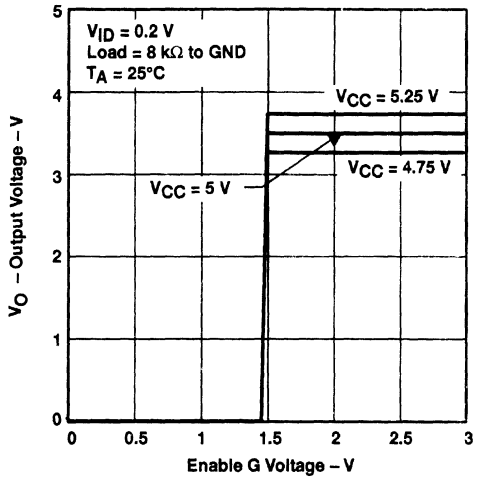


Figure 9

OUTPUT VOLTAGE
vs
ENABLE G VOLTAGE

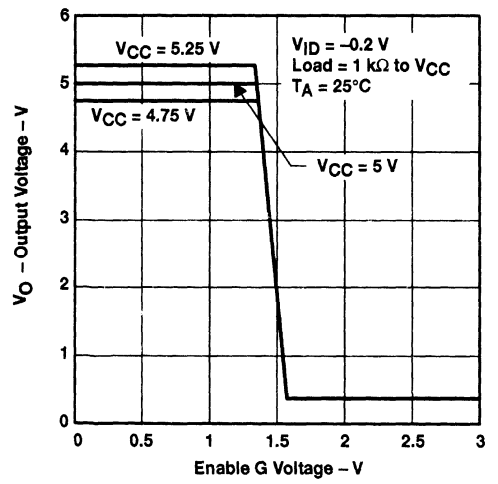


Figure 10

SUPPLY CURRENT (ALL RECEIVERS)
vs
SUPPLY VOLTAGE

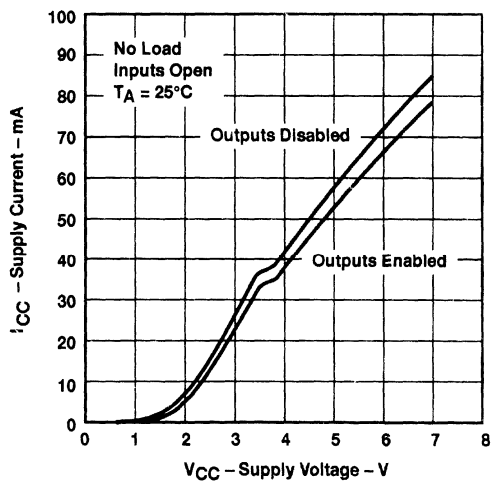


Figure 11

TYPICAL CHARACTERISTICS

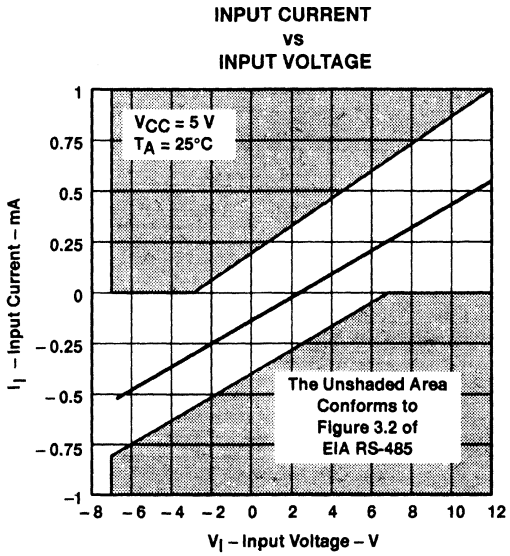


Figure 12

APPLICATION INFORMATION

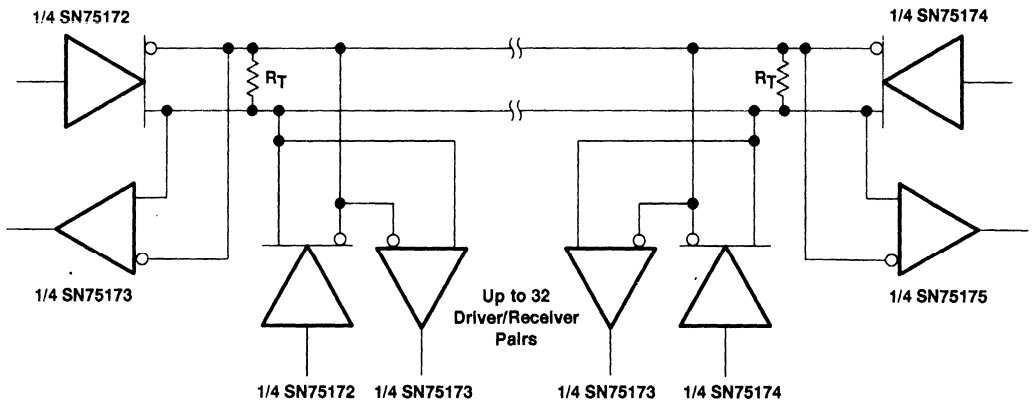


Figure 13. Typical Application Circuit

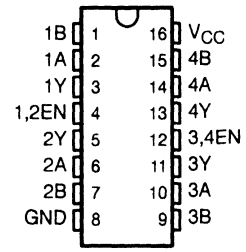
NOTE: The line should be terminated at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

SN75ALS175
QUADRUPLE DIFFERENTIAL LINE RECEIVER

SLLS131C – SEPTEMBER 1991 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of ANSI EIA/TIA-422-B, EIA/TIA-423-B, and RS-485**
- **Meets ITU Recommendations V.10, V.11, X.26, and X.27**
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments**
- **Low Supply Current Requirement 27 mA Max**
- **Common-Mode Input Voltage Range of −12 V to 12 V**
- **Input Sensitivity . . . ±200 mV**
- **Input Hysteresis . . . 50 mV Typ**
- **High Input Impedance . . . 12 kΩ Min**
- **Operates From Single 5-V Supply**

N OR NS† PACKAGE
(TOP VIEW)



† The NS package is only available left-ended taped and reeled (order device SN75ALS175NSLE).

FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL INPUTS A – B	ENABLE EN	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	H
-0.2 V $< V_{ID} < 0.2$ V	H	?
$V_{ID} \leq -0.2$ V	H	L
X	L	Z
Open Circuit	H	H

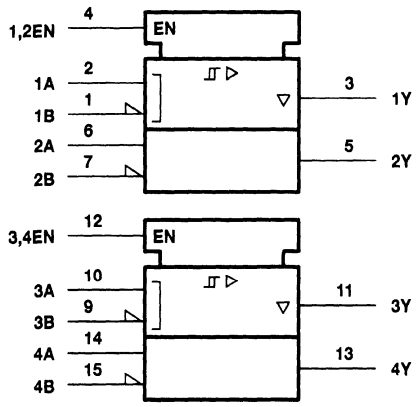
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

description

The SN75ALS175 is a monolithic quadruple differential line receiver with 3-state outputs. It is designed to meet the requirements of ANSI Standards EIA/TIA-422-B, EIA/TIA-423-B, and RS-485 and several ITU recommendations. Advanced low-power Schottky technology provides high speed without the usual power penalty. Each of the two pairs of receivers has a common active-high enable. The device features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of −12 V to 12 V.

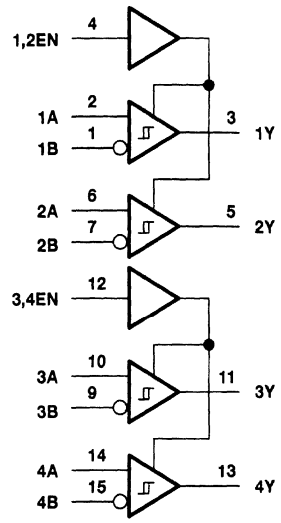
The SN75ALS175 is characterized for operation from 0°C to 70°C.

logic symbol‡

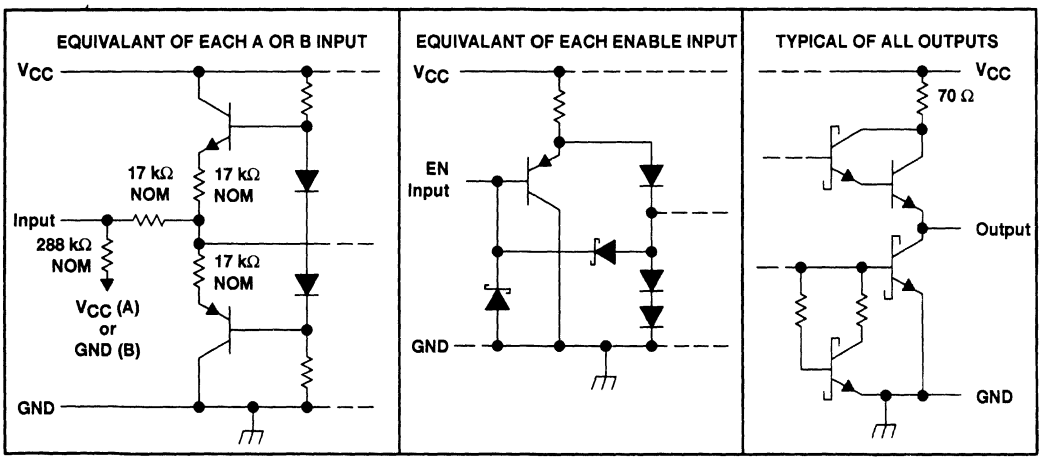


‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic



schematics of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I (A or B inputs) ..... ±14 V
Differential input voltage, V_{ID} (see Note 2) ..... ±14 V
Enable input voltage, V_I ..... 7 V
Low-level output current, I_{OL} ..... 50 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
N	1150 mW	9.2 mW/°C	736 mW
NS	625 mW	5.0 mW/°C	400 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±12	V
Differential input voltage, V_{ID}			±12	V
High-level enable-input voltage, V_{IH}	2			V
Low-level enable-input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−400	μA
Low-level output current, I_{OL}			8	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage and operating free-air temperature (unless otherwise noted) (see Note 3)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage						200	mV
V_{IT-}	Negative-going input threshold voltage				−200‡			mV
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)					50		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA					−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = −400 μA,	See Figure 1	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV,	I_{OL} = 8 mA,	See Figure 1			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V					±20	μA
I_I	Line input current	Other input at 0 V,	See Note 3	V_I = 12 V			1	mA
				V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	$V_{IH(E)}$ = 2.7 V					20	μA
I_{IL}	Low-level enable-input current	$V_{IL(E)}$ = 0.4 V					−100	μA
r_i	Input resistance				12			kΩ
I_{OS}	Short-circuit output current	V_O = 0			−15		−85	mA
I_{CC}	Suply current (total package)	No load,	Outputs enabled			16	24	mA
		No load,	Outputs disabled			18	27	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold voltage levels only.
NOTE 3: Refer to ANSI Standards RS-485 for exact conditions.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	V_{ID} = −2.5 V to 2.5 V,		9	18	27	ns
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 15 pF,	See Figure 2	9	18	27	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 3	4	12	18	ns
t_{PZL}	Output enable time to low level			6	13	21	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 3	10	21	27	ns
t_{PLZ}	Output disable time from low level			8	15	25	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

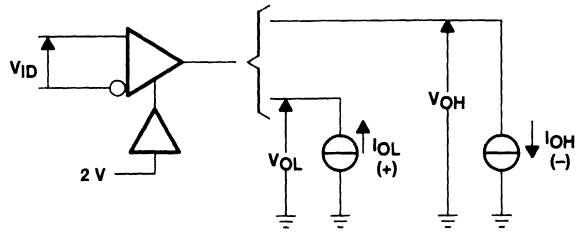
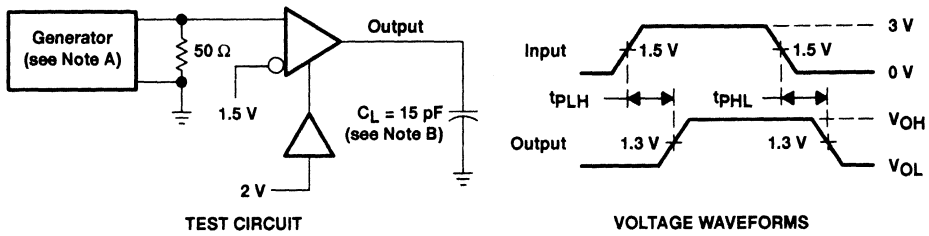


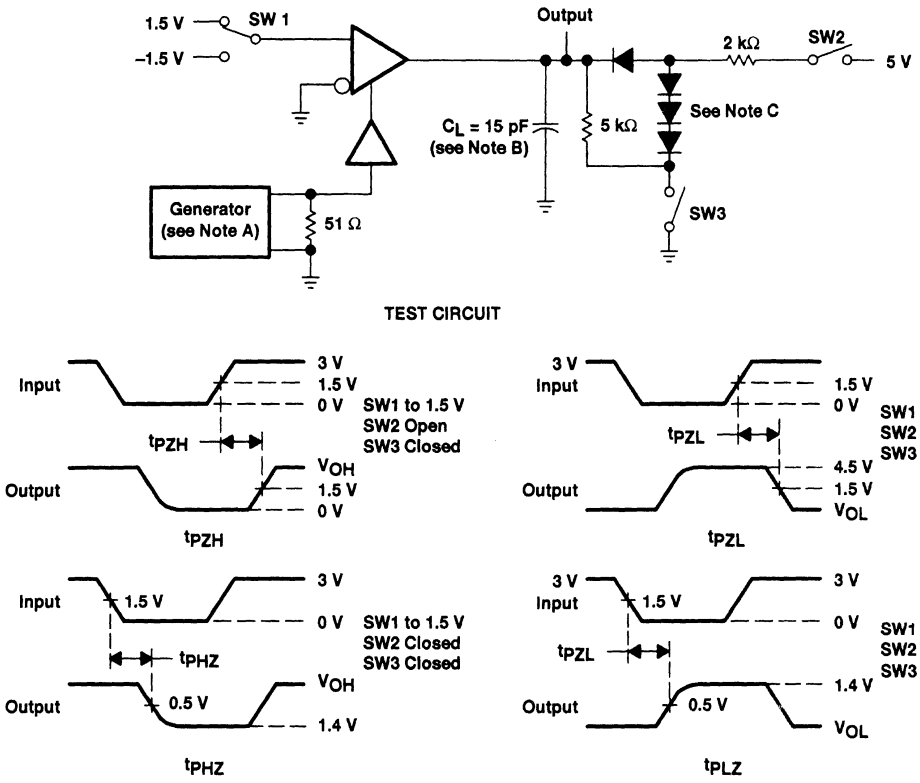
Figure 1. V_{OH}, V_{OL}



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f = 6$ ns.
B. C_L includes probe and jig capacitance.

Figure 2. Propagation Delay Times

PARAMETER MEASUREMENT INFORMATION



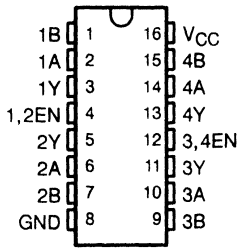
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f = 6$ ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

Figure 3. Enable and Disable Times

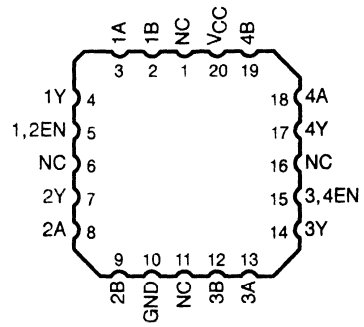
SN55LBC175
QUADRUPLE LOW-POWER DIFFERENTIAL LINE RECEIVER

- **Meet EIA Standards RS-422-A, RS-423-A, RS-485, and CCITT V.11**
- **Designed to Operate With Pulse Durations as Short as 20 ns**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Input Sensitivity . . . ±200 mV**
- **Low-Power Consumption . . . 20 mA Max**
- **Open-Circuit Fail-Safe Design**
- **Common-Mode Input Voltage Range of −7 V to 12 V**

J OR W PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN55LBC175 is a monolithic quadruple differential line receiver with 3-state outputs and is designed to meet the requirements of the EIA Standards RS-422-A, RS-423-A, RS-485, and CCITT V.11. This device is optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. The receivers are enabled in pairs with an active-high enable input. Each differential receiver input features high impedance, hysteresis for increased noise immunity, and sensitivity of ±200 mV over a common-mode input voltage range of 12 V to −7 V. Fail-safe design ensures that if the inputs are open circuited, the outputs are always high. This device is designed using the Texas Instruments proprietary LinBiCMOS™ technology allowing low power consumption, high switching speeds, and robustness.

This device offers optimum performance when used with the SN55LBC174 quadruple line driver. The SN55LBC175 is available in the 16-pin CDIP (J) package, a 16-pin CPAK (W) package, or a 20-pin LCCC (FK) package.

The SN55LBC175 is characterized over the military temperature range of −55°C to 125°C.

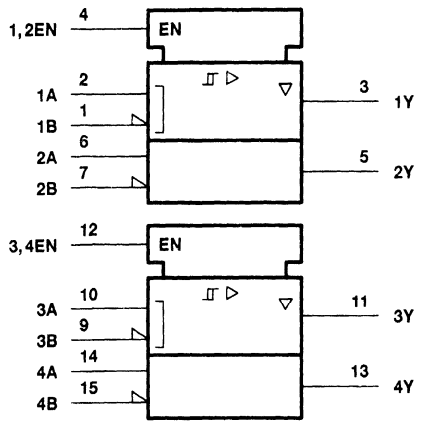
FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A–B	ENABLE	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	H
-0.2 V $< V_{ID} < 0.2$ V	H	?
$V_{ID} \leq -0.2$ V	H	L
X	L	Z
Open circuit	H	H

H = high level, L = low level, X = irrelevant,
Z = high impedance (off), ? = indeterminate

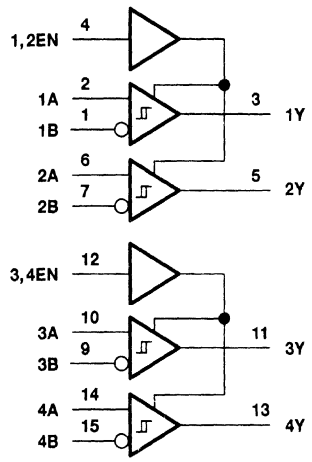
LinBiCMOS is a trademark of Texas Instruments Incorporated.

logic symbol†

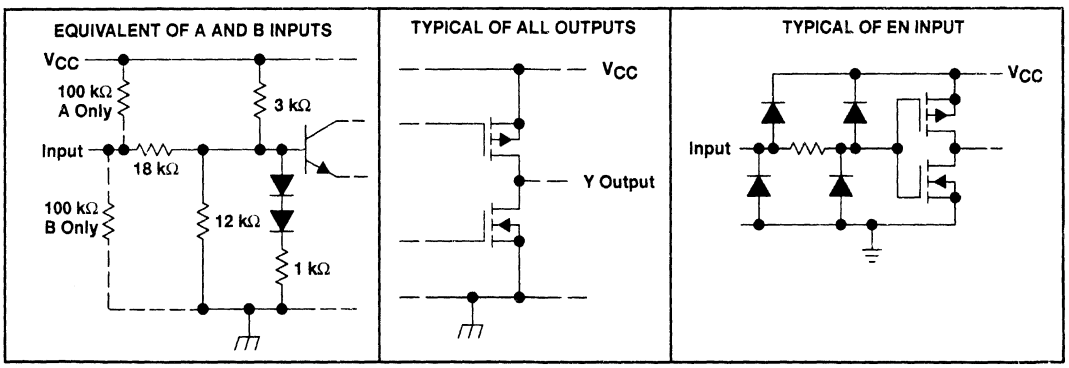


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the J or W package.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.3 V to 7 V
Input voltage, A or B inputs, V_I ..... ±25 V
Differential input voltage, V_{ID} (see Note 2) ..... ±25 V
Data and control voltage range ..... −0.3 V to 7 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −55°C to 125°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 125°C$ POWER RATING
FK	1375 mW	11.0 mW/°C	275 mW
J	1375 mW	11.0 mW/°C	275 mW
W	1000 mW	8.0 mW/°C	200 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Common-mode input voltage, V_{IC}		−7		12	V
Differential input voltage, V_{ID}				±6	V
High-level input voltage, V_{IH}	EN inputs	2			V
Low-level input voltage, V_{IL}	EN inputs			0.8	V
High-level output current, I_{OH}				−8	mA
Low-level output current, I_{OL}				16	mA
Operating free-air temperature, T_A		−55		125	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		I_O = −8 mA					0.2	V
V_{IT-}	Negative-going input threshold voltage		I_O =16 mA			−0.2			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)						45		mV
V_{IK}	Enable input clamp voltage		I_I = −18 mA				−0.9	−1.5	V
V_{OH}	High-level output voltage		V_{ID} = 200 mV,	I_{OH} = −8 mA		3.5	4.5		V
V_{OL}	Low-level output voltage		V_{ID} = −200 mV,	I_{OL} = 16 mA			0.3	0.5	V
			V_{ID} = −200 mV,	I_{OL} = 16 mA, T_A = 125°C				0.7	
I_{OZ}	High-impedance-state output current		V_O = 0 V to V_{CC}					±20	µA
I_I	Bus input current	A or B inputs	V_{IH} = 12 V,	V_{CC} = 5 V,	Other inputs at 0 V		0.7	1	mA
			V_{IH} = 12 V,	V_{CC} = 0 V,	Other inputs at 0 V		0.8	1	
			V_{IH} = −7 V,	V_{CC} = 5 V,	Other inputs at 0 V		−0.5	−0.8	
			V_{IH} = −7 V,	V_{CC} = 0 V,	Other inputs at 0 V		−0.4	−0.8	
I_{IH}	High-level enable input current		V_{IH} = 5 V					±20	µA
I_{IL}	Low-level enable input current		V_{IL} = 0 V					−20	µA
I_{OS}	Short-circuit output current		V_O = 0				−80	−120	mA
I_{CC}	Supply current		Outputs enabled,	I_O = 0,	V_{ID} = 5 V		11	20	mA
			Outputs disabled				0.9	1.4	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	V_{ID} = −1.5 V to 1.5 V, See Figure 1	25°C	11	22	30	ns
			−55°C to 125°C			35	
t_{PLH}	Propagation delay time, low- to high-level output	V_{ID} = −1.5 V to 1.5 V, See Figure 1	25°C	11	22	30	ns
			−55°C to 125°C			35	
t_{PZH}	Output enable time to high level	See Figure 2	25°C		17	40	ns
			−55°C to 125°C			45	
t_{PZL}	Output enable time to low level	See Figure 3	25°C		18	30	ns
			−55°C to 125°C			35	
t_{PHZ}	Output disable time from high level	See Figure 2	25°C		30	40	ns
			−55°C to 125°C			55	
t_{PLZ}	Output disable time from low level	See Figure 3	25°C		23	30	ns
			−55°C to 125°C			45	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	See Figure 1	25°C		4	6	ns
			−55°C to 125°C			7	
t_t	Transition time	See Figure 1	25°C		3	10	ns
			−55°C to 125°C			16	

PARAMETER MEASUREMENT INFORMATION

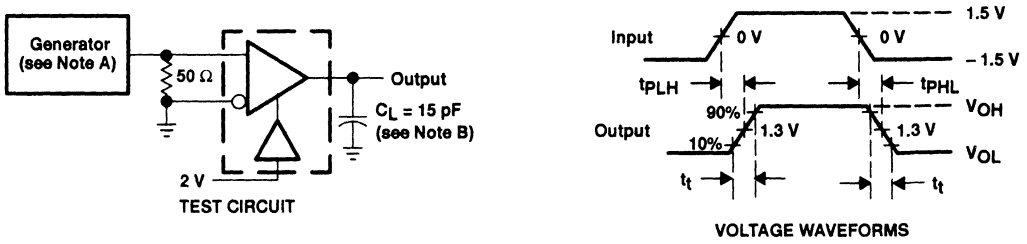


Figure 1. t_{PLH} and t_{PHL} Test Circuit and Voltage Waveforms

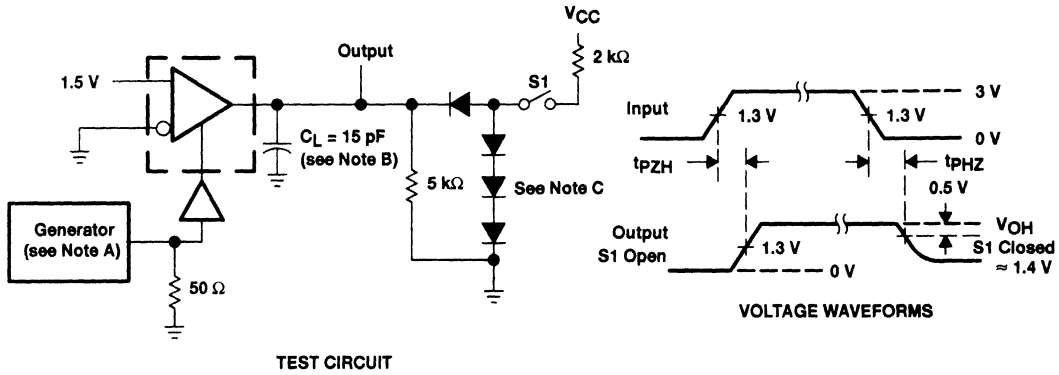


Figure 2. t_{PHZ} and t_{PZH} Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

PARAMETER MEASUREMENT INFORMATION

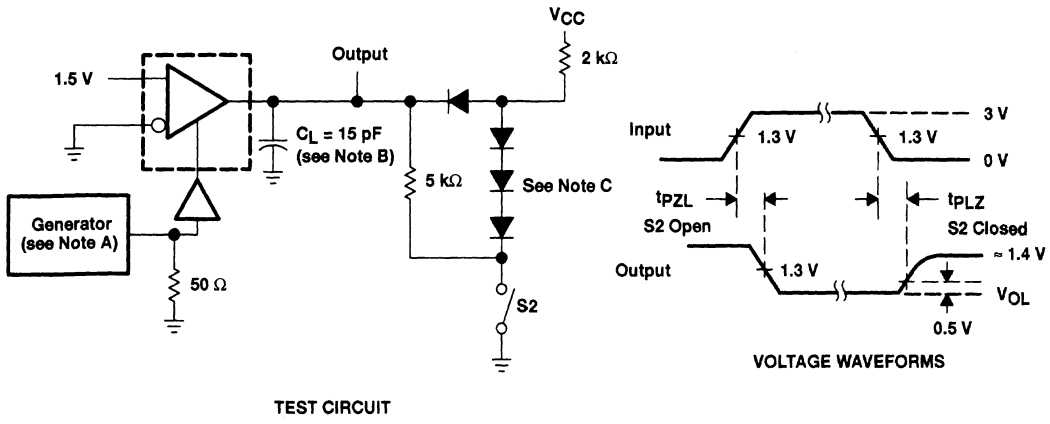


Figure 3. t_{PZL} and t_{PLZ} Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

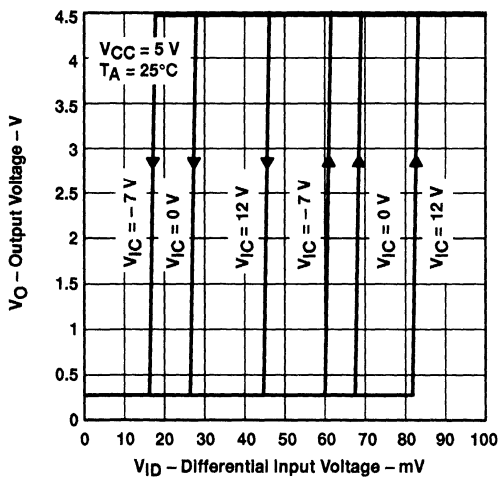


Figure 4

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

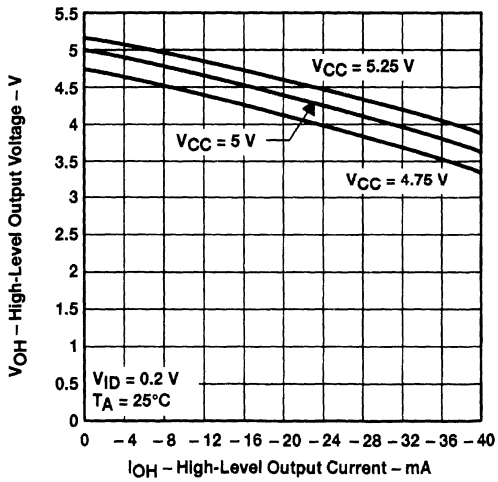


Figure 5

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

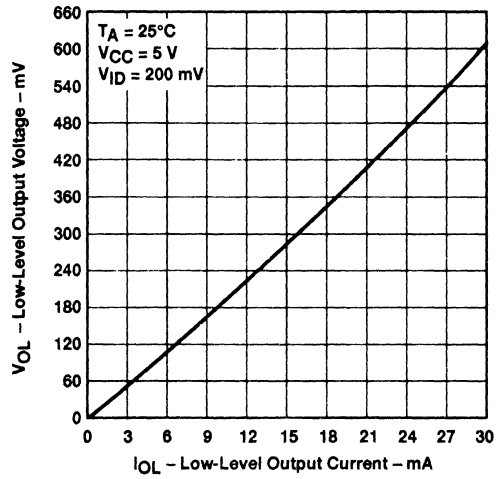


Figure 6

AVERAGE SUPPLY CURRENT
vs
FREQUENCY

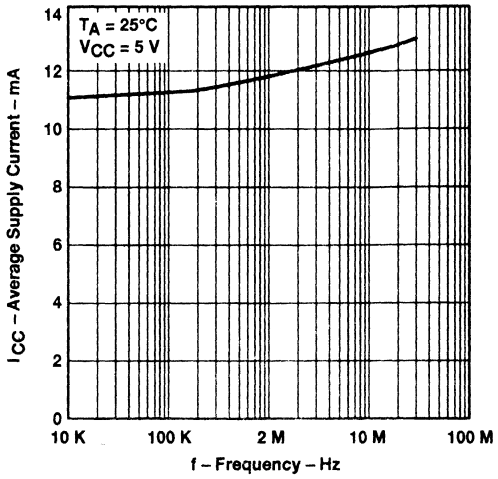


Figure 7

BUS
INPUT CURRENT
vs
INPUT VOLTAGE
(COMPLEMENTARY INPUT AT 0 V)

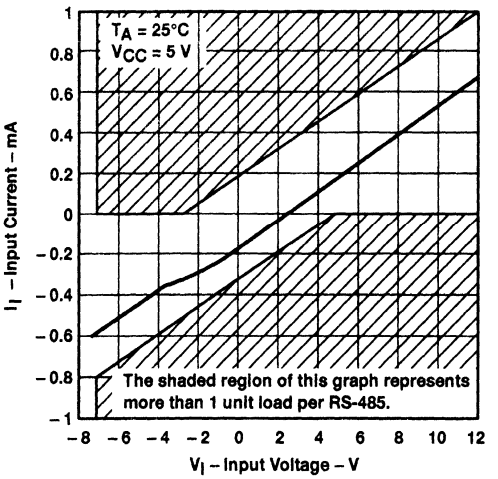


Figure 8

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

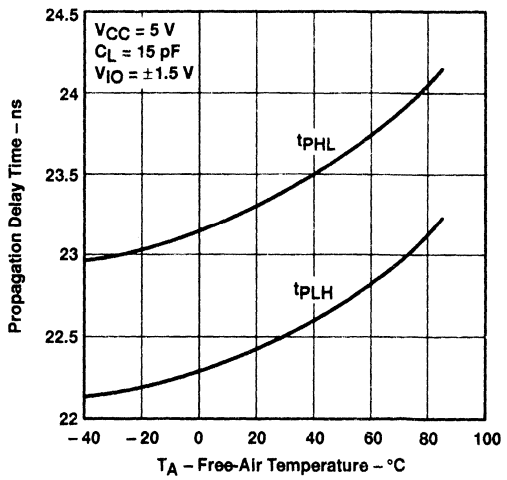


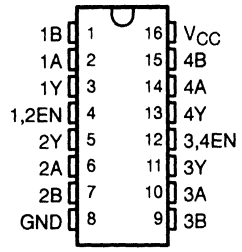
Figure 9

SN65LBC175, SN75LBC175
QUADRUPLE LOW-POWER DIFFERENTIAL LINE RECEIVERS

SLLS171 – OCTOBER 1993

- **Meet or Exceed the EIA Standards RS-422-A, RS-423-A, RS-485, and CCITT Recommendation V.11**
- **Designed to Operate With Pulse Durations as Short as 20 ns**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Input Sensitivity . . . ±200 mV**
- **Low-Power Consumption . . . 20 mA Max**
- **Open-Circuit Fail-Safe Design**
- **Common-Mode Input Voltage Range of −7 V to 12 V**
- **Pin Compatible With SN75175 and MC3486**

D OR N PACKAGE
(TOP VIEW)



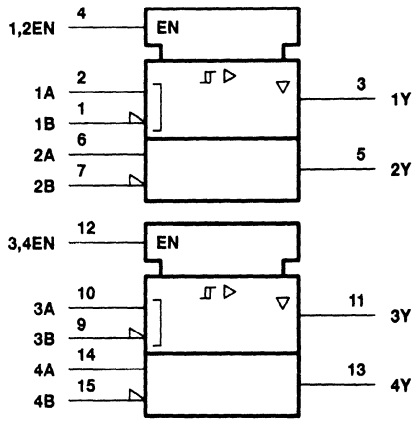
description

The SN65LBC175 and SN75LBC175 are monolithic, quadruple, differential line receivers with 3-state outputs and are designed to meet the requirements of the EIA standards RS-422-A, RS-423-A, RS-485, and CCITT Recommendation V.11. The devices are optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. The receivers are enabled in pairs with an active-high enable input. Each differential receiver input features high impedance, hysteresis for increased noise immunity, and sensitivity of ±200 mV over a common-mode input voltage range of 12 V to −7 V. The fail-safe design ensures that when the inputs are open circuited, the outputs are always high. Both devices are designed using the TI proprietary LinBiCMOS™ technology allowing low power consumption, high switching speeds, and robustness.

This device offers optimum performance when used with the SN75LBC172 or SN75LBC174 quadruple line drivers. The SN65LBC175 and SN75LBC175 are available in the 16-pin DIP (N) and small-outline inline circuit (SOIC) D packages.

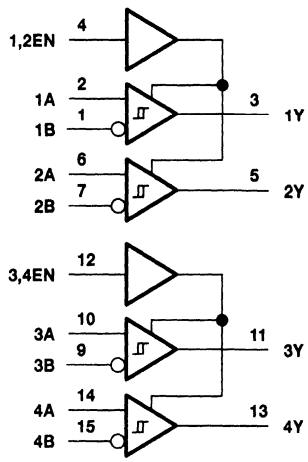
The SN65LBC175 is characterized over the industrial temperature range of −40°C to 85°C. The SN75LBC175 is characterized for operation over the commercial temperature range of 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



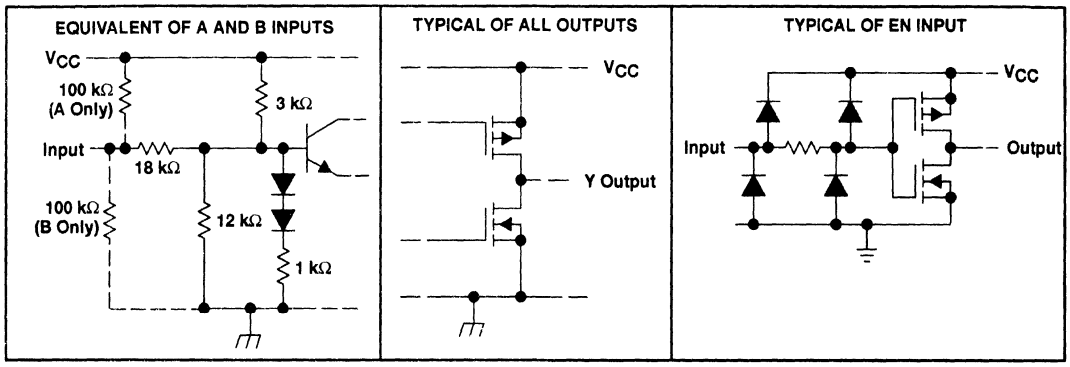
LinBiCMOS is a trademark of Texas Instruments Incorporated.

FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A–B	ENABLE	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	H
-0.2 V $< V_{ID} < 0.2$ V	H	?
$V_{ID} \leq -0.2$ V	H	L
X	L	Z
Open Circuit	H	H

H = high level, L = low level, X = irrelevant,
Z = high impedance (off), ? = indeterminate

schematics of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.3 V to 7 V
Input voltage, V_I (A or B inputs) ..... ±25 V
Differential input voltage, V_{ID} (see Note 2) ..... ±25 V
Data and control voltage range ..... −0.3 V to 7 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65LBC175 ..... −40°C to 85°C
SN75LBC175 ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	1100 mW	8.7 mW/°C	709 mW	578 mW
N	1510 mW	12.1 mW/°C	966 mW	784 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Common-mode input voltage, V_{IC}		−7		12	V
Differential input voltage, V_{ID}				±6	V
High-level input voltage, V_{IH}	EN inputs	2			V
Low-level input voltage, V_{IL}	EN inputs			0.8	V
High-level output current, I_{OH}				−8	mA
Low-level output current, I_{OL}				16	mA
Operating free-air temperature, T_A	SN65LBC175	−40		85	°C
	SN75LBC175	0		70	

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		I_O = −8 mA			0.2	V
V_{IT-}	Negative-going input threshold voltage		I_O =16 mA	−0.2			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)				45		mV
V_{IK}	Enable input clamp voltage		I_I = −18 mA		−0.9	−1.5	V
V_{OH}	High-level output voltage		V_{ID} = 200 mV, I_{OH} = −8 mA	3.5	4.5		V
V_{OL}	Low-level output voltage		V_{ID} = −200 mV, I_{OL} = 16 mA		0.3	0.5	V
I_{OZ}	High-impedance-state output current		V_O = 0 V to V_{CC}			±20	µA
I_I	Bus input current	A or B inputs	V_{IH} = 12 V, V_{CC} = 5 V, Other inputs at 0 V		0.7	1	mA
			V_{IH} = 12 V, V_{CC} = 0 V, Other inputs at 0 V		0.8	1	mA
			V_{IH} = −7 V, V_{CC} = 5 V, Other inputs at 0 V		−0.5	−0.8	mA
			V_{IH} = −7 V, V_{CC} = 0 V, Other inputs at 0 V		−0.4	−0.8	mA
I_{IH}	High-level enable input current		V_{IH} = 5 V			±20	µA
I_{IL}	Low-level enable input current		V_{IL} = 0 V			−20	µA
I_{OS}	Short-circuit output current		V_O = 0		−80	−120	mA
I_{CC}	Supply current		Outputs enabled, I_O = 0, V_{ID} = 5 V		11	20	mA
			Outputs disabled		0.9	1.4	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PHL}	Propagation delay time, high -to low-level output	V_{ID} = −1.5 V to 1.5 V, See Figure 1	11	22	30	ns
t_{PLH}	Propagation delay time, low- to high-level output		11	22	30	ns
t_{PZH}	Output enable time to high level	See Figure 2		17	30	ns
t_{PZL}	Output enable time to low level	See Figure 3		18	30	ns
t_{PHZ}	Output disable time from high level	See Figure 2		30	40	ns
t_{PLZ}	Output disable time from low level	See Figure 3		23	30	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	See Figure 2		4	6	ns
t_t	Transition time	See Figure 1		3	10	ns

PARAMETER MEASUREMENT INFORMATION

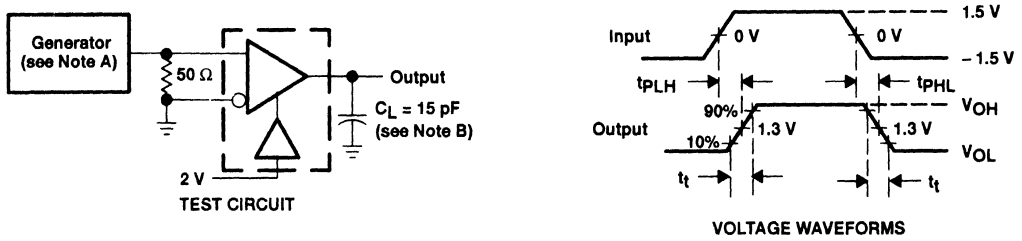


Figure 1. t_{PLH} and t_{PHL} Test Circuit and Voltage Waveforms

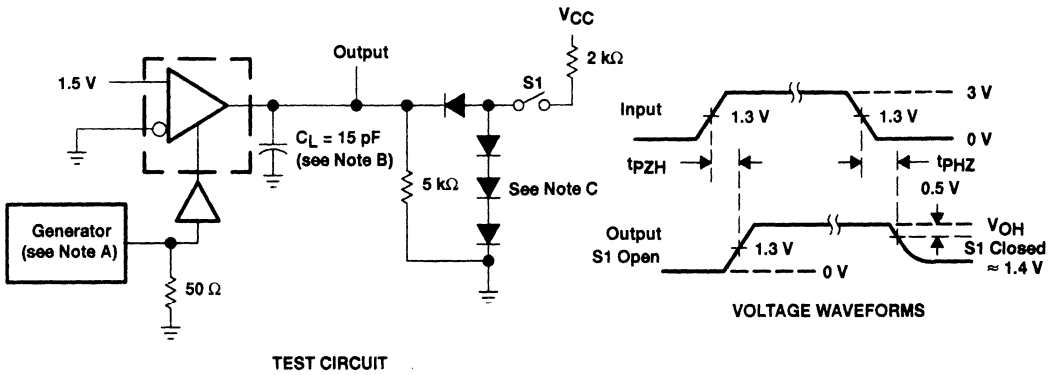


Figure 2. t_{PHZ} and t_{PZH} Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

PARAMETER MEASUREMENT INFORMATION

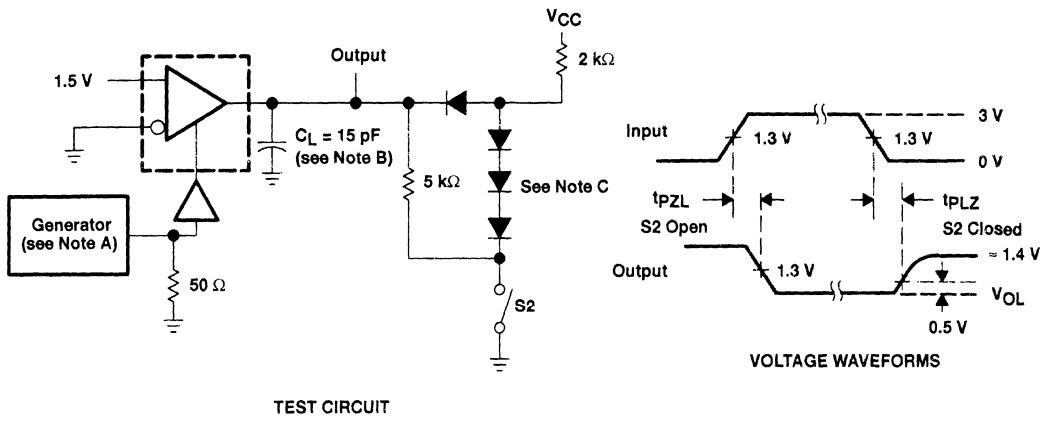


Figure 3. t_{PZL} and t_{PLZ} Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

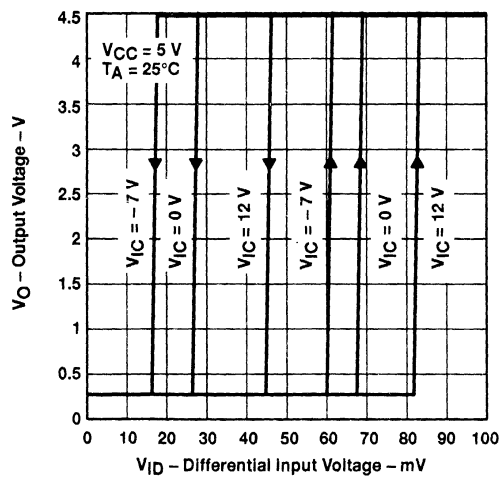


Figure 4

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

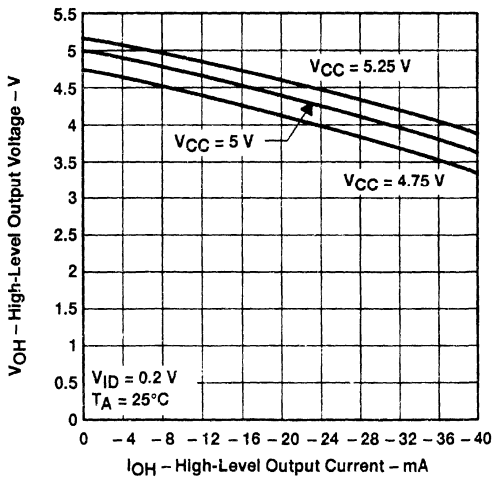


Figure 5

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

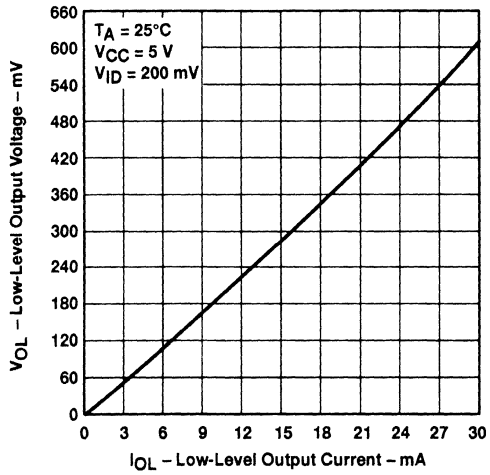


Figure 6

AVERAGE SUPPLY CURRENT
vs
FREQUENCY

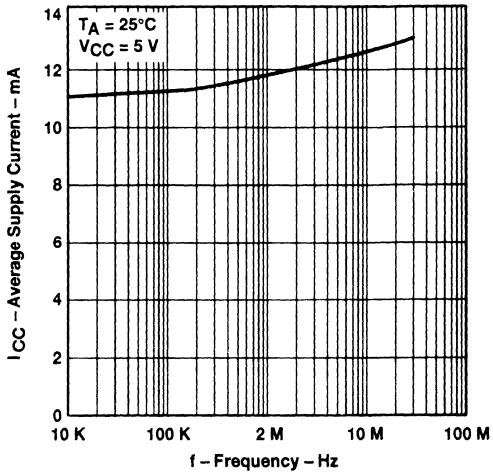


Figure 7

INPUT CURRENT
vs
INPUT VOLTAGE
(COMPLEMENTARY INPUT AT 0 V)

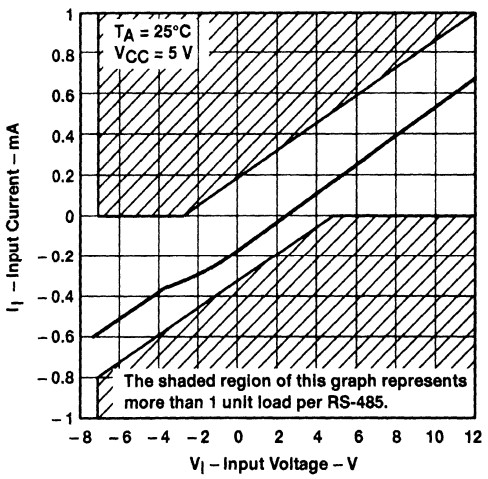


Figure 8

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

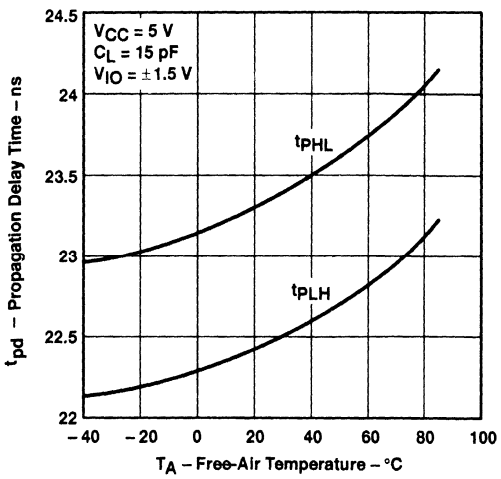
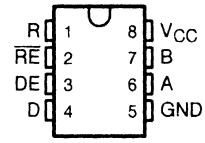


Figure 9

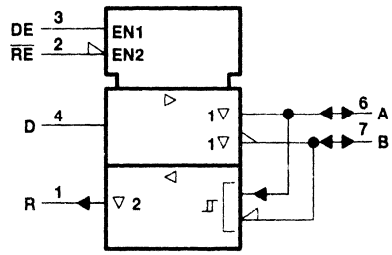
SLLS100A – JUNE 1984 – REVISED MAY 1995

- Bidirectional Transceiver
- Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-422-B and ITU Recommendation V.11
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Driver and Receiver Outputs
- Individual Driver and Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capability . . . ±60 mA Max
- Thermal-Shutdown Protection
- Driver Positive- and Negative-Current Limiting
- Receiver Input Impedance . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates From Single 5-V Supply
- Low Power Requirements

D OR P PACKAGE
(TOP VIEW)

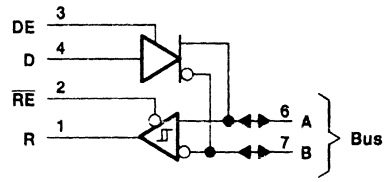


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



description

The SN75176A differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus-transmission lines. It is designed for balanced transmission lines and meets ANSI Standard EIA/TIA-422-B and ITU Recommendation V.11.

The SN75176A combines a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

Function Tables

DRIVER

INPUT D	ENABLE DE	OUTPUTS A	OUTPUTS B
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V < V_{ID} < 0.2 V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	?

H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

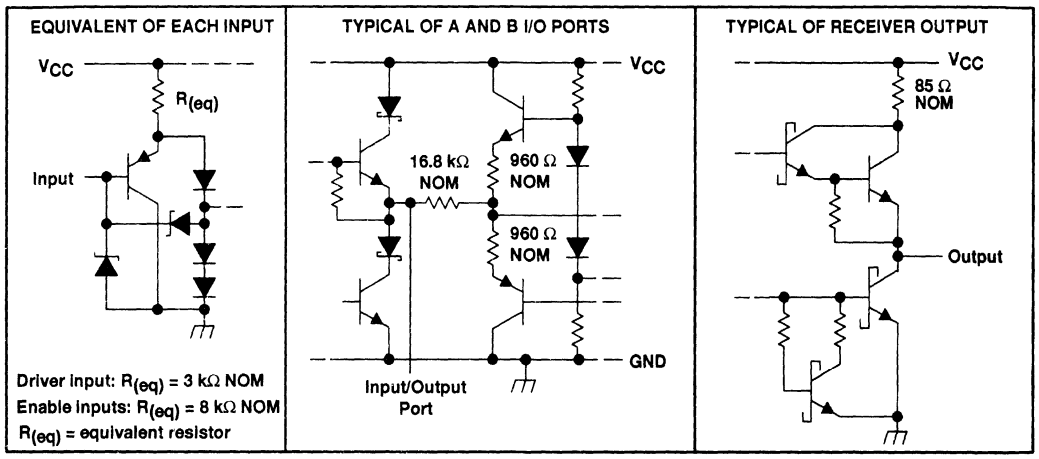
description (continued)

The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive- and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

The SN75176A can be used in transmission-line applications employing the SN75172 and SN75174 quadruple differential line drivers and SN75173 and SN75175 quadruple differential line receivers.

The SN75176A is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Voltage range at any bus terminal ..... −10 V to 15 V
Enable input voltage, V_I ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 105°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	261 mW
P	1100 mW	8.8 mW/°C	704 mW	396 mW

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}		−7		12	V
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	µA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V, I_{OH} = −33 mA	V_{IL} = 0.8 V,		3.7		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V, I_{OH} = 33 mA	V_{IL} = 0.8 V,		1.1		V
$\lvert V_{OD1}\rvert$	Differential output voltage	$I_O = 0$				$2V_{OD2}$	V
$\lvert V_{OD2}\rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 1	2	2.7		V
		R_L = 54 Ω,	See Figure 1	1.5	2.4		
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage‡					±0.2	V
V_{OC}	Common-mode output voltage§	R_L = 54 Ω or 100 Ω,	See Figure 1			3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage‡					±0.2	V
I_O	Output current	Output disabled, See Note 3	V_O = 12 V			1	mA
			V_O = −7 V			−0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−400	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−250	mA
		$V_O = V_{CC}$				250	
		V_O = 12 V				500	
I_{CC}	Supply current (total package)	No load	Outputs enabled		35	50	mA
			Outputs disabled		26	40	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.
§ In ANSI Standard EIA/TIA-422-B, V_{OC}, which is the average of the two output voltages with respect to GND, is called output offset voltage, V_{OS}.
NOTE 3: This applies for both power on and off; refer to ANSI Standard EIA/TIA-422-B for exact conditions.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	R_L = 60 Ω,	See Figure 3		40	60	ns
$t_{t(OD)}$	Differential-output transition time				65	95	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 4		55	90	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 5		30	50	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 4		85	130	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 5		20	40	ns

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{IT-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Input hysteresis voltage ($V_{IT+} - V_{IT-}$)				50		mV
V_{IK}	Enable clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, See Figure 2	I_{OH} = −400 μA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 2	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input = 0 V, See Note 3	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current			−15		−85	mA
I_{CC}	Supply current (total package)	No load	Outputs enabled		35	50	mA
			Outputs disabled		26	40	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
NOTE 3. This applies for both power on and power off. Refer to ANSI Standard EIA/TIA-422-B for exact conditions.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5 V to 1.5 V, See Figure 6		21	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output			23	35	ns
t_{PZH}	Output enable time to high level	See Figure 7		10	30	ns
t_{PZL}	Output enable time to low level			12	30	ns
t_{PHZ}	Output disable time from high level	See Figure 7		20	35	ns
t_{PLZ}	Output disable time from low level			17	25	ns

PARAMETER MEASUREMENT INFORMATION

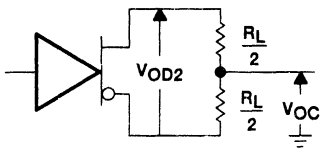


Figure 1. Driver V_{OD} and V_{OC}

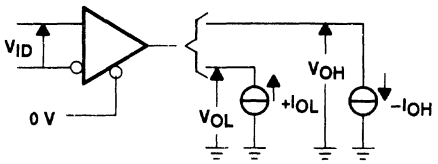


Figure 2. Receiver V_{OH} and V_{OL}

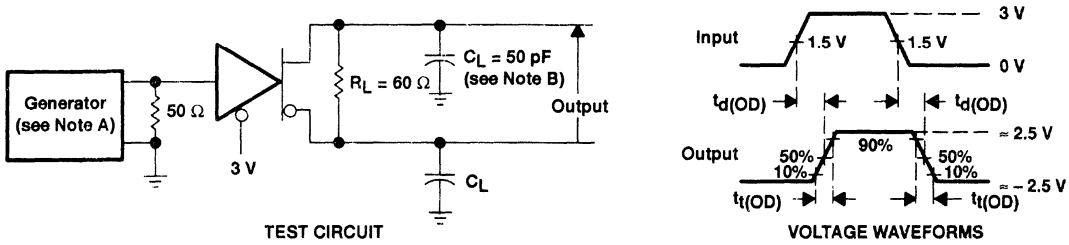


Figure 3. Driver Test Circuit and Voltage Waveforms

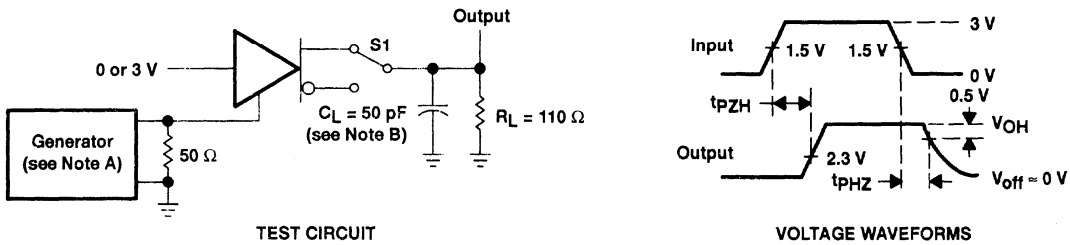


Figure 4. Driver Test Circuit and Voltage Waveforms

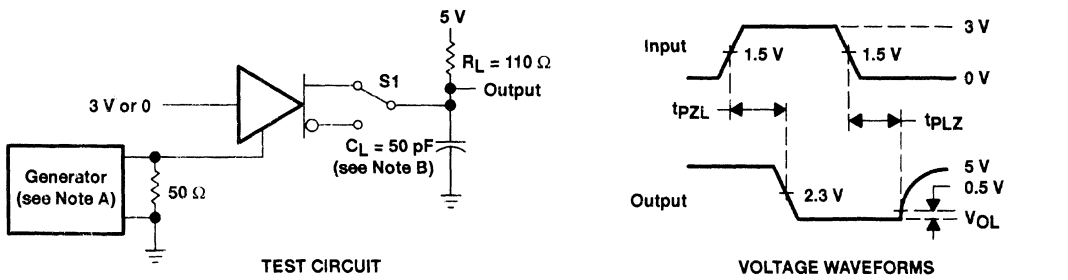


Figure 5. Driver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r \le 6$ ns, $t_f \le 6$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

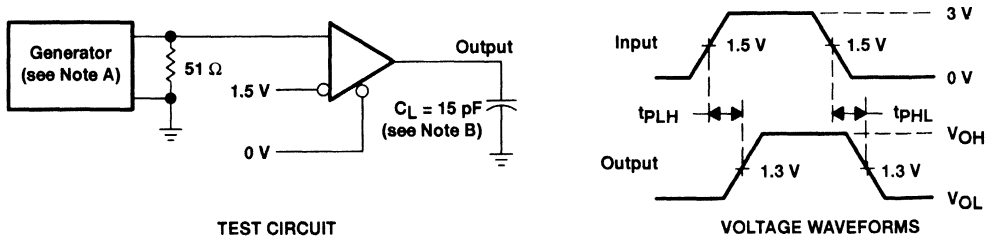


Figure 6. Receiver Test Circuit and Voltage Waveforms

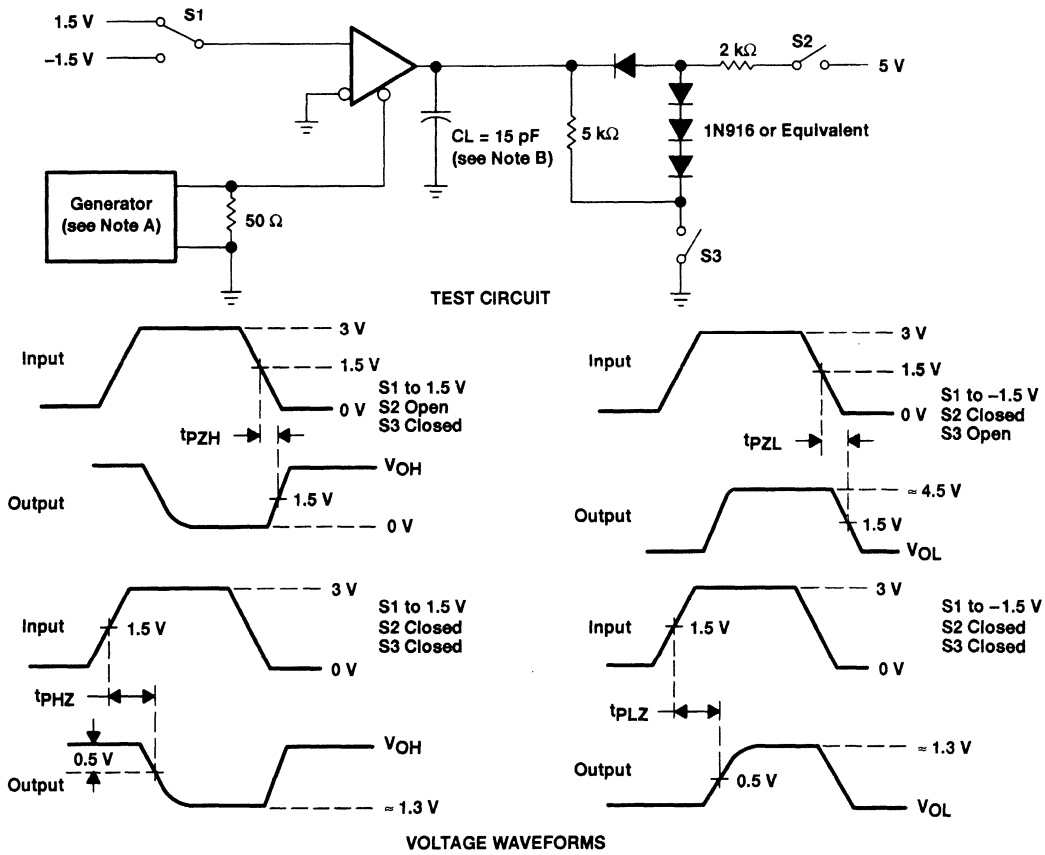


Figure 7. Receiver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

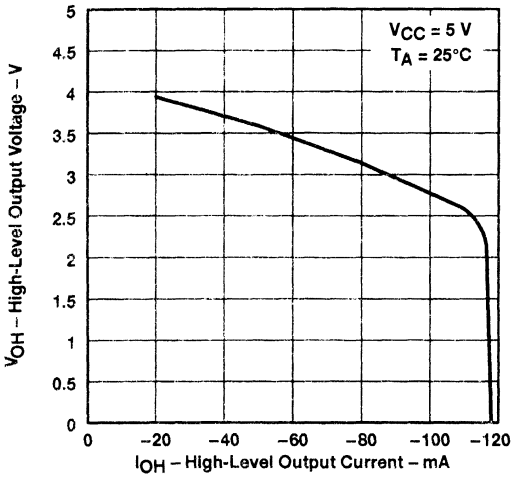


Figure 8

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

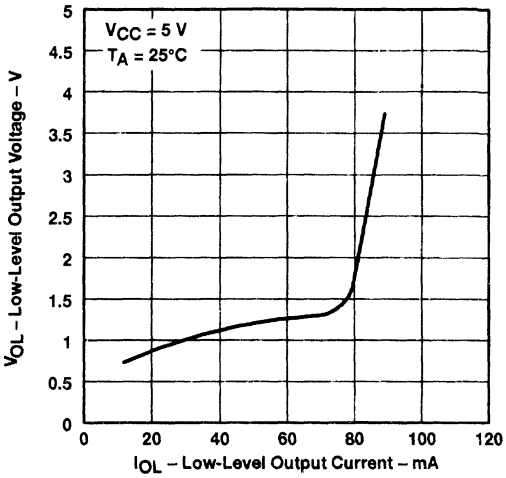


Figure 9

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

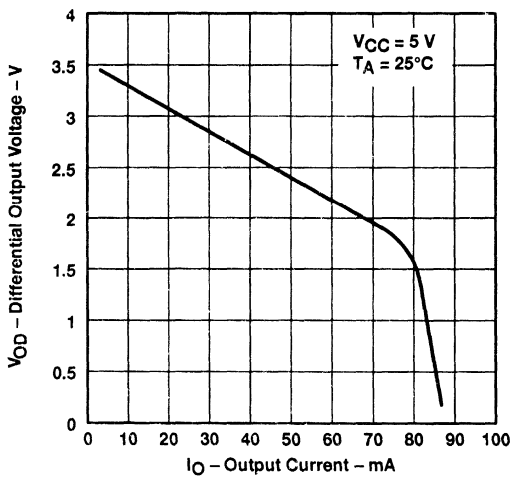


Figure 10

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

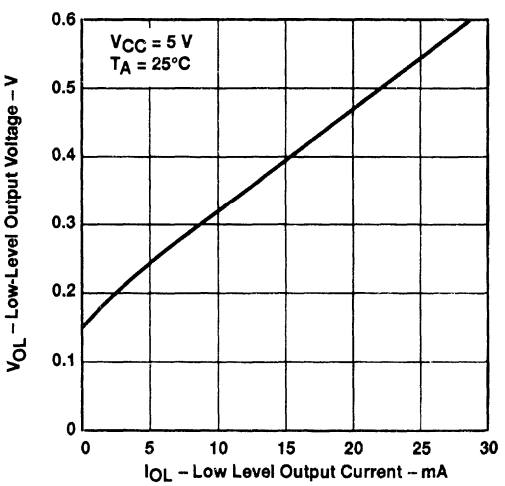


Figure 11

TYPICAL CHARACTERISTICS

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

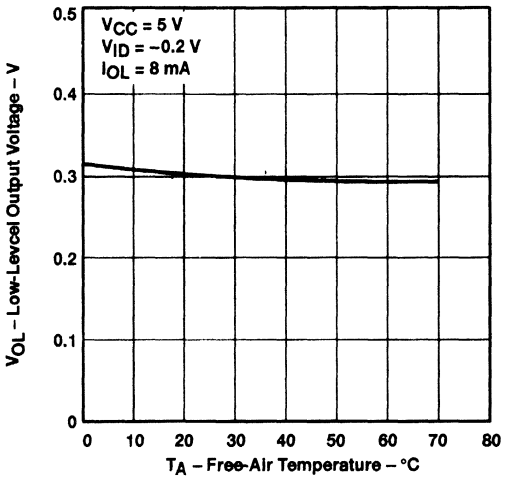


Figure 12

RECEIVER
OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

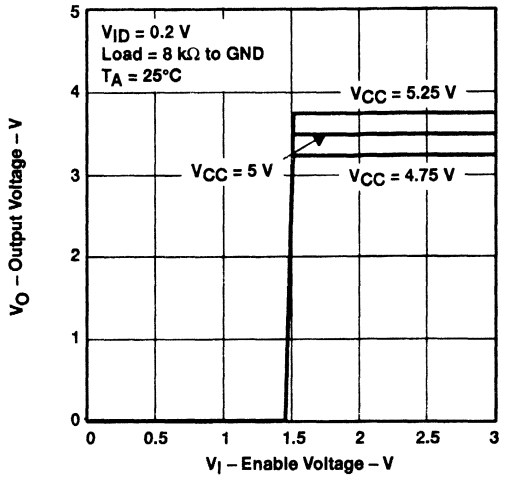


Figure 13

RECEIVER
OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

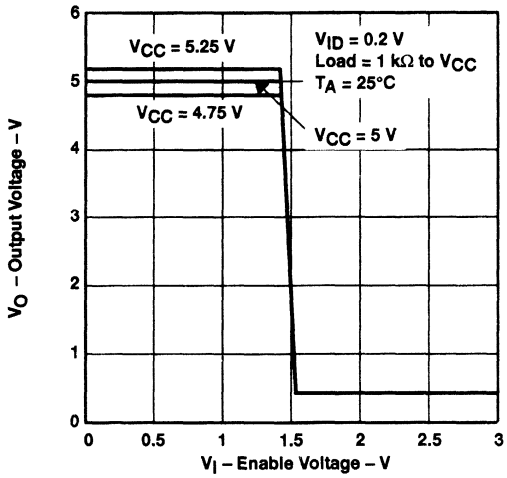


Figure 14

APPLICATION INFORMATION

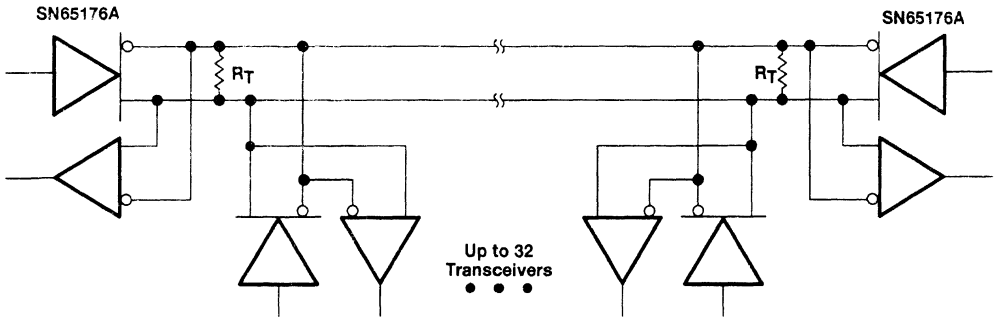


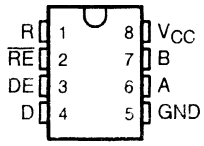
Figure 15. Typical Application Circuit

NOTE A: The line should be terminated at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

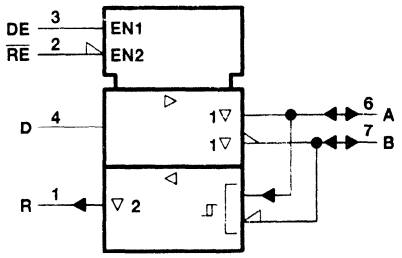
SLLS101A – JULY 1985 – REVISED MAY 1995

- Bidirectional Transceivers
- Meet or Exceed the Requirements of ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendations V.11 and X.27
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Driver and Receiver Outputs
- Individual Driver and Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capability . . . ±60 mA Max
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Impedance . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operate From Single 5-V Supply

D OR P PACKAGE
(TOP VIEW)

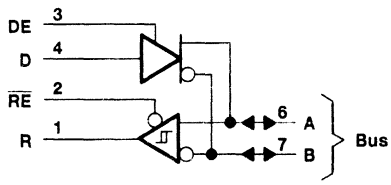


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



description

The SN65176B and SN75176B differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendations V.11 and X.27.

The SN65176B and SN75176B combine a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

Function Tables

DRIVER

INPUT D	ENABLE DE	OUTPUTS A	OUTPUTS B
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

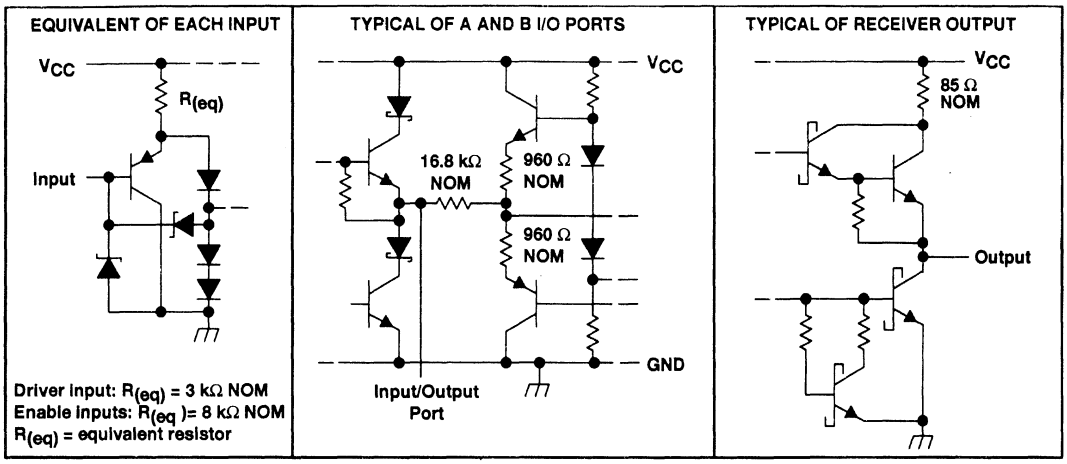
description (continued)

The driver is designed for up to 60 mA of sink or source current. The driver features positive- and negative-current limiting and thermal shutdown for protection from line-fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

The SN65176B and SN75176B can be used in transmission line applications employing the SN75172 and SN75174 quadruple differential line drivers and SN75173 and SN75175 quadruple differential line receivers.

The SN65176B is characterized for operation from −40°C to 105°C and the SN75176B is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Voltage range at any bus terminal ..... −10 V to 15 V
Enable input voltage, V_I ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65176B ..... −40°C to 105°C
SN75176B ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 105°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	261 mW
P	1100 mW	8.8 mW/°C	704 mW	396 mW

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12	V
				−7	
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A	SN65176B	−40		105	°C
	SN75176B	0		70	

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_O	Output voltage	$I_O = 0$		0		6	V
$\lvert V_{OD1}\rvert$	Differential output voltage	$I_O = 0$		1.5	3.6	6	V
$\lvert V_{OD2}\rvert$	Differential output voltage	$R_L = 100\ \Omega$, See Figure 1		1/2 V_{OD1} or 2¶			V
		$R_L = 54\ \Omega$, See Figure 1		1.5	2.5	5	V
V_{OD3}	Differential output voltage	See Note 4		1.5		5	V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage§	$R_L = 54\ \Omega$ or $100\ \Omega$, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage					+3 −1	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current	Output disabled, See Note 3	$V_O = 12$ V			1	mA
			$V_O = -7$ V			−0.8	
I_{IH}	High-level input current	$V_I = 2.4$ V				20	μA
I_{IL}	Low-level input current	$V_I = 0.4$ V				−400	μA
I_{OS}	Short-circuit output current	$V_O = -7$ V				−250	mA
		$V_O = 0$				150	
		$V_O = V_{CC}$				250	
		$V_O = 12$ V				250	
I_{CC}	Supply current (total package)	No load	Outputs enabled		42	70	mA
			Outputs disabled		26	35	

† The power-off measurement in ANSI Standard EIA/TIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
‡ All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.
§ $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
¶ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.

NOTES: 3. See ANSI Standard RS-485 Figure 3.5, Test Termination Measurement 2.
4. This applies for both power on and off; refer to ANSI Standard RS-485 for exact conditions. The EIA/TIA-422-B limit does not apply for a combined driver and receiver terminal.

switching characteristics, $V_{CC} = 5$ V, $R_L = 110\ k\Omega$, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	$R_L = 54\ \Omega$, See Figure 3		15	22	ns
$t_{t(OD)}$	Differential-output transition time			20	30	ns
t_{PZH}	Output enable time to high level	See Figure 4		85	120	ns
t_{PZL}	Output enable time to low level	See Figure 5		40	60	ns
t_{PHZ}	Output disable time from high level	See Figure 4		150	250	ns
t_{PLZ}	Output disable time from low level	See Figure 5		20	30	ns

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	EIA/TIA-422-B	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\lvert V_{OD1}\rvert$	V_o	V_o
$\lvert V_{OD2}\rvert$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\lvert V_{OD3}\rvert$		V_t (Test Termination Measurement 2)
$\Delta\lvert V_{OD}\rvert$	$\lvert\lvert V_t\rvert - \lvert\overline{V}_t\rvert\rvert$	$\lvert\lvert V_t\rvert - \lvert\overline{V}_t\rvert\rvert$
V_{OC}	$\lvert V_{os}\rvert$	$\lvert V_{os}\rvert$
$\Delta\lvert V_{OC}\rvert$	$\lvert V_{os} - \overline{V}_{os}\rvert$	$\lvert V_{os} - \overline{V}_{os}\rvert$
I_{OS}	$\lvert I_{sa}\rvert$, $\lvert I_{sb}\rvert$	
I_O	$\lvert I_{xa}\rvert$, $\lvert I_{xb}\rvert$	I_{ia}, I_{ib}

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{IT-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Input hysteresis voltage ($V_{IT+} - V_{IT-}$)				50		mV
V_{IK}	Enable Input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, See Figure 2	I_{OH} = −400 μA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 2	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input = 0 V, See Note 5	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable input current	V_{IL} = 0.4 V				−100	μA
r_I	Input resistance	V_I = 12 V		12			kΩ
I_{OS}	Short-circuit output current			−15		−85	mA
I_{CC}	Supply current (total package)	No load	Outputs enabled		42	55	mA
			Outputs disabled		26	35	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 5: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_{ID} = 0 to 3 V, See Figure 6		21	35	ns
t_{PHL}	Propagation delay time, high- to low-level output			23	35	ns
t_{PZH}	Output enable time to high level	See Figure 7		10	20	ns
t_{PZL}	Output enable time to low level			12	20	ns
t_{PHZ}	Output disable time from high level	See Figure 7		20	35	ns
t_{PLZ}	Output disable time from low level			17	25	ns

PARAMETER MEASUREMENT INFORMATION

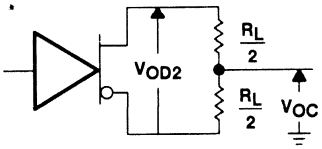


Figure 1. Driver V_{OD} and V_{OC}

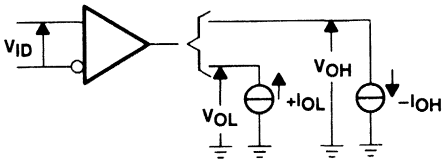
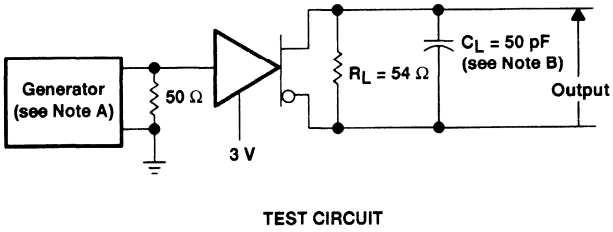
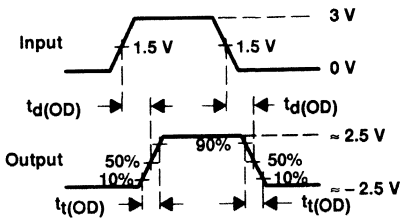


Figure 2. Receiver V_{OH} and V_{OL}

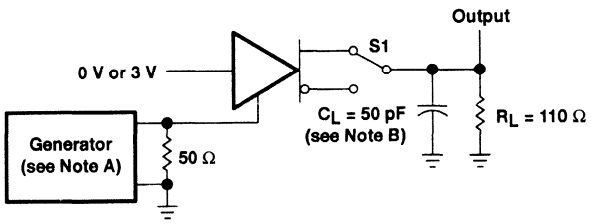


TEST CIRCUIT

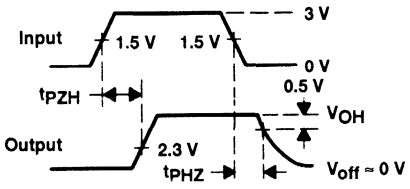


VOLTAGE WAVEFORMS

Figure 3. Driver Test Circuit and Voltage Waveforms

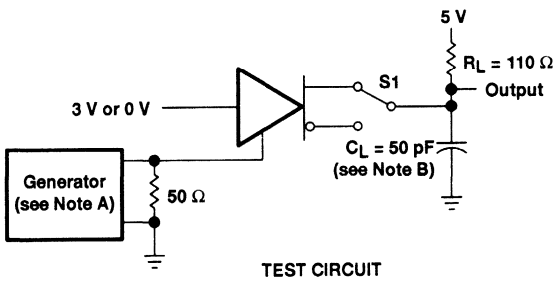


TEST CIRCUIT

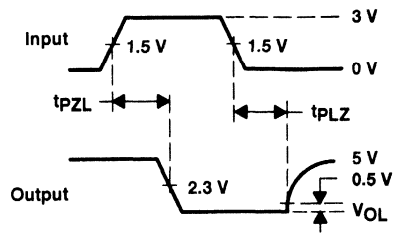


VOLTAGE WAVEFORMS

Figure 4. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 5. Driver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

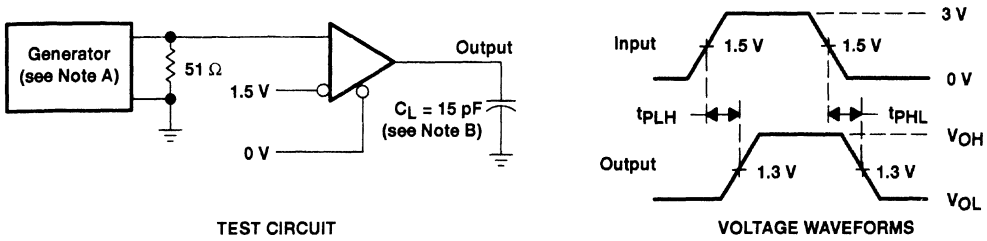


Figure 6. Receiver Test Circuit and Voltage Waveforms

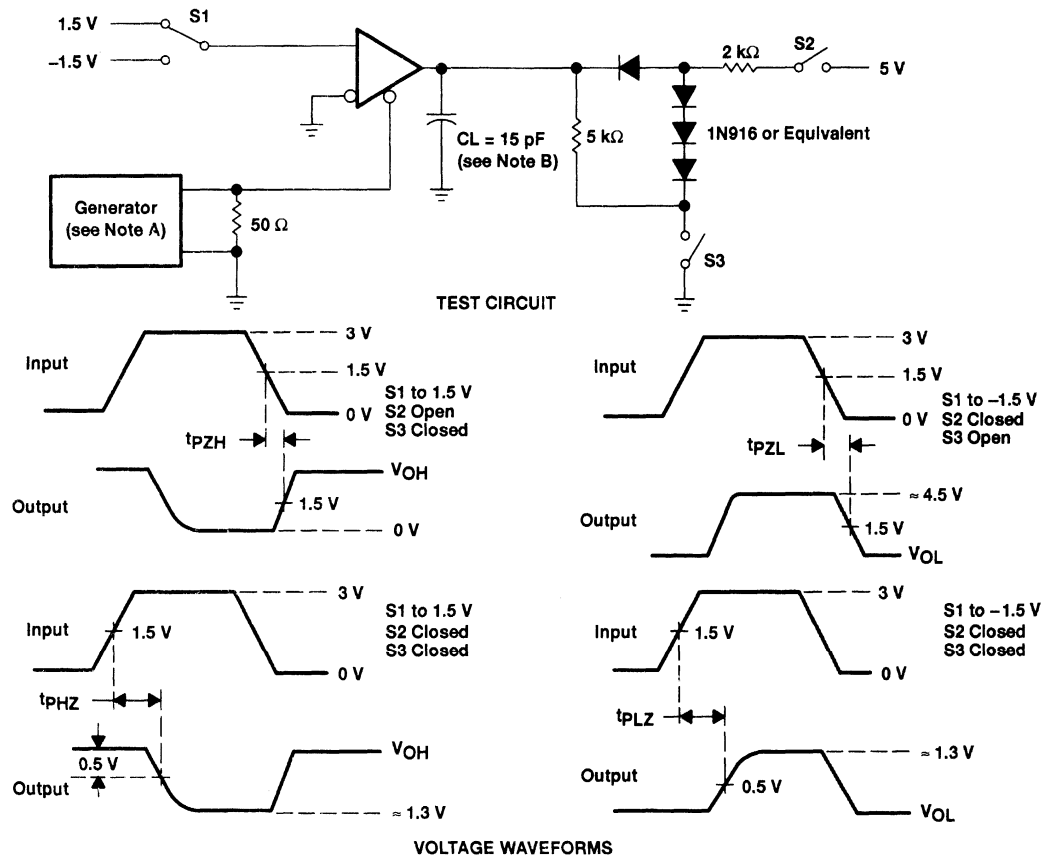


Figure 7. Receiver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

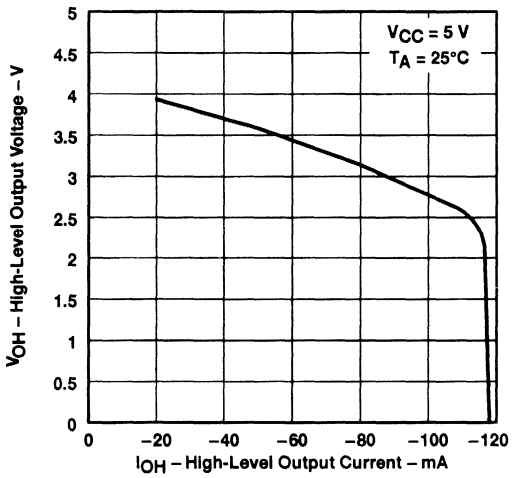


Figure 8

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

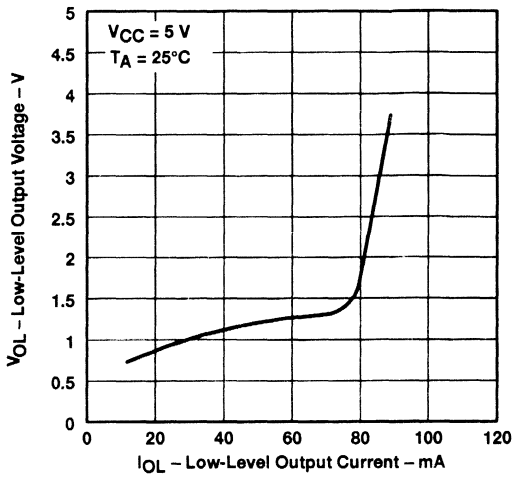


Figure 9

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

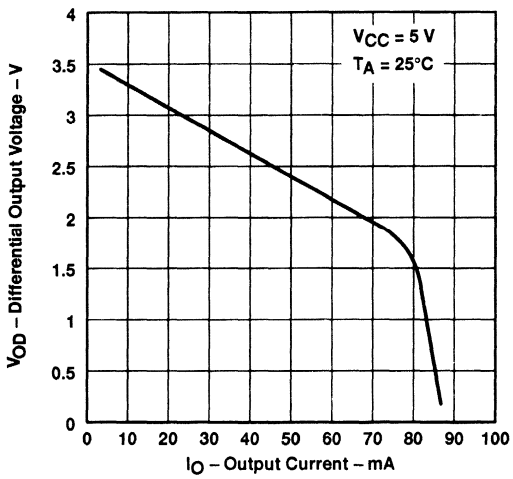


Figure 10

TYPICAL CHARACTERISTICS

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

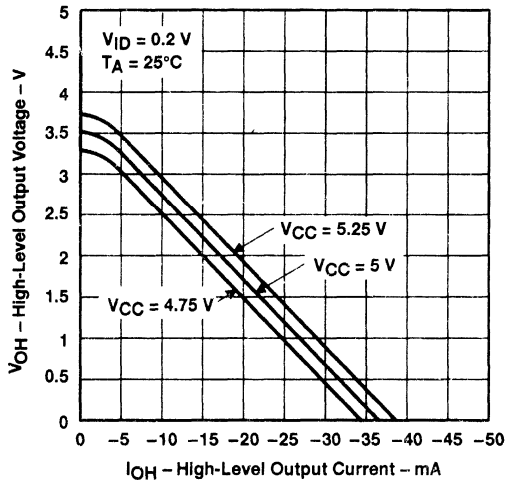
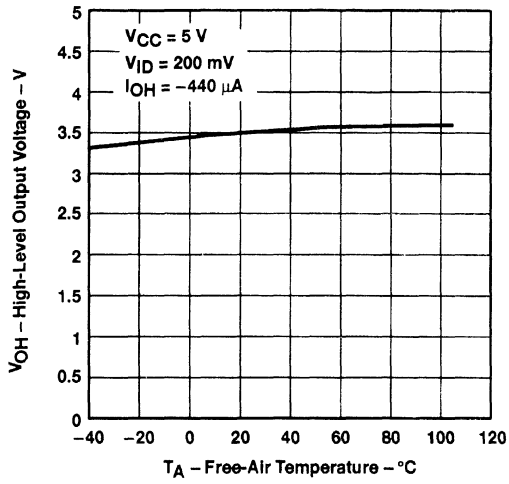


Figure 11

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE†



† Only the 0°C to 70°C portion of the curve applies to the SN75176B.

Figure 12

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

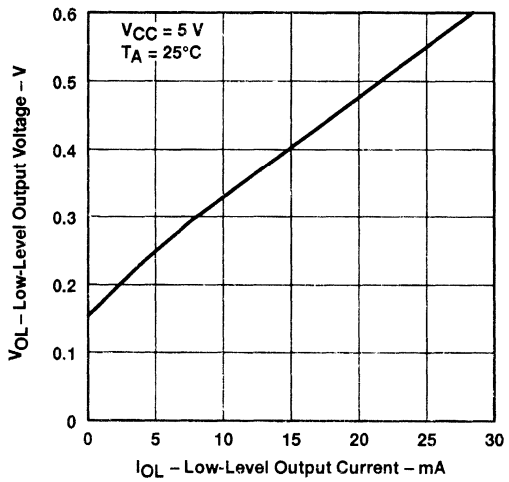


Figure 13

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

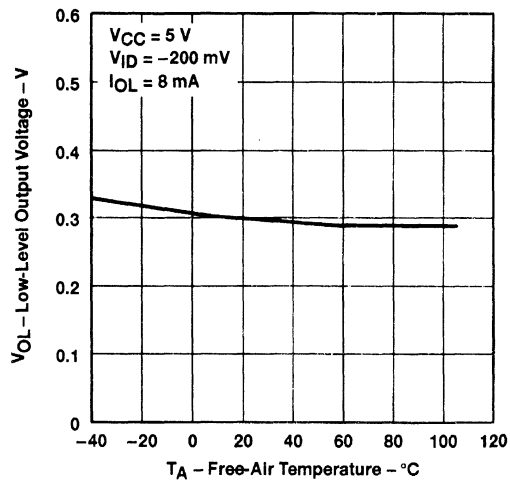


Figure 14

TYPICAL CHARACTERISTICS

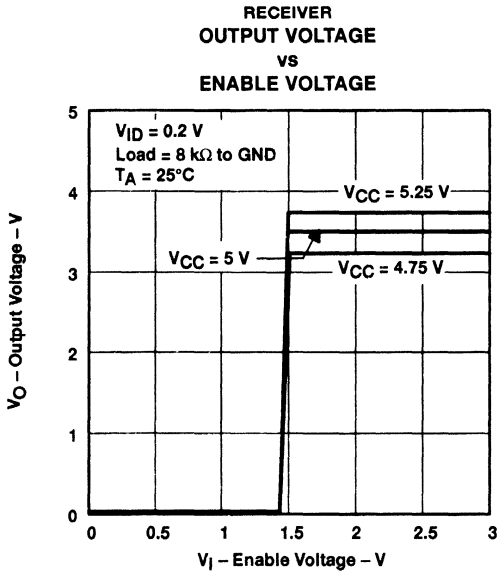


Figure 15

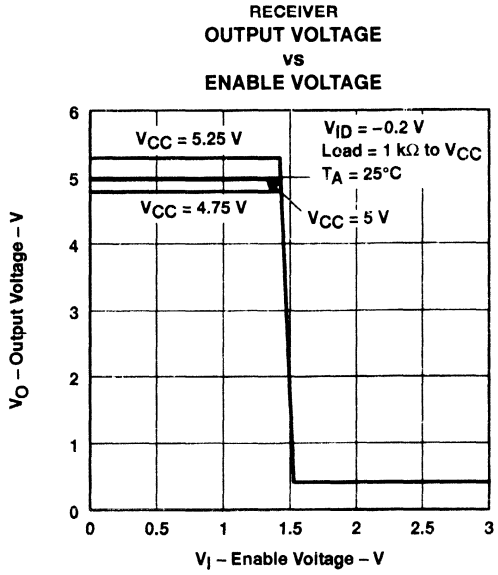


Figure 16

APPLICATION INFORMATION

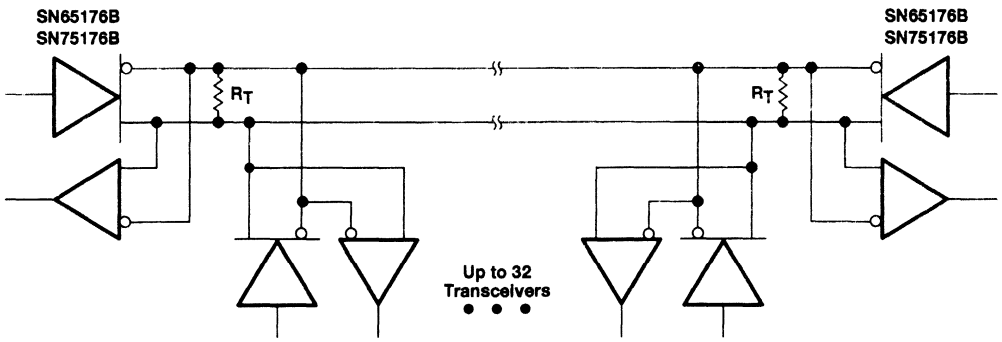


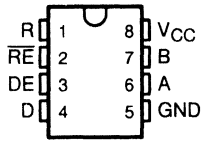
Figure 17. Typical Application Circuit

NOTE: The line should be terminated at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

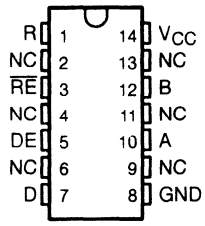
SGLS026A – MARCH 1989 – REVISED JUNE 1995

- **Bidirectional Transceiver**
- **Suitable for Most EIA Standards RS-422-A and RS-485 Applications**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **3-State Driver and Receiver Outputs**
- **Individual Driver and Receiver Enables**
- **Wide Positive and Negative Input/Output Bus Voltage Ranges**
- **Driver Output Capability . . . ±60 mA Max**
- **Thermal Shutdown Protection**
- **Driver Positive- and Negative-Current Limiting**
- **Receiver Input Sensitivity . . . ±200 mV**
- **Receiver Input Hysteresis . . . 50 mV Typ**
- **Operates From Single 5-V Supply**
- **Low Power Requirements**

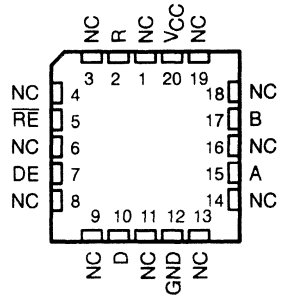
JG PACKAGE
(TOP VIEW)



W PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN95176B differential bus transceiver is a monolithic integrated circuit designed for bi-directional data communication on multipoint bus transmission lines. The transceiver is suitable for most RS-422-A and RS-485 applications to the extent of the specified data sheet characteristics and operating conditions.

The SN95176B combines a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive- and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

The SN95176B is characterized for operation from –40°C to 110°C.

Function Tables

DRIVER

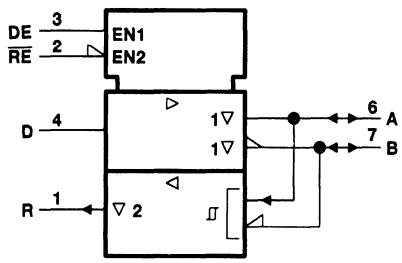
INPUT D	ENABLE DE	OUTPUTS A	OUTPUTS B
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z

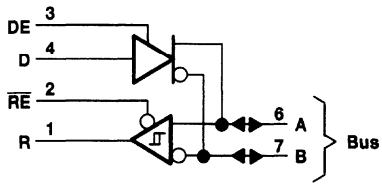
H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

logic symbol†

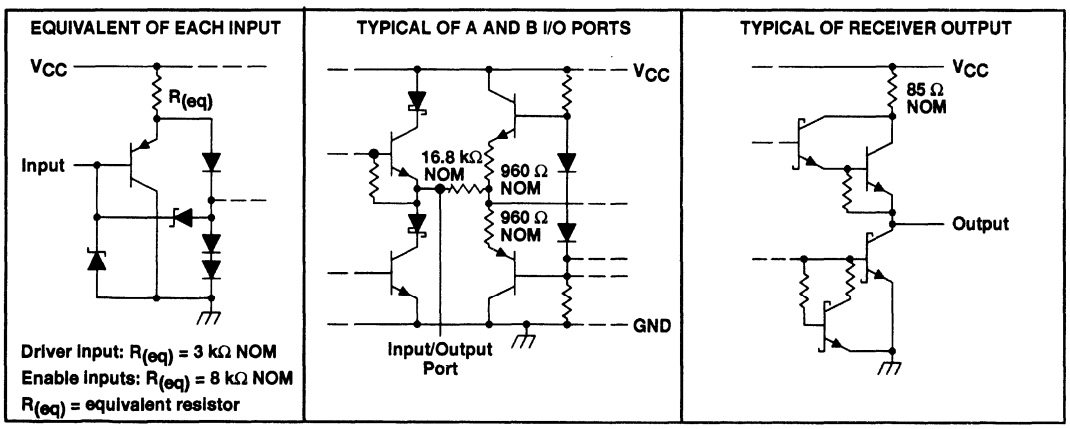


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Terminal numbers shown are for the JG package.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Voltage at any bus terminal ..... −10 V to 15 V
Enable input voltage, V_I ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −40°C to 110°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Case temperature for 60 seconds, T_C: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or W package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 110°C$ POWER RATING
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	440 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	336 mW
W	1000 mW	8.0 mW/°C	640 mW	520 mW	320 mW

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common-mode), V_I or V_{IC}				12	V
				−7	
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	µA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		−40		110	°C

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω, See Figure 1		2			V
		R_L = 54 Ω, See Figure 1		1.5	2.5	5	V
V_{OD3}	Differential output voltage	See Note 3			4		V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage§	R_L = 54 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage					3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current	Output disabled, See Note 4	V_O = 12 V			1	mA
			V_O = −7 V			−0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−400	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−250	mA
		V_O = 0				−150	
		V_O = V_{CC}				250	
		V_O = 12 V				250	
I_{CC}	Supply current (total package)	No load	Outputs enabled		42	70	mA
			Outputs disabled		26	35	

† The power-off measurement in EIA Standard RS-422-A applies to disabled outputs only and is not applied to combined inputs and outputs.
‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.
§ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

NOTES: 3. See EIA Standard RS-485 Figure 3.5, Test Termination Measurement 2.
4. This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The RS-422-A limit does not apply for a combined driver and receiver terminal.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω,	See Figure 3		15	22	ns
$t_{t(OD)}$	Differential output transition time				20	30	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 4		85	120	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 5		40	60	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 4		150	250	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 5		20	30	ns

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\lvert V_{OD1}\rvert$	V_o	V_o
$\lvert V_{OD2}\rvert$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\lvert V_{OD3}\rvert$	None	V_t (Test Termination Measurement 2)
$\Delta\lvert V_{OD}\rvert$	$\lvert\lvert V_t\rvert - \lvert\overline{V}_t\rvert\rvert$	$\lvert\lvert V_t\rvert - \lvert\overline{V}_t\rvert\rvert$
V_{OC}	$\lvert V_{os}\rvert$	$\lvert V_{os}\rvert$
$\Delta\lvert V_{OC}\rvert$	$\lvert V_{os} - \overline{V}_{os}\rvert$	$\lvert V_{os} - \overline{V}_{os}\rvert$
I_{OS}	$\lvert I_{sa}\rvert$, $\lvert I_{sb}\rvert$	None
I_O	$\lvert I_{xa}\rvert$, $\lvert I_{xb}\rvert$	I_{ia}, I_{ib}

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{IT-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Input hysteresis voltage ($V_{IT+} - V_{IT-}$)				50		mV
V_{IK}	Enable clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, See Figure 2	I_{OH} = −400 μA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 2	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input = 0 V, See Note 5	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance	V_I = 12 V		12			kΩ
I_{OS}	Short-circuit output current			−15		−85	mA
I_{CC}	Supply current (total package)	No load	Outputs enabled		42	70	mA
			Outputs disabled		26	35	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
NOTE 5: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_{ID} = 0 to 3 V, See Figure 6		21	35	ns
t_{PHL}	Propagation delay time, high- to low-level output			23	35	ns
t_{PZH}	Output enable time to high level	See Figure 7		10	20	ns
t_{PZL}	Output enable time to low level			12	20	ns
t_{PHZ}	Output disable time from high level	See Figure 7		20	35	ns
t_{PLZ}	Output disable time from low level			17	25	ns

PARAMETER MEASUREMENT INFORMATION

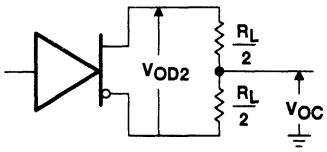


Figure 1. Driver V_{OD} and V_{OC}

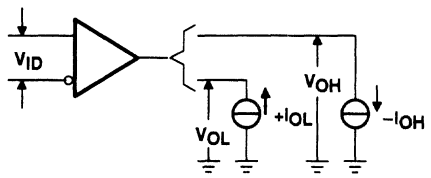
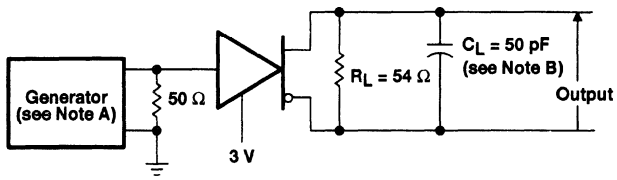
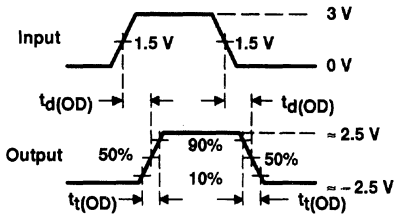


Figure 2. Receiver V_{OH} and V_{OL}



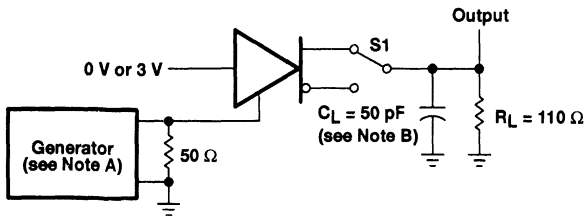
TEST CIRCUIT



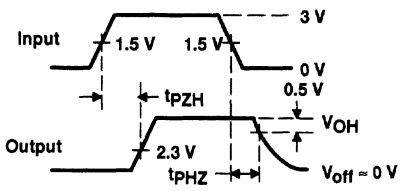
VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT

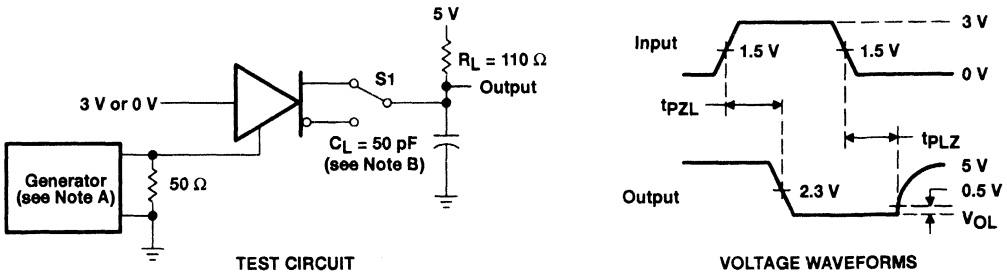


VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

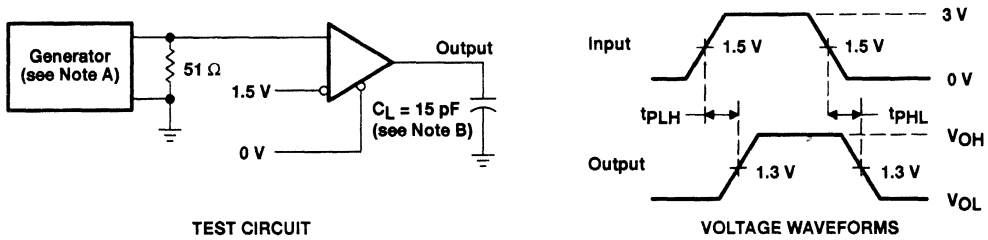
Figure 4. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

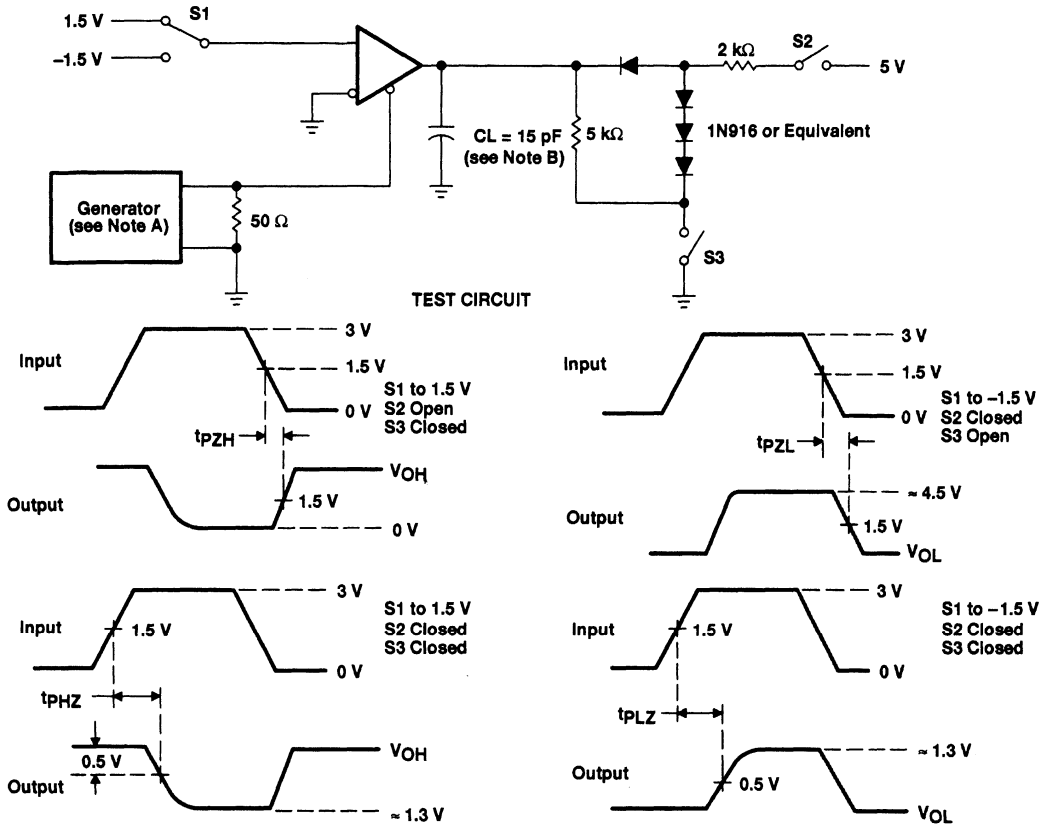
Figure 5. Driver Test Circuit and Voltage Waveforms



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 6. Receiver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 7. Receiver Test Circuit and Voltage Waveforms

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

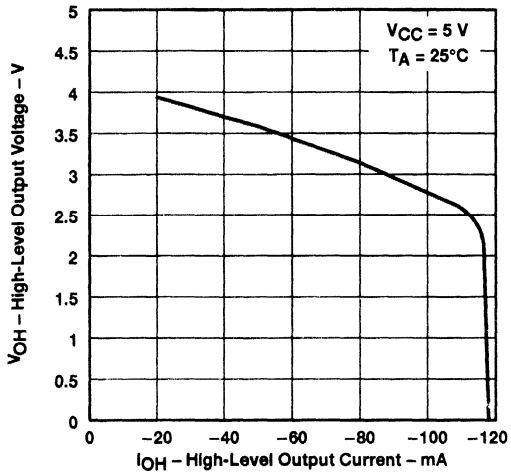


Figure 8

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

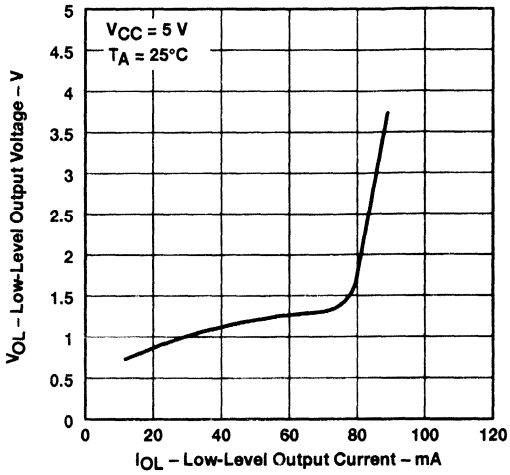


Figure 9

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

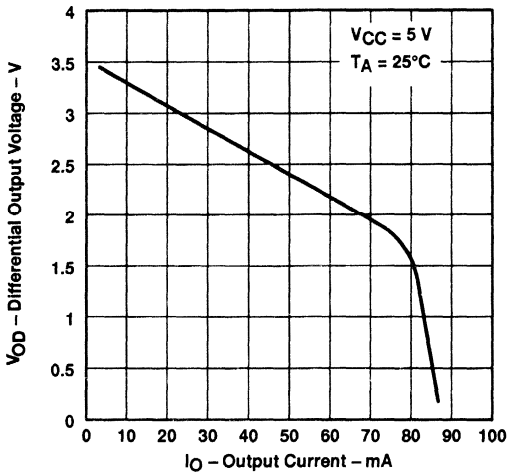


Figure 10

TYPICAL CHARACTERISTICS

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

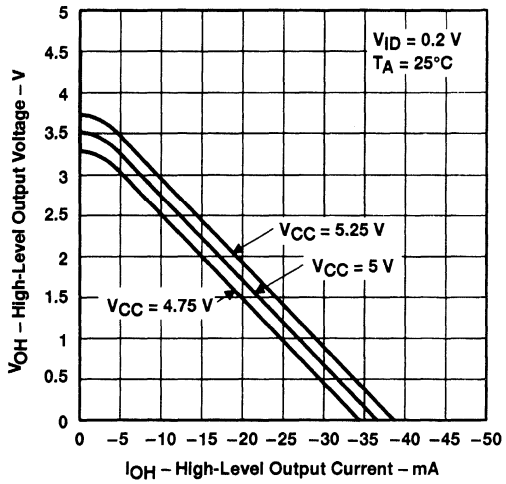


Figure 11

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

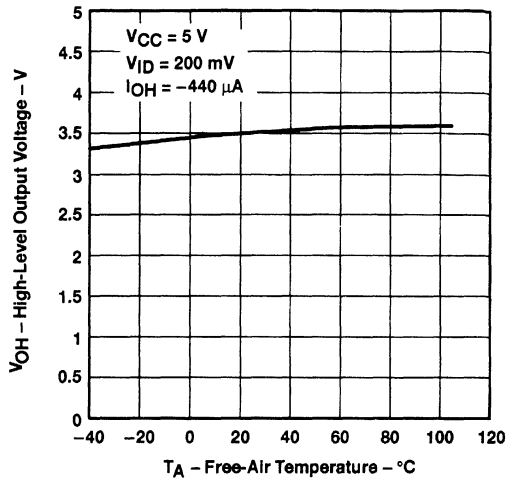


Figure 12

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

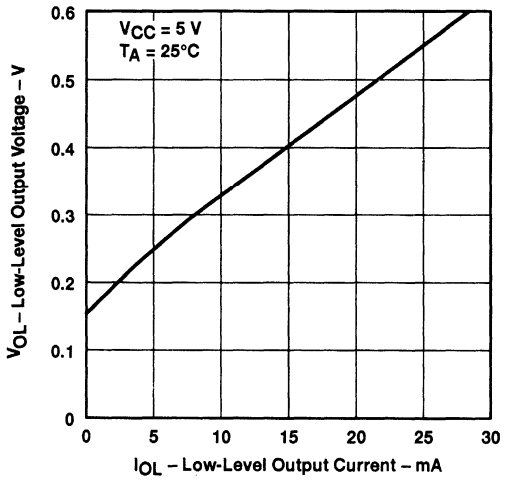


Figure 13

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

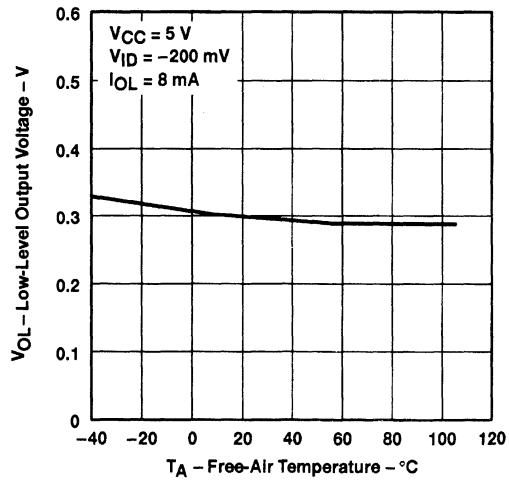


Figure 14

TYPICAL CHARACTERISTICS

RECEIVER
OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

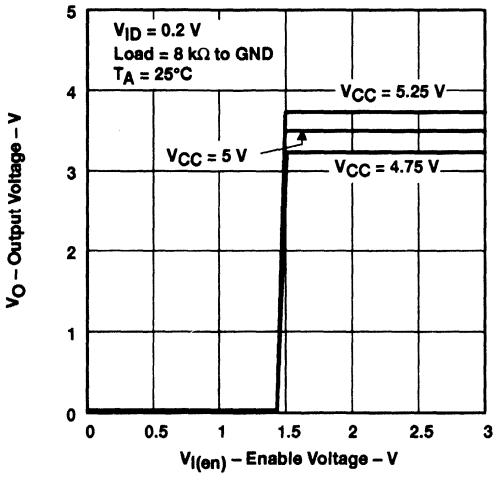


Figure 15

RECEIVER
OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

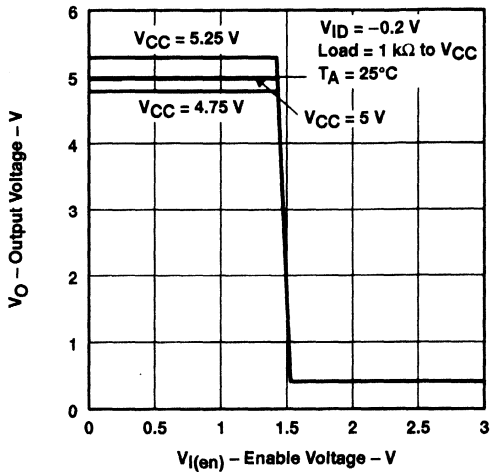


Figure 16

APPLICATION INFORMATION

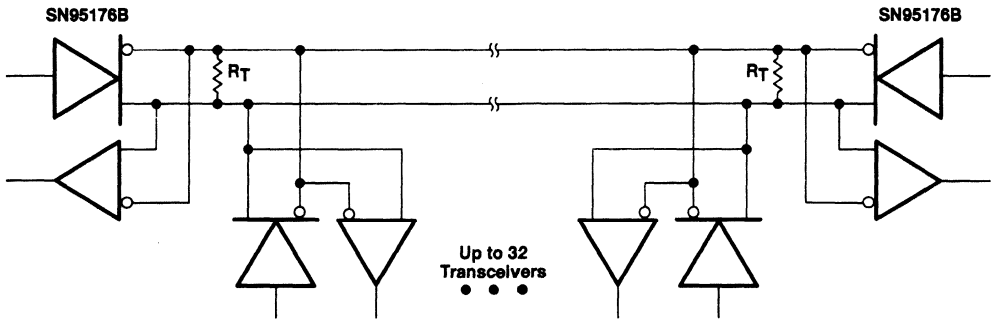


Figure 17. Typical Application Circuit

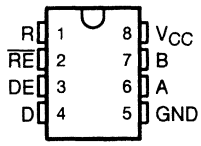
NOTE A: The line should terminate at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B
DIFFERENTIAL BUS TRANSCEIVERS

SLLS040E – AUGUST 1987 – REVISED MAY 1995

- **Meet or Exceed the Requirements of ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendations V.11 and X.27**
- **Designed and Tested to Operate at Data Rates up to 35 MBaud**
- **SN65ALS176 Operating Temperature −40°C to 85°C**
- **Three Skew Limits Available:**
  - **'ALS176 . . . 10 ns**
  - **'ALS176A . . . 7.5 ns**
  - **'ALS176B . . . 5 ns**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Low Supply Current Requirements 30 mA Max**
- **Wide Positive and Negative Input/Output Bus Voltage Ranges**
- **Thermal Shutdown Protection**
- **Driver Positive- and Negative-Current Limiting**
- **Receiver Input Hysteresis**
- **Glitch-Free Power-Up and Power-Down Protection**
- **Receiver Open-Circuit Fail-Safe Design**

D OR P PACKAGE
(TOP VIEW)



Function Tables

DRIVER

INPUT D	ENABLE DE	OUTPUTS A	OUTPUTS B
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS A–B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Inputs open	L	H

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

AVAILABLE OPTIONS

T_A	$t_{sk(LIM)}$†	PACKAGE: SMALL OUTLINE (D)‡	PACKAGE: PLASTIC DIP (P)
0°C to 70°C	10	SN75ALS176D	SN75ALS176P
	7.5	SN75ALS176AD	SN75ALS176AP
	5	SN75ALS176BD	SN75ALS176BP
−40°C to 85°C	15	SN65ALS176D	SN65ALS176P

† $t_{sk(LIM)}$ This is the maximum range that the driver or receiver delay times will vary over temperature, V_{CC}, and process (device to device).

‡ The D package is available taped and reeled. Add the suffix R to the device type (e.g., SN75ALS176DR).

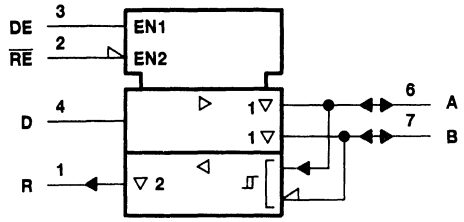
description

The SN65ALS176 and SN75ALS176 series differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendations V.11 and X.27.

The SN65ALS176 and SN75ALS176 series combine a 3-state, differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. This port features wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

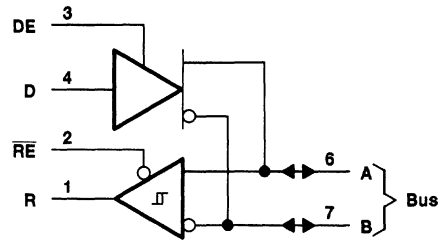
The SN65ALS176 is characterized for operation from −40°C to 85°C, and the SN75ALS176 series is characterized for operation from 0°C to 70°C.

logic symbol†

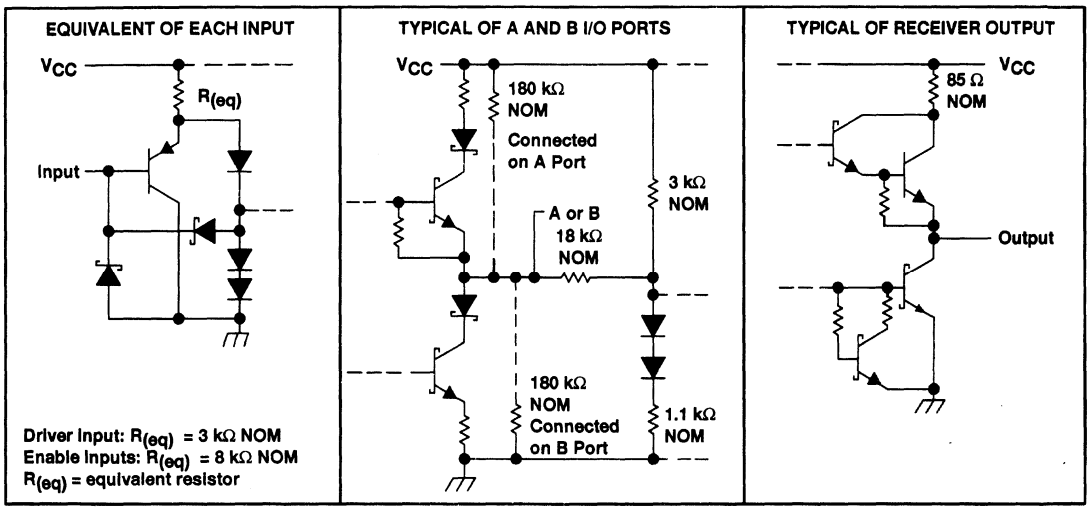


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Voltage range at any bus terminal ..... −7 V to 12 V
Enable input voltage, V_I ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65ALS176 ..... −40°C to 85°C
SN75ALS176 series ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Input voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12	V
				−7	
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A	SN65ALS176	−40		85	°C
	SN75ALS176	0		70	

NOTE 2: Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_O	Output voltage	$I_O = 0$		0		6	V
$\lvert V_{OD1} \rvert$	Differential output voltage	$I_O = 0$		1.5		6	V
$\lvert V_{OD2} \rvert$	Differential output voltage	$R_L = 100\ \Omega$,	See Figure 1	1/2 V_{OD1} or 2§			V
		$R_L = 54\ \Omega$,	See Figure 1	1.5	2.5	5	V
V_{OD3}	Differential output voltage	$V_{test} = -7$ V to 12 V,	See Figure 2	1.5		5	V
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of differential output voltage¶	$R_L = 54\ \Omega$ or 100 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage					3 −1	V
$\Delta\lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage¶					±0.2	V
I_O	Output current	Outputs disabled, See Note 3	$V_O = 12$ V			1	mA
			$V_O = -7$ V			−0.8	
I_{IH}	High-level input current	$V_I = 2.4$ V				20	µA
I_{IL}	Low-level input current	$V_I = 0.4$ V				−400	µA
I_{OS}	Short-circuit output current	$V_O = -4$ V	SN65ALS176			−250	mA
		$V_O = -6$ V	SN75ALS176				
		$V_O = 0$				−150	
		$V_O = V_{CC}$				250	
		$V_O = 8$ V					
I_{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

† The power-off measurement in ANSI Standard EIA/TIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
‡ All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.
§ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
¶ $\Delta\lvert V_{OD} \rvert$ and $\Delta\lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from one logic state to the other.

NOTE 3: This applies for both power on and power off; refer to ANSI standard RS-485 for exact conditions. The EIA/TIA-422-B limit does not apply for a combined driver and receiver terminal.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

SN65ALS176

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω, C_L = 50 pF, See Figure 3			15	ns
$t_{sk(p)}$	Pulse skew‡			0	2	ns
$t_{t(OD)}$	Differential output transition time			8		ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω, C_L = 50 pF, See Figure 4			80	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω, C_L = 50 pF, See Figure 5			30	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω, C_L = 50 pF, See Figure 4			50	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω, C_L = 50 pF, See Figure 5			30	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel.

SN75ALS176, SN75ALS176A, SN75ALS176B

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	'ALS176	R_L = 54 Ω, C_L = 50 pF, See Figure 3	3	8	13	ns
		'ALS176A		4	7	11.5	
		'ALS176B		5	8	10	
$t_{sk(p)}$	Pulse skew‡		R_L = 54 Ω, C_L = 50 pF, See Figure 3		0	2	ns
$t_{sk(lim)}$	Skew limit§	'ALS176	R_L = 54 Ω, C_L = 50 pF, See Figure 3			10	ns
		'ALS176A				7.5	
		'ALS176B				5	
$t_{t(OD)}$	Differential output transition time		R_L = 54 Ω, C_L = 50 pF, See Figure 3		8		ns
t_{PZH}	Output enable time to high level		R_L = 110 Ω, C_L = 50 pF, See Figure 4		23	50	ns
t_{PZL}	Output enable time to low level		R_L = 110 Ω, C_L = 50 pF, See Figure 5		14	20	ns
t_{PHZ}	Output disable time from high level		R_L = 110 Ω, C_L = 50 pF, See Figure 4		20	35	ns
t_{PLZ}	Output disable time from low level		R_L = 110 Ω, C_L = 50 pF, See Figure 5		8	17	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel.
§ Skew limit is the maximum difference in propagation delay times between any two channels of one device.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	EIA/TIA-422-B	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\lvert V_{OD1} \rvert$	V_o	V_o
$\lvert V_{OD2} \rvert$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\lvert V_{OD3} \rvert$	None	V_t (test termination measurement 2)
$\Delta \lvert V_{OD} \rvert$	$\lvert\lvert V_t \rvert - \lvert \overline{V}_t \rvert\rvert$	$\lvert\lvert V_t \rvert - \lvert \overline{V}_t \rvert\rvert$
V_{OC}	$\lvert V_{os} \rvert$	$\lvert V_{os} \rvert$
$\Delta \lvert V_{OC} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$
I_{OS}	$\lvert I_{sa} \rvert$, $\lvert I_{sb} \rvert$	None
I_O	$\lvert I_{xa} \rvert$, $\lvert I_{xb} \rvert$	I_{ia}, I_{ib}

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{IT-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)				60		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, See Figure 6	I_{OH} = −400 µA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 6	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	µA
V_I	Line input current	Other input = 0 V, See Note 4	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level-enable input current	V_{IH} = 2.7 V				20	µA
I_{IL}	Low-level-enable input current	V_{IL} = 0.4 V				−100	µA
r_I	Input resistance			12	20		kΩ
I_{OS}	Short-circuit output current	V_{ID} = 200 mV,	V_O = 0	−15		−85	mA
I_{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less-positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
NOTE 4: This applies for both power on and power off. Refer to ANSI Standard RS-485 for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

SN65ALS176

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{pd}	Propagation time		V_{ID} = −1.5 V to 1.5 V, See Figure 7 C_L = 15 pF,			25	ns
$t_{sk(p)}$	Pulse skew§				0	2	ns
$t_{sk(lim)}$	Skew limit¶	'ALS176	R_L = 54 Ω, See Figure 3 C_L = 50 pF,			10	ns
		'ALS176A				7.5	
		'ALS176B				5	
t_{PZH}	Output enable time to high level		C_L = 15 pF, See Figure 8		11	18	ns
t_{PZL}	Output enable time to low level				11	18	ns
t_{PHZ}	Output disable time from high level					50	ns
t_{PLZ}	Output disable time from low level					30	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel.
¶ Skew limit is the maximum difference in propagation delay times between any two channels of one device.

SN75ALS176, SN75ALS176A, SN75ALS176B

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{pd}	Propagation time	'ALS176	V_{ID} = −1.5 V to 1.5 V, C_L = 15 pF, See Figure 7	9	14	19	ns
		'ALS176A		10.5	14	18	
		'ALS176B		11.5	13	16.5	
$t_{sk(p)}$	Pulse skew‡				0	2	ns
t_{PZH}	Output enable time to high level		C_L = 15 pF, See Figure 8		7	14	ns
t_{PZL}	Output enable time to low level				20	35	ns
t_{PHZ}	Output disable time from high level				20	35	ns
t_{PLZ}	Output disable time from low level				8	17	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel.

PARAMETER MEASUREMENT INFORMATION

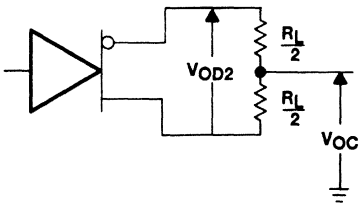


Figure 1. Driver V_{OD2} and V_{OC}

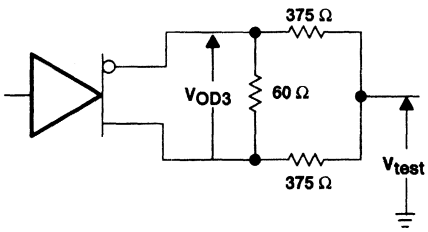
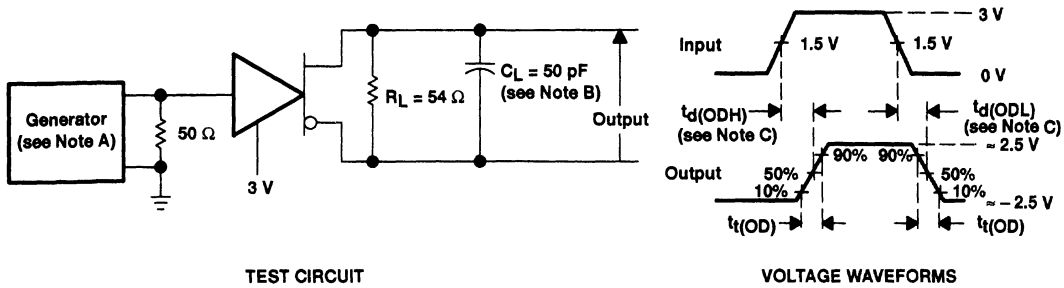


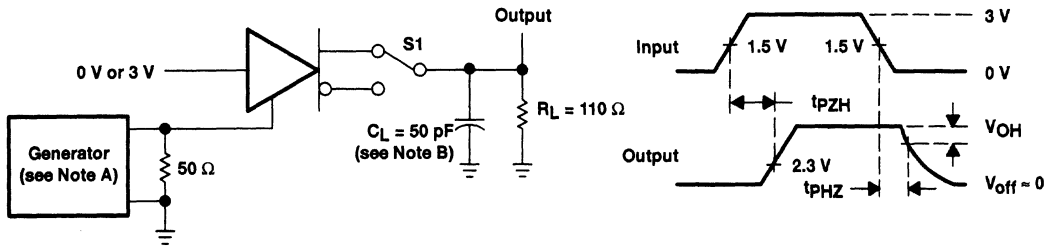
Figure 2. Driver V_{OD3}

PARAMETER MEASUREMENT INFORMATION



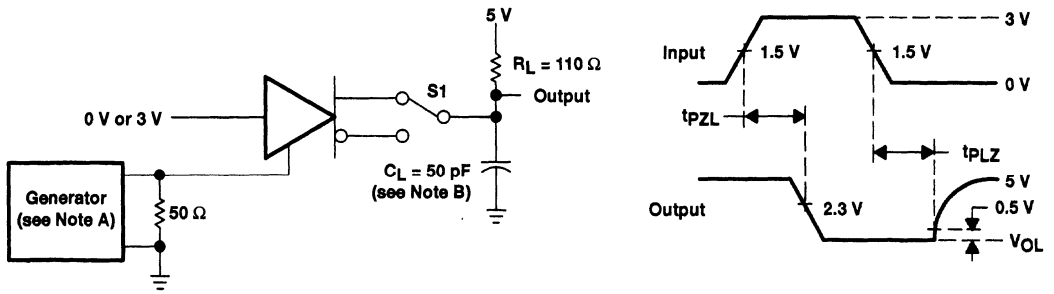
TEST CIRCUIT VOLTAGE WAVEFORMS

Figure 3. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT VOLTAGE WAVEFORMS

Figure 4. Driver Test Circuit and Voltage Waeforms



TEST CIRCUIT VOLTAGE WAVEFORMS

Figure 5. Driver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. $t_{d(OD)} = t_{d(ODH)}$ or $t_{d(ODL)}$

PARAMETER MEASUREMENT INFORMATION

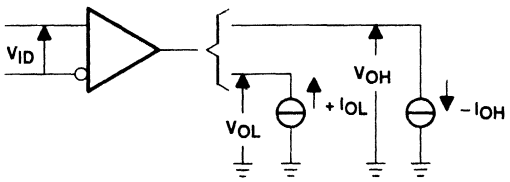
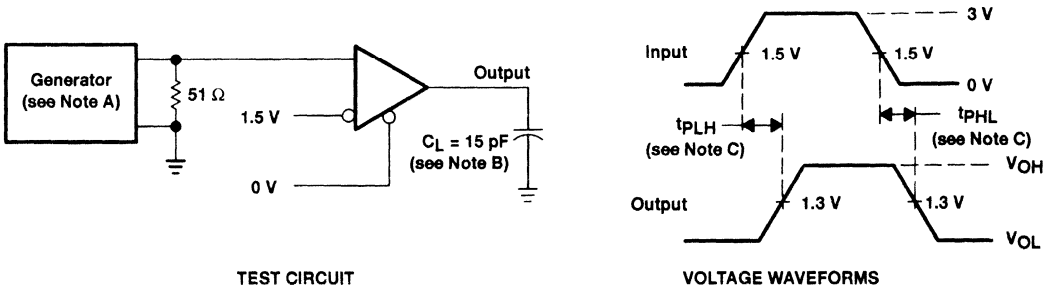


Figure 6. Receiver V_{OH} and V_{OL} Test Circuit



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. $t_{pd} = t_{PLH}$ or t_{PHL}

Figure 7. Receiver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

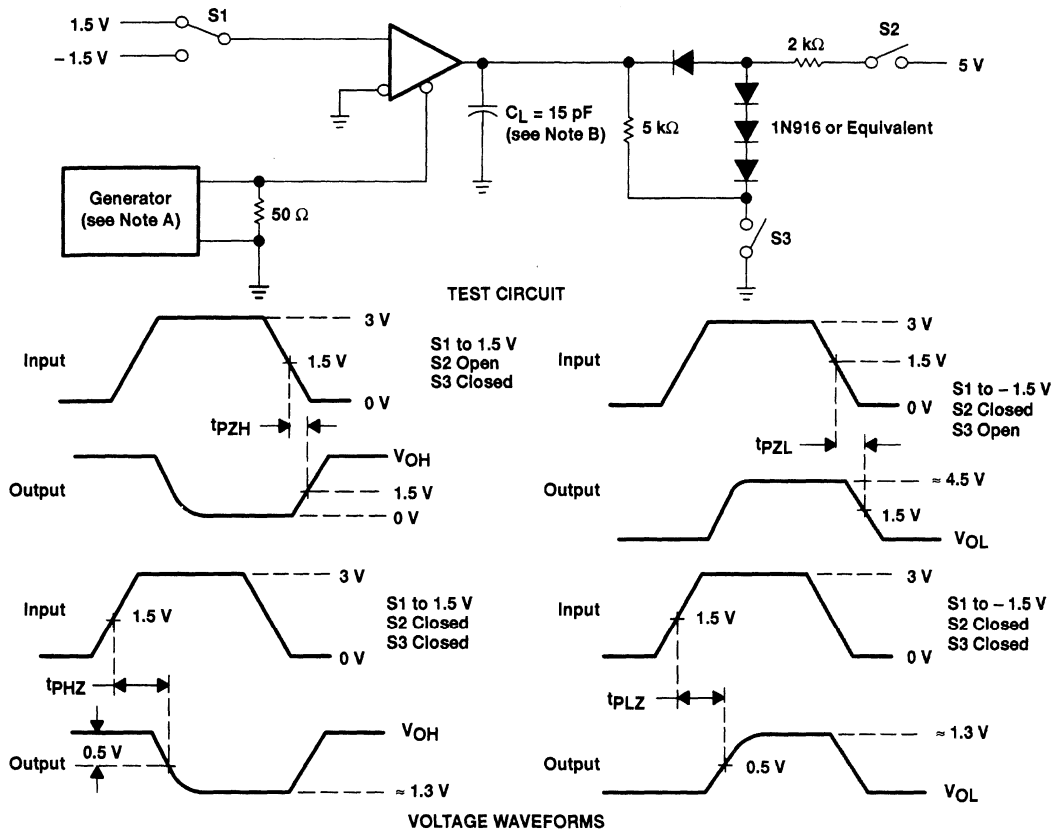


Figure 8. Receiver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

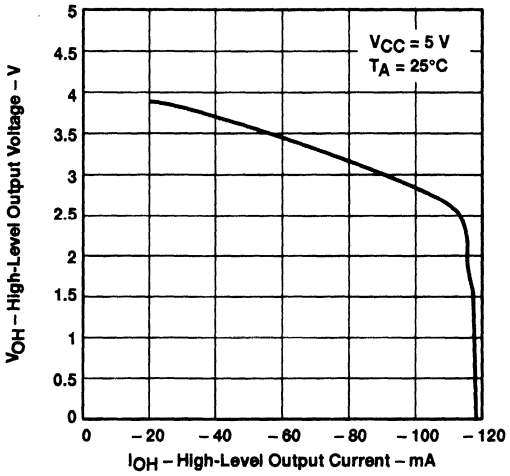


Figure 9

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

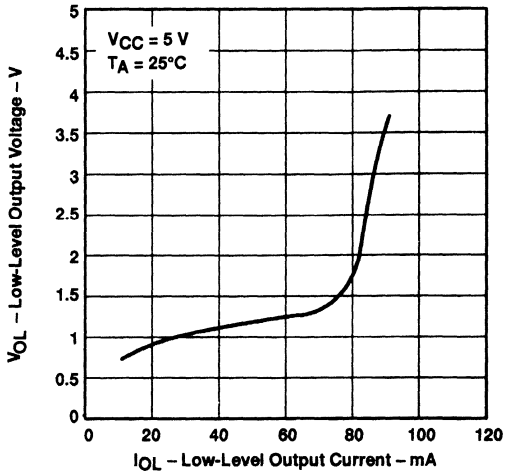


Figure 10

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

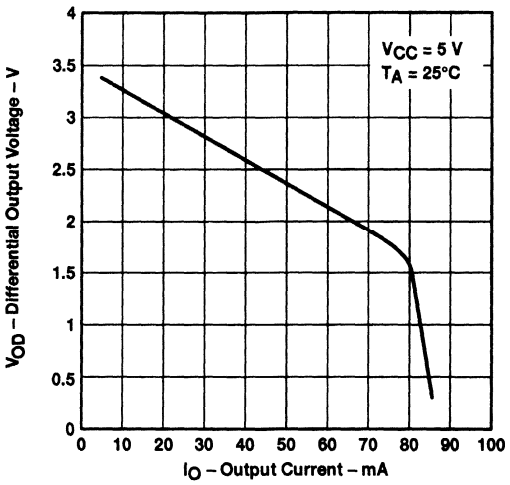


Figure 11

TYPICAL CHARACTERISTICS

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

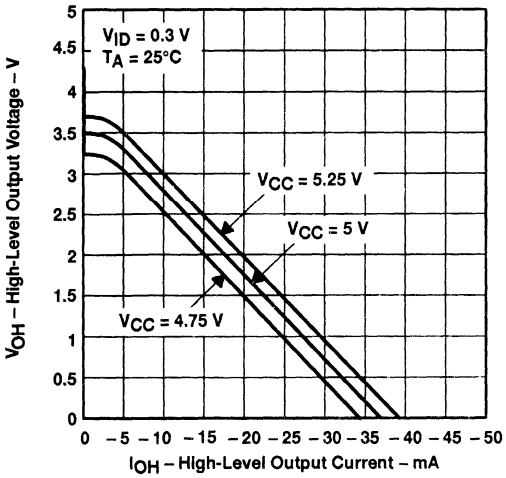


Figure 12

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

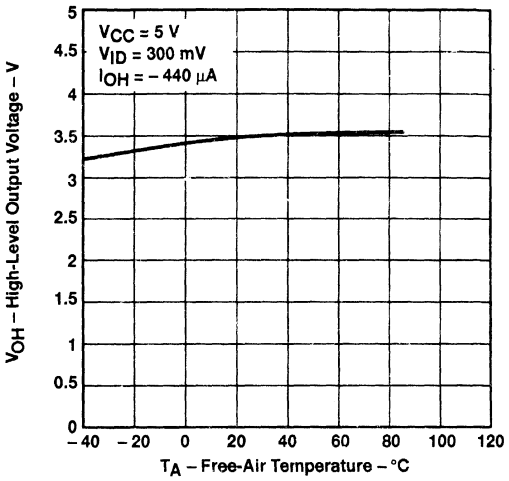


Figure 13

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

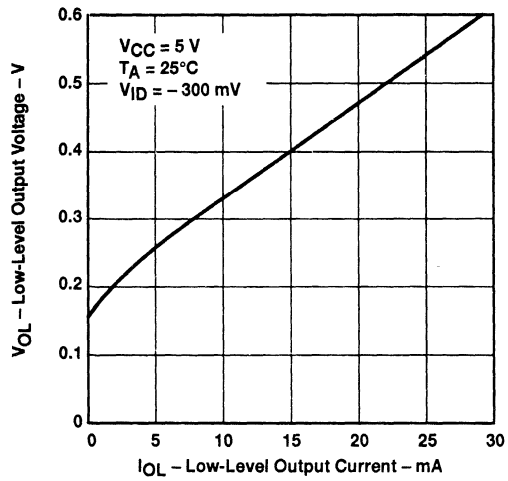


Figure 14

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

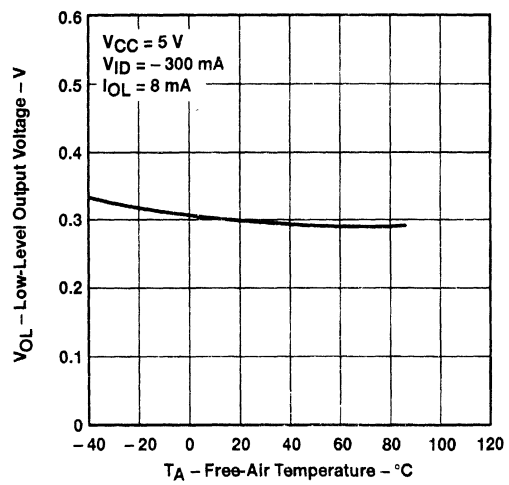


Figure 15

TYPICAL CHARACTERISTICS

RECEIVER
OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

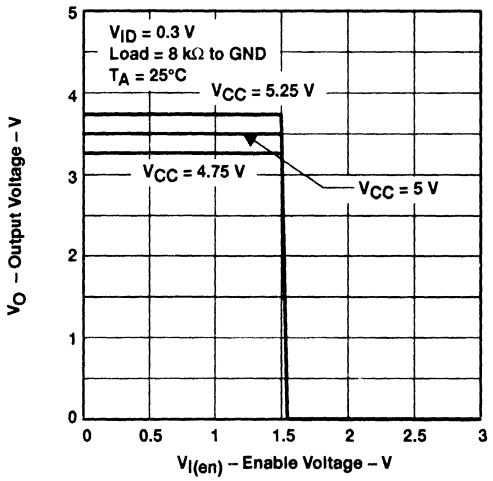


Figure 16

RECEIVER
OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

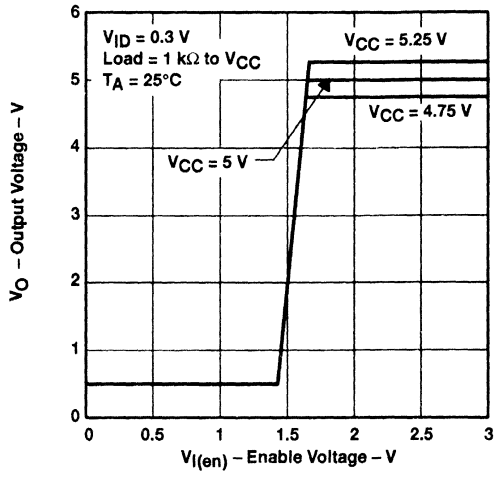
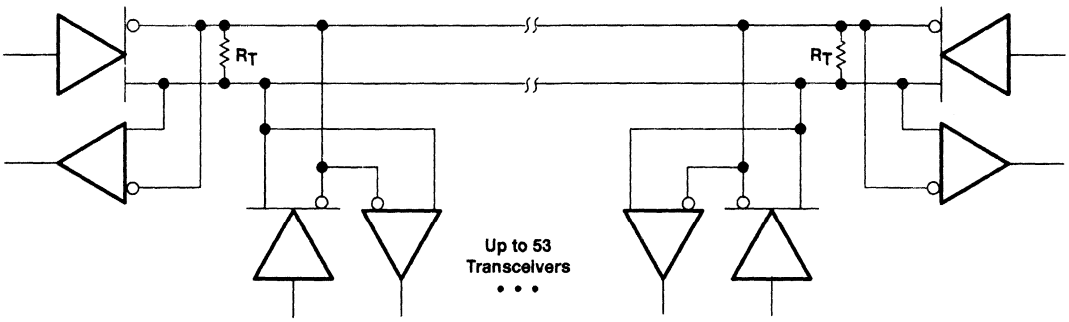


Figure 17

APPLICATION INFORMATION



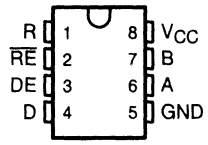
NOTE A: The line should terminate at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

Figure 18. Typical Application Circuit

SLLS067C – AUGUST 1990 – REVISED MAY 1995

- Bidirectional Transceiver
- Meet or Exceed the Requirements of ANSI Standard RS-485 and ISO 8482:1987(E)
- High-Speed Low-Power LinBICMOS™ Circuitry
- Designed for High-Speed Operation in Both Serial and Parallel Applications
- Low Skew
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Very Low Disabled Supply-Current Requirements . . . 200 μA Maximum
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capacity . . . ±60 mA
- Thermal-Shutdown Protection
- Driver Positive-and Negative-Current Limiting
- Open-Circuit Fail-Safe Receiver Design
- Receiver Input Sensitivity . . . ±200 mV Max
- Receiver Input Hysteresis . . . 50 mV Typ
- Operate From a Single 5-V Supply
- Glitch-Free Power-Up and Power-Down Protection

D, JG, OR P PACKAGE
(TOP VIEW)



Function Tables

DRIVER

INPUT D	ENABLE DE	OUTPUTS A	OUTPUTS B
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS A–B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

description

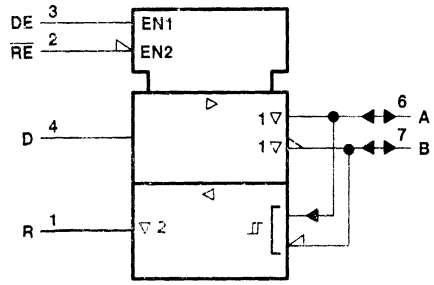
The SN55LBC176, SN65LBC176, and SN75LBC176 differential bus transceivers are monolithic, integrated circuits designed for bidirectional data communication on multipoint bus-transmission lines. They are designed for balanced transmission lines and meet ANSI Standard RS-485 and ISO 8482:1987(E).

The SN65LBC176 and SN75LBC176 combine a 3-state, differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can externally connect together to function as a direction control. The driver differential outputs and the receiver differential inputs connect internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or $V_{CC} = 0$. This port features wide positive and negative common-mode voltage ranges, making the device suitable for party-line applications. Very low device supply current can be achieved by disabling the driver and the receiver. Both the driver and receiver are available as cells in the Texas Instruments LinASIC™ Library.

These transceivers are suitable for ANSI Standard RS-485 and ISO 8482:1987 (E) applications to the extent that they are specified in the operating conditions and characteristics section of this data sheet. Certain limits contained in the ANSI Standard RS-485 and ISO 8482:1987 (E) are not met or cannot be tested over the entire military temperature range.

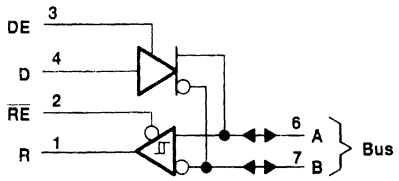
The SN55LBC176 is characterized for operation from −55°C to 125°C. The SN65LBC176 is characterized for operation from −40°C to 85°C, and the SN75LBC176 is characterized for operation from 0°C to 70°C.

logic symbol†

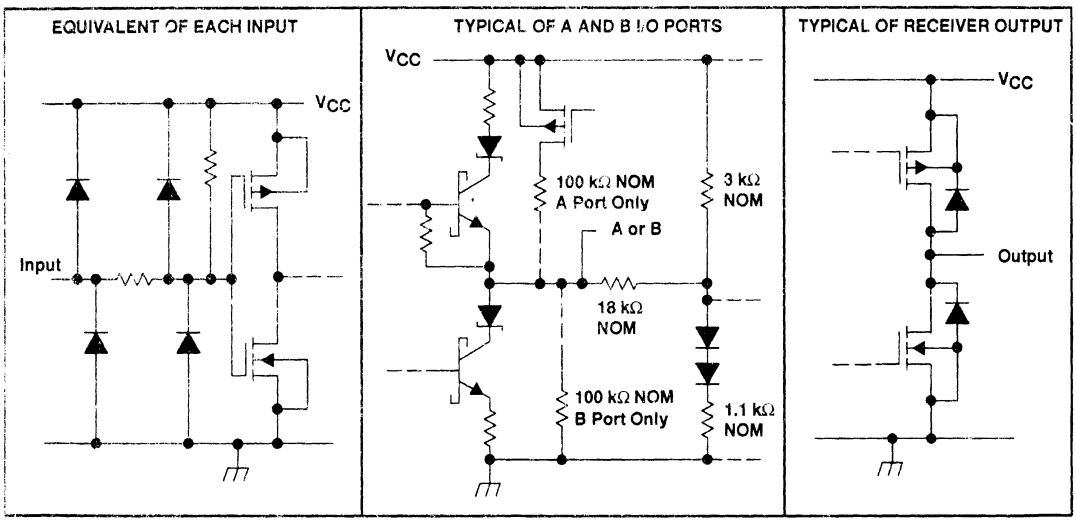


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Voltage range at any bus terminal ..... −10 V to 15 V
Enable input voltage, V_I ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN55LBC176 ..... −55°C to 125°C
SN65LBC176 ..... −40°C to 85°C
SN75LBC176 ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	—
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	—

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	SN55LBC176	4.5	5	5.5	V
	SN65/75LBC176	4.75	5	5.25	
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12	V
				−7	
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	µA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A	SN55LBC176	−55		125	°C
	SN65LBC176	−40		85	
	SN75LBC176	0		70	

NOTE 2: Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_O	Output voltage	$I_O = 0$			0	6	V
$\lvert V_{OD1} \rvert$	Differential output voltage	$I_O = 0$			1.5	6	V
$\lvert V_{OD2} \rvert$	Differential output voltage	$R_L = 54\ \Omega$, See Note 3	See Figure 1,	55LBC176	1.1		V
				65LBC176	1.1		
				75LBC176	1.5	5	
V_{OD3}	Differential output voltage	$V_{test} = -7$ V to 12 V, See Note 3	See Figure 2,	55LCB176	1.1		V
				65LBC176	1.1		
				75LBC176	1.5	5	
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of differential output voltage†	$R_L = 54\ \Omega$ or 100 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage					3	V
						−1	
$\Delta\lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage†					±0.2	V
I_O	Output current	Output disabled, See Note 4	$V_O = 12$ V			1	mA
			$V_O = -7$ V			−0.8	
I_{IH}	High-level input current	$V_I = 2.4$ V				−100	µA
I_{IL}	Low-level input current	$V_I = 0.4$ V				−100	µA
I_{OS}	Short-circuit output current	$V_O = -7$ V				−250	mA
		$V_O = 0$				−150	
		$V_O = V_{CC}$				250	
		$V_O = 12$ V					
I_{CC}	Supply current	$V_I = 0$ or V_{CC}, No load	Receiver disabled and driver enabled	55LBC176		1.75	mA
				65LBC176		1.5	
				75LBC176			
			Receiver and driver disabled	55LBC176		0.25	
				65LBC176			
				75LBC176		0.2	

† $\Delta\lvert V_{OD} \rvert$ and $\Delta\lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input changes from a high level to a low level.

NOTES: 3. This device meets the ANSI Standard RS-485 V_{OD} requirements above 0°C only.
4. This applies for both power on and off; refer to ANSI Standard RS-485 for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	SN55LBC176			SN65LBC176 SN75LBC176			UNIT
			MIN	TYP	MAX	MIN	TYP†	MAX	
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω, C_L = 50 pF, See Figure 3	8		31	8		25	ns
$t_{t(OD)}$	Differential output transition time			12			12		ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{d(ODH)} - t_{d(ODL)} \rvert$)				6		0	6	ns
t_{PLH}	Propagation time, low- to high-level single-ended output							26	ns
t_{PHL}	Propagation time, high- to low-level single-ended output							26	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω, See Figure 4			65			35	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω, See Figure 5			65			35	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω, See Figure 4			105			60	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω, See Figure 5			105			35	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-485
V_O	V_{oa}, V_{ob}
$\lvert V_{OD1} \rvert$	V_o
$\lvert V_{OD2} \rvert$	V_t (R_L = 54 Ω)
$\lvert V_{OD3} \rvert$	V_t (test termination measurement 2)
$\Delta \lvert V_{OD} \rvert$	$\lvert\lvert V_t \rvert - \lvert \overline{V}_t \rvert\rvert$
V_{OC}	$\lvert V_{os} \rvert$
$\Delta \lvert V_{OC} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$
I_{OS}	None
I_O	I_{ia}, I_{ib}

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA				0.2	V
V_{IT-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA		−0.2‡			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$) (see Figure 4)					50		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA					−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, See Figure 6	I_{OH} = −400 μA,		2.7			V
V_{OL}	Low-level output voltage	V_{ID} = 200 mV, See Figure 6	I_{OL} = 8 mA,				0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V					±20	μA
I_I	Line input current	Other input = 0 V, See Note 5	V_I = 12 V				1	mA
			V_I = −7 V				−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V					−100	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V					−100	μA
r_I	Input resistance				12			kΩ
I_{CC}	Supply current	V_I = 0 or V_{CC}, No load	Receiver enabled and driver disabled				3.9	mA
			Receiver and driver disabled	SN55LBC176			0.25	mA
				SN65LBC176				
				SN75LBC176			0.2	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
NOTE 5: This applies for both power on and power off. Refer to ANSI Standard RS-485 for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 15 pF

PARAMETER		TEST CONDITIONS	SN55LBC176		SN65LBC176 SN75LBC176			UNIT
			MIN	MAX	MIN	TYP†	MAX	
t_{PLH}	Propagation delay time, low- to high-level single-ended output	V_{ID} = −1.5 V to 1.5 V, See Figure 7	11	37	11		33	ns
t_{PHL}	Propagation delay time, high- to low-level single-ended output		11	37	11		33	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{d(ODH)} - t_{d(ODL)} \rvert$)			6		3	6	ns
t_{PZH}	Output enable time to high level	See Figure 8		35			35	ns
t_{PZL}	Output enable time to low level			35			30	ns
t_{PHZ}	Output disable time from high level	See Figure 8		35			35	ns
t_{PLZ}	Output disable time from low level			35			30	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

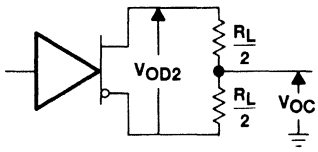


Figure 1. Driver V_{OD} and V_{OC}

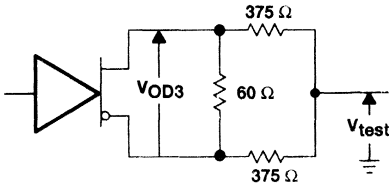
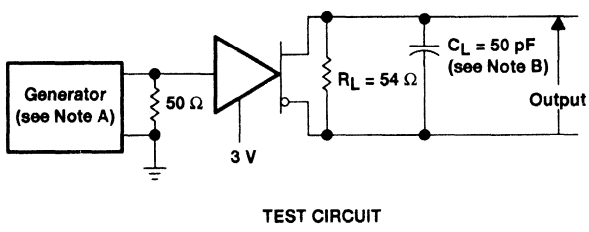


Figure 2. Driver V_{OD3}



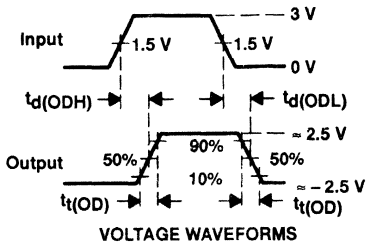
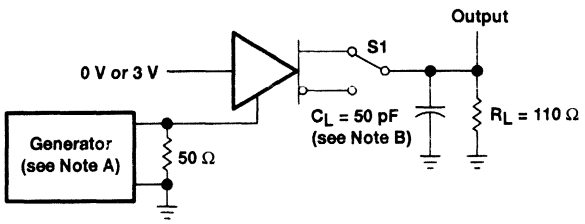


Figure 3. Driver Test Circuit and Voltage Waveforms



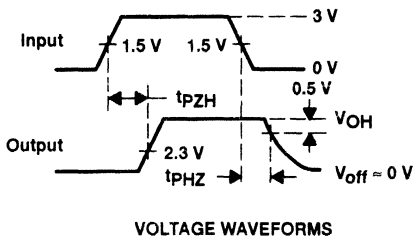
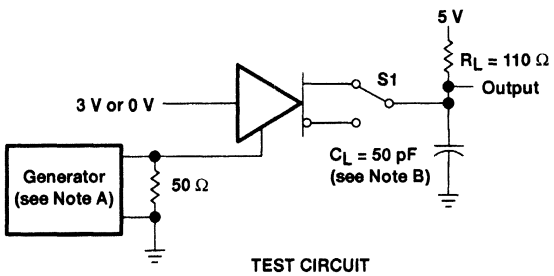


Figure 4. Driver Test Circuit and Voltage Waveforms



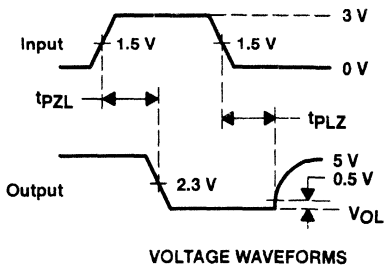


Figure 5. Driver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

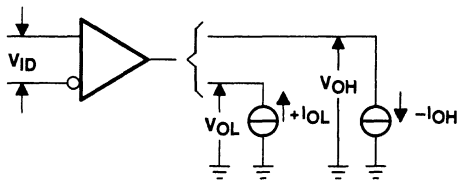
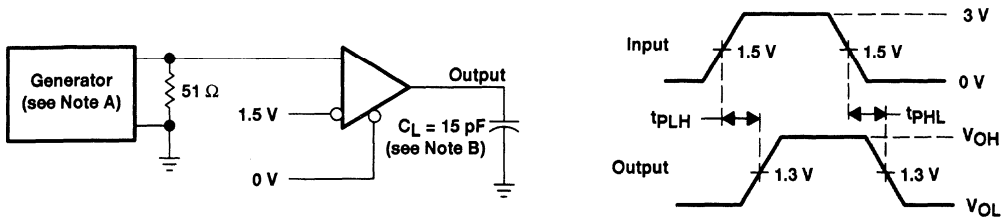


Figure 6. Receiver V_{OH} and V_{OL}



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 7. Receiver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

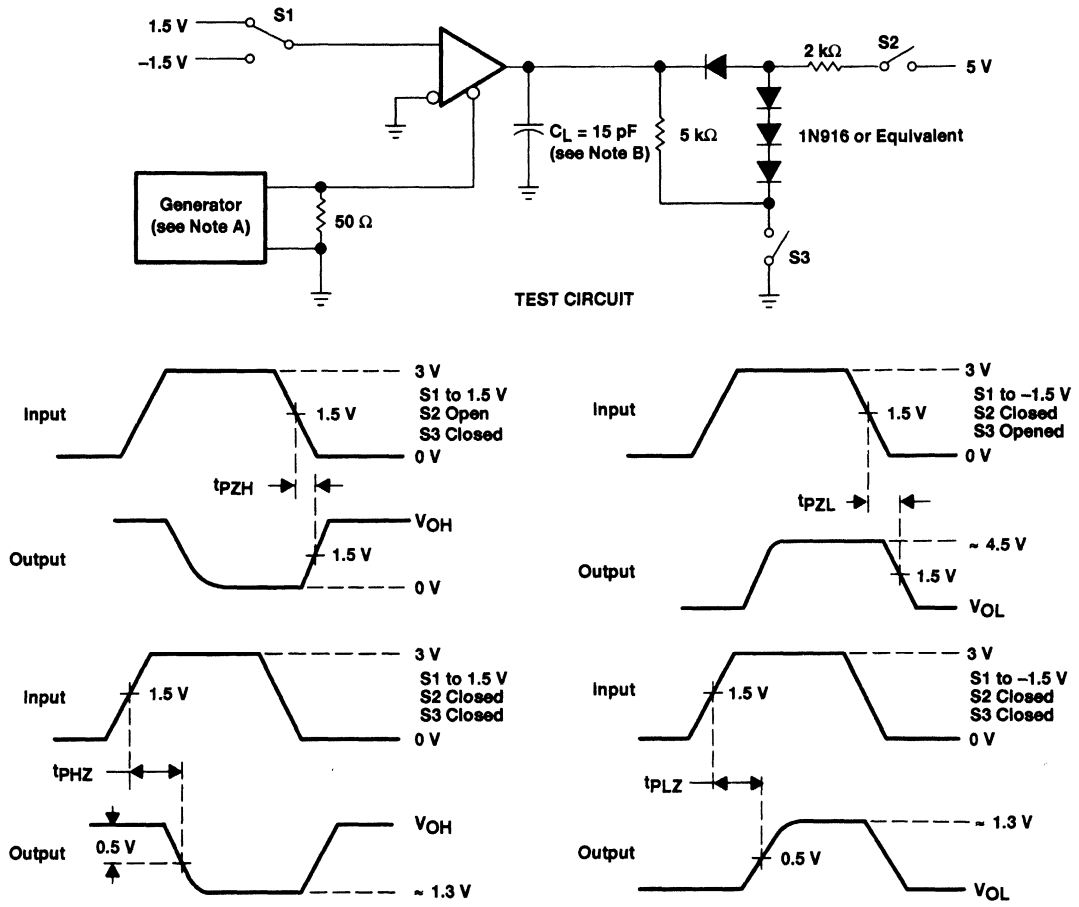


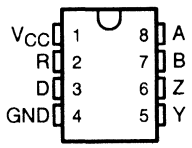
Figure 8. Receiver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

SLLS003D – OCTOBER 1985 – REVISED MAY 1995

- **Meet or Exceed the Requirements of ANSI Standards EIA/TIA-422-B, RS-485 and ITU Recommendation V.11**
- **Bus Voltage Range . . . –7 V to 12 V**
- **Positive- and Negative-Current Limiting**
- **Driver Output Capability . . . 60 mA Max**
- **Driver Thermal-Shutdown Protection**
- **Receiver Input Impedance . . . 12 kΩ Min**
- **Receiver Input Sensitivity . . . ±200 mV**
- **Receiver Input Hysteresis . . . 50 mV Typ**
- **Operate From Single 5-V Supply**
- **Low Power Requirements**

D OR P PACKAGE
(TOP VIEW)



Function Tables

DRIVER

INPUT	OUTPUTS	
D	Y	Z
H	H	L
L	L	H

RECEIVER

DIFFERENTIAL INPUTS A – B	OUTPUT R
$V_{ID} \geq 0.2$ V	H
-0.2 V $< V_{ID} < 0.2$ V	?
$V_{ID} \leq -0.2$ V	L
Open	?

H = high level, L = low level,
? = indeterminate

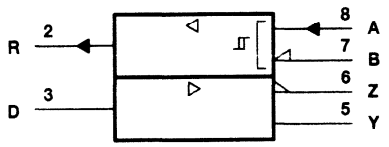
description

The SN75179B is a differential driver and receiver pair are monolithic integrated devices designed for balanced transmission-line applications and meet ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendation V.11. They are designed to improve the performance of full-duplex data communications over long bus lines.

The SN75179B driver output provides limiting for both positive and negative currents. The receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of –7 V to 12 V. The driver provides thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The SN75179B is designed to drive current loads of up to 60 mA maximum.

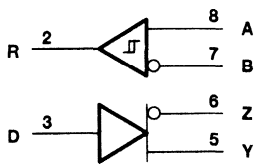
The SN75179B is characterized for operation from 0°C to 70°C.

logic symbol†

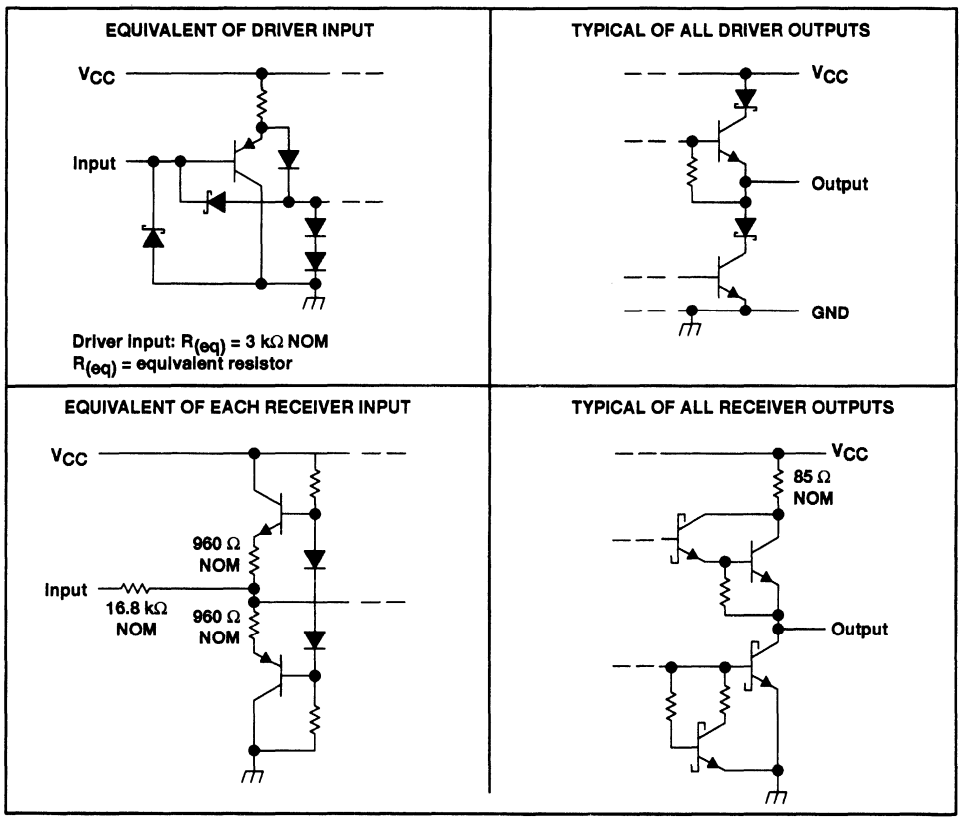


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Voltage range at any bus terminal ..... −10 V to 15 V
Differential input voltage, V_{ID} (see Note 2) ..... ±25 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	Driver	2			V
Low-level input voltage, V_{IL}	Driver			0.8	V
Common-mode input voltage, V_{IC}		−7†		12	V
Differential input voltage, V_{ID}				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	µA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

† The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = -18 mA				−1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\lvert V_{OD1} \rvert$	Differential output voltage	I_O = 0		1.5		6	V
$\lvert V_{OD2} \rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 1	1/2V_{OD1} or 2‡			V
		R_L = 54 Ω,	See Figure 1	1.5	2.5	5	V
$\lvert V_{OD3} \rvert$	Differential output voltage	See Note 3		1.5		5	V
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of common-mode output voltage§					±0.2	V
V_{OC}	Common-mode output voltage	R_L = 54 Ω or 100 Ω,	See Figure 1			3 −1	V
$\Delta\lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current	V_{CC} = 0,	V_O = −7 V to 12 V			±100	μA
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−200	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−250	mA
		V_O = V_{CC} or 12 V				250	
I_{CC}	Supply current (total package)	No load			57	70	mA

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The minimum V_{OD2} with 100-Ω load is either 1/2 V_{OD2} or 2 V, whichever is greater.
§ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input changes from a high level to a low level.
NOTE 3: See ANSI Standard RS-485, Figure 3.5, Test Termination Measurement 2.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω,	See Figure 3		15	22	ns
$t_{t(OD)}$	Differential output transition time				20	30	ns

Symbol Equivalents

DATA SHEET PARAMETER	EIA/TIA-422-B	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\lvert V_{OD1} \rvert$	V_o	V_o
$\lvert V_{OD2} \rvert$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\lvert V_{OD3} \rvert$		V_t (Test Termination Measurement 2)
$\Delta\lvert V_{OD} \rvert$	$\lvert\lvert V_t \rvert - \lvert \overline{V}_t \rvert\rvert$	$\lvert\lvert V_t \rvert - \lvert \overline{V}_t \rvert\rvert$
V_{OC}	$\lvert V_{os} \rvert$	$\lvert V_{os} \rvert$
$\Delta\lvert V_{OC} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$
I_{OS}	$\lvert I_{sa} \rvert$, $\lvert I_{sb} \rvert$	
I_O	$\lvert I_{xa} \rvert$, $\lvert I_{xb} \rvert$	I_{ia}, I_{ib}

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA				0.2	V
V_{IT-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA		−0.2‡			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)					50		mV
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = −400 μA,	See Figure 2	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV,	I_{OL} = 8 mA,	See Figure 2			0.45	V
I_I	Line input current	Other input at 0 V,	See Note 4	V_I = 12 V			1	mA
				V_I = −7 V			−0.8	
r_i	Input resistance				12			kΩ
I_{OS}	Short-circuit output current				−15		−85	mA
I_{CC}	Supply current (total package)	No load				57	70	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 4: Refer to ANSI Standard EIA/TIA-422-B for exact conditions.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_{ID} = −1.5 V to 1.5 V,			19	35	ns
t_{PHL}	Propagation delay time, high- to low-level output	C_L = 15 pF,	See Figure 4		30	40	ns

PARAMETER MEASUREMENT INFORMATION

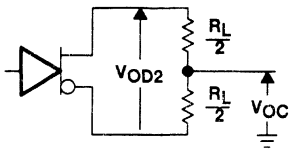


Figure 1. Driver V_{DD} and V_{OC}

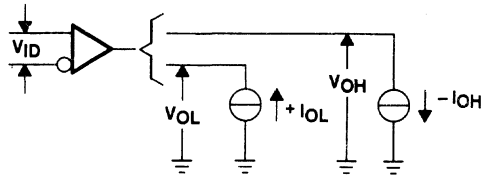
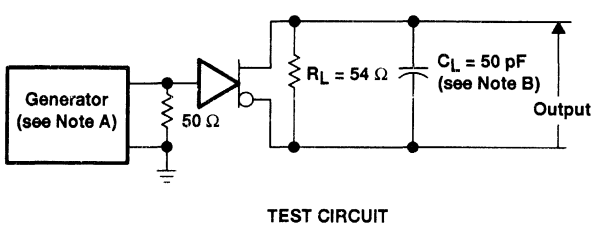
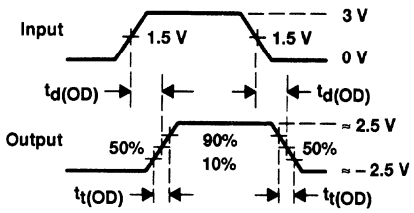


Figure 2. Receiver V_{OH} and V_{OL}

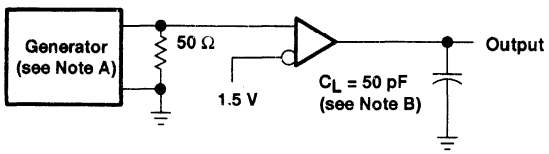


TEST CIRCUIT

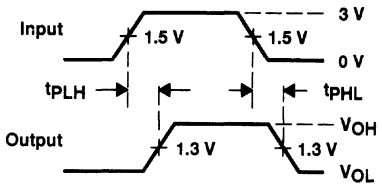


VOLTAGE WAVEFORMS

Figure 3. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 4. Receiver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O ≈ 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

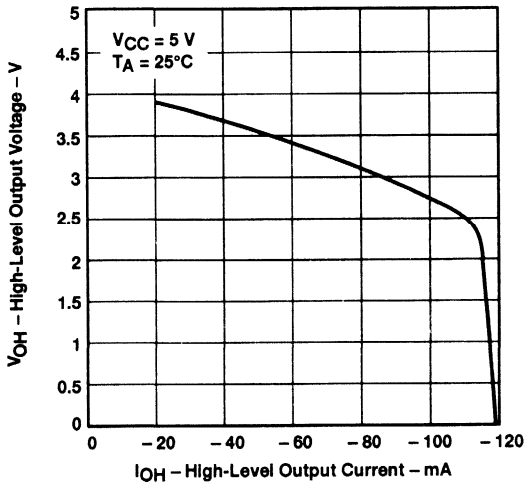


Figure 5

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

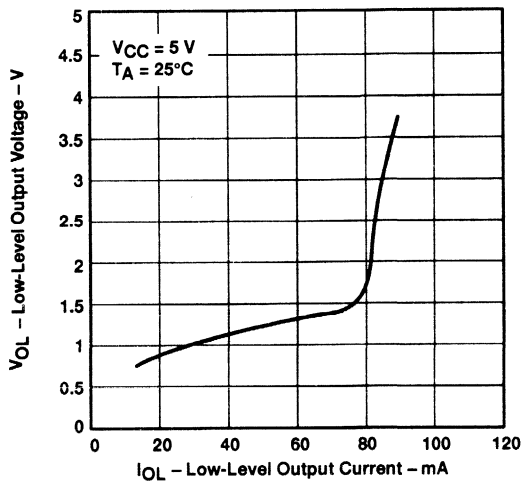


Figure 6

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

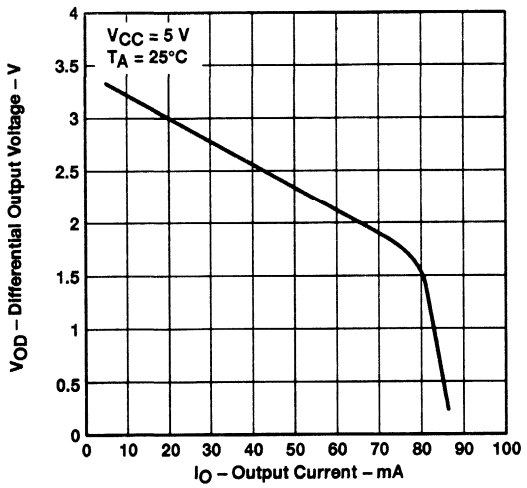


Figure 7

RECEIVER
OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

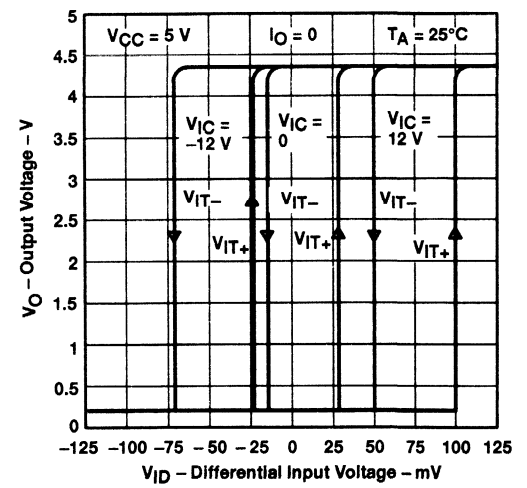


Figure 8

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

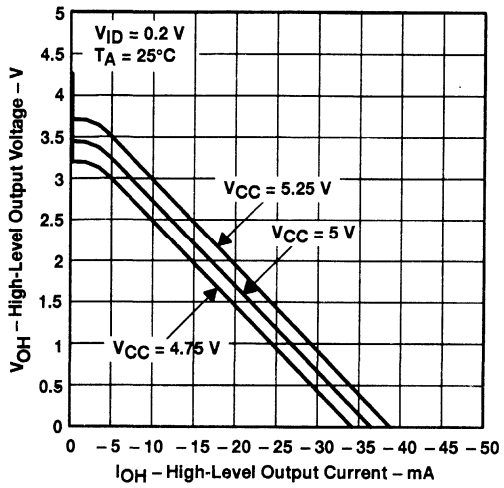


Figure 9

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

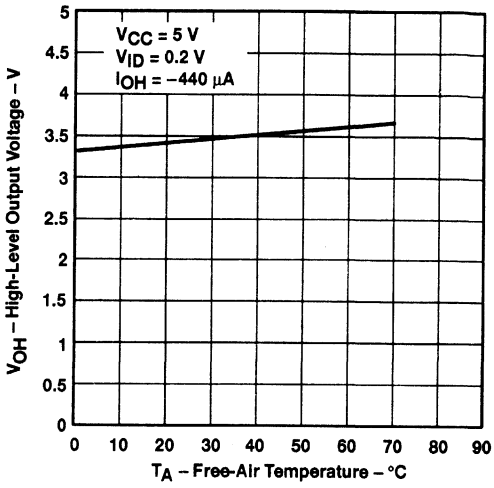


Figure 10

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

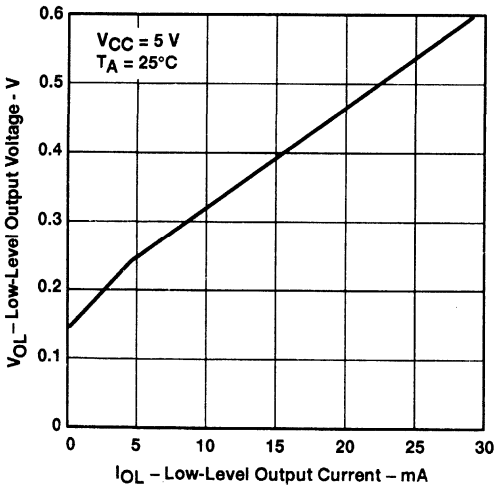


Figure 11

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

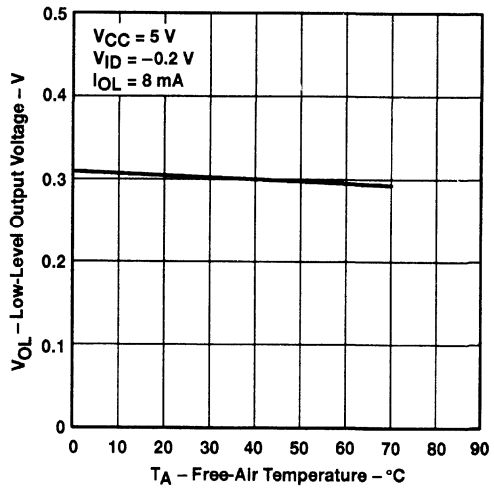
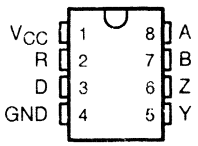


Figure 12

SLLS173A – JANUARY 1994 – REVISED MAY 1995

- **Designed for High-Speed Multipoint Data Transmission Over Long Cables**
- **Operate With Pulse Widths as Low as 30 ns**
- **Low Supply Current . . . 5 mA Max**
- **Meets or Exceeds the Standard Requirements of ANSI RS-485 and ISO 8482:1987(E)**
- **Common-Mode Voltage Range of –7 V to 12 V**
- **Positive- and Negative-Output Current Limiting**
- **Driver Thermal Shutdown Protection**
- **Pin Compatible With the SN75179B**

D OR P PACKAGE
(TOP VIEW)



Function Tables

DRIVER

INPUT D	OUTPUTS Y	Z
H	H	L
L	L	H

RECEIVER

DIFFERENTIAL INPUTS A–B	OUTPUT R
$V_{ID} \geq 0.2$ V	H
-0.2 V $< V_{ID} < 0.2$ V	?
$V_{ID} \leq -0.2$ V	L
Open circuit	H

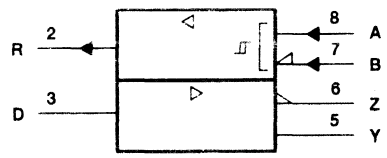
H = high level, L = low level,
? = indeterminate, Z = high impedance (off)

description

The SN65LBC179 and SN75LBC179 differential driver and receiver pairs are monolithic integrated circuits designed for bidirectional data communication over long cables that take on the characteristics of transmission lines. They are balanced, or differential, voltage mode devices that meet or exceed the requirements of industry standards ANSI RS-485 and ISO 8482:1987(E). Both devices are designed using TI's proprietary LinBiCMOS™ with the low power consumption of CMOS and the precision and robustness of bipolar transistors in the same circuit.

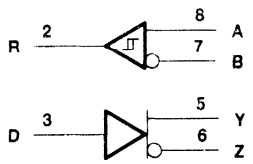
Both the SN65LBC179 and SN75LBC179 combine a differential line driver and differential line receiver and operate from a single 5-V supply. The driver differential outputs and the receiver differential inputs are connected to separate terminals for full-duplex operation and are designed to present minimum loading to the bus when powered off ($V_{CC} = 0$). These parts feature a wide common-mode voltage range making them suitable for point-to-point or multipoint data bus applications. The devices also provide positive- and negative-current limiting and thermal shutdown for protection from line fault conditions. The line driver shuts down at a junction temperature of approximately 172°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

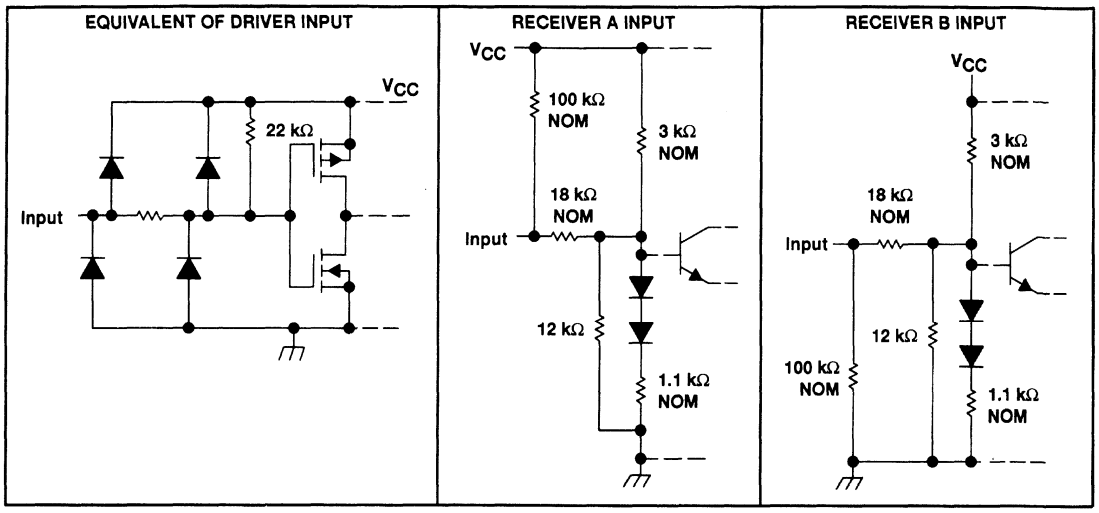
logic diagram (positive logic)

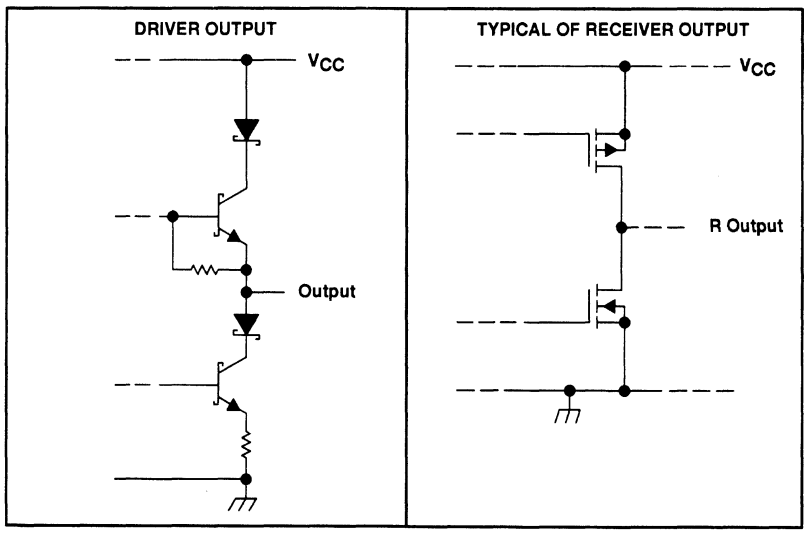


The SN65LBC179 and SN75LBC179 are available in the 8-pin dual-in-line and small-outline packages. The SN75LBC179 is characterized for operation over the commercial temperature range of 0°C to 70°C. The SN65LBC179 is characterized over the industrial temperature range of –40°C to 85°C.

LinBiCMOS is a trademark of Texas Instruments Incorporated.

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.3 V to 7 V
Voltage range at A, B, Y, or Z (see Note 1) ..... −10 V to 15 V
Voltage range at D or R (see Note 1) ..... −0.3 V to 7 V
Continuous total power dissipation (see Note 2) ..... Internally limited
Total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65LBC179 ..... −40°C to 85°C
SN75LBC179 ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. The maximum operating junction temperature is internally limited. Uses the dissipation rating table to operate below this temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1100 mW	8.8 mW/°C	704 mW	572 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	D	2			V
Low-level input voltage, V_{IL}	D			0.8	V
Differential input voltage, V_{ID}		−6‡		6	V
Voltage at any bus terminal (separately or common-mode), V_O, V_I, or V_{IC}	A, B, Y, or Z	−7		12	V
High-level output current, I_{OH}	Y or Z			−60	mA
	R			−8	
Low-level output current, I_{OL}	Y or Z			60	mA
	R			8	
Operating free-air temperature, T_A	SN65LBC179	−40		85	°C
	SN75LBC179	0		70	

‡ The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet for differential input voltage, voltage at any bus terminal (separately or common mode), operating temperature, input threshold voltage, and common-mode output voltage.

DRIVER SECTION

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
$\lvert V_{OD} \rvert$	Differential output voltage (see Note 3)	R_L = 54 Ω, See Figure 1	SN65LBC179	1.1	2.2	5	V
			SN75LBC179	1.5	2.2	5	
		R_L = 60 Ω, See Figure 2	SN65LBC179	1.1	2.2	5	
			SN75LBC179	1.5	2.2	5	
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of differential output voltage (see Note 4)	See Figures 1 and 2				±0.2	V
V_{OC}	Common-mode output voltage	R_L = 54 Ω, See Figure 1		1	2.5	3	V
$\Delta\lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage (see Note 4)					±0.2	V
I_O	Output current with power off	V_{CC} = 0, V_O = −7 V to 12 V				±100	μA
I_{OZ}	High-impedance-state output current	V_O = −7 V to 12 V				±100	μA
I_{IH}	High-level input current	V_I = 2.4 V				−100	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−100	μA
I_{OS}	Short-circuit output current	−7 V ≤ V_O ≤ 12 V				±250	mA
I_{CC}	Supply current	No load			4.2	5	mA

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

NOTES: 3. The minimum V_{OD} specification of the SN65179 may not fully comply with ANSI RS-485 at operating temperatures below 0°C. System designers should take the possibly lower output signal into account in determining the maximum signal transmission distance.

4. $\Delta\lvert V_{OD} \rvert$ and $\Delta\lvert V_{OC} \rvert$ are the changes in the steady-state magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	R_L = 54 Ω, See Figure 3	7	18	ns
$t_{t(OD)}$	Differential transition time		5	20	ns

RECEIVER SECTION

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	I_O = −8 mA				0.2	V
V_{IT-}	Negative-going input threshold voltage	I_O = 8 mA		−0.2			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)				45		mV
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = −8 mA	3.5	4.5		V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV,	I_{OL} = 16 mA		0.3	0.5	V
I_I	Bus input current	V_I = 12 V, Other inputs at 0 V	V_{CC} = 5 V,		0.7	1	mA
		V_I = 12 V, Other inputs at 0 V	V_{CC} = 0 V,		0.8	1	
		V_I = −7 V, Other inputs at 0 V	V_{CC} = 5 V,		−0.5	−0.8	
		V_I = −7 V, Other inputs at 0 V	V_{CC} = 0 V,		−0.5	−0.8	

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	V_{ID} = −1.5 V to 1.5 V, See Figure 4	15		30	ns
t_{PLH}	Propagation delay time, low- to high-level output		15		30	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)	See Figure 4		3	6	ns
t_t	Transition time			3	5	ns

PARAMETER MEASUREMENT INFORMATION

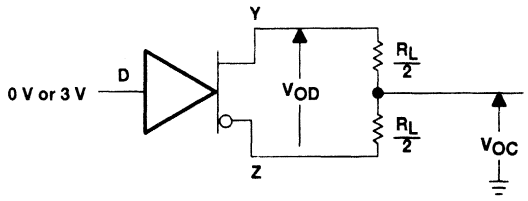


Figure 1. Differential and Common-Mode Output Voltage Test Circuit

PARAMETER MEASUREMENT INFORMATION

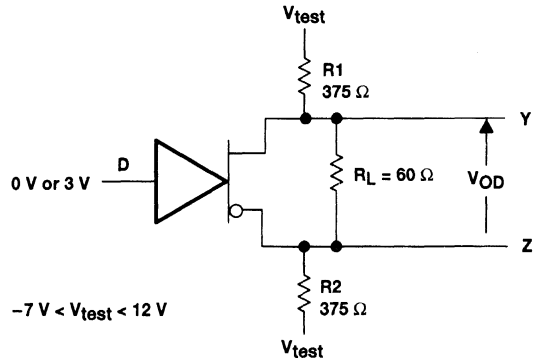


Figure 2. Differential Output Voltage Test Circuit

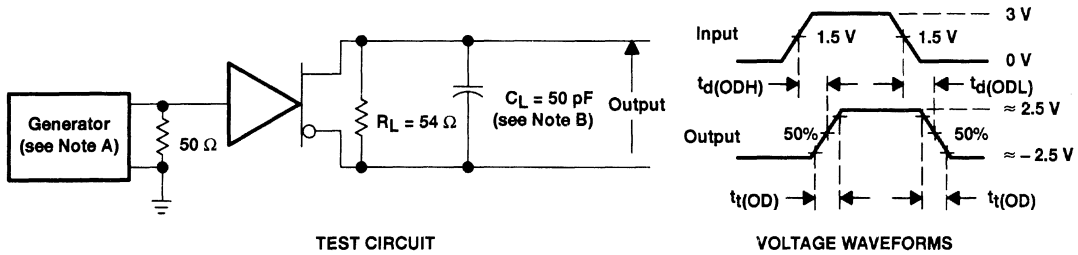


Figure 3. Driver Test Circuits and Differential Output Delay and Transition Time Voltage Waveforms

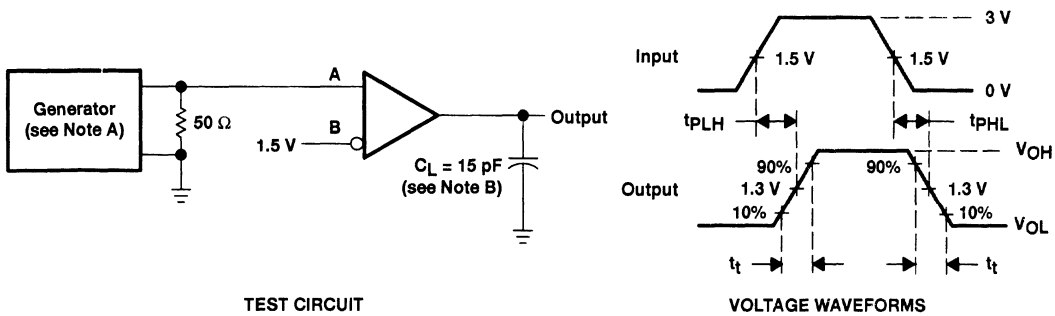


Figure 4. Receiver Test Circuit and Propagation Delay and Transition Time Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR > 1 MHz, 50% duty cycle, $t_r \le 6$ ns, $t_f \le 6$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

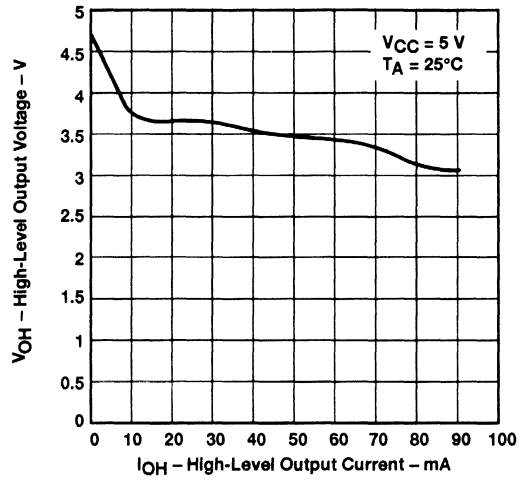


Figure 5

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

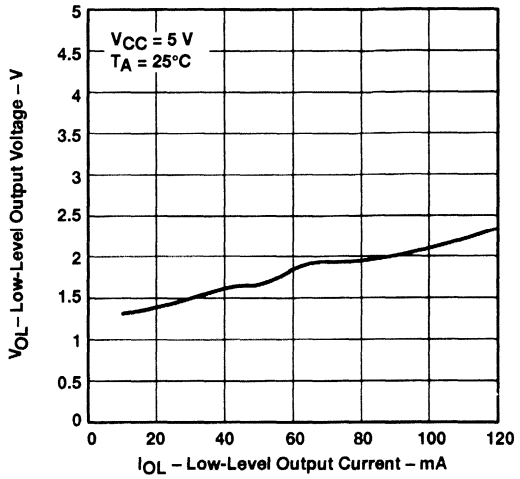


Figure 6

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

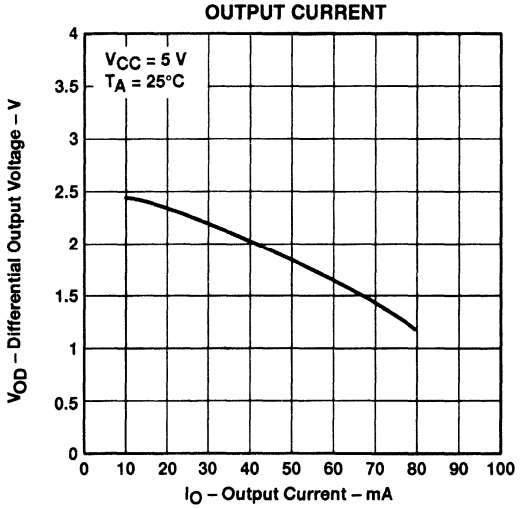


Figure 7

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

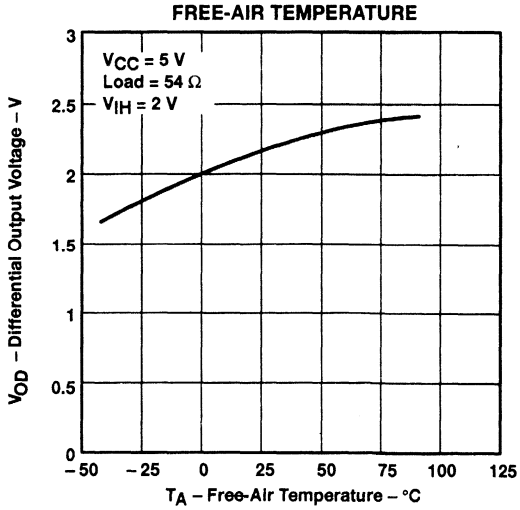


Figure 8

TYPICAL CHARACTERISTICS

DRIVER
DIFFERENTIAL DELAY TIME
vs
FREE-AIR TEMPERATURE

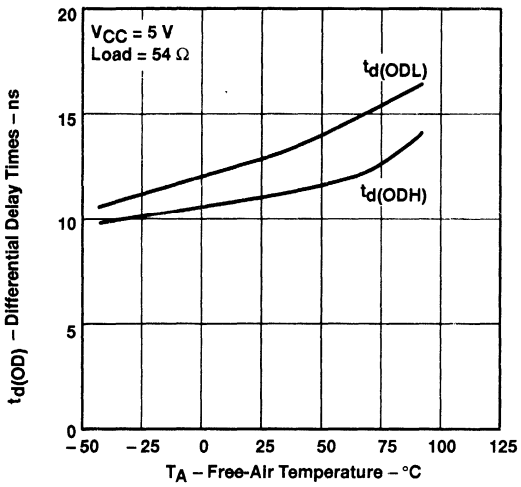


Figure 9

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

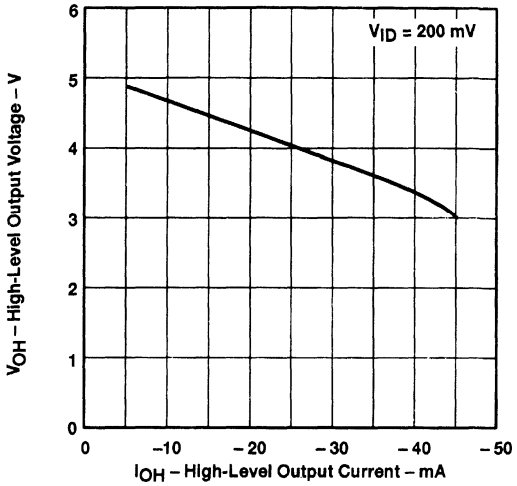


Figure 10

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

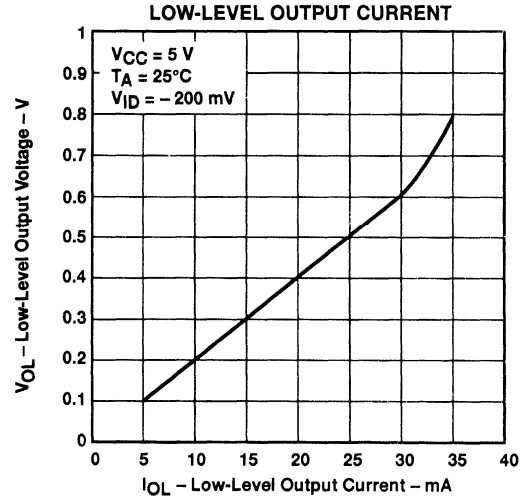


Figure 11

RECEIVER
OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

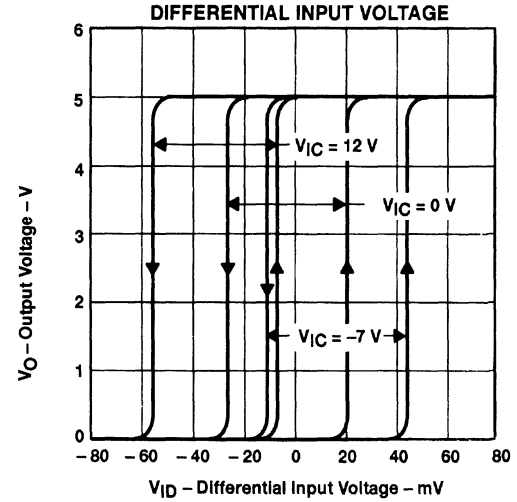


Figure 12

TYPICAL CHARACTERISTICS

AVERAGE SUPPLY CURRENT
vs
FREQUENCY

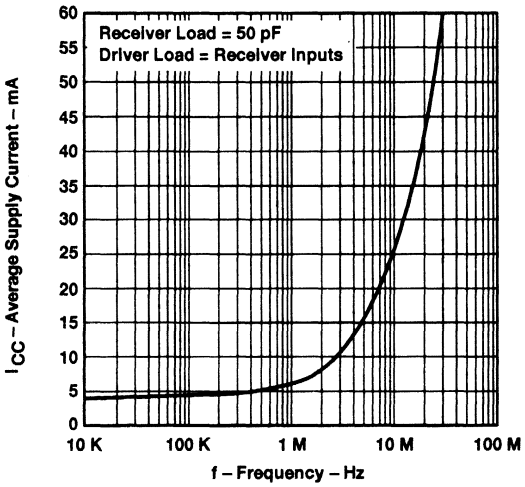


Figure 13

RECEIVER
INPUT CURRENT
vs
INPUT VOLTAGE
(COMPLEMENTARY INPUT AT 0 V)

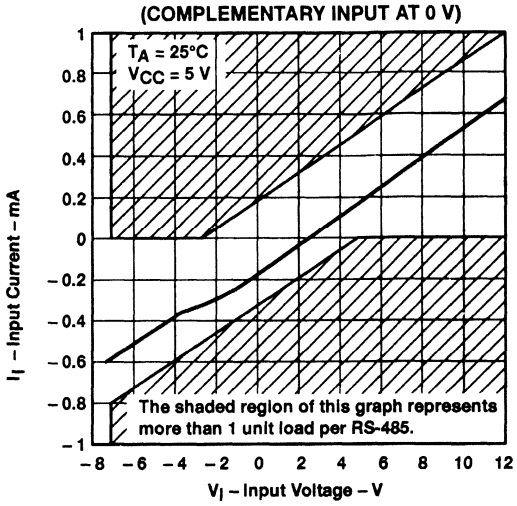


Figure 14

RECEIVER
PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

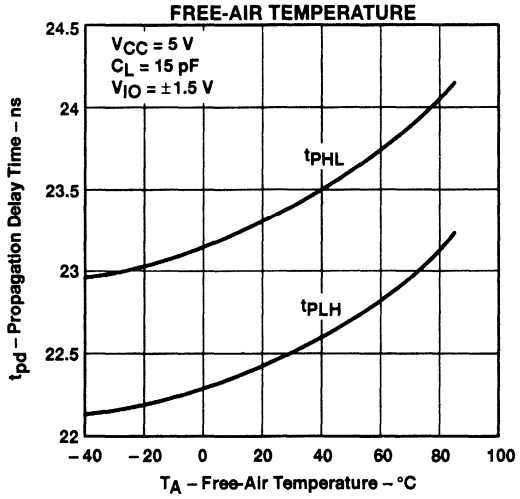
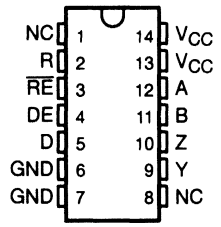


Figure 15

SLLS052D – AUGUST 1987 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of ANSI Standard EIA/TIA-422-B and RS-485† and ITU Recommendation V.11**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Designed for 25-MBaud Operation in Both Serial and Parallel Applications**
- **Low Skew Between Devices . . . 6 ns Max**
- **Low Supply-Current Requirements 30 mA Max**
- **Individual Driver and Receiver I/O Pins With Dual V_{CC} and Dual GND**
- **Wide Positive and Negative Input/Output Bus Voltage Ranges**
- **Driver Output Capacity . . . ±60 mA**
- **Thermal Shutdown Protection**
- **Driver Positive- and Negative-Current Limiting**
- **Receiver Input Impedance . . . 12 kΩ Min**
- **Receiver Input Sensitivity . . . ±200 mV Max**
- **Receiver Input Hysteresis . . . 60 mV Typ**
- **Operate From a Single 5-V Supply**
- **Glitch-Free Power-Up and Power-Down Protection**

D OR N PACKAGE
(TOP VIEW)



NC – No internal connection

Function Tables

DRIVER

INPUT D	ENABLE DE	OUTPUTS Y	OUTPUTS Z
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS A–B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

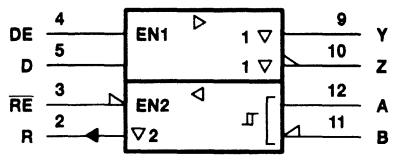
H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

description

The SN65ALS180 and SN75ALS180 differential driver and receiver pairs are monolithic integrated circuits designed for bidirectional data communication on multipoint bus-transmission lines. They are designed for balanced transmission lines and meet ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendation V.11.

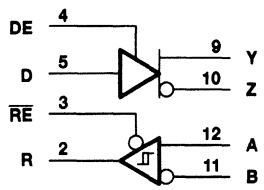
The SN65ALS180 and SN75ALS180 combine a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected to separate terminals for greater flexibility and are designed to offer minimum loading to the bus when the driver is disabled or V_{CC} = 0.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



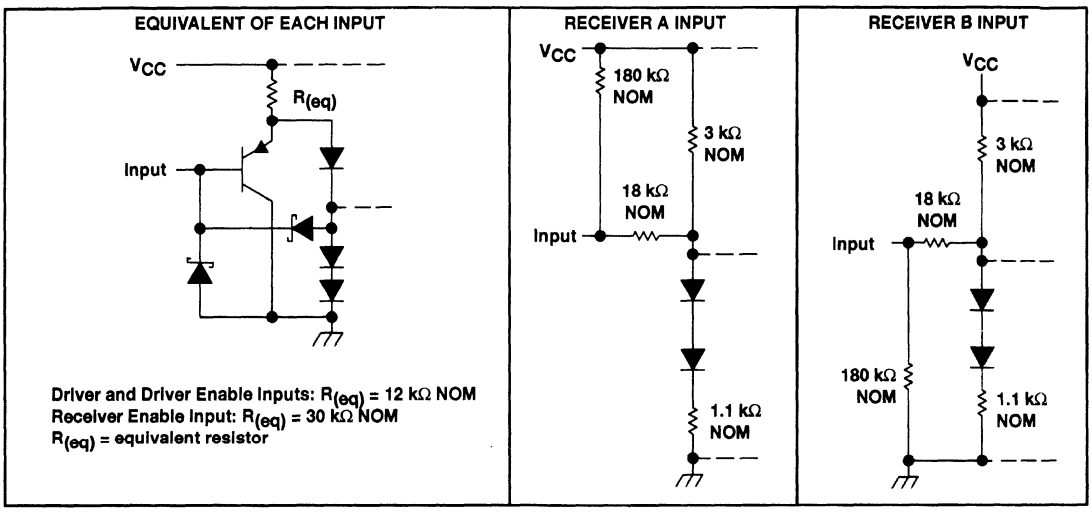
† These devices meet or exceed the requirements of ANSI RS-485 except for the Generator Contention Test (para. 3.4.2) and the Generator Current Limit (para. 3.4.3). The applied test voltage ranges are –6 V to 8 V for the SN75ALS180 and –4.5 V to 8 V for the SN65ALS180.

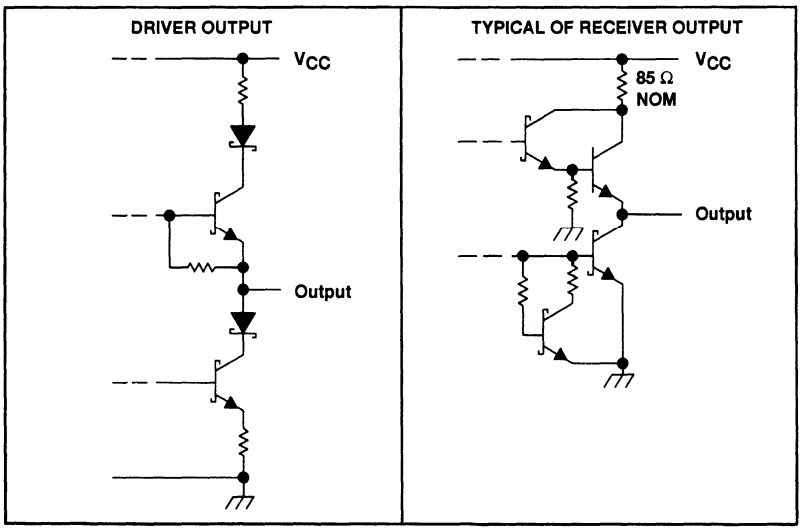
description (continued)

These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The SN65ALS180 is characterized for operation from −40°C to 85°C. The SN75ALS180 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Voltage range at any bus terminal ..... −10 V to 15 V
Enable input voltage, V_I ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65ALS180 ..... −40°C to 85°C
SN75ALS180 ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12 −7	V
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A	SN65ALS180	−40		85	°C
	SN75ALS180	0		70	

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A/Y with respect to the inverting terminal B/Z.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_O	Output voltage	$I_O = 0$		0		6	V
$\lvert V_{OD1} \rvert$	Differential output voltage	$I_O = 0$		1.5		6	V
$\lvert V_{OD2} \rvert$	Differential output voltage	$R_L = 100\ \Omega$,	See Figure 1	1/2 V_{OD1} or 2§			V
		$R_L = 54\ \Omega$,	See Figure 1	1.5	2.5	5	
V_{OD3}	Differential output voltage	$V_{test} = -7$ V to 12 V,	See Figure 2	1.5		5	V
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of differential output voltage¶	$R_L = 54\ \Omega$ or 100 Ω,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage					3 −1	V
$\Delta\lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage¶					±0.2	V
I_O	Output current	Output disabled, See Note 3	$V_O = 12$ V			1	mA
			$V_O = -7$ V			−0.8	
I_{IH}	High-level input current	$V_I = 2.4$ V				20	µA
I_{IL}	Low-level input current	$V_I = 0.4$ V				−400	µA
I_{OS}	Short-circuit output current#	$V_O = -6$ V	SN75ALS180			−250	mA
		$V_O = -4$ V	SN65ALS180				
		$V_O = 0$	All			−150	
		$V_O = V_{CC}$	All				
		$V_O = 8$ V	All				
I_{CC}	Supply current	No load	Driver outputs enabled, Receiver disabled		25	30	mA
			Outputs disabled		19	26	

† The power-off measurement in ANSI Standard EIA/TIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
‡ All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
§ The minimum V_{OD2} with 100-Ω load is either 1/2 V_{OD2} or 2 V, whichever is greater.
¶ $\Delta\lvert V_{OD} \rvert$ and $\Delta\lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
# Duration of the short circuit should not exceed one second for this test.
NOTE 3: This applies for both power on and off; refer to ANSI Standard RS-485 for exact conditions. The EIA/TIA-422-B limit does not apply for a combined driver and receiver terminal.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	$R_L = 54\ \Omega$,	$C_L = 50$ pF, See Figure 3	3	8	13	ns
	Pulse skew ($\lvert t_{d(ODH)} - t_{d(ODL)} \rvert$)				1	6	ns
$t_{t(OD)}$	Differential output transition time			3	8	13	ns
t_{PZH}	Output enable time to high level	$R_L = 110\ \Omega$,	See Figure 4		23	50	ns
t_{PZL}	Output enable time to low level	$R_L = 110\ \Omega$,	See Figure 5		19	24	ns
t_{PHZ}	Output disable time from high level	$R_L = 110\ \Omega$,	See Figure 4		8	13	ns
t_{PLZ}	Output disable time from low level	$R_L = 110\ \Omega$,	See Figure 5		8	13	ns

‡ All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	EIA/TIA-422-B	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\lvert V_{OD1} \rvert$	V_o	V_o
$\lvert VOD2 \rvert$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\lvert VOD3 \rvert$		V_t (test termination measurement 2)
V_{test}		V_{tst}
$\Delta \lvert V_{OD} \rvert$	$\lvert\lvert V_t \rvert - \lvert \overline{V}_t \rvert\rvert$	$\lvert\lvert V_t \rvert - \lvert \overline{V}_t \rvert\rvert$
V_{OC}	$\lvert V_{os} \rvert$	$\lvert V_{os} \rvert$
$\Delta \lvert V_{OC} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$
I_{OS}	$\lvert I_{sa} \rvert$, $\lvert I_{sb} \rvert$	
I_O	$\lvert I_{xa} \rvert$, $\lvert I_{xb} \rvert$	I_{ia}, I_{ib}

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{IT-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)				60		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = −200 mV, See Figure 6	I_{OH} = −400 μA,	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 6	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input = 0 V, See Note 4	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current	V_{ID} = 200 mV,	V_O = 0	−15		−85	mA
I_{CC}	Supply current	No load	Receiver outputs enabled, Driver inputs disabled		19	30	mA
			Outputs disabled		19	26	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 4: This applies for both power on and power off. Refer to ANSI Standard RS-485 for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_{ID} = –1.5 V to 1.5 V, C_L = 15 pF, See Figure 7	9	14	19	ns
t_{PHL}	Propagation delay time, high- to low-level output		9	14	19	ns
	Skew ($\lvert t_{PHL} - t_{PLH} \rvert$)			2	6	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF, See Figure 8		7	14	ns
t_{PZL}	Output enable time to low level			7	14	ns
t_{PHZ}	Output disable time from high level			20	35	ns
t_{PLZ}	Output disable time from low level			8	17	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

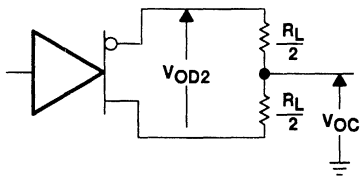


Figure 1. Driver V_{OD} and V_{OC}

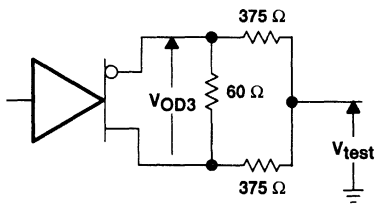
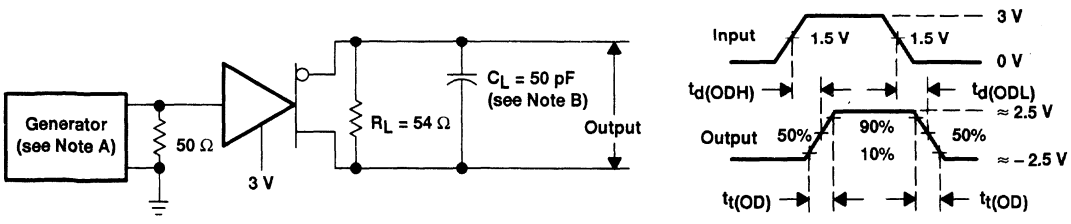


Figure 2. Driver V_{OD3}



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

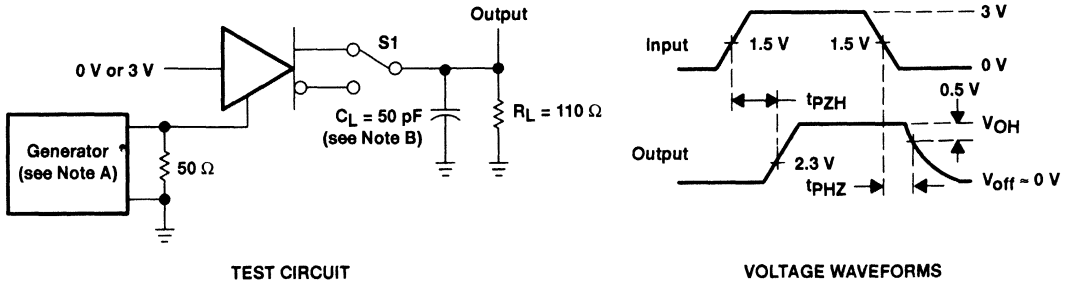


Figure 4. Driver Test Circuit and Voltage Waveforms

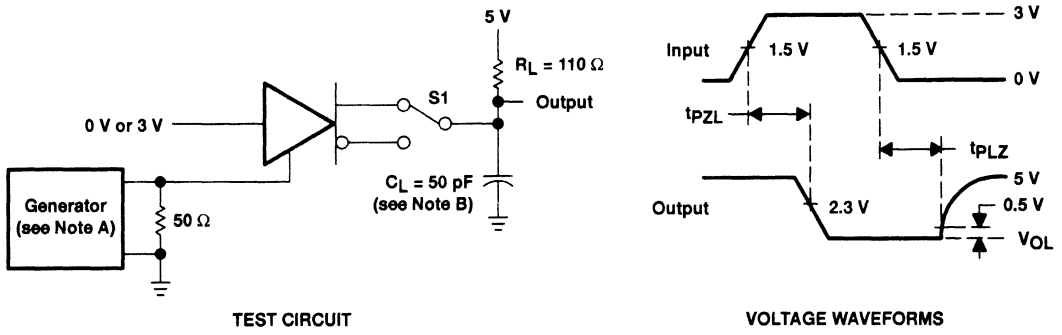


Figure 5. Driver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

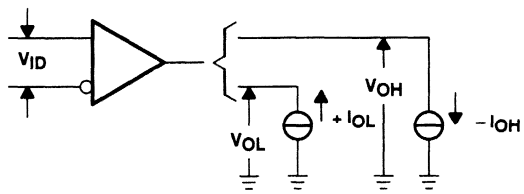
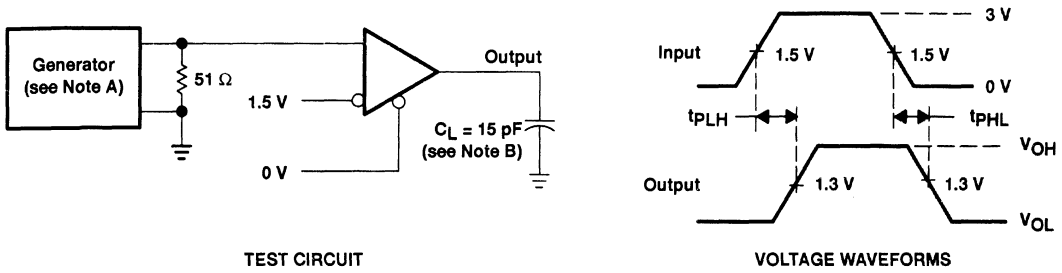


Figure 6. Receiver V_{OH} and V_{OL}

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

Figure 7. Receiver Test Circuit and Voltage Waveforms

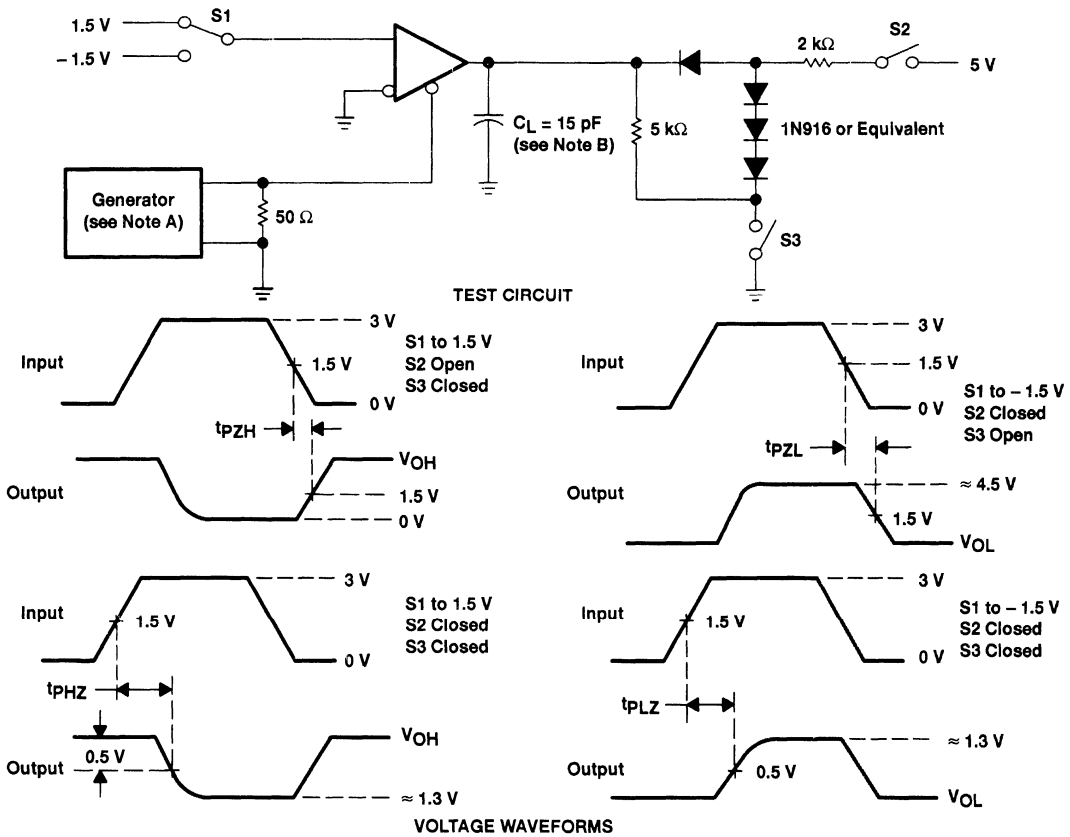


Figure 8. Receiver Test Circuit and Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

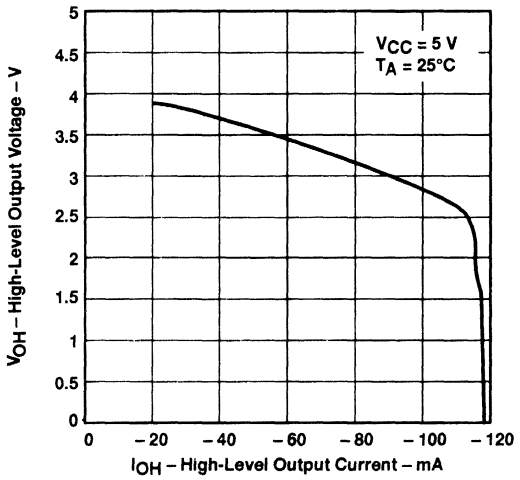


Figure 9

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

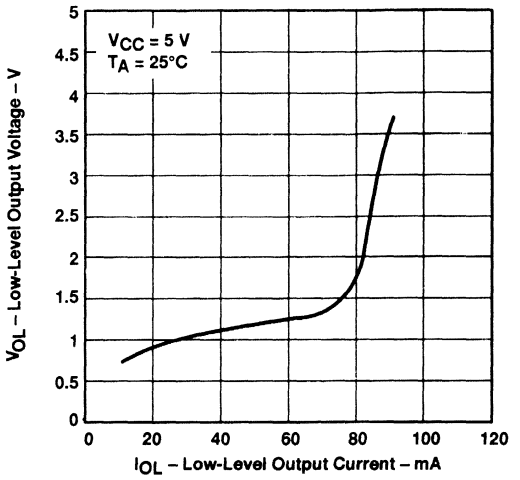


Figure 10

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

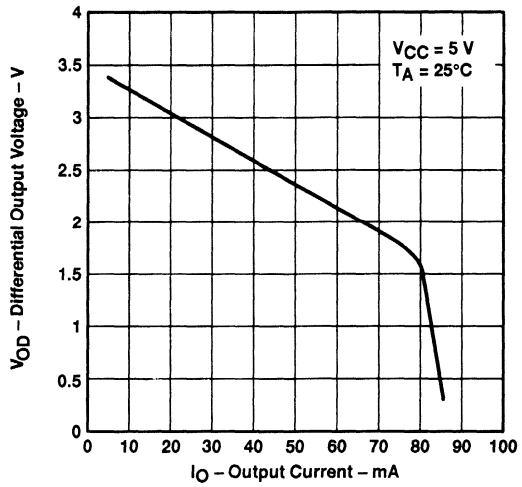


Figure 11

TYPICAL CHARACTERISTICS

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

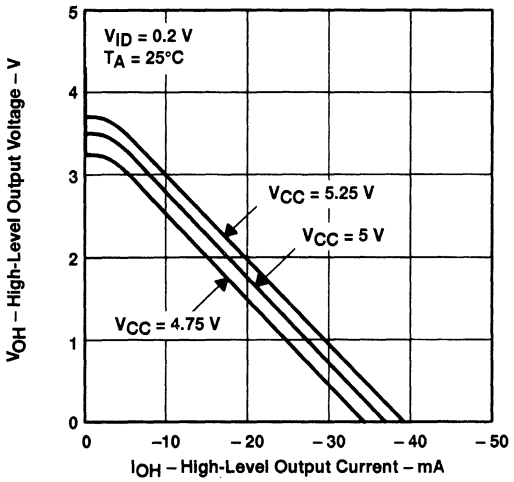


Figure 12

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

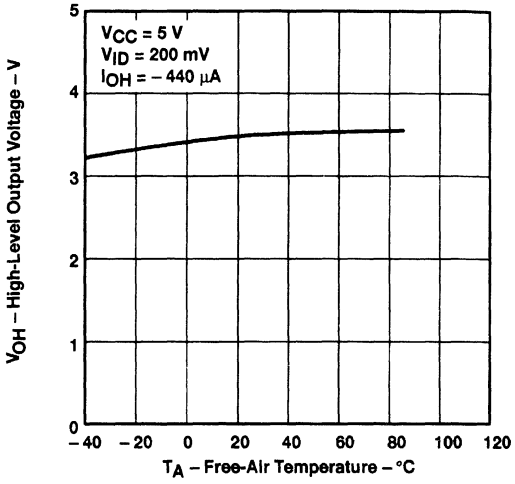


Figure 13

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

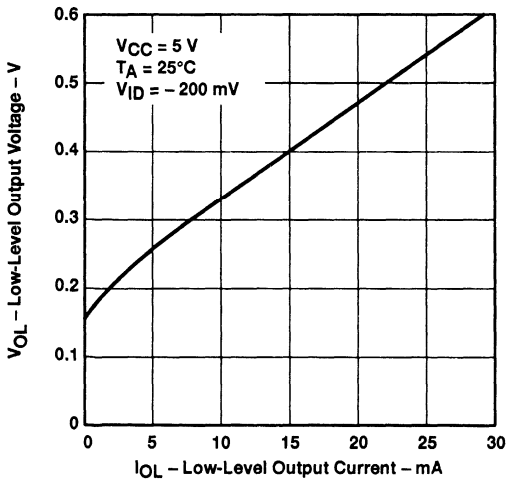


Figure 14

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

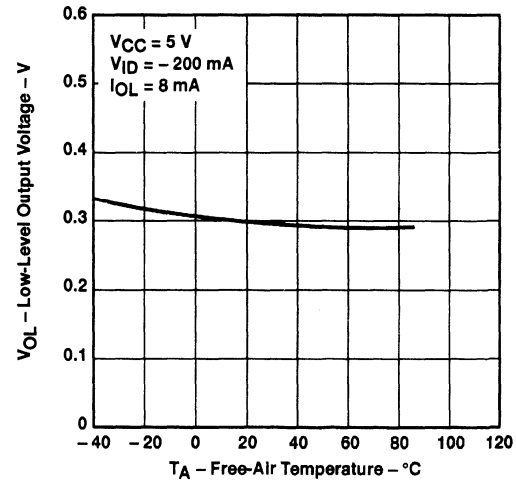


Figure 15

TYPICAL CHARACTERISTICS

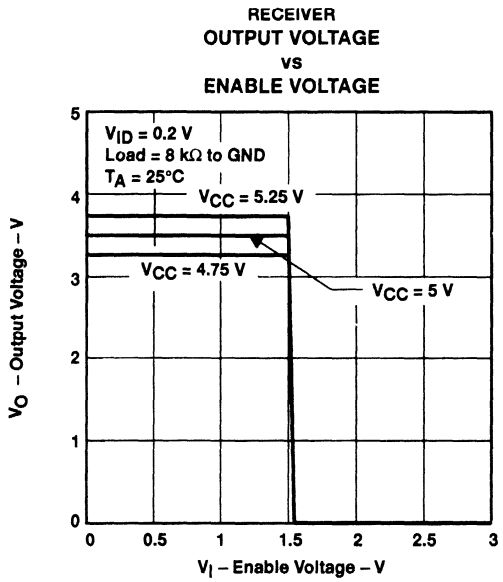


Figure 16

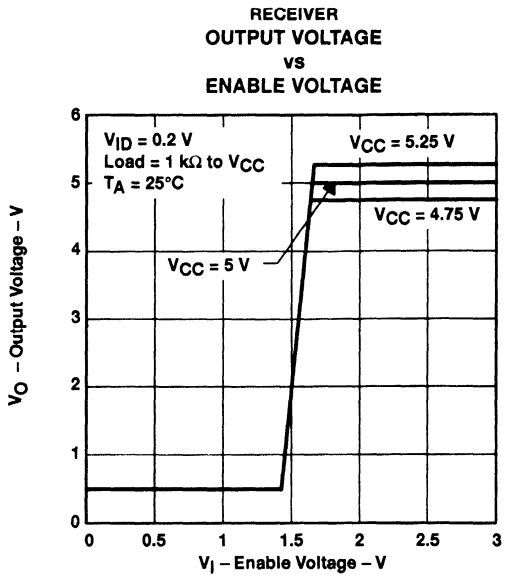
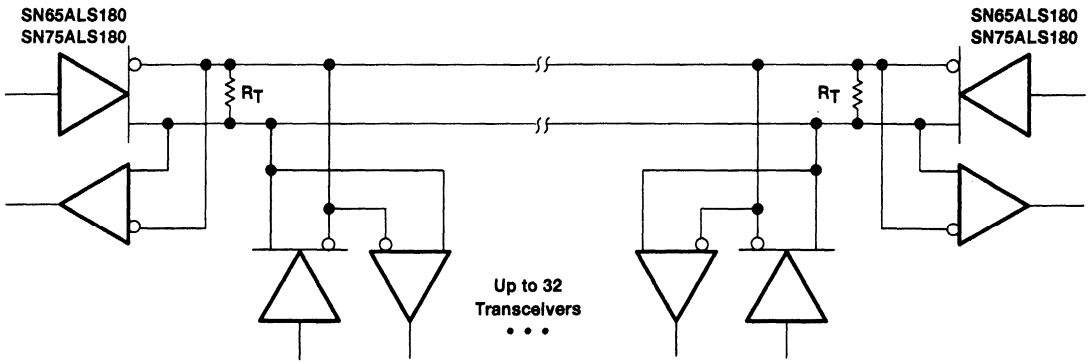


Figure 17

APPLICATION INFORMATION



NOTE A. The line should be terminated at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

Figure 18. Typical Application Circuit

SLLS174A – FEBRUARY 1994 – REVISED MAY 1995

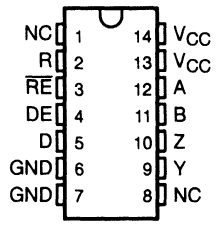
- **Designed for High-Speed Multipoint Data Transmission Over Long Cables**
- **Operate With Pulse Durations as Low as 30 ns**
- **Low Supply Current . . . 5 mA Max**
- **Meet or Exceed the Requirements of ANSI Standard RS-485 and ISO 8482:1987(E)**
- **3-State Outputs for Party-Line Buses**
- **Common-Mode Voltage Range of –7 V to 12 V**
- **Thermal Shutdown Protection Prevents Driver Damage From Bus Contention**
- **Positive and Negative Output Current Limiting**
- **Pin Compatible With the SN75ALS180**

description

The SN65LBC180 and SN75LBC180 differential driver and receiver pairs are monolithic integrated circuits designed for bidirectional data communication over long cables that take on the characteristics of transmission lines. They are balanced, or differential, voltage mode devices that meet or exceed the requirements of industry standards ANSI RS-485 and ISO 8482:1987(E). Both devices are designed using TI's proprietary LinBiCMOS™ with the low power consumption of CMOS and the precision and robustness of bipolar transistors in the same circuit.

Both the SN65LBC180 and SN75LBC180 combine a differential line driver and receiver with 3-state outputs and operate from a single 5-V supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected to function as a direction control. The driver differential outputs and the receiver differential inputs are connected to separate terminals for full-duplex operation and are designed to present minimum loading to the bus whether disabled or powered off (V_{CC} = 0). These parts feature a wide common-mode voltage range making them suitable for point-to-point or multipoint data-bus applications.

D OR N PACKAGE
(TOP VIEW)



NC – No internal connection

Function Tables

DRIVER

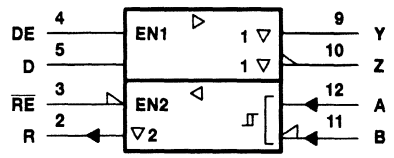
INPUT D	ENABLE DE	OUTPUTS Y	OUTPUTS Z
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS A–B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open circuit	L	H

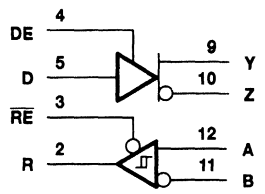
H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



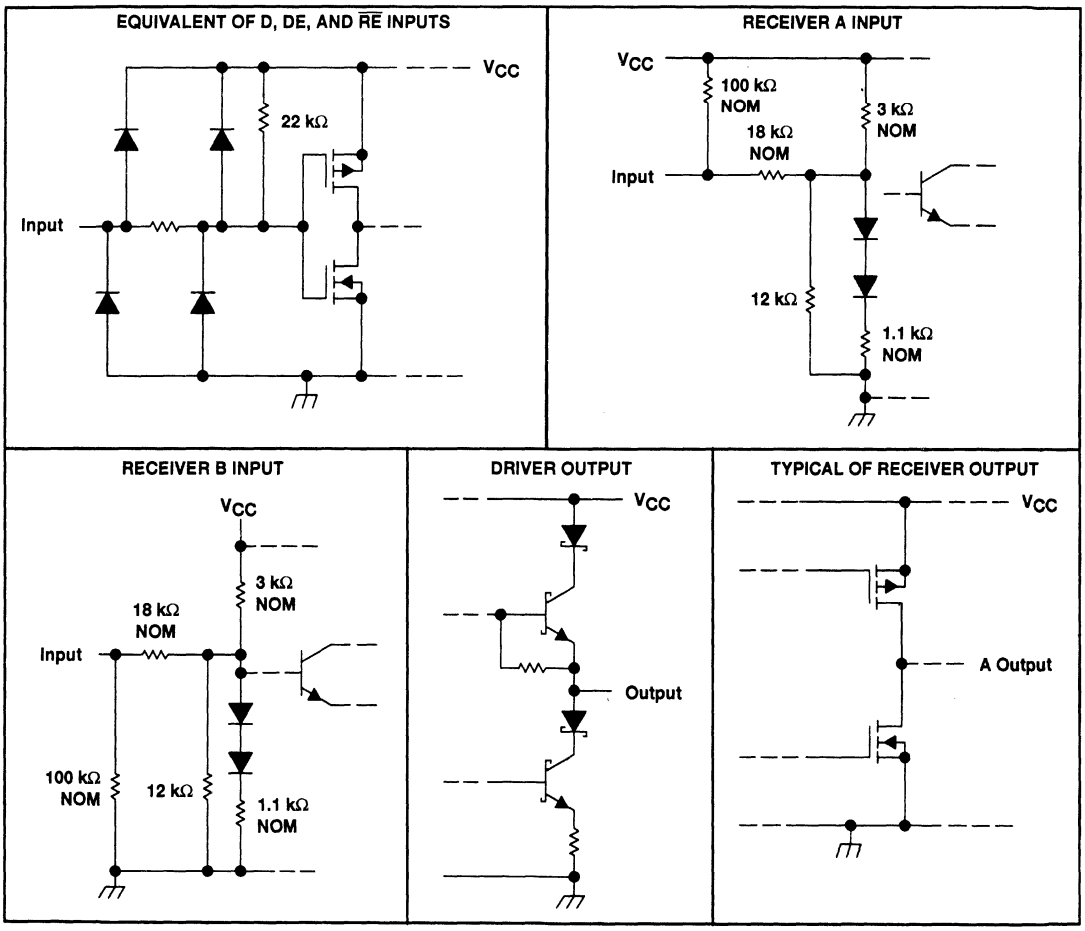
LinBiCMOS is a trademark of Texas Instruments Incorporated.

description (continued)

The devices also provide positive and negative output-current limiting and thermal shutdown for protection from line fault conditions. The line driver shuts down at a junction temperature of approximately 172°C.

The SN65LBC180 and SN75LBC180 are available in the 14-pin dual-in-line and small-outline packages. The SN75LBC180 is characterized for operation over the commercial temperature range of 0°C to 70°C. The SN65LBC180 is characterized over the industrial temperature range of –40°C to 85°C.

schematics of inputs and outputs



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.3 V to 7 V
Input voltage range, V_I (A, B)(see Note 1) ..... −10 V to 15 V
Input voltage range, V_I (DE, $\overline{RE}$, D, or R)(see Note 1) ..... −0.3 V to 7 V
Continuous total power dissipation (see Note 2) ..... internally limited
Total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65LBC180 ..... −40°C to 85°C
SN75LBC180 ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID}		−6‡		6	V
Voltage at any bus terminal (separately or common mode), V_O, V_I, or V_{IC}	A, B, Y, or Z	−7‡		12	V
High-level output current, I_{OH}	Y or Z			−60	mA
	R			−8	
Low-level output current, I_{OL}	Y or Z			60	mA
	R			8	
Operating free-air temperature, T_A	SN65LBC180	−40		85	°C
	SN75LBC180	0		70	

‡ The algebraic convention where the least positive (more negative) limit is designated minimum, is used in this data sheet for the differential input voltage, voltage at any bus terminal, operating temperature, input threshold voltage, and common-mode output voltage.

DRIVER SECTION

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
$\lvert V_{OD} \rvert$	Differential output voltage magnitude (see Note 3)	$R_L = 54\ \Omega$, See Figure 1	SN65LBC180	1.1	2.5	5	V
			SN75LBC180	1.5	2.5	5	
		$R_L = 60\ \Omega$, See Figure 2	SN65LBC180	1.1	2	5	
			SN75LBC180	1.5	2	5	
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of differential output voltage (see Note 4)	See Figures 1 and 2				±0.2	V
V_{OC}	Common-mode output voltage	$R_L = 54\ \Omega$, See Figure 1		1	2.5	3	V
$\Delta\lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage (see Note 4)					±0.2	V
I_O	Output current with power off	$V_{CC} = 0$, $V_O = -7$ V to 12 V				±100	μA
I_{OZ}	High-impedance-state output current	$V_O = -7$ V to 12 V				±100	μA
I_{IH}	High-level input current	$V_I = 2.4$ V				−100	μA
I_{IL}	Low-level input current	$V_I = 0.4$ V				−100	μA
I_{OS}	Short-circuit output current	$-7\ V \le V_O \le 12$ V				±250	mA
I_{CC}	Supply current	Receiver disabled	Outputs enabled			5	mA
			Outputs disabled			3	

† All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.

NOTES: 3. The minimum V_{OD} specification of the SN65LBC180 may not fully comply with ANSI RS-485 at operating temperatures below 0°C. System designers should take the possibly lower output signal into account in determining the maximum signal-transmission distance.

4. $\Delta\lvert V_{OD} \rvert$ and $\Delta\lvert V_{OC} \rvert$ are the changes in the steady-state magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	$R_L = 54\ \Omega$,	See Figure 3	7	12	18	ns
$t_{t(OD)}$	Differential output transition time			5	10	20	ns
t_{PZH}	Output enable time to high level	$R_L = 110\ \Omega$,	See Figure 4			35	ns
t_{PZL}	Output enable time to low level	$R_L = 110\ \Omega$,	See Figure 5			35	ns
t_{PHZ}	Output disable time from high level	$R_L = 110\ \Omega$,	See Figure 4			50	ns
t_{PLZ}	Output disable time from low level	$R_L = 110\ \Omega$,	See Figure 5			35	ns

RECEIVER SECTION

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	I_O = −8 mA				0.2	V
V_{IT-}	Negative-going input threshold voltage	I_O = 8 mA		−0.2			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)				45		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = −8 mA	3.5	4.5		V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV,	I_{OL} = 8 mA		0.3	0.5	V
I_{OZ}	High-impedance-state output current	V_O = 0 V to V_{CC}				±20	μA
I_{IH}	High-level enable-input current	V_{IH} = 2.4 V				−50	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
I_I	Bus input current	V_I = 12 V, Other input at 0 V	V_{CC} = 5 V,		0.7	1	mA
		V_I = 12 V, Other input at 0 V	V_{CC} = 0 V,		0.8	1	
		V_I = −7 V, Other input at 0 V	V_{CC} = 5 V,		−0.5	−0.8	
		V_I = −7 V, Other input at 0 V	V_{CC} = 0 V,		−0.5	−0.8	
I_{CC}	Supply current	Driver disabled	Outputs enabled			5	mA
			Outputs disabled			3	

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	V_{ID} = −1.5 V to 1.5 V,	See Figure 6	11	22	33	ns
t_{PLH}	Propagation delay time, low- to high-level output			11	22	33	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)				3	6	ns
t_t	Transition time				5	8	ns
t_{PZH}	Output enable time to high level	See Figure 7				35	ns
t_{PZL}	Output enable time to low level					30	ns
t_{PHZ}	Output disable time from high level					35	ns
t_{PLZ}	Output disable time from low level					30	ns

PARAMETER MEASUREMENT INFORMATION

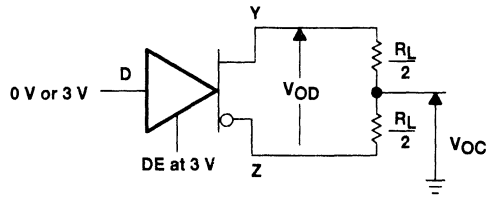


Figure 1. Differential and Common-Mode Output Voltages

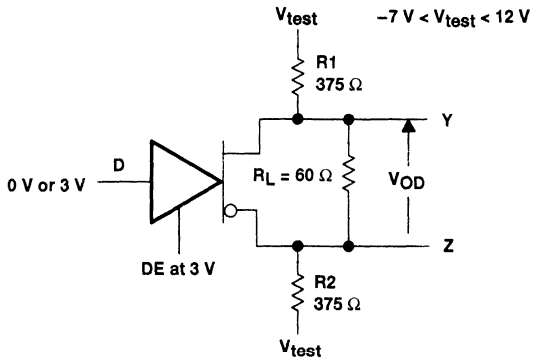
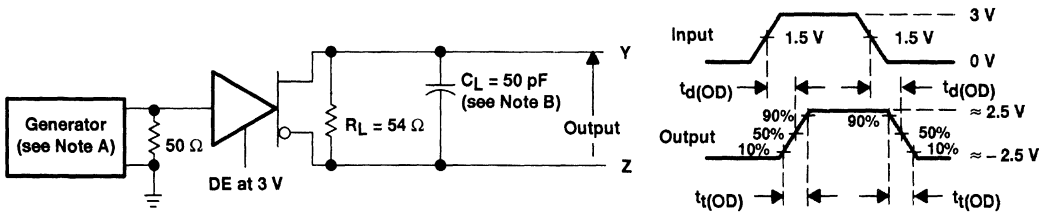


Figure 2. Driver V_{OD} Test Circuit



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR > 1 MHz, 50% duty cycle, $t_r \le 6$ ns, $t_f \le 6$ ns, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Differential Output Delay and Transition Time Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

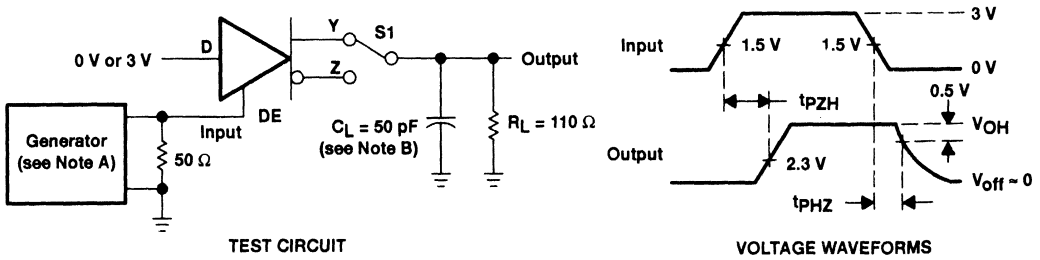


Figure 4. Driver Test Circuit and Enable and Disable Time Waveforms

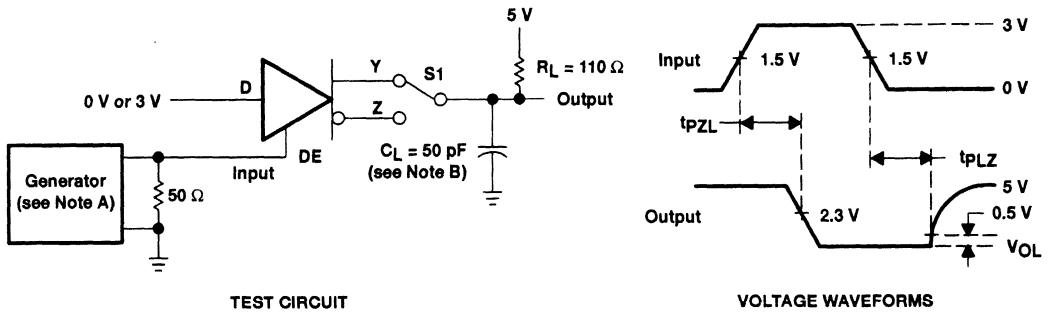


Figure 5. Driver Test Circuit and Enable and Disable Time Voltage Waveforms

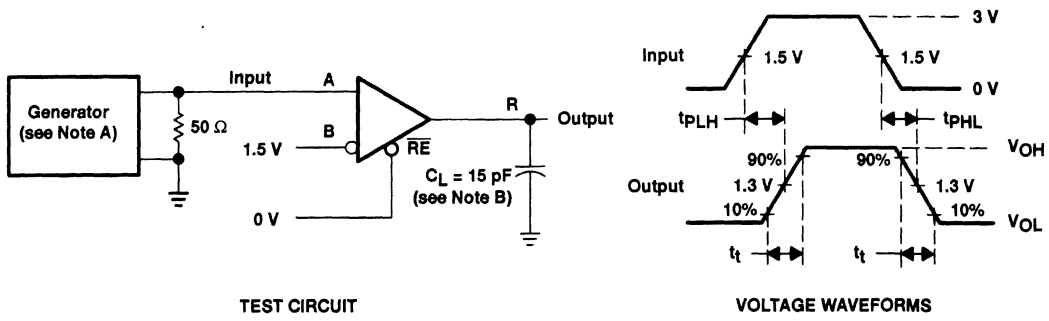


Figure 6. Receiver Test Circuit and Propagation Delay Time Voltage Waveforms

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

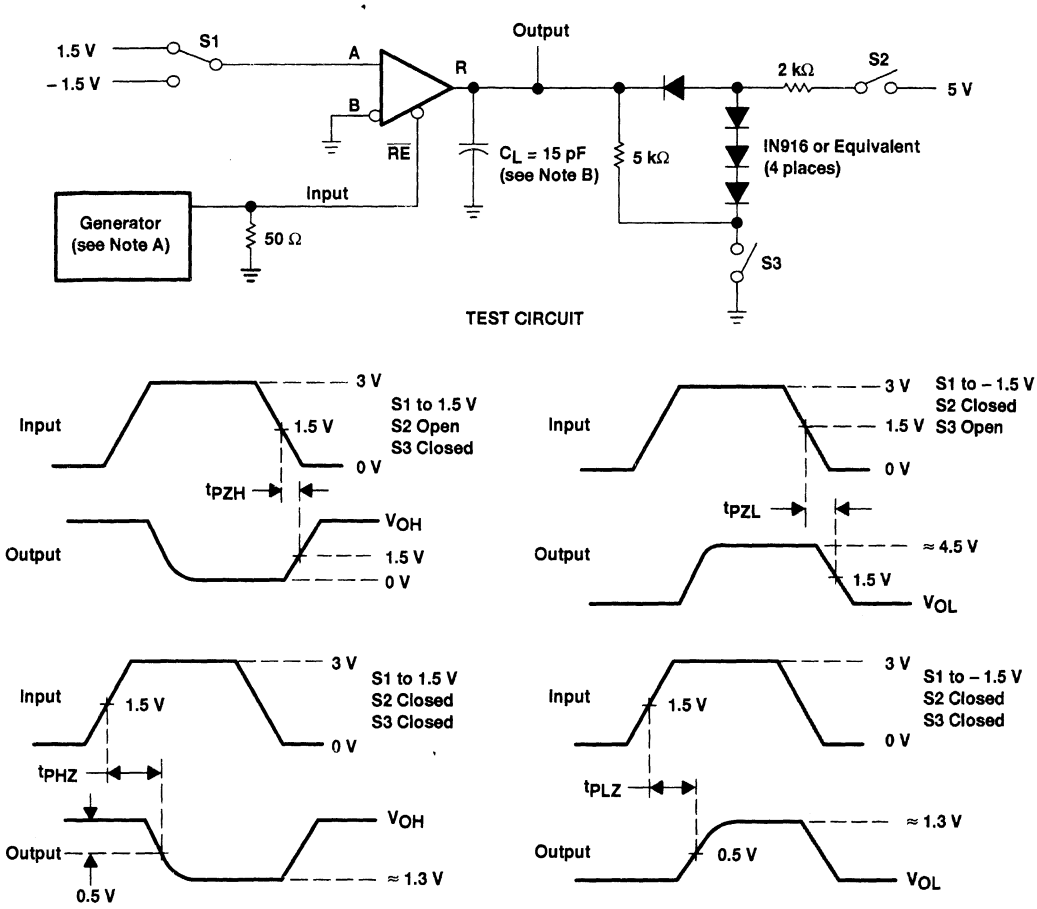


Figure 7. Receiver Output Enable and Disable Times

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

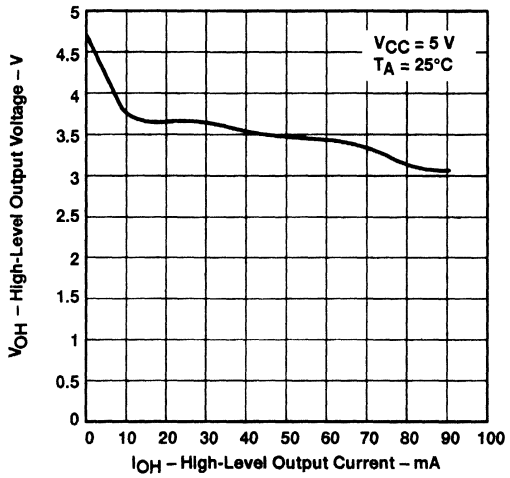


Figure 8

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

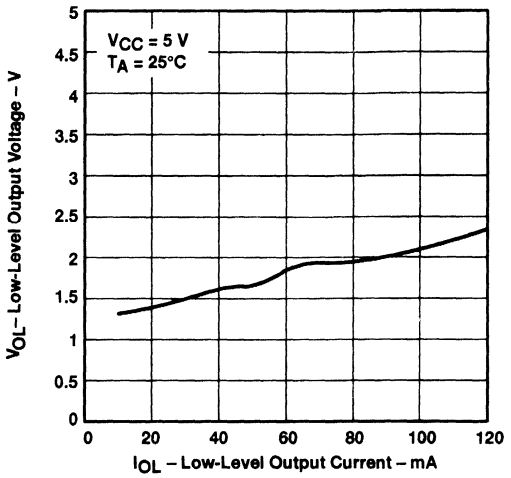


Figure 9

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

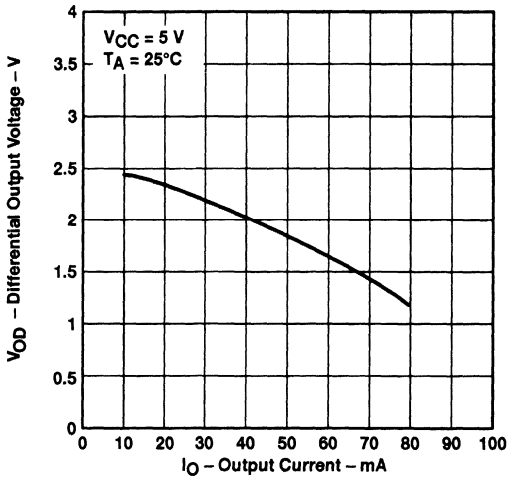


Figure 10

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

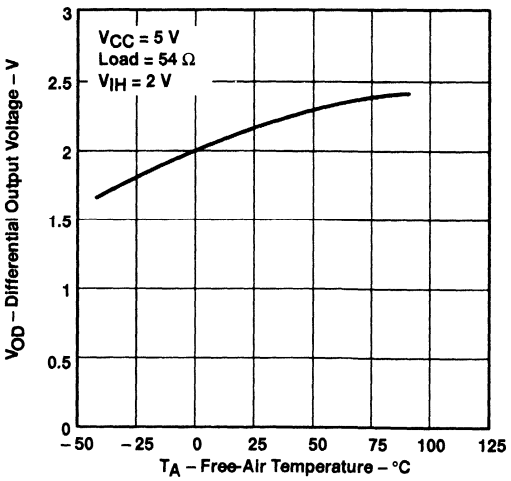


Figure 11

TYPICAL CHARACTERISTICS

DRIVER
DIFFERENTIAL DELAY TIMES
vs
FREE-AIR TEMPERATURE

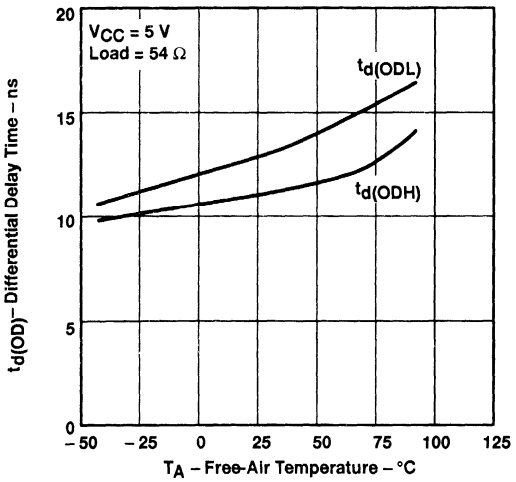


Figure 12

DRIVER
OUTPUT CURRENT
vs
SUPPLY VOLTAGE

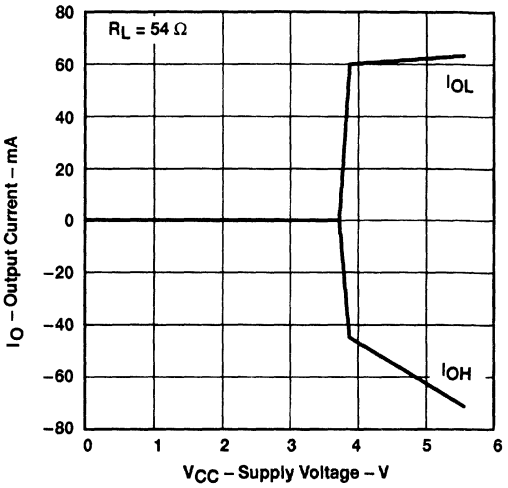


Figure 13

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

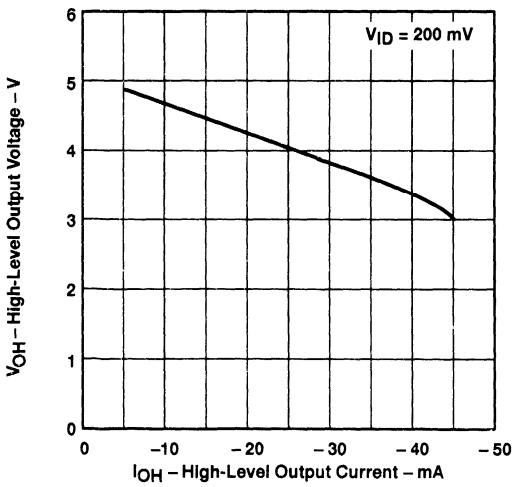


Figure 14

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

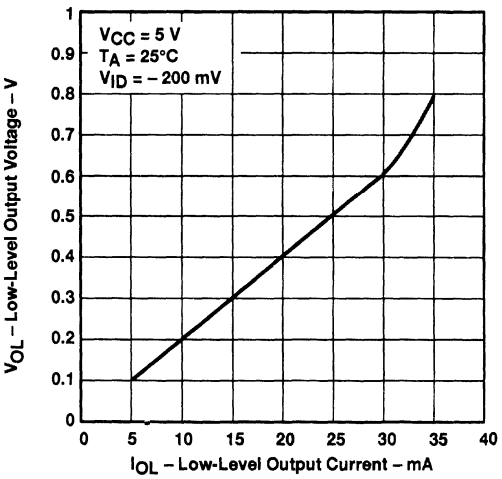


Figure 15

TYPICAL CHARACTERISTICS

RECEIVER
OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

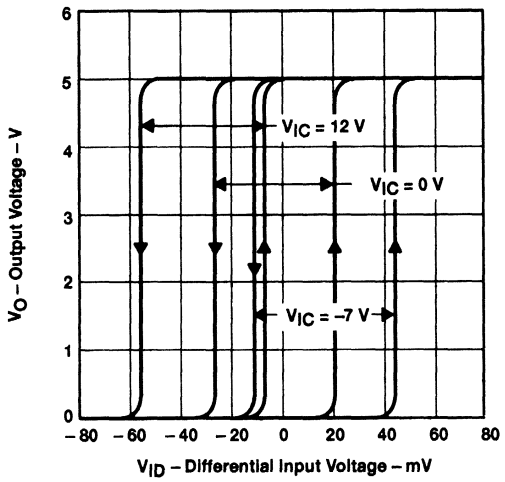


Figure 16

AVERAGE SUPPLY CURRENT
vs
FREQUENCY

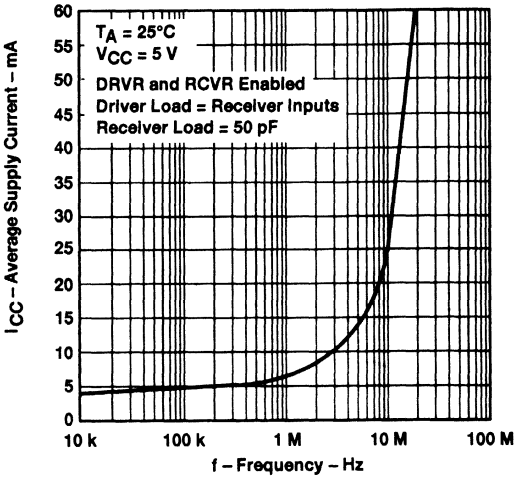


Figure 17

RECEIVER
BUS INPUT CURRENT
vs
INPUT VOLTAGE
(COMPLEMENTARY INPUT AT 0 V)

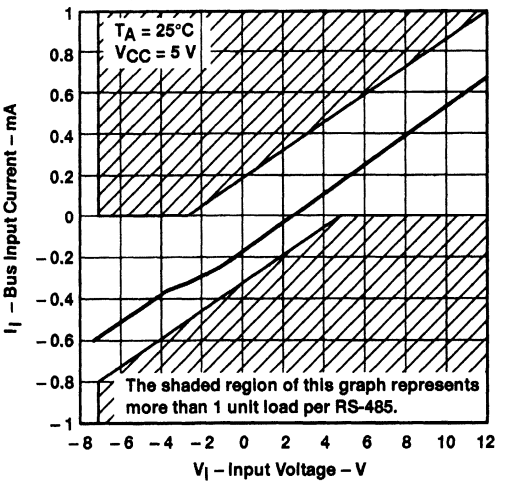


Figure 18

RECEIVER
PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

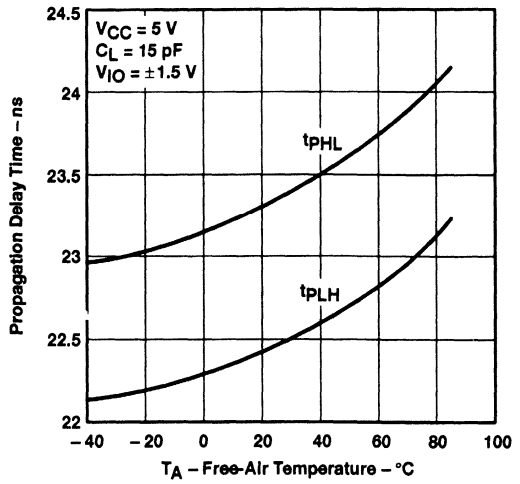
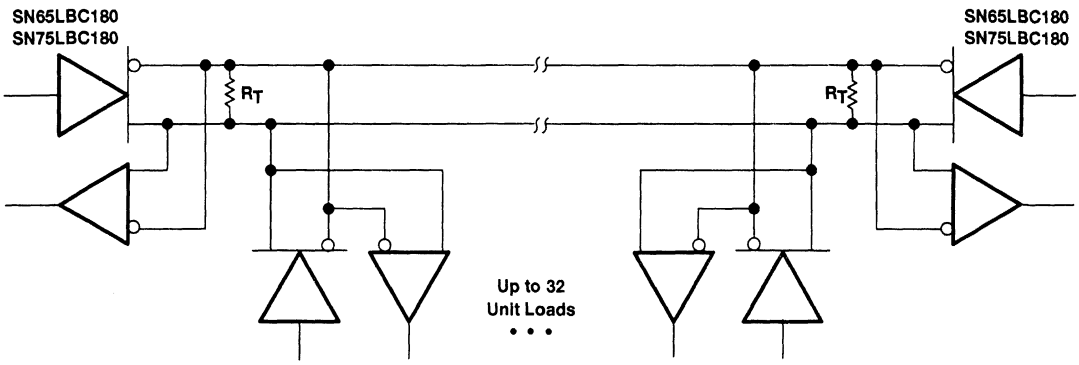


Figure 19

APPLICATION INFORMATION



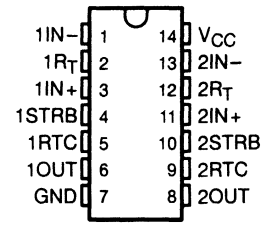
NOTE A. The line should be terminated at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible. One SN75LBC180 typically represents less than one unit load.

Figure 20. Typical Application Circuit

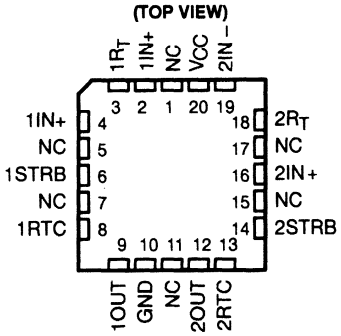
SLLS092B – OCTOBER 1972 – REVISED MAY 1995

- **Single 5-V Supply**
- **Differential Line Operation**
- **Dual Channels**
- **TTL Compatibility**
- **±15-V Common-Mode Input Voltage Range**
- **±15-V Differential Input Voltage Range**
- **Individual Channel Strobes**
- **Built-In Optional Line-Termination Resistor**
- **Individual Frequency Response Controls**
- **Designed for Use With Dual Differential Drivers SN55183 and SN75183**
- **Designed to Be Interchangeable With National Semiconductor DS7820A and DS8820A**

SN55182 . . . J OR W PACKAGE
DS8820A, SN75182 . . . D OR N PACKAGE
(TOP VIEW)



SN55182 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

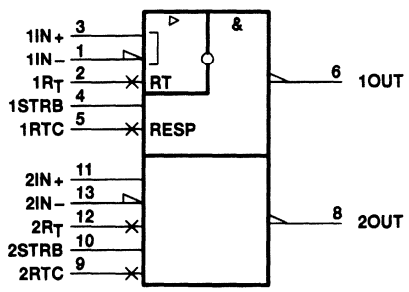
description

The DS8820A, SN55182, and SN75182 dual differential line receivers are designed to sense small differential signals in the presence of large common-mode noise. These devices give TTL-compatible output signals as a function of the polarity of the differential input voltage. The frequency response of each channel may be easily controlled by a single external capacitor to provide immunity to differential noise spikes. The output goes to a high level when the inputs are open circuited. A strobe input is provided which, when in the low level, disables the receiver and forces the output to a high level.

The receiver is of monolithic single-chip construction, and both halves of the dual circuits use common power supply and ground terminals.

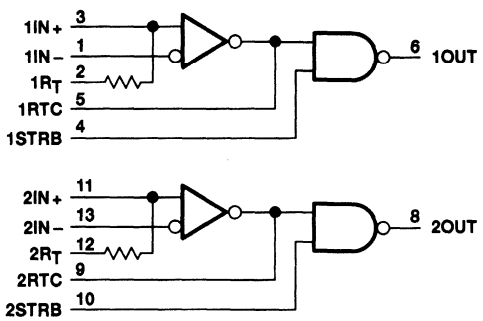
The SN55182 is characterized for operation over the full military temperature range of –55°C to 125°C. The DS8820A and SN75182 are characterized for operation from 0°C to 70°C.

logic symbol†

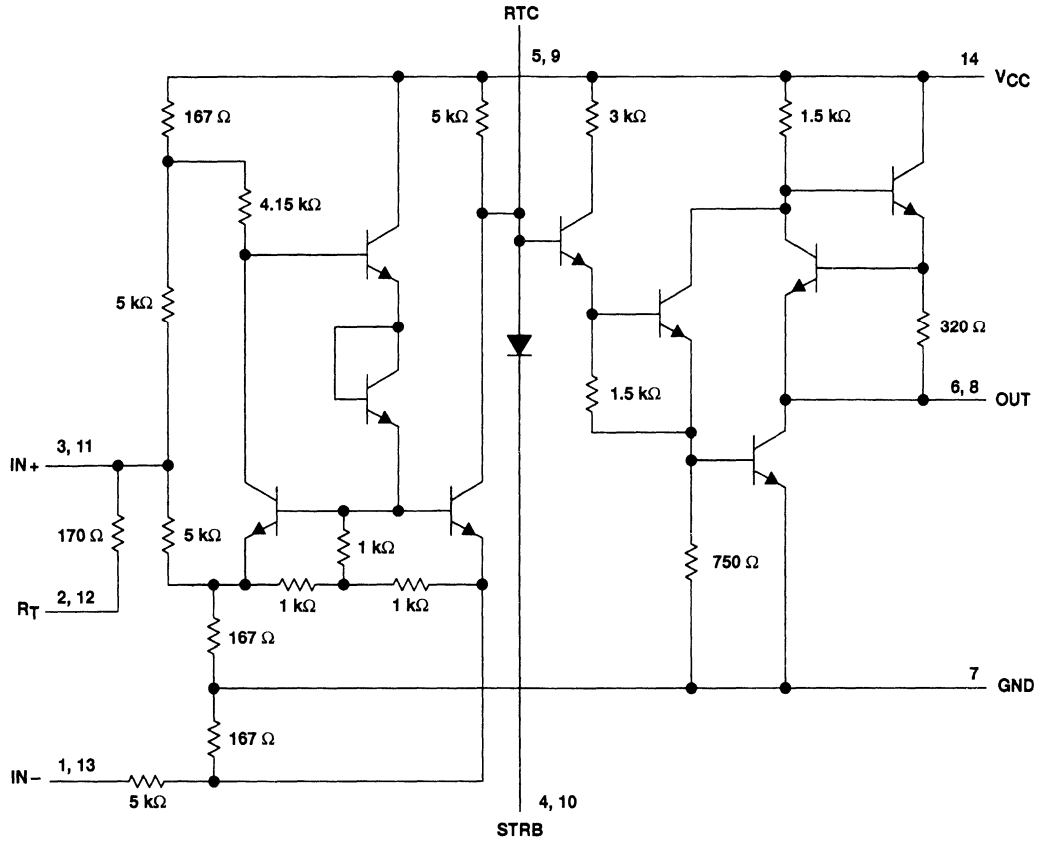


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)



schematic (each receiver)



Resistor values shown are nominal.
Pin numbers shown are for the D, J, N, and W packages.

FUNCTION TABLE

STRB	V_{ID}	OUT
L	X	H
H	H	H
H	L	L

H = $V_I \geq V_{IH}$ min or V_{ID} more positive than V_{TH} max
L = $V_I \leq V_{IL}$ max or V_{ID} more negative than V_{TL} max
X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

	SN55182	DS8820A SN75182	UNIT
Supply voltage, V_{CC} (see Note 1)	8	8	V
Common-mode input voltage, V_{IC}	±20	±20	V
Differential input voltage, V_{ID} (see Note 2)	±20	±20	V
Strobe input voltage, $V_{I(STROB)}$	8	8	V
Output sink current	50	50	mA
Continuous total power dissipation	See Dissipation Rating Table		
Operating free-air temperature range, T_A	−55 to 125	0 to 70	°C
Storage temperature range, T_{stg}	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package		260	°C
Case temperature for 60 seconds, T_C: FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package	300	300	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltage values are at the noninverting terminal with respect to the inverting terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	—
FK‡	1375 mW	11.0 mW/°C	880 mW	275 mW
J‡	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—
W‡	1000 mW	8.0 mW/°C	640 mW	200 mW

‡ In the FK, J, and W packages, SN55182 chips are alloy mounted.

recommended operating conditions

	SN55182			DS8820A, SN75182			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
Common-mode input voltage, V_{IC}			±15			±15	V
High-level strobe input voltage, $V_{IH(STRB)}$	2.1		5.5	2.1		5.5	V
Low-level strobe input voltage, $V_{IL(STRB)}$	0		0.9	0		0.9	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended ranges of V_{CC}, V_{IC}, and operating free-air temperature (unless otherwise noted)

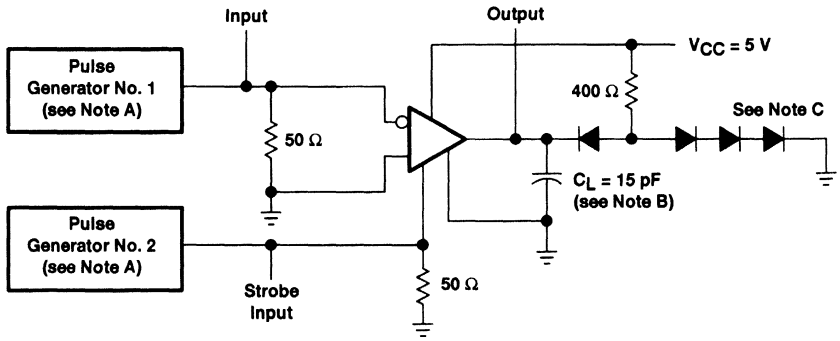
PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		V_O = 2.5 V, I_{OH} = −400 μA	V_{IC} = −3 V to 3 V			0.5	V
				V_{IC} = −15 V to 15 V			1	
V_{IT-}	Negative-going input threshold voltage		V_O = 0.4 V, I_{OL} = 16 mA	V_{IC} = −3 V to 3 V			−0.5	V
				V_{IC} = −15 V to 15 V			−1	
V_{OH}	High-level output voltage		V_{ID} = 1 V, I_{OH} = −400 μA	$V_{(STRB)}$ = 2.1 V,	2.5	4.2	5.5	V
			V_{ID} = −1 V, I_{OH} = −400 μA	$V_{(STRB)}$ = 0.4 V,	2.5	4.2	5.5	
V_{OL}	Low-level output voltage		V_{ID} = −1 V, I_{OL} = 16 mA	$V_{(STRB)}$ = 2.1 V,		0.25	0.4	V
I_I	Input current	Inverting input	V_{IC} = 15 V			3	4.2	mA
			V_{IC} = 0			0	−0.5	
			V_{IC} = −15 V			−3	−4.2	
		Noninverting input	V_{IC} = 15 V			5	7	mA
			V_{IC} = 0			−1	−1.4	
			V_{IC} = −15 V			−7	−9.8	
$I_{IH(STRB)}$	High-level strobe input current		$V_{(STRB)}$ = 5.5 V				5	μA
$I_{IL(STRB)}$	Low-level strobe input current		$V_{(STRB)}$ = 0			−1	−1.4	mA
r_i	Input resistance	Inverting input			3.6	5		kΩ
		Noninverting input			1.8	2.5		kΩ
	Line terminating resistance		T_A = 25°C		120	170	250	Ω
I_{OS}	Short-circuit output current		V_{CC} = 5.5 V,	V_O = 0	−2.8	−4.5	−6.7	mA
I_{CC}	Supply current (average per receiver)		V_{IC} = 15 V,	V_{ID} = −1 V		4.2	6	mA
			V_{IC} = 0,	V_{ID} = −0.5 V		6.8	10.2	
			V_{IC} = −15 V,	V_{ID} = −1 V		9.4	14	

† Unless otherwise noted, $V_{(STRB)} \geq 2.1$ V or open.
‡ All typical values are at V_{CC} = 5 V, V_{IC} = 0, and T_A = 25°C.

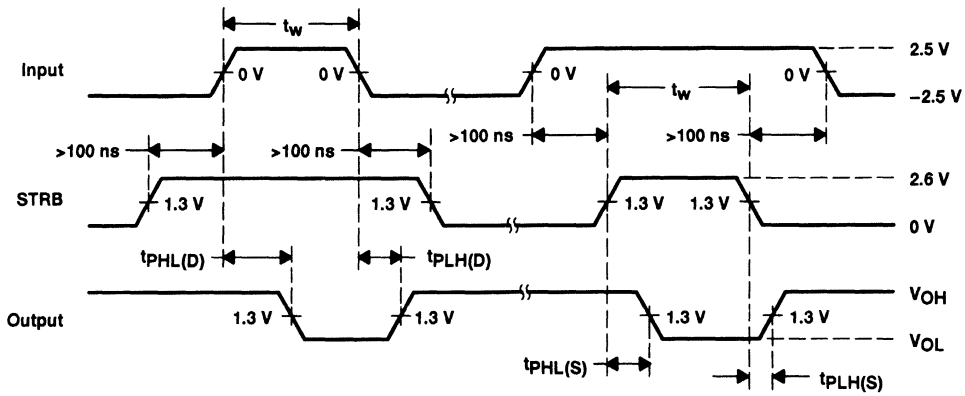
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH(D)}$	Propagation delay time, low- to high-level output from differential input	R_L = 400 Ω, C_L = 15 pF, See Figure 1		18	40	ns
$t_{PHL(D)}$	Propagation delay time, high- to low-level output from differential input			31	45	ns
$t_{PLH(S)}$	Propagation delay time, low- to high-level output from STRB input			9	30	ns
$t_{PHL(S)}$	Propagation delay time, high- to low-level output from STRB input			15	25	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_O = 50 Ω, $t_r \leq 10$ ns, $t_f \leq 10$ ns, t_w = 0.5 ±0.1 µs, PRR ≤ 1 MHz.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

DIFFERENTIAL INPUT THRESHOLD VOLTAGE
vs
SUPPLY VOLTAGE

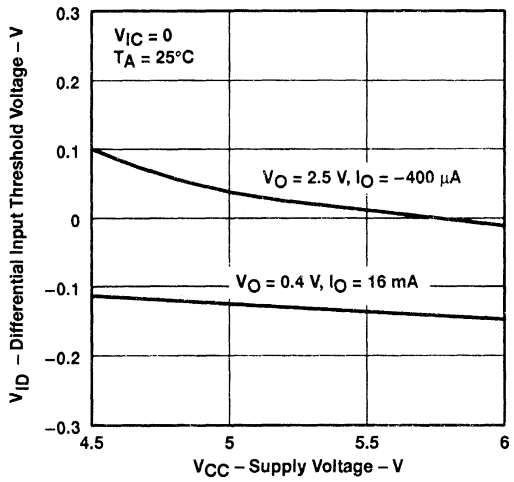


Figure 2

DIFFERENTIAL INPUT THRESHOLD VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

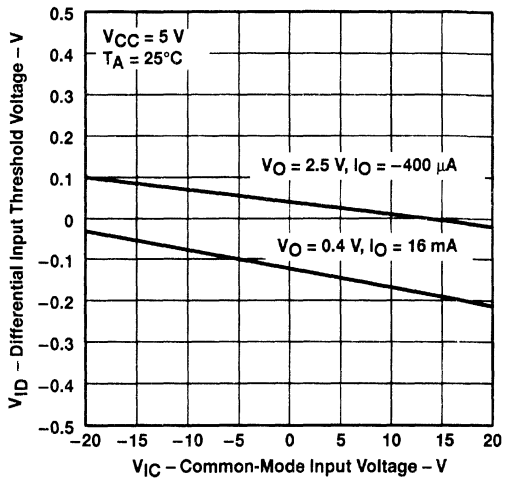


Figure 3

DIFFERENTIAL INPUT THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

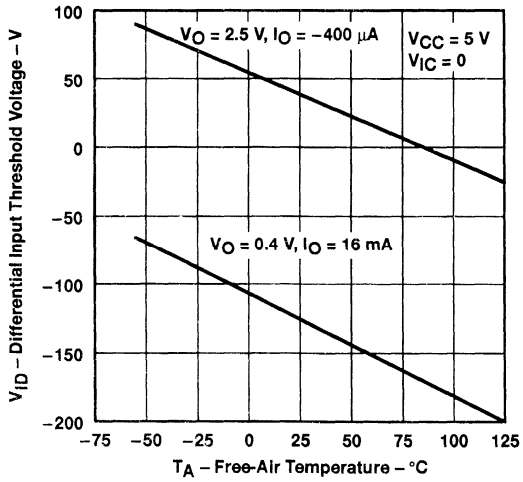


Figure 4

† Data for temperatures below 0°C and above 70°C are applicable to SN55182 circuits only.

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

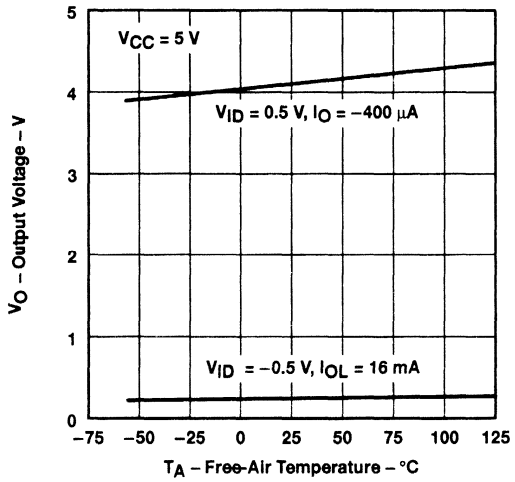


Figure 5

VOLTAGE TRANSFER CHARACTERISTICS

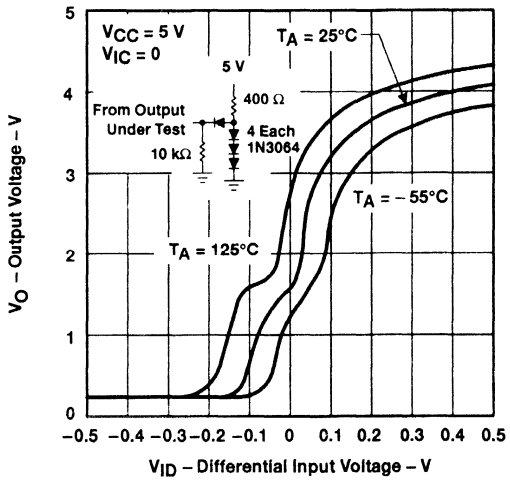


Figure 6

INPUT CURRENT
vs
INPUT VOLTAGE

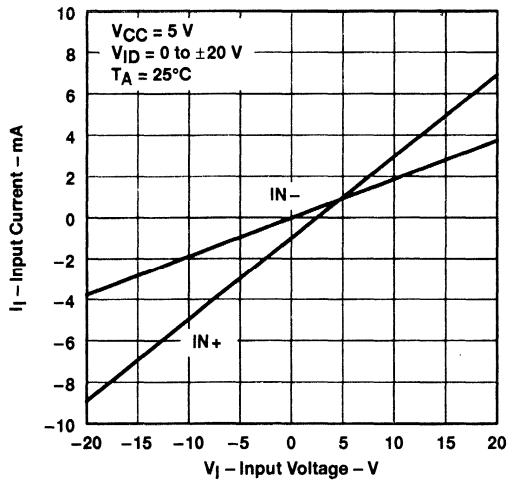


Figure 7

TERMINATING RESISTANCE
vs
FREE-AIR TEMPERATURE

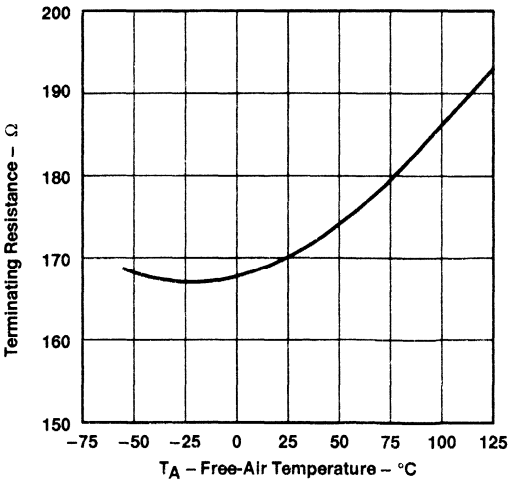


Figure 8

† Data for temperatures below 0°C and above 70°C are applicable to SN55182 circuits only.

TYPICAL CHARACTERISTICS†

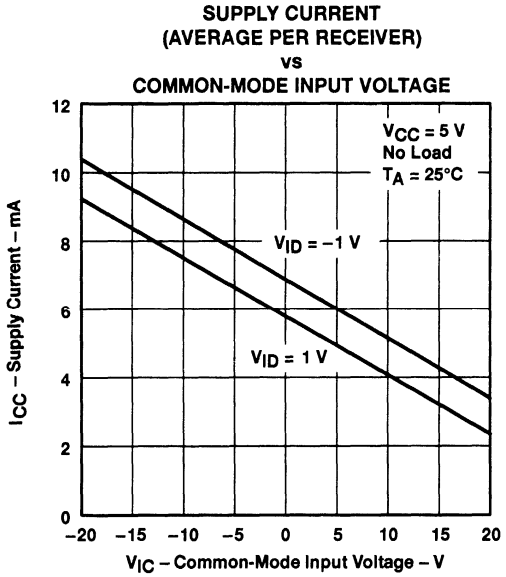


Figure 9

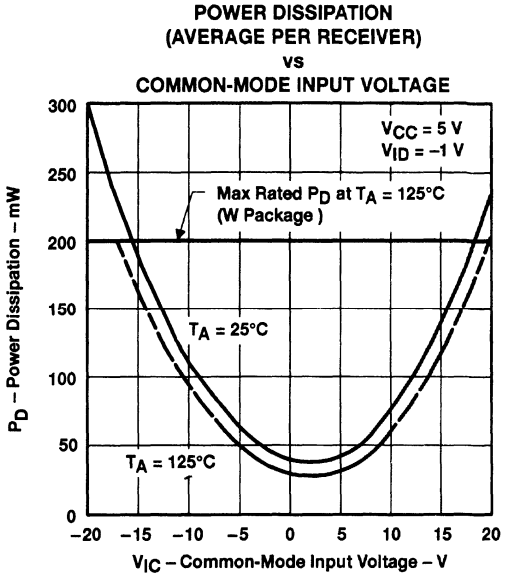
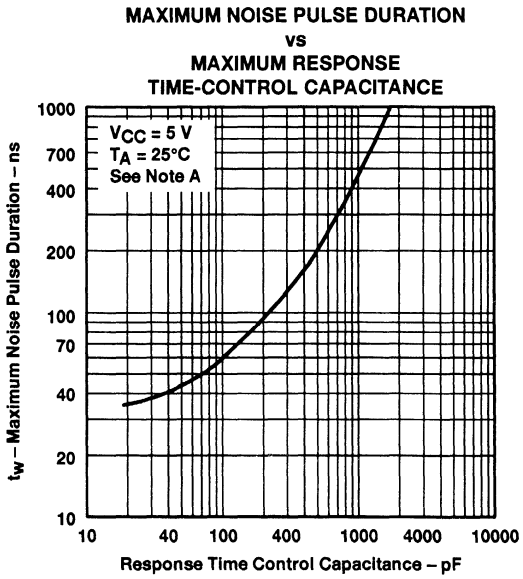
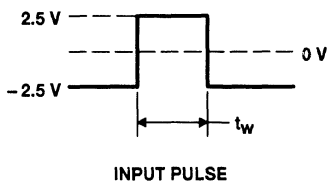


Figure 10





NOTE A: Figure 11 shows the maximum duration of the illustrated pulse that can be applied differently without the output changing from the low to high level.

Figure 11

† Data for temperatures below 0°C and above 70°C are applicable to SN55182 circuits only.

TYPICAL CHARACTERISTICS†

PROPAGATION DELAY TIME FROM DIFFERENTIAL INPUT VS FREE-AIR TEMPERATURE

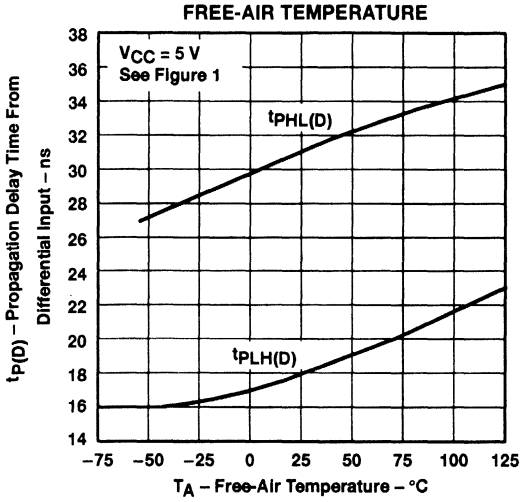


Figure 12

PROPAGATION DELAY TIME FROM STROBE INPUT VS FREE-AIR TEMPERATURE

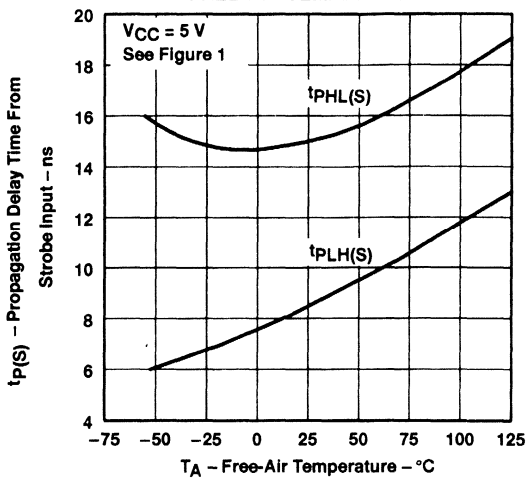
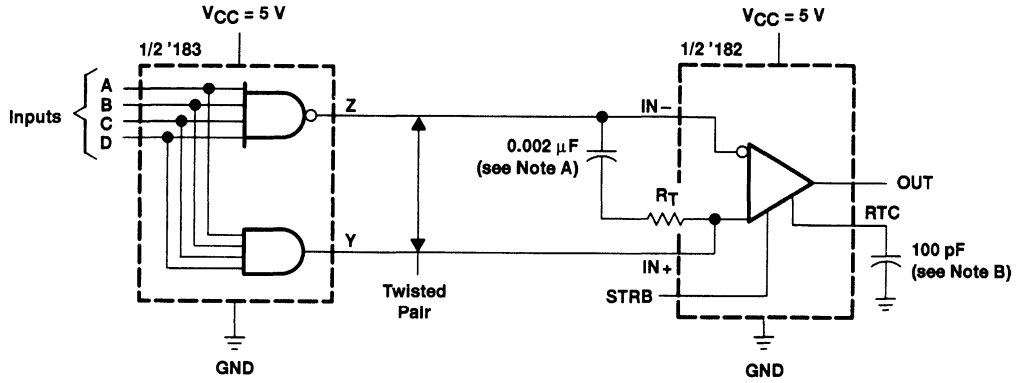


Figure 13

† Data for temperatures below 0°C and above 70°C are applicable to SN55182 circuits only.

APPLICATION INFORMATION



NOTES: A. When the inputs are open circuited, the output is high. A capacitor may be used for dc isolation of the line-terminating resistor. At the frequency of operation, the impedance of the capacitor should be relatively small.

Example: let $f = 5$ MHz
$C = 0.002\ \mu F$

$$Z_{(C)} = \frac{1}{2\pi fC} = \frac{1}{2\pi\ (5 \times 10^{6})\ (0.002 \times 10^{-6})}$$

$$Z_{(C)} \approx 16\ \Omega$$

B. Use of a capacitor to control response time is optional.

Figure 14. Transmission of Digital Data Over Twisted-Pair Line

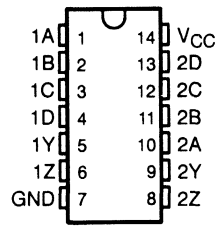
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

DS8830, SN55183, SN75183
DUAL DIFFERENTIAL LINE DRIVERS

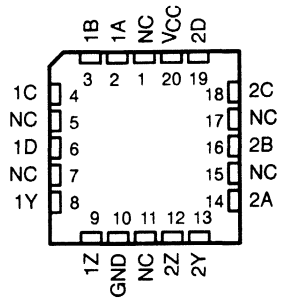
SLLS093B – OCTOBER 1972 – REVISED – MAY 1995

- **Single 5-V Supply**
- **Differential Line Operation**
- **Dual Channels**
- **TTL Compatibility**
- **Short-Circuit Protection of Outputs**
- **Output Clamp Diodes to Terminate Line Transients**
- **High-Current Outputs**
- **Quad Inputs**
- **Single-Ended or Differential AND/NAND Outputs**
- **Designed for Use With Dual Differential Drivers SN55182 and SN75182**
- **Designed to Be Interchangeable With National Semiconductor DS7830 and DS8830**

SN55183 . . . J OR W PACKAGE
DS8830, SN75183 . . . D OR N PACKAGE
(TOP VIEW)



SN55183 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

THE DS8830 AND SN75183 ARE NOT RECOMMENDED FOR NEW DESIGNS

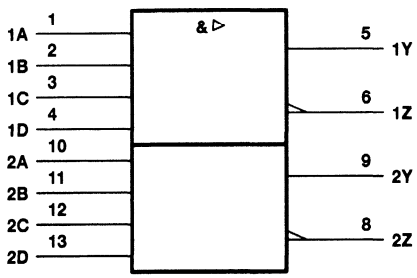
description

The DS8830, SN55183, and SN75183 dual differential line drivers are designed to provide differential output signals with high-current capability for driving balanced lines, such as twisted pair, at normal line impedances without high power dissipation. These devices may be used as TTL expander/phase splitters, as the output stages are similar to TTL totem-pole outputs.

The driver is of monolithic single-chip construction, and both halves of the dual circuits use common power supply and ground terminals.

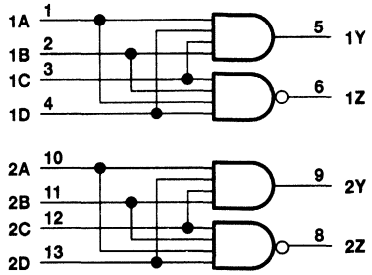
The SN55183 is characterized for operation over the full military temperature range of −55°C to 125°C. The DS8830 and SN75183 are characterized for operation from 0°C to 70°C.

logic symbol†



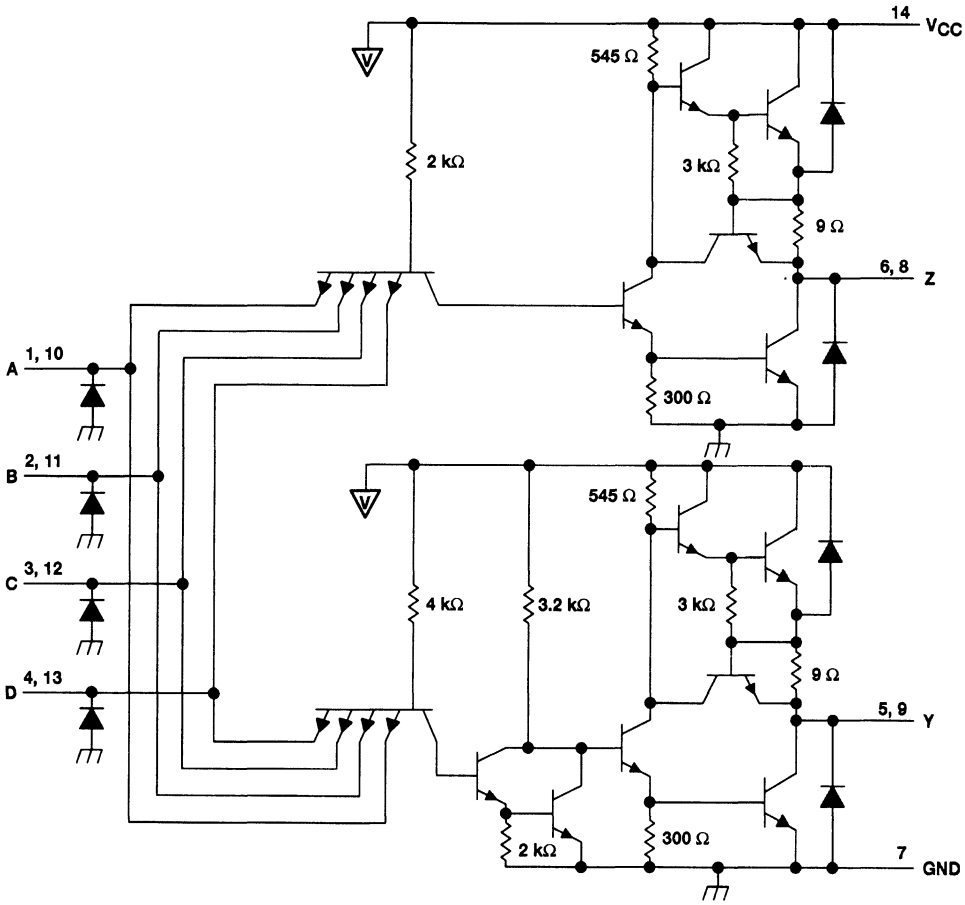
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)



positive logic: $Y = ABCD$, $Z = \overline{ABCD}$

schematic (each driver)



Resistor values shown are nominal.
Pin numbers shown are for the D, N, J, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

	SN55183	DS8830 SN75183	UNIT
Supply voltage, V_{CC} (see Note 1)	7	7	V
Input voltage, V_I	5.5	5.5	V
Duration of output short circuit (see Note 2)	1	1	s
Continuous total power dissipation	See Dissipation Rating Table		
Operating free-air temperature range, T_A	−55 to 125	0 to 70	°C
Storage temperature range, T_{stg}	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds, T_C: FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package		260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300	300	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Not more than one output should be shorted to ground at any one time.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	–
FK‡	1375 mW	11.0 mW/°C	880 mW	275 mW
J‡	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	–
W	1000 mW	8.0 mW/°C	640 mW	200 mW

‡ In the FK and J packages, SN55183 chips are alloy mounted and SN75183 chips are glass mounted.

recommended operating conditions

	SN55183			DS8830, SN75183			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
High-level output current, I_{OH}			−40			−40	mA
Low-level output current, I_{OL}			40			40	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended ranges of V_{CC} and operating free-air temperature (unless otherwise noted)

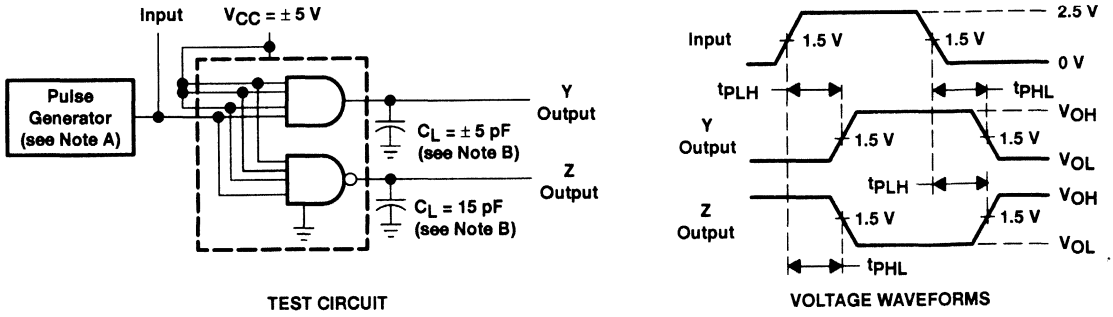
PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	Y (AND) outputs	V_{IH} = 2 V,	I_{OH} = −0.8 mA		2.4			V
			V_{IH} = 2 V,	I_{OH} = −40 mA		1.8	3.3		
V_{OL}	Low-level output voltage		V_{IL} = 0.8 V,	I_{OL} = 32 mA			0.2		V
			V_{IL} = 0.8 V,	I_{OL} = 40 mA			0.22	0.4	
V_{OH}	High-level output voltage	Z (NAND) outputs	V_{IL} = 0.8 V,	I_{OH} = −0.8 mA		2.4			V
			V_{IL} = 0.8 V,	I_{OH} = −40 mA		1.8	3.3		
V_{OL}	Low-level output voltage		V_{IH} = 2 V,	I_{OL} = 32 mA			0.2		V
			V_{IH} = 2 V,	I_{OL} = 40 mA			0.22	0.4	
I_{IH}	High-level input current		V_{IH} = 2.4 V					120	µA
I_I	Input current at maximum input voltage		V_{IH} = 5.5 V					2	mA
I_{IL}	Low-level input current		V_{IL} = 0.4 V					−4.8	mA
I_{OS}	Short-circuit output current‡		V_{CC} = 5 V,	T_A = 125°C		−40	−100	−120	mA
I_{CC}	Supply current (average per driver)		V_{CC} = 5 V,	All inputs at 5 V,	No load		10	18	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level Y output	AND gates	C_L = 15 pF, See Figure 1(a)		8	12	ns
t_{PHL}	Propagation delay time, high- to low-level Y output				12	18	ns
t_{PLH}	Propagation delay time, low- to high-level Z output	NAND gates			6	12	ns
t_{PHL}	Propagation delay time, high- to low-level Z output				6	8	
t_{PLH}	Propagation delay time, low- to high-level differential output	Y output with respect to Z output	R_L = 100 Ω in series with 5000 pF, See Figure 1(b)		9	16	ns
t_{PHL}	Propagation delay time, high- to low-level differential output				8	16	ns

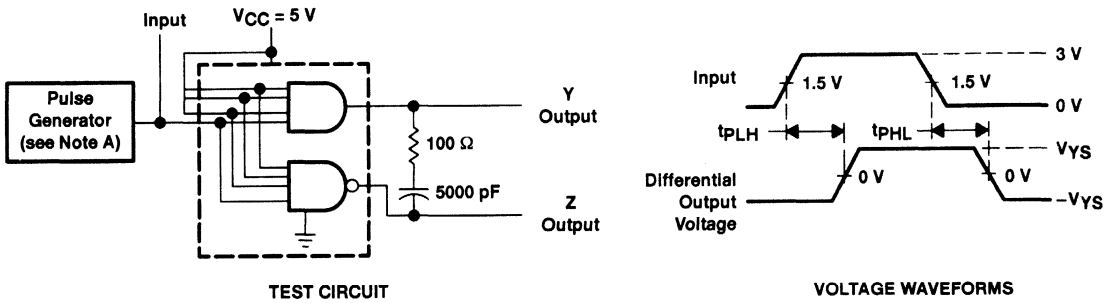
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

VOLTAGE WAVEFORMS

(a) OUTPUTS Y AND Z



TEST CIRCUIT

VOLTAGE WAVEFORMS

(b) DIFFERENTIAL OUTPUT

NOTES: A. The pulse generators have the following characteristics: Z_O = 50 Ω, $t_r \leq 10$ ns, $t_f \leq 10$ ns, t_w = 0.5 μS, PRR ≤ 1 MHz.
B. C_L includes probe and jig capacitance.
C. Waveforms are monitored on an oscilloscope with $r_i \geq 1$ MΩ.

Figure 1. Test Circuits and Voltage Waveforms

TYPICAL CHARACTERISTICS†

INPUT THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

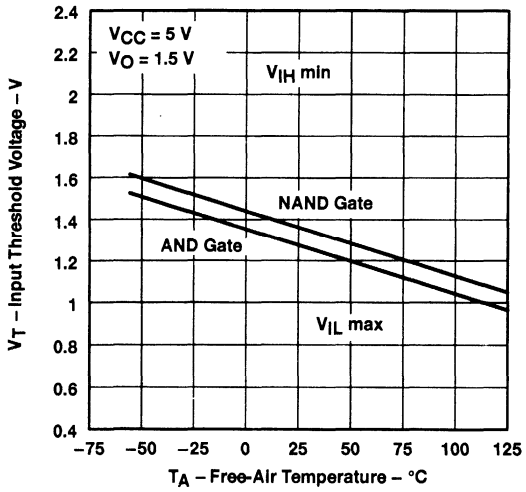


Figure 2

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

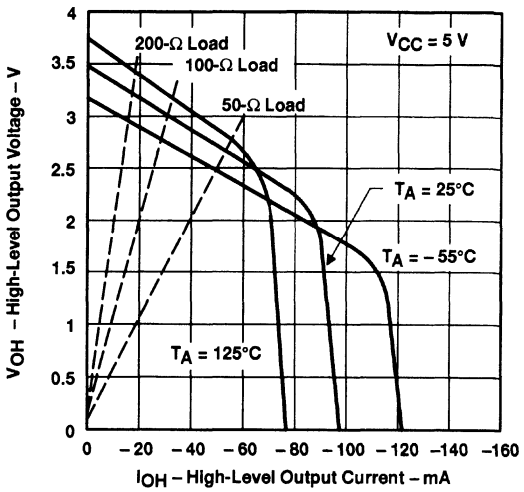


Figure 3

DIFFERENTIAL OUTPUT VOLTAGE
vs
DIFFERENTIAL OUTPUT CURRENT

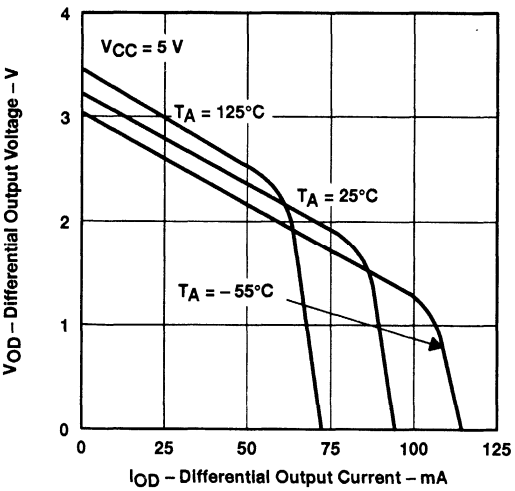


Figure 4

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

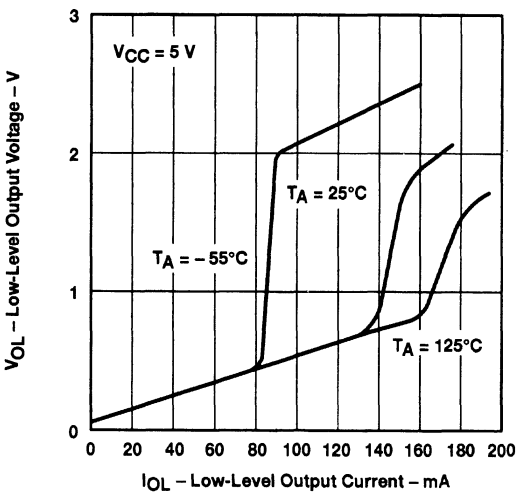


Figure 5

† Data for temperatures below 0°C and above 70°C are applicable to SN55183 circuits only.

TYPICAL CHARACTERISTICS†

PROPAGATION DELAY TIME (DIFFERENTIAL OUTPUT) vs FREE-AIR TEMPERATURE

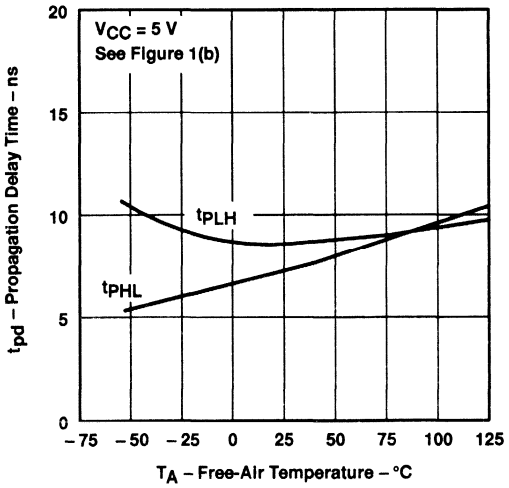


Figure 6

TOTAL POWER DISSIPATION (BOTH DRIVERS) vs FREQUENCY

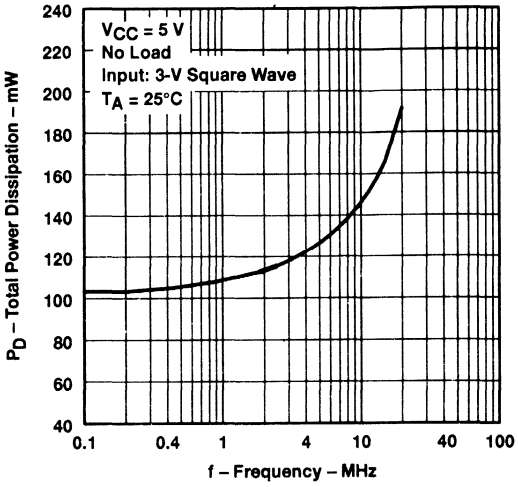
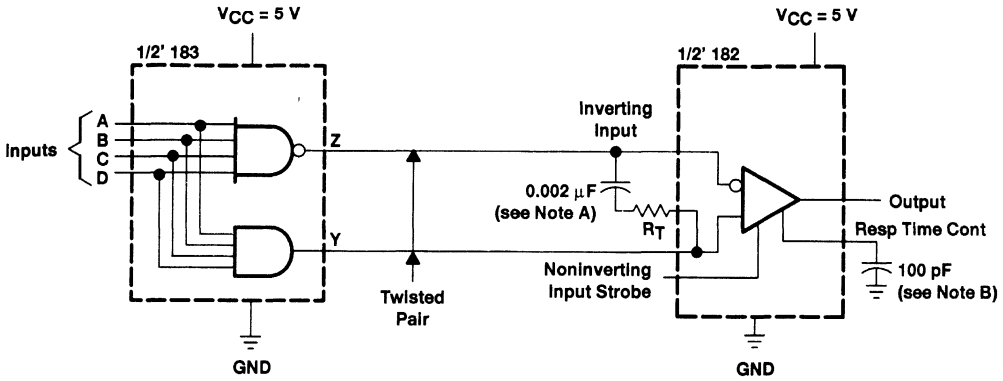


Figure 7

† Data for temperatures below 0°C and above 70°C are applicable to SN55183 circuits only.

APPLICATION INFORMATION



NOTES: A. When the inputs are open circuited, the output is high. A capacitor may be used for dc isolation of the line-terminating resistor. At the frequency of operation, the impedance of the capacitor should be relatively small.

Example: let $f = 5$ MHz
$C = 0.002\ \mu F$

$$Z_{(circuit)} = \frac{1}{2\pi fC} = \frac{1}{2\pi\ (5 \times 10^{6})\ (0.002 \times 10^{-6})}$$

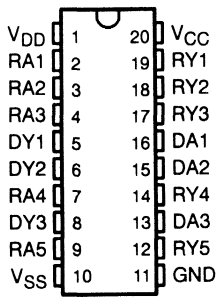
$$Z_{(circuit)} \approx 16\ \Omega$$

B. Use of a capacitor to control response time is optional.

Figure 8. Transmission of Digital Data Over Twisted-Pair Line

- **Single Chip With Easy Interface Between UART and Serial Port Connector of IBM PC/AT™ and Compatibles**
- **Three Drivers and Five Receivers Meet or Exceed the Requirements of EIA/TIA-232-E and ITU v.28 Standards**
- **Designed to Support Data Rates Up To 120 kbps**
- **ESD Protection Meets or Exceeds 10 kV on RS-232 Pins and 5 kV on All Other Pins (Human-Body Model)**
- **Pinout Compatible With the SN75C185**

DW OR N PACKAGE
(TOP VIEW)



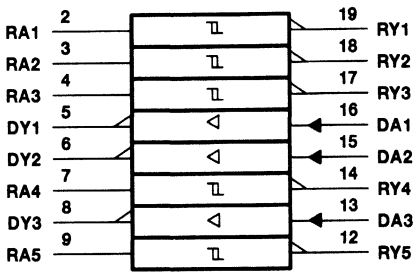
description

The SN75185 combines three drivers and five receivers from TI trade-standard SN75188 and SN75189 bipolar quadruple drivers and receivers, respectively. The pinout matches the flow-through design of the SN75C185 to decrease the part count, reduce the board space required, and allow easy interconnection of the UART and serial-port connector of IBM PC/AT™ and compatibles. The bipolar circuits and processing of the SN75185 provides a rugged low-cost solution for this function at the expense of quiescent power and external passive components relative to the SN75C185.

The SN75185 complies with the requirements of the EIA/TIA 232-E and ITU (formally CCITT) v.28 standards. These standards are for data interchange between a host computer and peripheral at signalling rates up to 20 k-bits/s. The switching speeds of the SN75185 are fast enough to support rates up to 120 k-bits/s with lower capacitive loads (shorter cables). Interoperability at the higher signalling rates cannot be assured unless the designer has design control of the cable and the interface circuits at both ends. For interoperability at signalling rates to 120 k-bits/s, use of EIA/ITA-423-B (ITU v.10) and EIA/ITA-422-B (ITU v.11) standards are recommended.

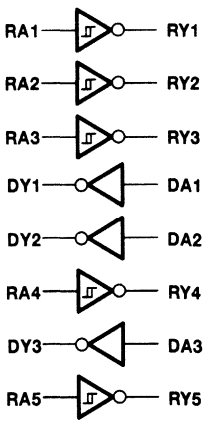
The SN75185 is characterized for operation over the temperature range of 0°C to 70°C.

logic symbol†



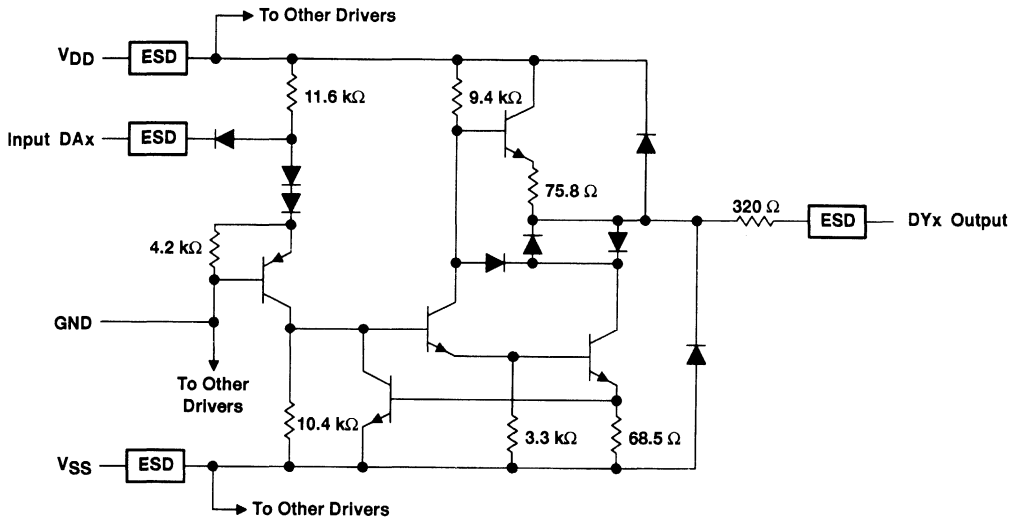
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



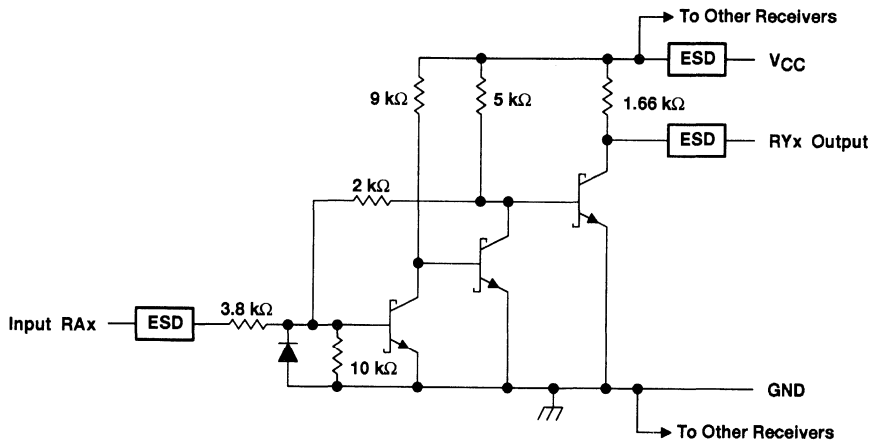
PC/AT is a trademark of IBM Corporation.

schematic of drivers



Resistor values shown are nominal.

schematic (each receiver)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 10 V
Supply voltage, V_{DD} (see Note 1) ..... 15 V
Supply voltage, V_{SS} (see Note 1) ..... −15 V
Input voltage range: Driver ..... −15 V to 7 V
Receiver ..... −30 V to 30 V
Driver output voltage range ..... −15 V to 15 V
Receiver low-level output current ..... 20 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Electrostatic discharge: Human-body model: RS-232 pins, class 3, A (see Note 2) ..... 10 kV
Human-body model: All pins, class 3, A (see Note 3) ..... 5 kV
Machine model: RS-232 pins, class 3, B (see Note 4) ..... 600 V
Machine model: All pins, class 3, B (see Note 3) ..... 300 V
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to the network ground terminal.
2. RS-232 pins are tested with respect to ground and each other.
3. Per MIL-STD 883C, Method 3015.7
4. RS-232 pins are tested with respect to ground.

DISSIPATION RATING TABLE‡

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A \le 70°C$ POWER RATING
DW	1125 mW	9 mW/°C	720 mW
N	1150 mW	9.2 mW/°C	736 mW

‡ This is the inverse of the traditional junction-to-case thermal resistance ($R_{\theta JA}$).

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		7.5	9	15	V
Supply voltage, V_{SS}		−7.5	−9	−15	V
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level input voltage, V_{IH} (driver only)		1.9			V
Low-level input voltage, V_{IL} (driver only)				0.8	V
High-level output current, I_{OH}	Driver			−6	mA
	Receiver			−0.5	
Low-level output current, I_{OL}	Driver			6	mA
	Receiver			16	
Operating free-air temperature, T_A		0		70	°C

supply currents

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
I_{DD}	Supply current from V_{DD}	All inputs at 1.9 V,	No load	V_{DD} = 9 V, V_{SS} = −9 V		15	mA
				V_{DD} = 12 V, V_{SS} = −12 V		19	
				V_{DD} = 15 V, V_{SS} = −15 V		25	
		All inputs at 0.8 V,	No load	V_{DD} = 9 V, V_{SS} = −9 V		4.5	mA
				V_{DD} = 12 V, V_{SS} = −12 V		5.5	
				V_{DD} = 15 V, V_{SS} = −15 V		9	
I_{SS}	Supply current from V_{SS}	All inputs at 1.9 V,	No load	V_{DD} = 9 V, V_{SS} = −9 V		−15	mA
				V_{DD} = 12 V, V_{SS} = −12 V		−19	
				V_{DD} = 15 V, V_{SS} = −15 V		−25	
		All inputs at 0.8 V,	No load	V_{DD} = 9 V, V_{SS} = −9 V		−3.2	mA
				V_{DD} = 12 V, V_{SS} = −12 V		−3.2	
				V_{DD} = 15 V, V_{SS} = −15 V		−3.2	
I_{CC}	Supply current from V_{CC}	V_{CC} = 5 V,	All inputs at 5 V,	No load		30	mA

DRIVER SECTION

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 9 V, V_{SS} = −9 V, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_{IL} = 0.8 V,	R_L = 3 kΩ,	See Figure 1	6	7.5		V
V_{OL}	Low-level output voltage (see Note 5)	V_{IH} = 1.9 V,	R_L = 3 kΩ,	See Figure 1		−7.5	−6	V
I_{IH}	High-level input current	V_I = 5 V,	See Figure 2				10	μA
I_{IL}	Low-level input current	V_I = 0,	See Figure 2				−1.6	mA
$I_{OS(H)}$	High-level short-circuit output current (see Note 6)	V_{IL} = 0.8 V,	V_O = 0,	See Figure 1	−4.5	−12	−19.5	mA
$I_{OS(L)}$	Low-level short-circuit output current	V_{IH} = 2 V,	V_O = 0,	See Figure 1	4.5	12	19.5	mA
r_o	Output resistance (see Note 7)	V_{CC} = V_{DD} = V_{SS} = 0,	V_O = −2 V to 2 V		300			Ω

NOTES: 5. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only (e.g., if −10 V is maximum, the typical value is a more negative voltage).
6. Output short-circuit conditions must maintain the total power dissipation below absolute maximum ratings.
7. Test conditions are those specified by EIA-232-E and as listed above.

switching characteristics, V_{CC} = 5 V, V_{DD} = 12 V, V_{SS} = −12 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 3		315	500	ns
t_{PHL}	Propagation delay time, high-to-low-level output			75	175	ns
t_{TLH}	Transition time, low-to-high-level output	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 3		60	100	ns
		R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF, See Figure 3 and Note 8		1.7	2.5	μs
t_{THL}	Transition time, high-to-low-level output	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 3		40	75	ns
		R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF, See Figure 3 and Note 9		1.5	2.5	μs

NOTES: 8. Measured between −3-V and 3-V points of the output waveform (EIA-232-E conditions), all unused inputs are tied.
9. Measured between 3-V and −3-V points of the output waveform (EIA-232-E conditions), all unused inputs are tied.

RECEIVER SECTION

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{T+}	Positive-going threshold voltage	See Figure 5	T_A = 25°C	1.75	1.9	2.3	V
			T_A = 0°C to 70 °C	1.55		2.3	
V_{T-}	Negative-going threshold voltage			0.75	0.97	1.25	
V_{hys}	Input hysteresis ($V_{T+} - V_{T-}$)			0.5			
V_{OH}	High-level output voltage	I_{OH} = −0.5 mA	V_{IH} = 0.75 V	2.6	4	5	V
			Inputs open	2.6			
V_{OL}	Low-level input voltage	I_{OL} = 10 mA,	V_I = 3 V		0.2	0.45	V
I_{IH}	High-level input current	V_I = 25 V,	See Figure 5	3.6		8.3	mA
		V_I = 3 V,	See Figure 5	0.43			
I_{IL}	Low-level output current	V_I = −25 V,	See Figure 5	−3.6		−8.3	mA
		V_I = −3 V,	See Figure 5	−0.43			
I_{OS}	Short-circuit output current	See Figure 4			−3.4	−12	mA

† All typical values are at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 9 V, and V_{SS} = −9 V.

switching characteristics, V_{CC} = 5 V, V_{DD} = 12 V, V_{SS} = −12 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 5 kΩ, See Figure 6		107	500	ns
t_{PHL}	Propagation delay time, high-to-low-level output			42	150	ns
t_{TLH}	Transition time, low-to-high-level output			175	525	ns
t_{THL}	Transition time, high-to-low-level output			16	60	ns

PARAMETER MEASUREMENT INFORMATION

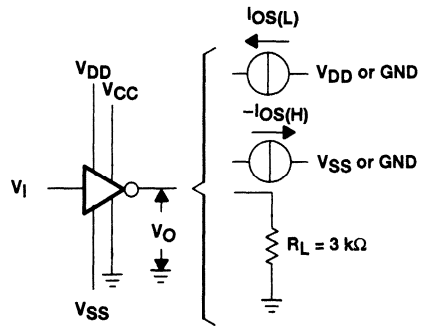


Figure 1. Driver Test Circuit for V_{OH}, V_{OL}, $I_{OS(H)}$, and $I_{OS(L)}$

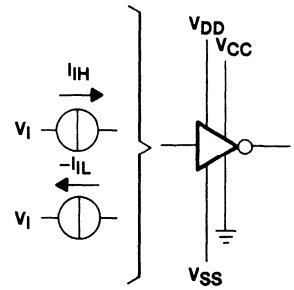
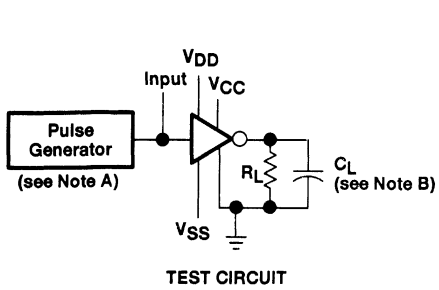
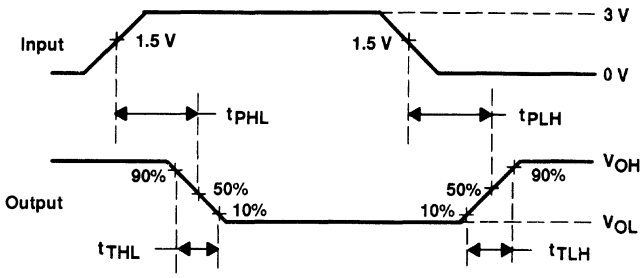


Figure 2. Driver Test Circuit for I_{IH} and I_{IL}

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: t_w = 25 µs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

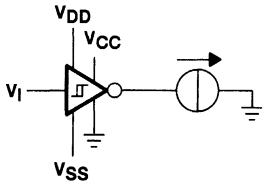


Figure 4. Receiver Test Circuit for I_{OS}

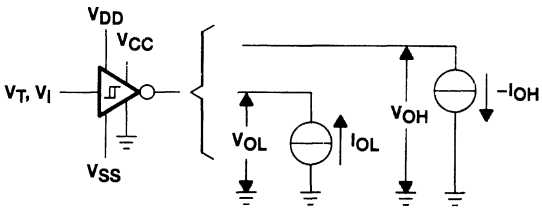
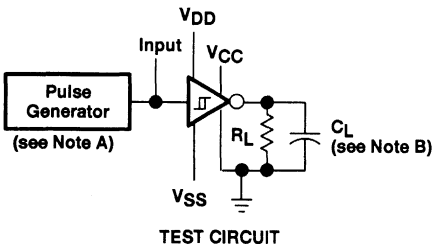
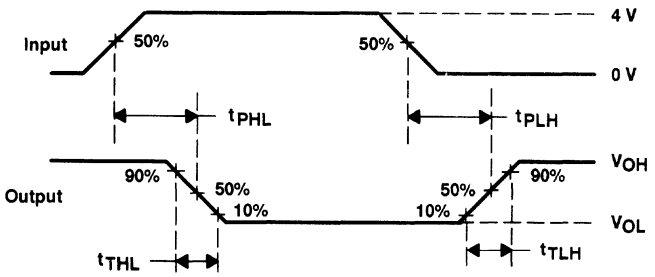


Figure 5. Receiver Test Circuit for V_T, V_{OH}, and V_{OL}



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: t_w = 25 µs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.
B. C_L includes probe and jig capacitance.

Figure 6. Receiver Propagation and Transition Times

TYPICAL CHARACTERISTICS

DRIVER SECTION

VOLTAGE TRANSFER CHARACTERISTICS

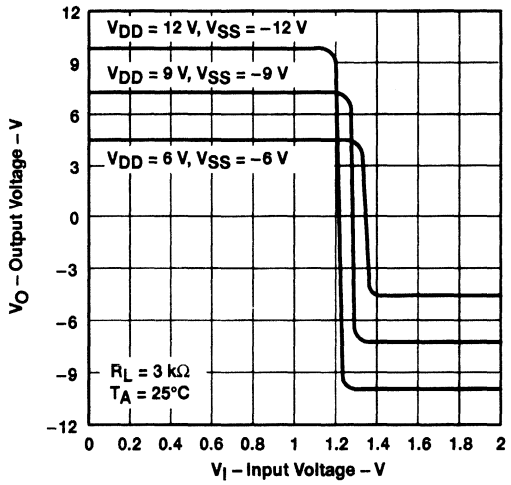


Figure 7

OUTPUT CURRENT vs OUTPUT VOLTAGE

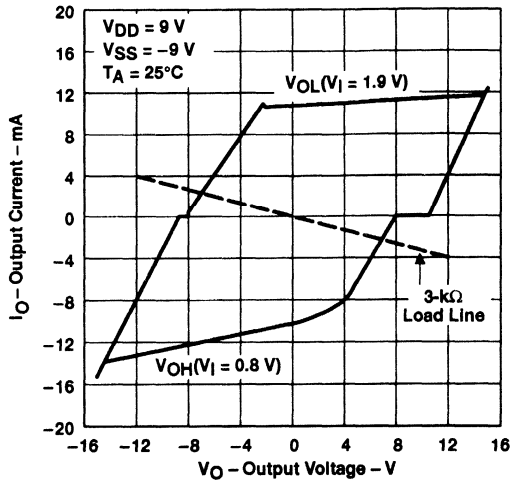


Figure 8

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

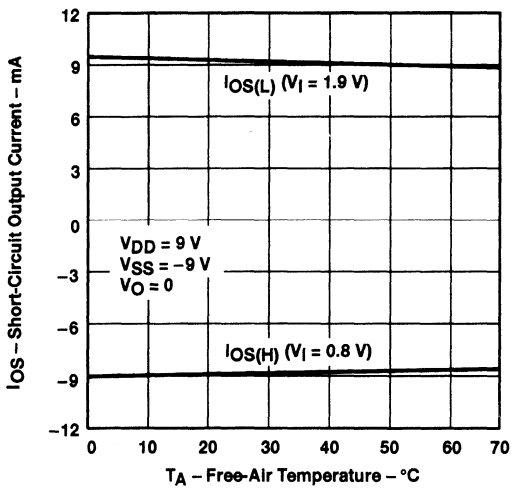


Figure 9

SLEW RATE vs LOAD CAPACITANCE

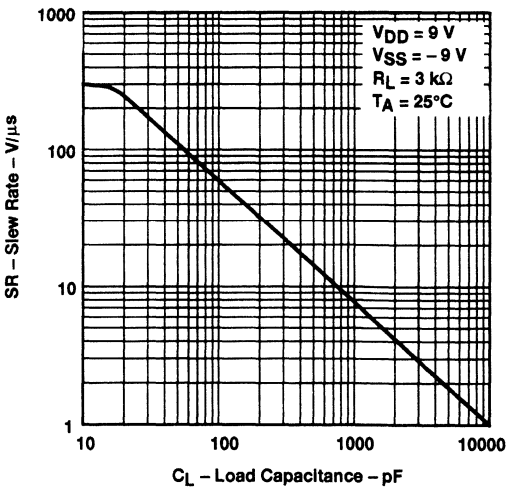


Figure 10

TYPICAL CHARACTERISTICS

RECEIVER SECTION

INPUT THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

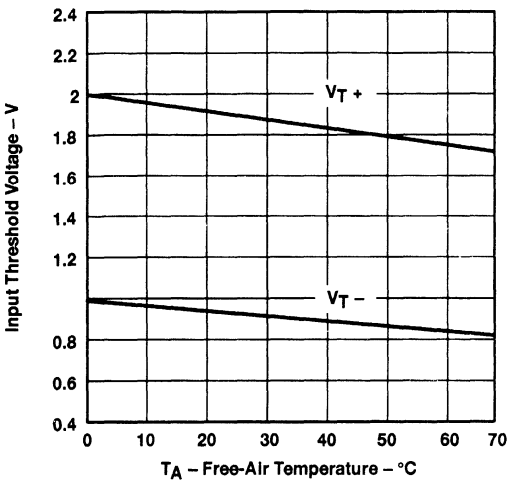


Figure 11

INPUT THRESHOLD VOLTAGE
vs
SUPPLY VOLTAGE

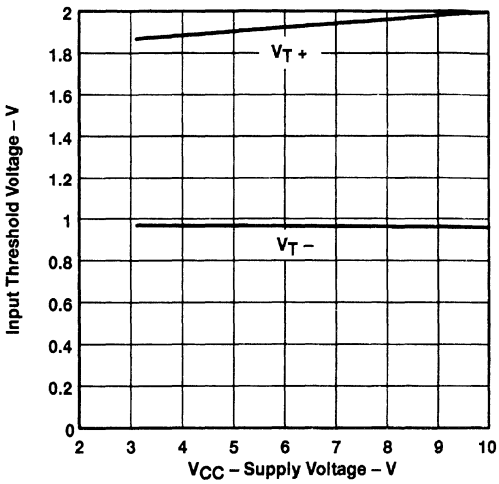
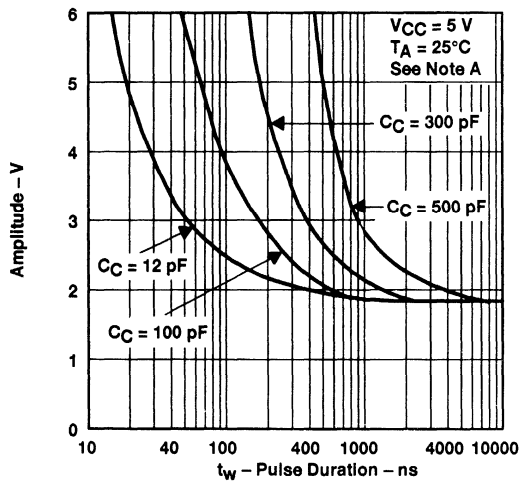


Figure 12

NOISE REJECTION



NOTE A: This figure shows the maximum amplitude of a positive-going pulse that, starting from 0 V, will not cause a change of the output level.

Figure 13

MAXIMUM SUPPLY VOLTAGE
vs
FREE-AIR TEMPERATURE

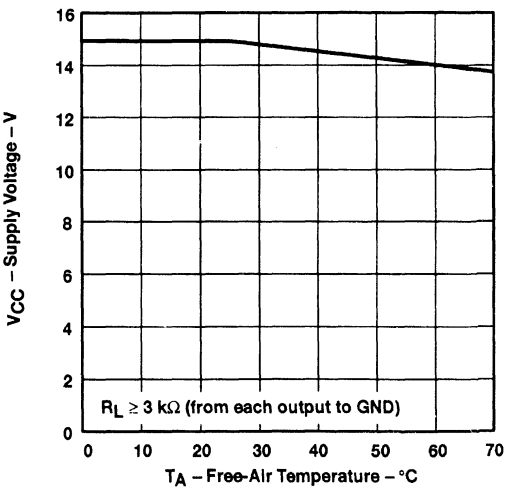


Figure 14

APPLICATION INFORMATION

Diodes placed in series with the V_{DD} and V_{SS} leads protect the SN75185 in the fault condition in which the device outputs are shorted to ±15 V and the power supplies are at low and provide low-impedance paths to ground (see Figure 15).

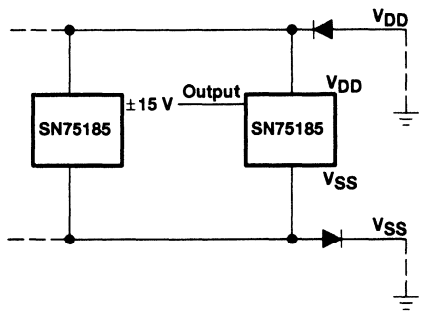
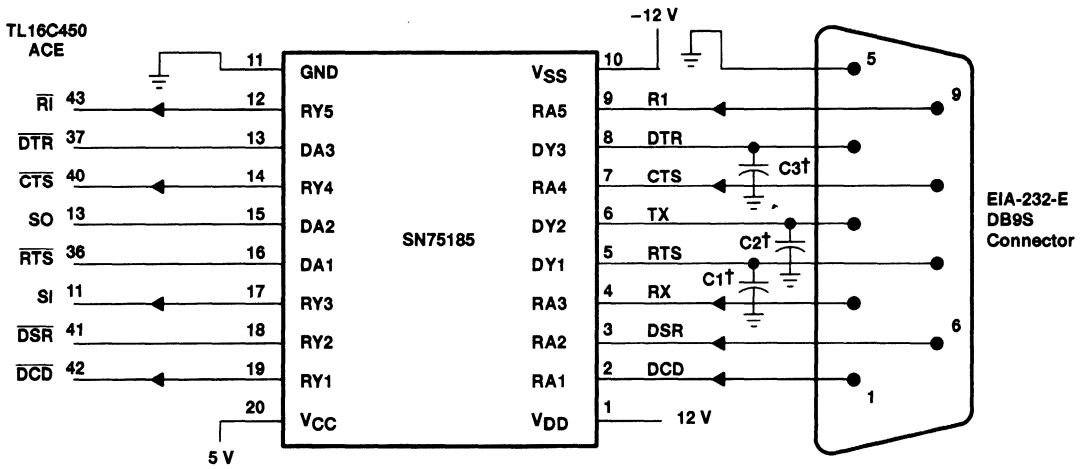


Figure 15. Power-Supply Protection to Meet Power-Off Fault Conditions of EIA/TIA-RS-232-E



† See Figure 10 to select the correct values for the loading capacitors (C1, C2, and C3), which may be required to meet the RS232 maximum slew-rate requirement of 30 V/µs. The value of the loading capacitors required depends upon the line length and desired slew rate, but is typically 330 pF.

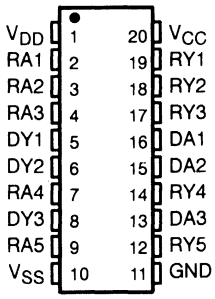
NOTE C. To use the receivers only, V_{DD} and V_{SS} must both be powered or tied to ground.

Figure 16. Typical Connection

SLLS065C – AUGUST 1989 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of ANSI EIA/TIA-232-E and ITU Recommendation V.28**
- **Single Chip With Easy Interface Between UART and Serial Port Connector**
- **Less Than 9-mW Power Consumption**
- **Wide Driver Supply Voltage . . . 4.5 V to 13.2 V**
- **Driver Output Slew Rate Limited to 30 V/μs Max**
- **Receiver Input Hysteresis . . . 1100 mV Typ**
- **Push-Pull Receiver Outputs**
- **On-Chip Receiver 1-μs Noise Filter**
- **Functionally Interchangeable With Texas Instruments SN75185**

DW OR N PACKAGE
(TOP VIEW)



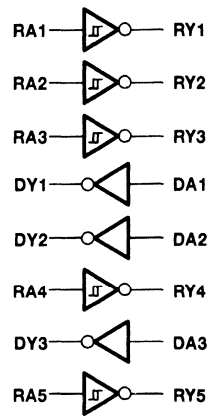
description

The SN65C185 and SN75C185 are low-power BiMOS devices containing three independent drivers and five receivers that are used to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). The SN65C185 and SN75C185 will typically replace one SN75188 and two SN75189 devices. These devices have been designed to conform to ANSI Standards EIA/TIA-232-E. The three drivers and five receivers of the SN65C185 and SN75C185 are similar to those of the SN75C188 quad drivers and SN75C189A quad receivers, respectively. The drivers have a controlled output slew rate that is limited to a maximum of 30 V/μs and the receivers have filters that reject input noise pulses that are shorter than 1 μs. Both these features eliminate the need for external components.

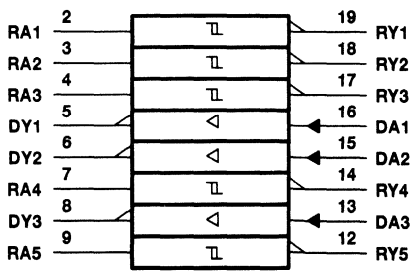
The SN65C185 and SN75C185 have been designed using low-power techniques in a BiMOS technology. In most applications, the receivers contained in these devices will interface to single inputs of peripheral devices such as ACEs, UARTS, or microprocessors. By using sampling, such peripheral devices are usually insensitive to the transition times of the input signals. If this is not the case, or for other uses, it is recommended that the SN65C185 and SN75C185 receiver outputs be buffered by single Schmitt input gates or single gates of the HCMOS, ALS, or 74F logic families.

The SN65C185 is characterized for operation from −40°C to 85°C. The SN75C185 is characterized for operation from 0°C to 70°C.

logic diagram (positive logic)

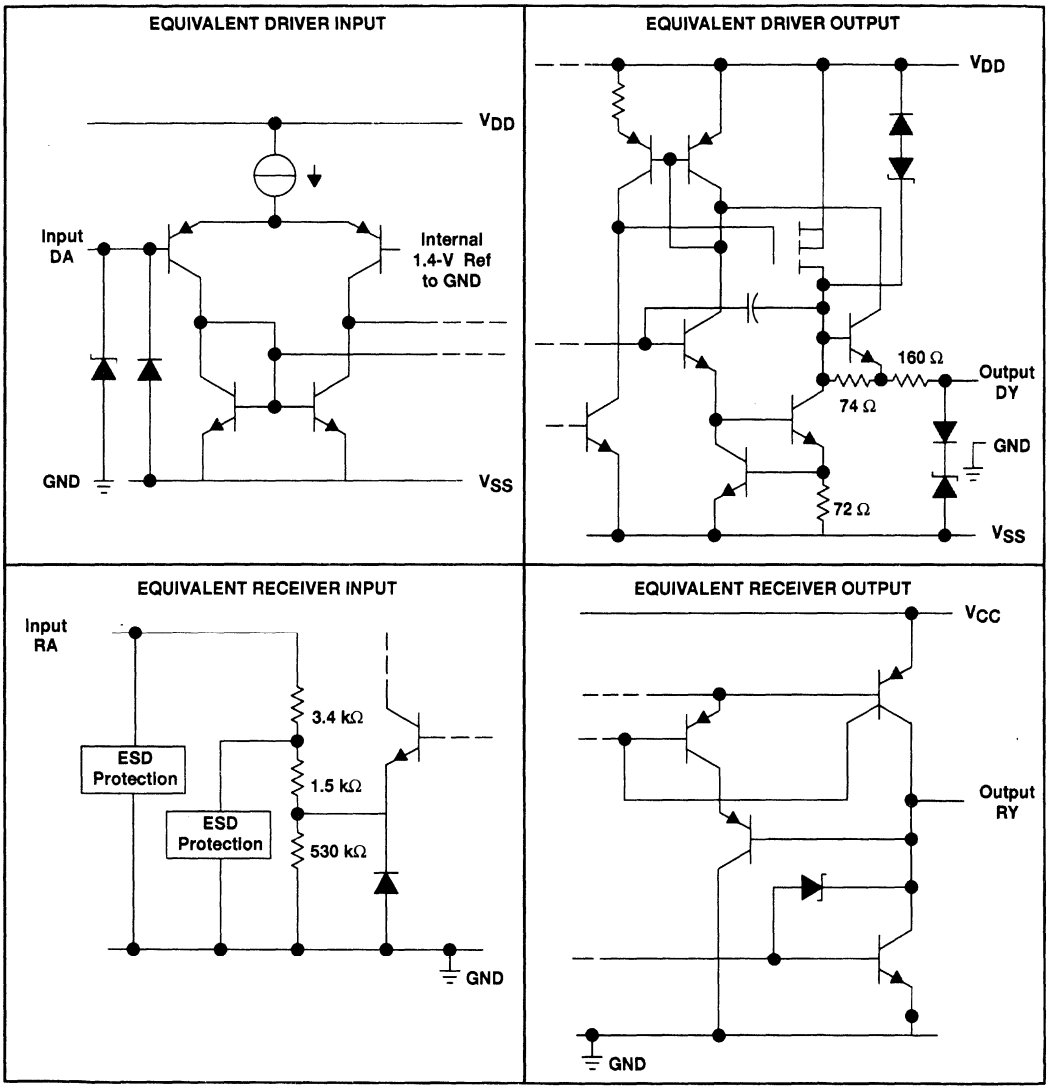


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

equivalent schematics of inputs and outputs



All resistor values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 13.5 V
Supply voltage, V_{SS} ..... −13.5 V
Supply voltage, V_{CC} ..... 7 V
Input voltage range, V_I: Driver ..... V_{SS} to V_{DD}
Receiver ..... −30 V to 30 V
Output voltage range, V_O: Driver ..... V_{SS} − 6 V to V_{DD} + 6 V
Receiver ..... −0.3 V to V_{CC} + 0.3 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65C185 ..... −40°C to 85°C
SN75C185 ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	585 mW
N	1150 mW	9.2 mW/°C	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.5	12	13.2	V
Supply voltage, V_{SS}		−4.5	−12	−13.2	V
Supply voltage, V_{CC}		4.5	5	6	V
Input voltage, V_I (see Note 2)	Driver	V_{SS}+2		V_{DD}	V
	Receiver	−25		25	
High-level input voltage, V_{IH}	Driver	2			V
Low-level input voltage, V_{IL}				0.8	
High-level output current, I_{OH}	Receiver			−1	mA
High-level output current, I_{OL}				3.2	mA
Operating free-air temperature, T_A	SN65C185	−40		85	°C
	SN75C185	0		70	

NOTE 2: The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if −10 V is a maximum, the typical value is a more negative voltage.

supply currents

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_{DD}	Supply current from V_{DD}	No load, All inputs at 2 V or 0.8 V	V_{DD} = 5 V,	V_{SS} = −5 V		115	200	µA
			V_{DD} = 12 V,	V_{SS} = −12 V		115	200	
I_{SS}	Supply current from V_{SS}	No load, All inputs at 2 V or 0.8 V	V_{DD} = 5 V,	V_{SS} = −5 V		−115	−200	µA
			V_{DD} = 12 V,	V_{SS} = −12 V		−115	−200	
I_{CC}	Supply current from V_{CC}	No load All inputs at 0 or 5 V	V_{DD} = 5 V,	V_{SS} = −5 V			750	µA
			V_{DD} = 12 V,	V_{SS} = −12 V			750	

DRIVER SECTION

electrical characteristics over operating free-air temperature range, V_{DD} = 12 V, V_{SS} = –12 V, V_{CC} = 5 V ±10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{IL} = 0.8 V, R_L = 3 kΩ, See Figure 1	V_{DD} = 5 V,	V_{SS} = –5 V	4	4.5		V
			V_{DD} = 12 V,	V_{SS} = –12 V	10	10.8		
V_{OL}	Low-level output voltage (see Note 2)	V_{IH} = 0.8 V, R_L = 3 kΩ, See Figure 1	V_{DD} = 5 V,	V_{SS} = –5 V		–4.4	–4	V
			V_{DD} = 12 V,	V_{SS} = –12 V		–10.7	–10	
I_{IH}	High-level input current	V_I = 5 V, See Figure 2					1	µA
I_{IL}	Low-level input current	V_I = 0, See Figure 2					–1	µA
$I_{OS(H)}$	High-level short-circuit output current (see Note 3)	V_I = 0.8 V, See Figure 1	V_O = 0 or V_O = V_{SS},		–4.5	–12	–19.5	mA
$I_{OS(L)}$	Low-level short-circuit output current (see Note 3)	V_I = 2 V, See Figure 1	V_O = 0 or V_O = V_{DD},		4.5	12	19.5	mA
r_o	Output resistance	V_{DD} = V_{SS} = V_{CC} = 0, See Note 4	V_O = –2 V to 2 V,		300	400		Ω

† All typical values are at T_A = 25°C.

NOTES: 2. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if –10 V is a maximum, the typical value is a more negative voltage.
3. Not more than one output should be shorted at one time.
4. Test conditions are those specified by EIA/TIA-232-E.

switching characteristics, V_{DD} = 12 V, V_{SS} = –12 V, V_{CC} = 5 V ±10%, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output (see Note 5)	R_L = 3 kΩ to 7 kΩ, See Figure 3	C_L = 15 pF,		1.2	3	µs
t_{PHL}	Propagation delay time, high- to low-level output (see Note 5)				2.5	3.5	µs
t_{TLH}	Transition time, low- to high-level output			0.53	2	3.2	µs
t_{THL}	Transition time, high- to low-level output			0.53	2	3.2	µs
t_{TLH}	Transition time, low- to high-level output (see Note 6)	R_L = 3 kΩ to 7 kΩ, See Figure 3	C_L = 2500 pF,		1		µs
t_{THL}	Transition time, high- to low-level output (see Note 6)				1		µs
S_R	Output slew rate (see Note 6)	R_L = 3 kΩ to 7 kΩ, See Figure 3	C_L = 15 pF,	4	10	30	V/µs

NOTES: 5. t_{PHL} and t_{PLH} include the additional time due to on-chip slew rate and is measured at the 50% points.
6. Measured between 3-V and –3-V points of output waveform (EIA/TIA-232-E conditions), all unused inputs tied either high or low.

RECEIVER SECTION

electrical characteristics over operating free-air temperature range, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ±10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshhold voltage	See Figure 5			1.6	2.1	2.55	V
V_{IT-}	Negative-going input threshhold voltage	See Figure 5			0.65	1	1.25	V
V_{hys}	Input hysteresis voltage ($V_{IT+} - V_{IT-}$)				600	1100		mV
V_{OH}	High-level output voltage	V_I = 0.75 V,	I_{OH} = −20 µA,	See Figure 5 and Note 7	3.5			V
		V_I = 0.75 V, I_{OH} = −1 mA, See Figure 5	V_{CC} = 4.5 V		2.8	4.4		
			V_{CC} = 5 V		3.8	4.9		
			V_{CC} = 5.5 V		4.3	5.4		
V_{OL}	Low-level output voltage	V_I = 3 V,	I_{OL} = 3.2 mA,	See Figure 5		0.17	0.4	V
I_{IH}	High-level input current	V_I = 3 V			0.43	0.55	1	mA
		V_I = 25 V			3.6	4.6	8.3	
I_{IL}	Low-level input current	V_I = −3 V			−0.43	−0.55	−1	mA
		V_I = −25 V			−3.6	−5.0	−8.3	
$I_{OS(H)}$	Short-circuit output at high level	V_I = 0.75 V,	V_O = 0,	See Figure 4		−8	−15	mA
$I_{OS(L)}$	Short-circuit output at low level	V_I = V_{CC},	V_O = V_{CC},	See Figure 4		13	25	mA

† All typical values are at T_A = 25 °C.

NOTE 7: If the inputs are left unconnected, the receiver interprets this as an input low, and the receiver outputs will remain in the high state.

switching characteristics, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ±10%, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 5 kΩ, C_L = 50 pF, See Figure 6		3	4	µs
t_{PHL}	Propagation delay time, high- to low-level output			3	4	µs
t_{TLH}	Transition time, low- to high-level output			300	450	ns
t_{THL}	Transition time, high- to low-level output			100	300	ns
$t_{w(N)}$	Duration of longest pulse rejected as noise (see Note 8)	R_L = 5 kΩ, C_L = 50 pF, See Figure 6	1		4	µs

NOTE 8: The receiver ignores any postive- or negative-going pulse that is less than the minimum value of $t_{w(N)}$ and accepts any positive- or negative-going pulse greater than the maximum of $t_{w(N)}$.

PARAMETER MEASUREMENT INFORMATION

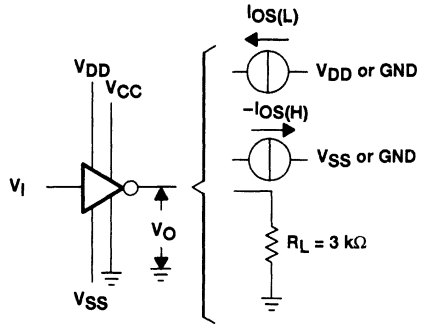


Figure 1. Driver Test Circuit for V_{OH}, V_{OL}, $I_{OS(H)}$, and $I_{OS(L)}$

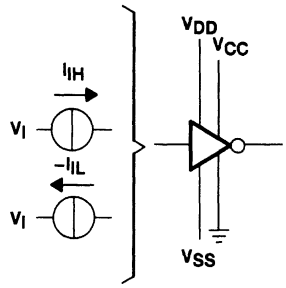
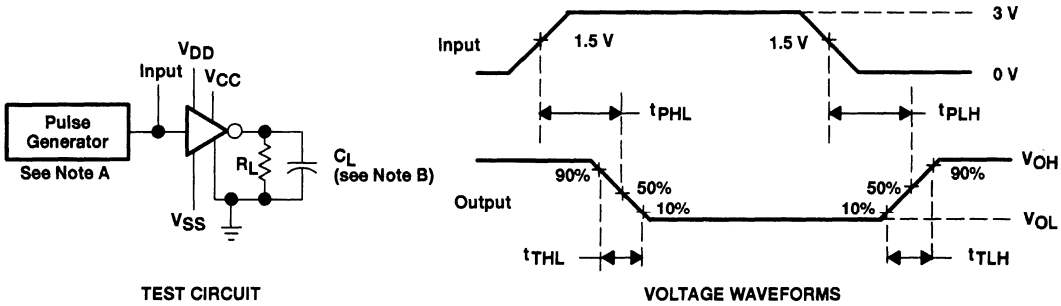


Figure 2. Driver Test Circuit for I_{IH} and I_{IL}



NOTES: A. The pulse generator has the following characteristics: t_w = 25 μs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f < 50$ ns.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

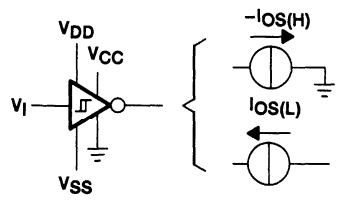


Figure 4. Receiver Test Circuit for $I_{OS(H)}$ and $I_{OS(L)}$

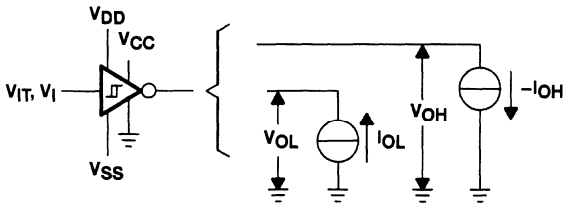
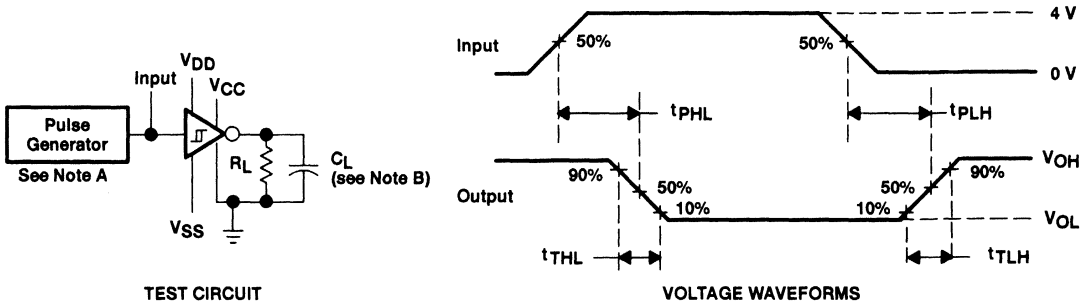


Figure 5. Receiver Test Circuit for V_{IT}, V_{OH}, and V_{OL}

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: t_w = 25 µs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.
B. C_L includes probe and jig capacitance.

Figure 6. Receiver Propagation and Transition Times

APPLICATION INFORMATION

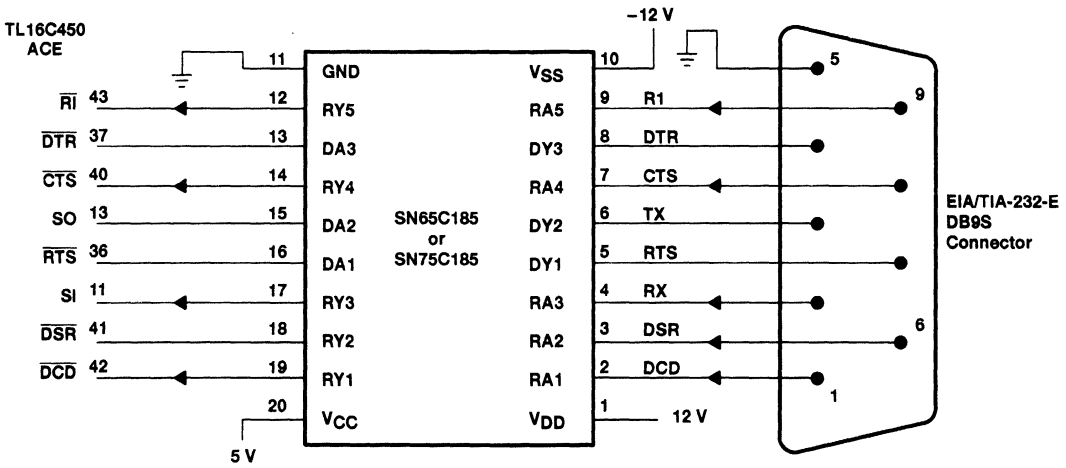


Figure 7. Typical Connection

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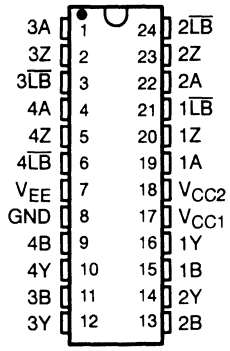
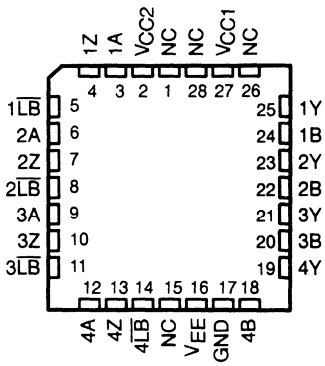
- **Meets or Exceeds the Requirements of ANSI EIA/TIA-232-E and ITU Recommendation V.28**
- **Four Independent Drivers and Receivers**
- **Loopback Mode Functionally Self-Tests Drivers and Receivers Without Disconnection From Line**
- **Driver Slew Rate Limited to 30 V/μs Max**
- **Built-In Receiver 1-μs Noise Filter**
- **Internal Thermal Overload Protection**
- **EIA/TIA-232-E Inputs and Outputs Withstand ±30 V**
- **Low Supply Current . . . 2.5 mA Typ**
- **ESD Protection Exceeds 4000 V Per MIL-STD-833C Method 3015**

DW PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN75186 is a low-power bipolar device containing four driver/receiver pairs designed to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). Additionally, the SN75186 has a loopback mode that may be used by a data communication system to perform a functional self test on each driver/receiver pair, removing the need to locally disconnect cables and install a loopback connector. Flexibility of control is ensured by each driver/receiver pair having its own loopback control input. The SN75186 is designed to conform to standards ANSI EIA/TIA-232-E and ITU Recommendation V.28.

The maximum slew rate is limited to 30 V/μs at the driver outputs, and the SN75186 drives a capacitive load of 2500 pF at 20 kBaud. The receivers have input filters that disregard input noise pulses shorter than 1 μs. The SN75186 is a robust device capable of withstanding ±30 V at driver outputs and at receiver inputs whether powered or unpowered. This device has an internal ESD protection rated at 4 kV to prevent functional failures.

The SN75186 is characterized for operation from 0°C to 70°C.

Function Tables

EACH RECEIVER

LOOPBACK	INPUTS		OUTPUT
$\overline{LB}$	A	B†	Z
H	X	H	L
H	X	L	H
L	L	X	L
L	H	X	H

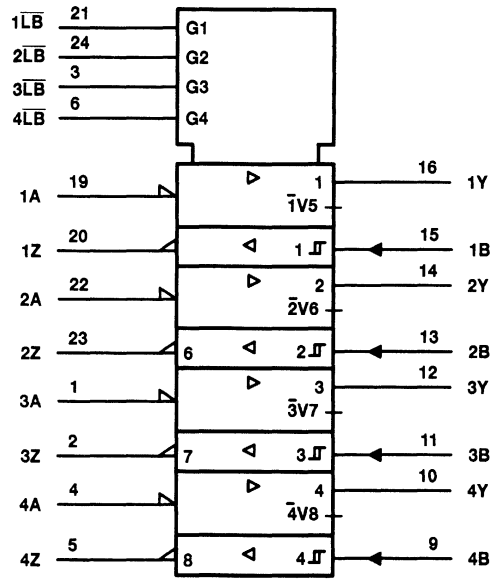
EACH DRIVER

LOOPBACK	INPUT	OUTPUT
$\overline{LB}$	A	Y†
H	H	L
H	L	H
L	X	L

† Voltages are EIA/TIA-232-E, and V.28 levels

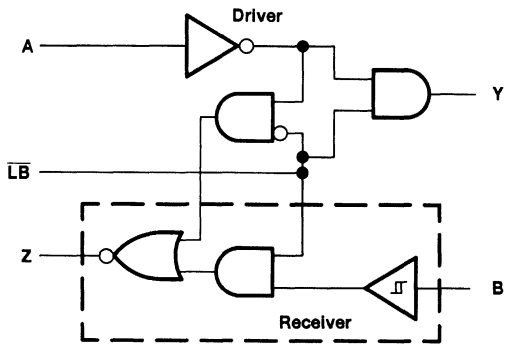
H = high level, L = low level, X = irrelevant

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW package.

logic diagram, each driver/receiver pair (positive logic)



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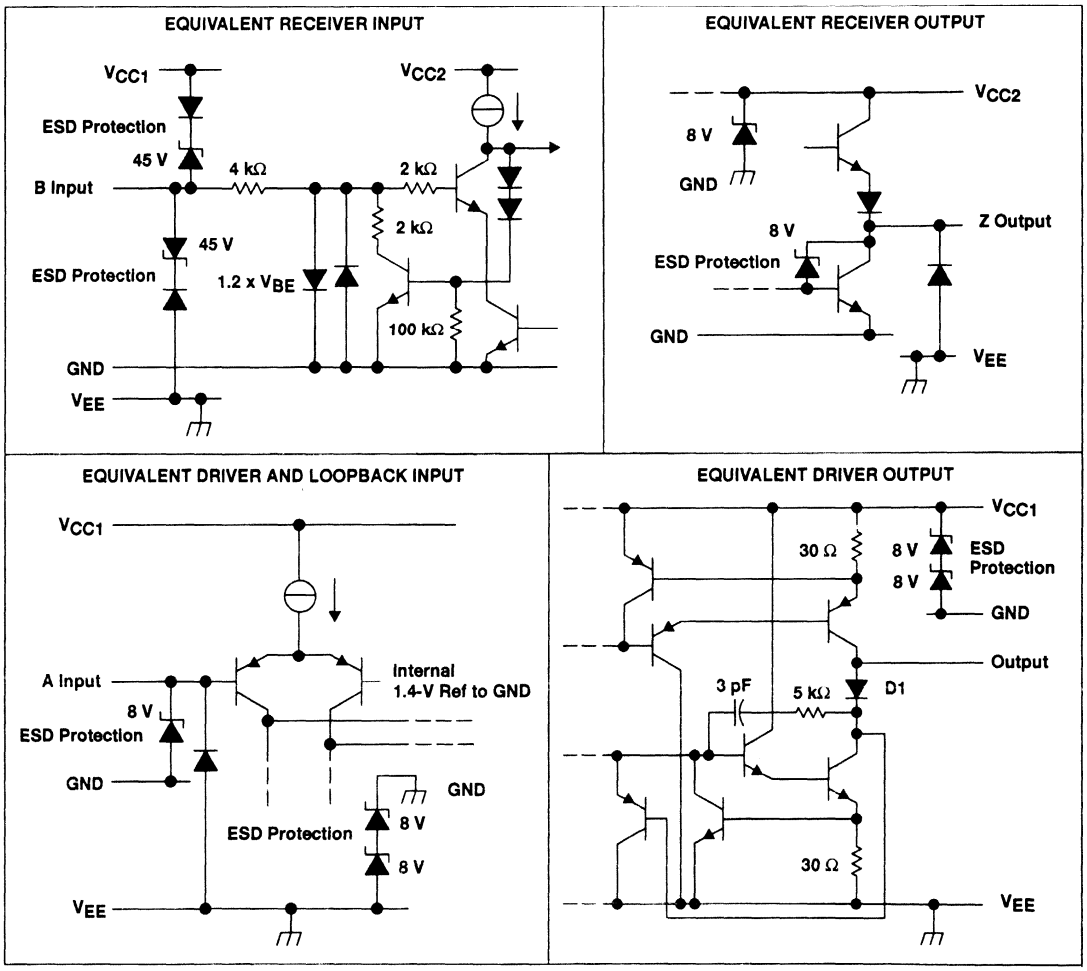
schematics of inputs and outputs



All component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC1} (see Note 1) ..... 15 V
Supply voltage, V_{CC2} ..... 7 V
Supply voltage, V_{EE} ..... −15 V
Receiver input voltage range, V_I ..... −30 V to 30 V
Driver input voltage range, V_I ..... (V_{EE} + 2 V) to V_{CC1}
Loopback input voltage range, V_I ..... 0 V to 7 V
Driver output voltage range, V_O ..... −30 V to 30 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Case temperature for 10 seconds: FN package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW package ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1350 mW	10.8 mW/°C	864 mW
FN	1400 mW	11.2 mW/°C	896 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}		10.8	12	13.2	V
Supply voltage, V_{CC2}		4.5	5	5.5	V
Supply voltage, V_{EE}		−10.8	−12	−13.2	V
Input voltage, V_I	Driver and loopback	0		V_{CC2}	V
Input voltage, V_I (see Note 2)	Receiver			±30	V
High-level input voltage, V_{IH}	Driver and loopback	2			V
Low-level input voltage, V_{IL}	Driver and loopback			0.8	V
Output voltage powered on or off, V_O	Driver			±30	V
High-level output current, I_{OH}	Receiver			−4	mA
Low-level output current, I_{OL}	Receiver			4	mA
Operating free-air temperature, T_A		0		70	°C

NOTE 2: If all receiver inputs are held at ±30 V, the thermal dissipation limit of the package may be exceeded. The thermal shutdown may not protect the device, as this dissipation occurs in the receiver input resistors.

DRIVER SECTION

electrical characteristics over full recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	R_L = 3 kΩ,	V_{IL} = 0.8 V,	See Figure 1	7			V
V_{OL}	Low-level output voltage‡	R_L = 3 kΩ,	V_{IH} = 2 V,	See Figure 1			−7	V
$V_{OH(LB)}$	High-level output voltage in loopback mode‡§¶	R_L = 3 kΩ,	$\overline{LB}$ at 0.8 V,	V_{IL} = 0.8 V			−7	V
I_{IH}	High-level input current (driver and loopback inputs)#	V_I = 5 V,	See Figure 2				100	μA
I_{IL}	Low-level input current (driver and loopback inputs)#						−100	μA
$V_{OS(H)}$	High-level short-circuit output current	V_I = 0.8 V, See Note 3 and Figure 1	V_O = 0,		−10	−20	−35	mA
$V_{OS(L)}$	Low-level short-circuit output current	V_I = 2 V, See Note 3 and Figure 1	V_O = 0,		10	20	35	mA
I_{CC1}	Supply current from V_{CC1}	No load				2.5	4	mA
$I_{CC1(LB)}$	Supply current from V_{CC1} with loopback on	No load,	$\overline{LB}$ at 0.8 V				10	mA
I_{EE}	Supply current from V_{EE}	No load				−2.5	−4	mA
$I_{EE(LB)}$	Supply current from V_{EE} with loopback on	No load,	$\overline{LB}$ at 0.8 V				−10	mA
I_{CC2}	Supply current from V_{CC2}	No load,	V_I = 0,	See Note 5		−10	−100	μA
$I_{CC2(LB)}$	Supply current from V_{CC2} with loopback on	No load, See Note 5	LB at 0.8 V,	V_I = 0,		−10	−100	μA
r_o	Output resistance	V_{CC1} = V_{EE} = V_{CC2} = 0, V_O = −2 V to 2 V,		See Note 4	0.3	5		kΩ

† All typical values are at T_A = 25°C.

‡ The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only.

§ This is the most positive level that the driver output will rise to when the device is in the loopback mode and the driver input is at a low level.

¶ The loopback mode should be entered only when the driver output is in the low (marking) state.

Unused driver inputs should be tied to 0 V or V_{CC2}; unused loopback inputs should be tied to V_{CC2}.

NOTES: 3. Minimum $I_{OS(H)}$ and $I_{OS(L)}$ are specified at V_O = 0, as this more accurately describes the output current needed to dynamically drive capacitive lines. A minimum of ±10 mA is sufficient to drive 2500 pF in parallel with 3 kΩ at a slew rate of 4 V/μs (in accordance with EIA/TIA-232-E and V.28).

4. Test conditions are those specified by EIA/TIA-232-E.

5. Without a load and V_I = 0, the worst-case conditions, V_{CC2} sources a small current originating from V_{CC1} giving I_{CC2} supply current a negative sign. When a receiver has an output load, V_{CC2} sinks static and dynamic supply currents to meet load requirements.

switching characteristics over full recommended ranges of supply voltages and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 3		0.6	5	µs
t_{PHL}	Propagation delay time, high- to low-level output			0.8	5	µs
t_{sk}	$\lvert t_{PLH} - t_{PHL} \rvert$	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF to 2500 pF		0.2	1	µs
SR	Output slew rate	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF to 2500 pF	4		30	V/µs
$t_{pd(ILB)}$	Propagation delay time going into loopback mode‡	R_L = 3 kΩ to 7 kΩ, See Note 6 and Figure 7		3	50	µs
$t_{pd(OLB)}$	Propagation delay time going out of loopback mode§	R_L = 3 kΩ to 7 kΩ, See Note 6 and Figure 7		3	50	µs
$t_{pd(LB)}$	Propagation delay time in loopback mode¶	R_L = 3 kΩ to 7 kΩ, See Note 6 and Figure 8		3	15	µs
t_{sk}	Skew time in loopback mode	R_L = 3 kΩ to 7 kΩ, See Note 6		4	10	µs

† All typical values are at T_A = 25°C.
‡ This is the delay between entering the loopback mode and when the data on the receiver output becomes valid.
§ This is the worst-case (rising or falling edges) total propagation delay between driver input and receiver output when in the loopback mode.
¶ This is the magnitude of the difference between the propagation delay time of the rising and falling edges of $t_{pd(LB)}$.
NOTE 6: Skew time is the magnitude of the difference between t_{PHL} and t_{PLH} and is measured with a 0 to 3-V input pulse.

RECEIVER SECTION

electrical characteristics over full recommended ranges of supply voltages and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	See Figure 5		1.3	2	2.5	V
V_{IT-}	Negative-going input threshold voltage	See Figure 5		0.5	1	1.7	V
V_{hys}	Input hysteresis voltage ($V_{IT+} - V_{IT-}$)			0.5	1	1.5	V
V_{OH}	High-level output voltage	V_I = −3 V or inputs open,	I_{OH} = −20 μA	3.5			V
		I_{OH} = −4 mA,	See Note 7 and Figure 5	2.4			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 5	V_I = 3 V,			0.4	V
$I_{OS(H)}$	Short-circuit output current at high level	V_{OH} = 0,	See Figure 4		−20	−60	mA
$I_{OS(L)}$	Short-circuit output current at low level	$V_{OL} = V_{CC2}$,	See Figure 4		20	60	mA
r_i	Input resistance	$\lvert V_I \rvert \le 25$ V		3			kΩ
		$\lvert V_I \rvert$ = 3 V to 25 V				7	

NOTE 7: If the inputs are left unconnected, the receiver interprets this as a low input and the receiver outputs will remain in the high state.

switching characteristics over full recommended ranges of supply voltages and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 6			2	6	μs
t_{PHL}	Propagation delay time, high- to low-level output				2	6	μs
t_{TLH}	Transition time, low- to high-level output‡	C_L = 50 pF,	See Figure 6		200	300	ns
t_{THL}	Transition time, high- to low-level output‡				50	300	ns
t_{sk}	$\lvert t_{PLH} - t_{PHL} \rvert$				0.1	1	μs
t_w	Maximum pulse duration assumed to be noise§	Pulse amplitude = 5 V		1	2	4	μs

† All typical values are at T_A = 25°C.

‡ Transition times are measured between 10% and 90% points on output waveform.

§ The receiver will ignore any positive- or negative-going pulse whose duration is less than the minimum value of t_w and accept any positive- or negative-going pulse whose duration is greater than the maximum value of t_w.

PARAMETER MEASUREMENT INFORMATION

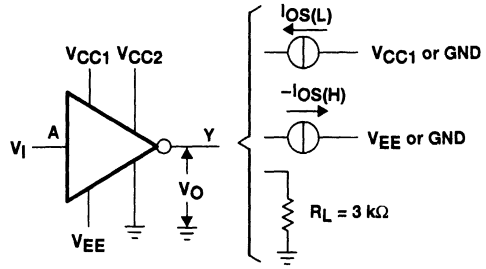


Figure 1. Driver Test Circuit, V_{OH}, V_{OL}, $I_{OS(L)}$, $I_{OS(H)}$

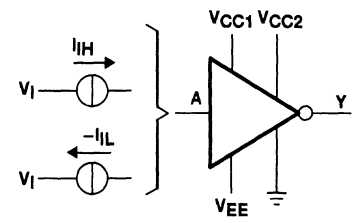
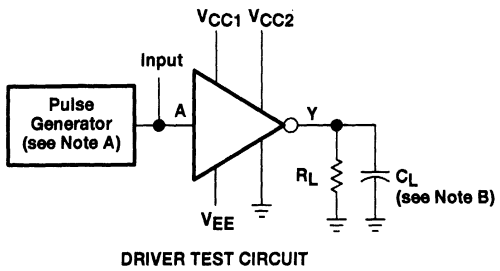


Figure 2. Driver and Loopback Test Circuit, I_{IL}, I_{IH}



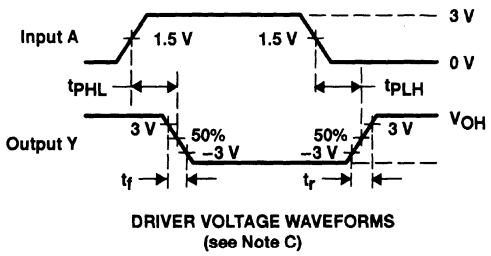


Figure 3. Driver Test Circuit and Voltage Waveforms

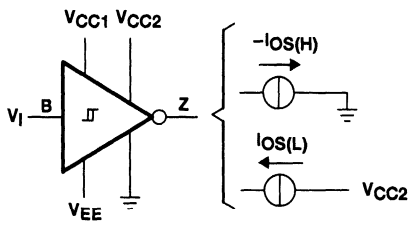


Figure 4. Receiver Test Circuit, $I_{OS(H)}$, $I_{OS(L)}$

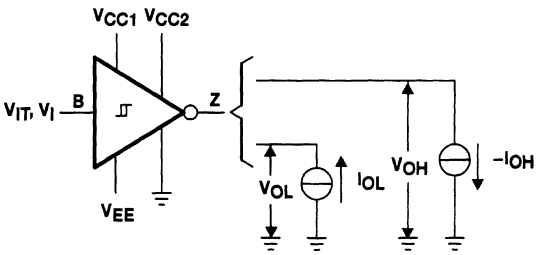


Figure 5. Receiver Test Circuit, V_{IT}, V_{OL}, V_{OH}

NOTES: A. The pulse generator has the following characteristics: t_w = 25 μs, PRR = 20 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. Slew rate = $\frac{6\ V}{t_r \text{ or } t_f}$

PARAMETER MEASUREMENT INFORMATION

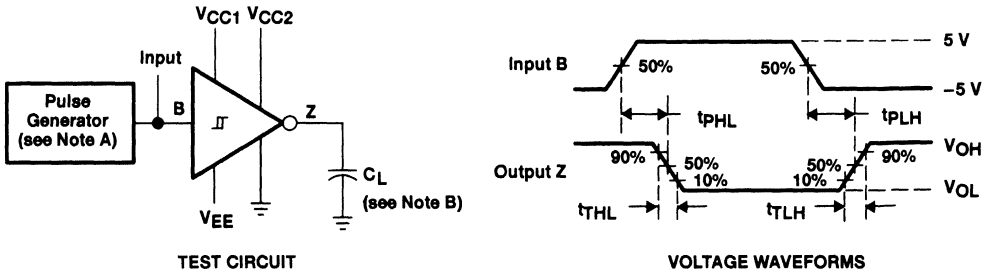


Figure 6. Receiver Propagation and Transition Times

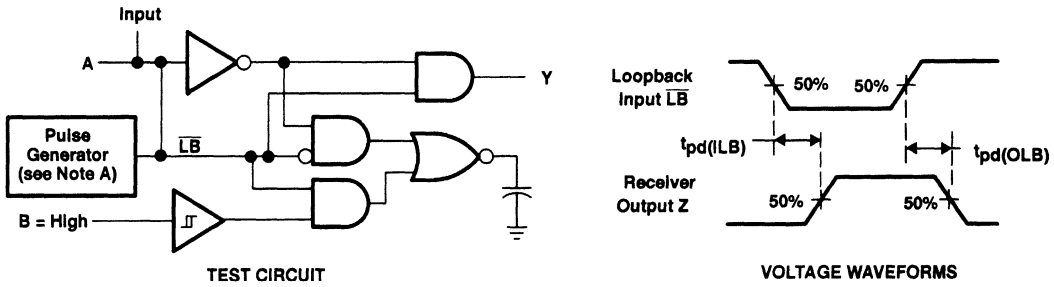


Figure 7. Loopback Entry and Exit Propagation Times

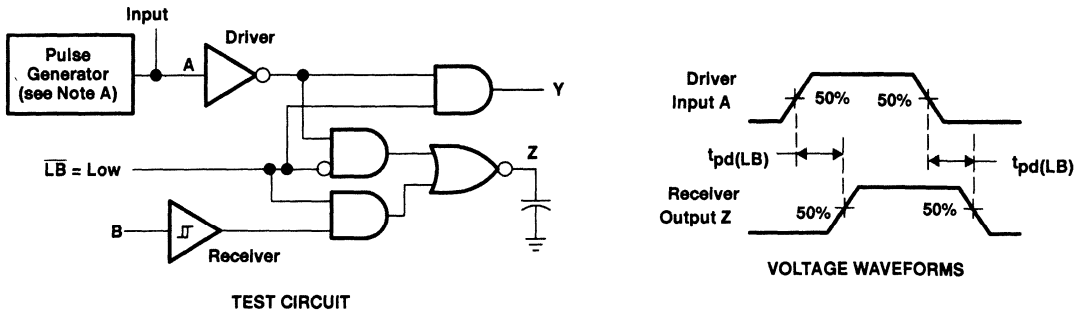


Figure 8. Loop Propagation Times in Loopback Mode

NOTES: A. The pulse generator has the following characteristics: t_w = 25 µs, PRR = 20 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

PRINCIPLES OF OPERATION

In normal operation, the SN75186 acts as four independent drivers and receivers; the loopback mode is held off by keeping logic inputs $\overline{LB}$ high. Taking a particular $\overline{LB}$ input low activates the loopback mode in the corresponding driver/receiver pair. This causes the output from that driver to be fed back to the input of its receiver through dedicated internal loopback circuitry. Data from the receiver output can then be compared, by a communication system, with the data transmitted to the driver to determine if the functional operation of the driver and receiver together is correct.

In the loopback mode, external data at the input of the receiver is ignored and the driver does not transmit data onto the line. Extraneous data is prevented internally from being sent by the driver in the loopback mode by clamping its output to a level below the maximum interface voltage, –5 V, or the EIA/TIA-232-E marking state. Below this marking level, a reduced 1.5-V output amplitude is used at the driver output. This signal is detected by an on-chip loopback comparator and fed to the input stage of the receiver to complete the loop.

Line faults external to the SN75186 are detected in addition to device failures. These line faults include short circuits to ground and to external supply voltages that are greater than (V_{EE} + 7 V) and less than V_{EE} typically. For example, with V_{EE} = –12 V, line short circuits to voltages greater than –5 V and less than –12 V will be detected. The loopback mode should be entered only when the driver output is low, that is, the marking state of EIA/TIA-232-E. It is recommended that loopback not be entered when the driver output is in a high state as this may cause a low-level, nondamaging oscillation at the driver output.

When in the loopback mode, approximately 95% of the SN75186 circuit is functionally checked. There exists some low probability of fault mechanisms in circuitry not being checked in the loopback mode. To reduce the chances of undetected failure, the unchecked circuitry has been designed to be more robust than that within the loopback test loop. The areas where special attention has been paid are the receiver input potential divider and resistors, the driver output blocking diode (D1), and parts of the driver clamp circuit.

Protection of the SN75186 is achieved by means of driver output current limits and a thermal trip. Although this device will withstand ±30 V at its receiver input, package thermal dissipation limitations have to be taken into consideration if more than one receiver is connected simultaneously. This is due to the possible dissipation in the 3 kΩ minimum input resistors, which is not under the control of the thermal trip. Although the supply current is higher in the loopback mode than in normal operation, the total power dissipation is not sufficient under normal worst-case conditions (of receiver input V_I = 15 V + 10%, receiver output voltage = 2.4 V at 4 mA, driver load of 3 kΩ) to cause the thermal limiting circuitry to trip.

If the SN75186 goes into thermal trip, the output of the driver goes to a high-impedance state and the receiver output is held in a logic-high marking state. Both driver and receiver outputs maintain a marking state and do not allow indeterminate conditions to exist.

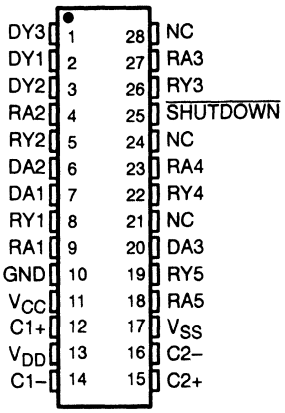
The standards specify a minimum driver output resistance to ground of 300 Ω when the device is powered off. To fully comply with EIA/TIA-232-E power-off fault conditions, many drivers need diodes in series with each supply voltage to prevent reverse current flow and driver damage. The SN75186 overcomes this need by providing a high-impedance driver output of typically 5 kΩ under power-off conditions through the use of the equivalent of these series diodes in the driver output circuit.

SN75LBC187
MULTICHANNEL EIA-232 DRIVER/RECEIVER WITH CHARGE PUMP

SLLS130C – SEPTEMBER 1991 – REVISED MAY 1995

- **Single IC and Single 5-V Supply Interface for Serial Communication Ports**
- **Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-232-E-1991, EIA/TIA-562, and ITU Recommendation V.28**
- **Switched-Capacitor Voltage Converter Eliminates Need for ±12-V Supplies**
- **Voltage Converter Operates With Low Capacitance . . . 0.1 μF Min**
- **Designed for Data Rates up to 120 kb/s Over 3-m Cable**
- **Available in Shrink Small-Outline 25-mil-Pitch Package**
- **Shutdown Mode to Save Power When Not in Use**
- **±30-V Receiver Input Voltage Range**
- **LinBiCMOS™ Process Technology**
- **Applications**
  - **Laptop or Notebook Computers**
  - **Portable Terminals**
  - **Single-Board Computers**
  - **Portable Test Equipment**

DB PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN75LBC187 is a low-power LinBiCMOS™ device containing three drivers, five receivers, and a switched-capacitor voltage converter. The SN75LBC187 provides a single chip and single 5-V supply interface between the asynchronous communications element and the serial port connector of the data terminal equipment (DTE). This device has been designed to conform to ANSI Standards EIA/TIA-232-E, EIA/TIA-562, and ITU recommendation V.28.

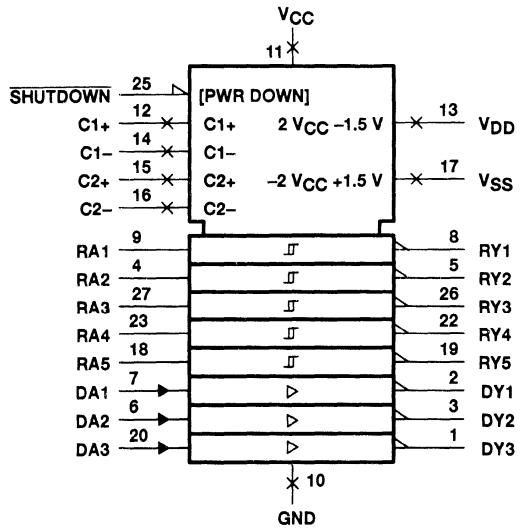
The switched-capacitor voltage converter of the SN75LBC187 uses four small external capacitors to generate the positive and negative voltages required by EIA/TIA-232-E (and V.28) line drivers from a single 5-V input. The drivers feature output slew-rate limiting to eliminate the need for external filter capacitors. The receivers can accept ±30 V without damage. The device also features a reduced power or shutdown mode that cuts the quiescent power to the IC when not transmitting data between the CPU and peripheral.

The SN75LBC187 has been designed using LinBiCMOS™ technology and cells contained in the Texas Instruments LinASIC™ library. The SN75LBC187 is characterized for operation from 0°C to 70°C.

NOTE:
This device includes circuit designs and process technologies that have patents pending.

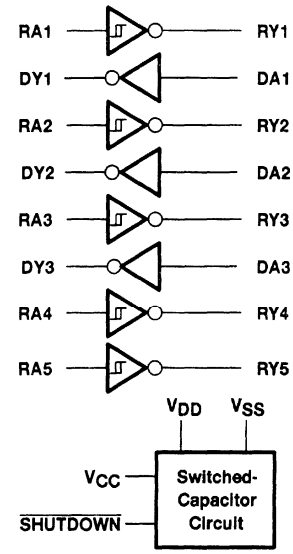
LinBiCMOS and LinASIC are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... 0.3 V to 6 V
Positive output supply voltage range, V_{DD} ..... V_{CC} –0.3 V to 15 V
Negative output supply voltage range, V_{SS} ..... 0.3 V to –15 V
Input voltage range, V_I: RA ..... ±30 V
All other inputs ..... –0.3 V to V_{CC} + 3 V
Output voltage range, V_O: DY ..... –2 V_{CC} + 1.2 V to 2 V_{CC} – 1.2 V
All other outputs ..... –0.3 V to V_{CC} + 3 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DB	1025 mW	8.2 mW/°C	656 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level input voltage, V_{IH}	DA	2			V
	RA, $\overline{\text{SHUTDOWN}}$	2.4			
Low-level input voltage, V_{IL}	RA, DA, $\overline{\text{SHUTDOWN}}$			0.8	V
Receiver input voltage, V_I		−25		25	V
High-level output current, I_{OH}	RY			−1	mA
Low-level output current, I_{OL}	RY			3.2	mA
Output current, I_O	V_{DD}			±10	μA
	V_{SS}			±10	μA
C1, C2, C3, C4 charge pump capacitors		0.1	0.47		μF
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	Receiver	I_O = −1 mA	3.5			V
		Driver	R_L = 3 kΩ to GND	5	7		
V_{OL}	Low-level output voltage	Receiver	I_O = 3.2 mA			0.4	V
		Driver	R_L = 3 kΩ to GND		−7	−5	
V_{IT+}	Receiver positive-going input voltage threshold				1.7	2.4	V
V_{IT-}	Receiver negative-going input voltage threshold			0.8	1.2		V
V_{hys}	Receiver input hysteresis voltage ($V_{IT+} - V_{IT-}$)				0.5	1	V
r_i	Receiver input resistance		V_{CC} = 5 V, T_A = 25°C	3	5	7	kΩ
r_o	Driver output resistance		V_{CC} = 0, V_O = ±2 V	300			Ω
I_I	Input current (DA, $\overline{\text{SHUTDOWN}}$)		V_I = 0 to V_{CC}			±50	μA
I_{OS}	Driver output short-circuit current		V_O = 0	±10			mA
I_{CC}	Supply current	Normal operation	All outputs open, $\overline{\text{SHUTDOWN}}$ at 2.4 V		15	30	mA
		Shutdown mode	All outputs open, $\overline{\text{SHUTDOWN}}$ at 0.1 V			10	μA

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

switching characteristics over recommended operating conditions, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	Receiver	R_L = 5 kΩ, See Figure 1	C_L = 50 pF,		1.25	µs
		Driver	R_L = 3 kΩ, See Figure 2	C_L = 1200 pF,		1.25	µs
t_{PHL}	Propagation delay time, high- to low-level output	Receiver	R_L = 5 kΩ, See Figure 1	C_L = 50 pF,		1.25	µs
		Driver	R_L = 3 kΩ, See Figure 2	C_L = 1200 pF,		1.25	µs
t_r	Rise time, driver output		R_L = 3 kΩ, V_O = −3 V to 3 V,	C_L = 50 pF, See Note 2	200		ns
			R_L = 3 kΩ, V_O = −3.3 V to 3.3 V,	C_L = 2500 pF, See Note 3		1.5	µs
t_f	Fall time, driver output		R_L = 3 kΩ, V_O = 3 V to −3 V	C_L = 50 pF,	200		ns
			R_L = 3 kΩ, V_O = 3.3 V to −3.3 V	C_L = 2500 pF,		1.5	µs

NOTES: 2. The 200 ns for the output to change from −3 V to 3 V (or vice versa) corresponds to the 30 V/µs maximum slew rate of EIA/TIA-232-E, EIA/TIA-562, and ITU Recommendation V.28.
3. The more stringent requirement for transition times comes from the EIA/TIA-562, which requires the rise and fall times to be measured from 3.3 V.

PARAMETER MEASUREMENT INFORMATION

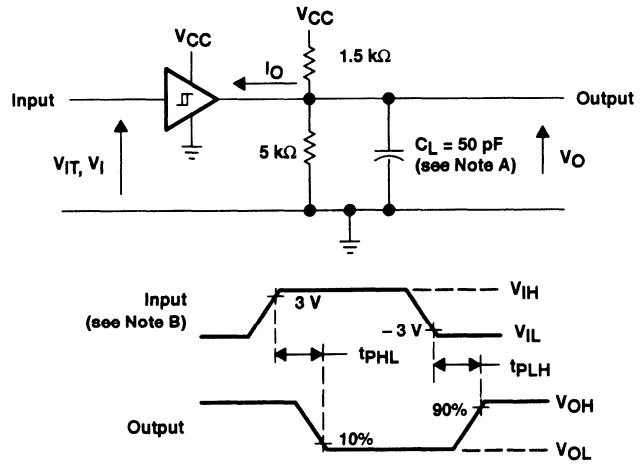


Figure 1. Receiver Test Circuit and Waveforms

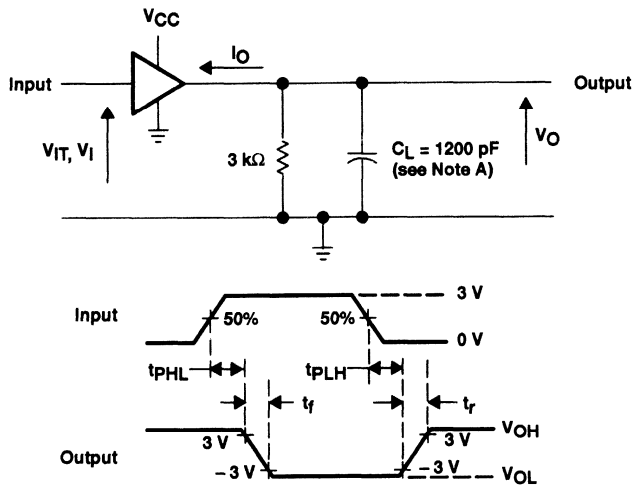
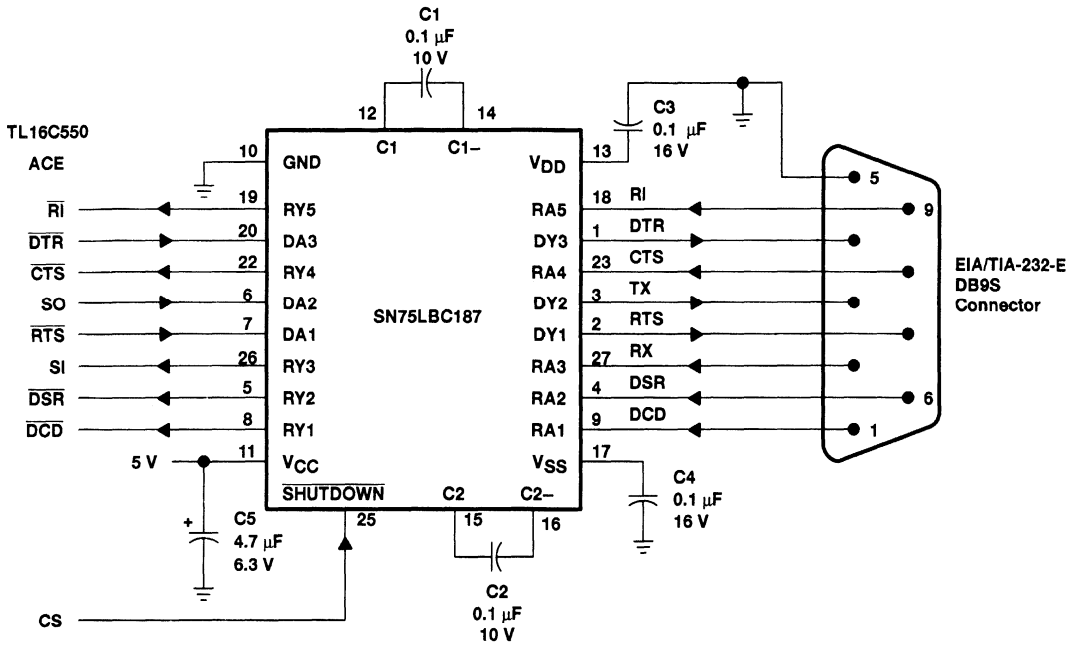


Figure 2. Driver Test Circuit and Waveforms

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: t_w = 8.33 µs, PRR = 60 kHz, $t_r = t_f \leq 50$ ns.

APPLICATION INFORMATION



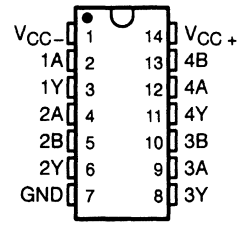
NOTE: C1, C2, C3, and C4 are Z5U-type ceramic-chip capacitors.

Figure 3. Typical SN75LBC187 Connection

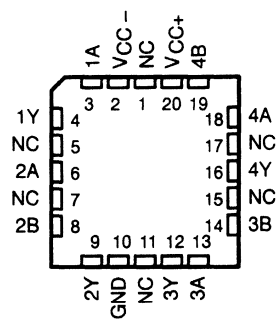
SLLS094B – SEPTEMBER 1983 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of ANSI EIA/TIA-232-E and ITU Recommendation V.28**
- **Designed to Be Interchangeable With Motorola MC1488**
- **Current-Limited Output: 10 mA Typ**
- **Power-Off Output Impedance: 300 Ω Min**
- **Slew Rate Control by Load Capacitor**
- **Flexible Supply Voltage Range**
- **Input Compatible With Most TTL Circuits**

SN55188 . . . J OR W PACKAGE
MC1488, SN75188 . . . D OR N PACKAGE
(TOP VIEW)



SN55188 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The MC1488, SN55188, and SN75188 are monolithic quadruple line drivers designed to interface data terminal equipment with data communications equipment in conformance with ANSI EIA/TIA-232-E using a diode in series with each supply-voltage terminal as shown under typical applications.

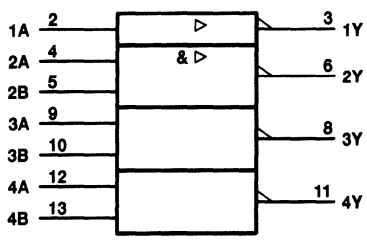
The SN55188 is characterized for operation over the full military temperature range of –55°C to 125°C. The MC1488 and SN75188 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(drivers 2 through 4)

A	B	Y
H	H	L
L	X	H
X	L	H

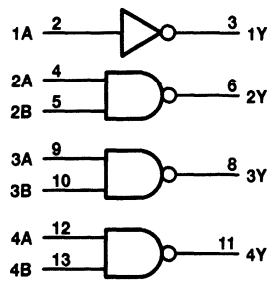
H = high level, L = low level,
X = irrelevant

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

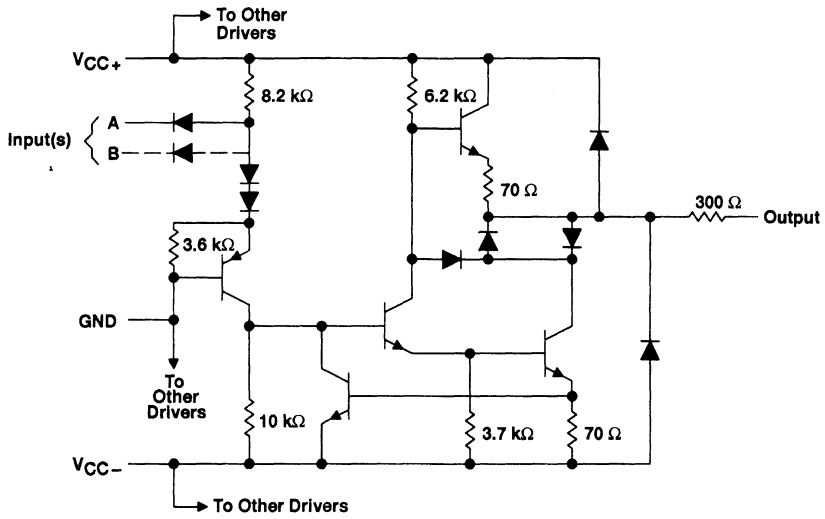
logic diagram (positive logic)



Positive logic
$Y = \overline{A}$ (driver 1)
$Y = \overline{AB}$ or $\overline{A} + \overline{B}$ (drivers 2 thru 4)

Pin numbers shown are for the D and N packages.

schematic (each driver)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

		SN55188	MC1488 SN75188	UNIT
Supply voltage, V_{CC+}, at (or below) 25°C free-air temperature (see Notes 1 and 2)		15	15	V
Supply voltage, V_{CC-}, at (or below) 25°C free-air temperature (see Notes 1 and 2)		−15	−15	V
Input voltage range, V_I		−15 to 7	−15 to 7	V
Output voltage range, V_O		−15 to 15	−15 to 15	V
Continuous total power dissipation (see Note 2)		See Dissipation Rating Table		
Operating free-air temperature range, T_A		−55 to 125	0 to 70	°C
Storage temperature range, T_{stg}		−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or W package	300		°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, refer to the maximum supply voltage curve, Figure 6. In the FK and J packages, SN55188 chips are alloy mounted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	–
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	–
W	1000 mW	8.0 mW/°C	640 mW	200 mW

recommended operating conditions

	SN55188			MC1488, SN75188			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC+}	7.5	9	15	7.5	9	15	V
Supply voltage, V_{CC-}	−7.5	−9	−15	−7.5	−9	−15	V
High-level input voltage, V_{IH}	1.9			1.9			V
Low-level input voltage, V_{IL}			0.8			0.8	V
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over operating free-air temperature range, $V_{CC\pm}$ = ±9 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN55188			MC1488, SN75188			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	V_{IL} = 0.8 V, R_L = 3 kΩ	V_{CC+} = 9 V, V_{CC-} = −9 V	6	7		6	7		V
			V_{CC+} = 13.2 V, V_{CC-} = −13.2 V	9	10.5		9	10.5		
V_{OL}	Low-level output voltage	V_{IH} = 1.9 V, R_L = 3 kΩ	V_{CC+} = 9 V, V_{CC-} = −9 V		−7‡	−6		−7	−6	V
			V_{CC+} = 13.2 V, V_{CC-} = −13.2 V		−10.5‡	−9		−10.5	−9	
I_{IH}	High-level input current	V_I = 5 V				10			10	μA
I_{IL}	Low-level input current	V_I = 0			−1	−1.6		−1	−1.6	mA
$I_{OS(H)}$	Short-circuit output current at high level§	V_I = 0.8 V,	V_O = 0	−4.6	−9	−13.5	−6	−9	−12	mA
$I_{OS(L)}$	Short-circuit output current at low level§	V_I = 1.9 V,	V_O = 0	4.6	9	13.5	6	9	12	mA
r_o	Output resistance, power off	V_{CC+} = 0, V_O = −2 V to 2 V	V_{CC-} = 0,	300			300			Ω
I_{CC+}	Supply current from V_{CC+}	V_{CC+} = 9 V, No load	All inputs at 1.9 V		15	20		15	20	mA
			All inputs at 0.8 V		4.5	6		4.5	6	
		V_{CC+} = 12 V, No load	All inputs at 1.9 V		19	25		19	25	
			All inputs at 0.8 V		5.5	7		5.5	7	
		V_{CC+} = 15 V, No load, T_A = 25°C	All inputs at 1.9 V			34			34	
			All inputs at 0.8 V			12			12	
I_{CC-}	Supply current from I_{CC-}	V_{CC-} = −9 V, No load	All inputs at 1.9 V		−13	−17		−13	−17	mA
			All inputs at 0.8 V			−0.5			−0.015	
		V_{CC-} = −12 V, No load	All inputs at 1.9 V		−18	−23		−18	−23	
			All inputs at 0.8 V			−0.5			−0.015	
		V_{CC-} = −15 V, No load, T_A = 25°C	All inputs at 1.9 V			−34			−34	
			All inputs at 0.8 V			−2.5			−2.5	
P_D	Total power dissipation	V_{CC+} = 9 V, No load	V_{CC-} = −9 V,			333			333	mW
		V_{CC+} = 12 V, No load	V_{CC-} = −12 V,			576			576	

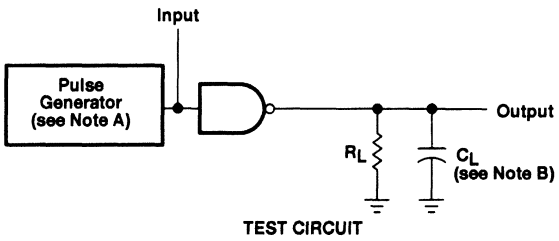
† All typical values are at T_A = 25°C.
‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only, e.g., if −6 V is a maximum, the typical value is a more negative voltage.
§ Not more than one output should be shorted at a time.

switching characteristics, $V_{CC\pm}$ = ±9 V, T_A = 25°C

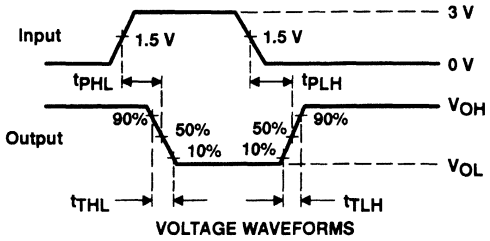
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 3 kΩ, See Figure 1	C_L = 15 pF,		220	350	ns
t_{PHL}	Propagation delay time, high- to low-level output				100	175	ns
t_{TLH}	Transition time, low- to high-level output†				55	100	ns
t_{THL}	Transition time, high- to low-level output†				45	75	ns
t_{TLH}	Transition time, low- to high-level output‡	R_L = 3 kΩ to 7 kΩ, See Figure 1	C_L = 2500 pF,		2.5		µs
t_{THL}	Transition time, high- to low-level output‡				3.0		µs

† Measured between 10% and 90% points of output waveform.
‡ Measured between 3 V and −3 V points on the output waveform (EIA/TIA-232-E conditions).

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: t_w = 0.5 µs, PRR ≤ 1 MHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

VOLTAGE TRANSFER CHARACTERISTICS

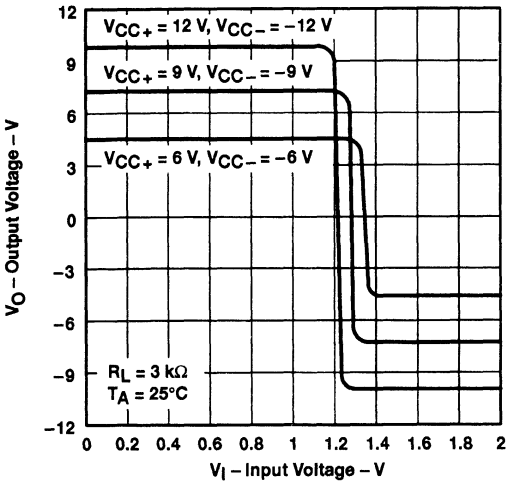


Figure 2

OUPUT CURRENT vs OUTPUT VOLTAGE

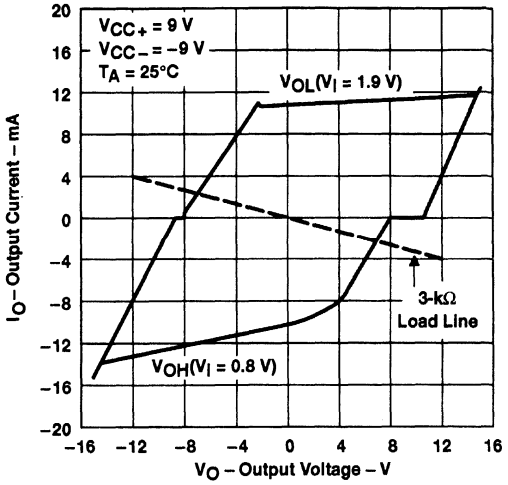


Figure 3

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

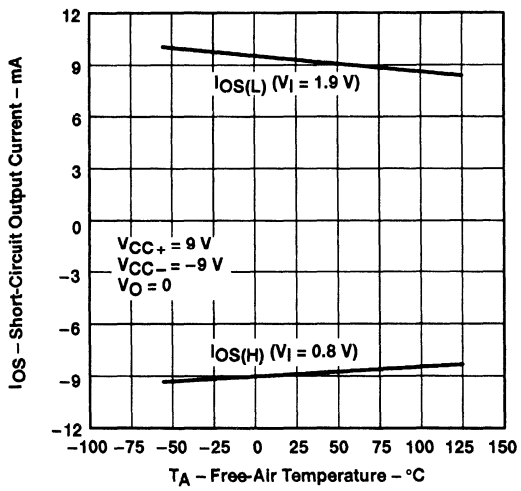


Figure 4

SLEW RATE vs LOAD CAPACITANCE

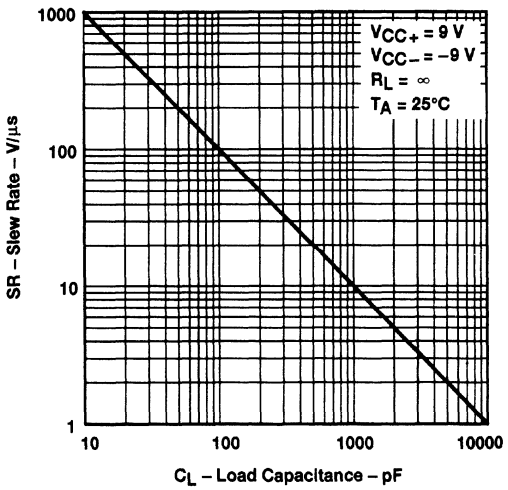


Figure 5

† Data for temperatures below 0°C and above 70°C are applicable to SN55188 circuit only.

THERMAL INFORMATION†

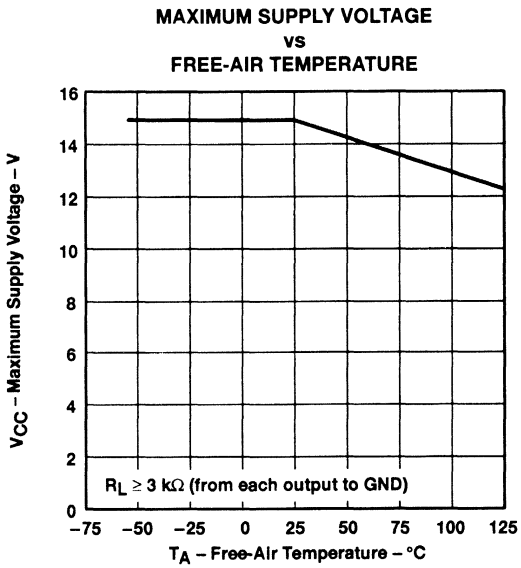


Figure 6

† Data for temperatures below 0°C and above 70°C are applicable to SN55188 circuit only.

APPLICATION INFORMATION

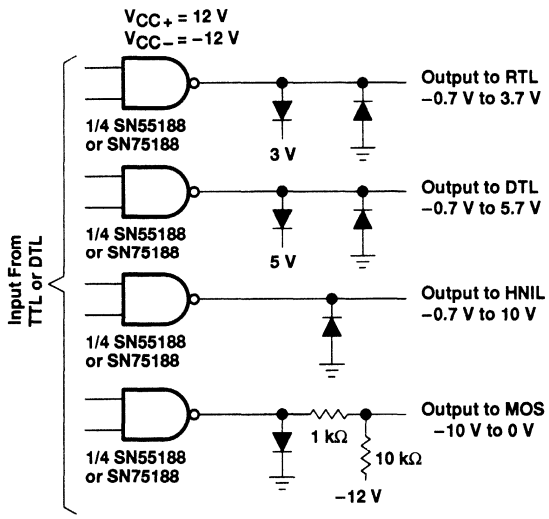
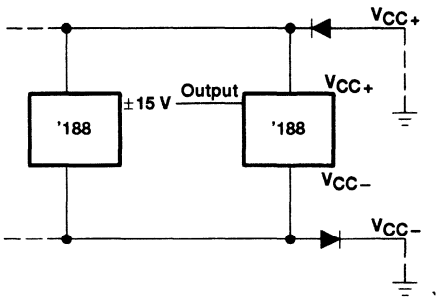


Figure 7. Logic Translator Applications

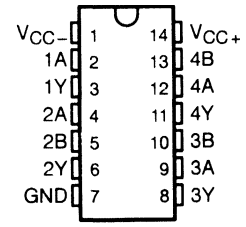


Diodes placed in series with the V_{CC+} and V_{CC-} leads will protect the SN55188/SN75188 in the fault condition in which the device outputs are shorted to ±15 V and the power supplies are at low voltage and provide low-impedance paths to ground.

Figure 8. Power Supply Protection to Meet Power-Off Fault Conditions of ANSI EIA/TIA-232-E

- **Bi-MOS Technology With TTL and CMOS Compatibility**
- **Meets or Exceeds the Requirements of ANSI EIA/TIA-232-E and ITU Recommendation V.28**
- **Very Low Quiescent Current . . . 95 μA Typ**
  $V_{CC\pm}$ = ±12 V
- **Current-Limited Outputs . . . 10 mA Typ**
- **CMOS-and TTL-Compatible Inputs**
- **On-Chip Slew Rate Limited to 30 V/μs max**
- **Flexible Supply Voltage Range**
- **Characterized at $V_{CC\pm}$ of ±4.5 V and ±15 V**
- **Functionally Interchangeable With Texas Instruments SN75188, Motorola MC1488, and National Semiconductor DS14C88**

D, DB†, OR N PACKAGE
(TOP VIEW)



† The DB package is only avalable left-end taped and reeled, i.e., order device SN75C188DBLE.

Function Tables

DRIVER 1

B	Y
H	L
L	H

DRIVERS 2 THRU 4

A	B	Y
H	H	L
L	X	H
X	L	H

H = high level, L = low level, X = don't care

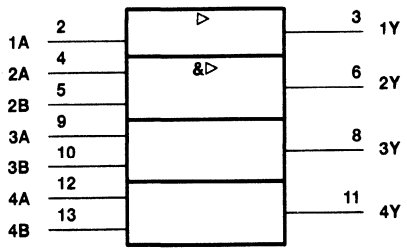
description

The SN65C188 and SN75C188 are monolithic, low-power, quadruple line drivers that interface data terminal equipment with data communications equipment. These devices are designed to conform to ANSI Standard EIA/TIA-232-E.

An external diode in series with each supply-voltage terminal is needed to protect the SN65C188 and SN75C188 under certain fault conditions to comply with EIA/TIA-232-E.

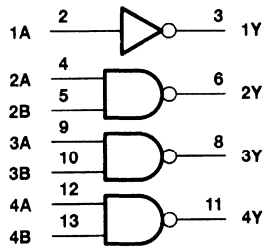
The SN65C188 is characterized for operation from −40°C to 85°C. The SN75C188 is characterized for operation from 0°C to 70°C.

logic symbol‡



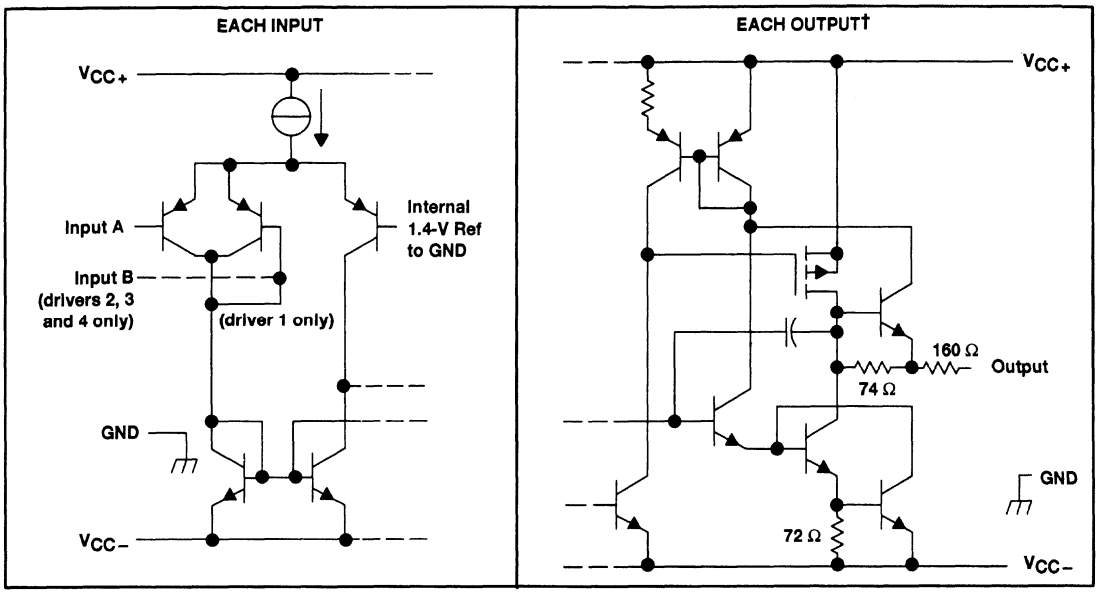
‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



positive logic
$Y = \overline{A}$ (driver 1)
$Y = \overline{AB}$ or $\overline{A} + \overline{B}$ (drivers 2 through 4)

schematics of inputs and outputs



† All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) ..... 15 V
Supply voltage, V_{CC-} (see Note 1) ..... −15 V
Input voltage range, V_I ..... V_{CC-} to V_{CC+}
Output voltage range, V_O ..... V_{CC-} −6 V to V_{CC+} +6 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65C188 ..... −40°C to 85°C
SN75C188 ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
DB	525 mW	4.2 mW/°C	336 mW	273 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}		4.5	12	15	V
Supply voltage, V_{CC-}		−4.5	−12	−15	V
Input voltage, V_I		V_{CC-}+2		V_{CC+}	V
High-level Input voltage, V_{IH}		2			V
Low-level Input voltage, V_{IL}				0.8	V
Operating free-air temperature, T_A	SN65C188	−40		85	°C
	SN75C188	0		70	

electrical characteristics over operating free-air temperature range, V_{CC+} = 12 V, V_{CC-} = −12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{IL} = 0.8 V, R_L = 3 kΩ	V_{CC+} = 5 V, V_{CC-} = −5 V		4			V
			V_{CC+} = 12 V, V_{CC-} = −12 V		10			
V_{OL}	Low-level output voltage (see Note 2)	V_{IH} = 2 V, R_L = 3 kΩ	V_{CC+} = 5 V, V_{CC-} = −5 V				−4	V
			V_{CC+} = 12 V, V_{CC-} = −12 V				−10	
I_{IH}	High-level input current	V_I = 5 V					10	µA
I_{IL}	Low-level input current	V_I = 0					−10	µA
$I_{OS(H)}$	High-level short-circuit output current‡	V_I = 0.8 V, V_O = 0 or V_{CC-}			−5.5	−10	−19.5	mA
$I_{OS(L)}$	Low-level short-circuit output current‡	V_I = 2 V, V_O = 0 or V_{CC+}			5.5	10	19.5	mA
r_O	Output resistance, power off	V_{CC+} = 0, V_{CC-} = 0,		V_I = −2 V to 2 V	300			Ω
I_{CC+}	Supply current from V_{CC+}	V_{CC+} = 5 V, No load	V_{CC-} = −5 V,	All inputs at 2 V or 0.8 V		90	160	µA
		V_{CC+} = 12 V, No load	V_{CC-} = −12 V,	All inputs at 2 V or 0.8 V		95	160	
I_{CC-}	Supply current from V_{CC-}	V_{CC+} = 5 V, No load	V_{CC-} = −5 V,	All inputs at 2 V or 0.8 V		−90	−160	µA
		V_{CC+} = 12 V, No load	V_{CC-} = −12 V,	All inputs at 2 V or 0.8 V		−95	−160	

† All typical values are at T_A = 25°C.

‡ Not more than one output should be shorted at a time.

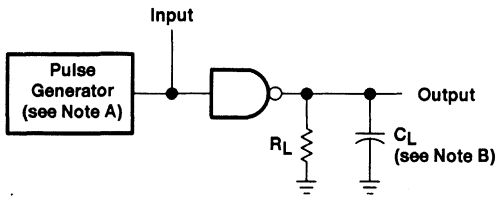
NOTE 2: The algebraic convention, in which the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only; e.g., if −4 V is a maximum, the typical value is a more negative voltage..

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −12 V, T_A = 25°C

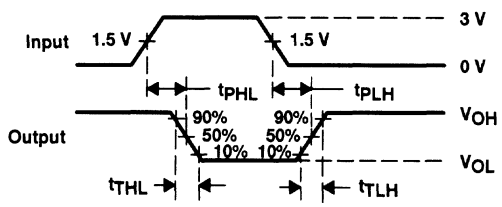
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output†	R_L = 3 kΩ, C_L = 15 pF, See Figure 1			3	µs
t_{PHL}	Propagation delay time, high- to low-level output†				3.5	µs
t_{TLH}	Transition time, low- to high-level output‡		0.53		3.2	µs
t_{THL}	Transition time, high- to low-level output‡		0.53		3.2	µs
t_{TLH}	Transition time, low- to high-level output§	R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF, See Figure 1		1.5		µs
t_{THL}	Transition time, high- to low-level output§			1.5		µs
SR	Output slew rate§	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF	6	15	30	V/µs

† Measured at the 50% level
‡ Measured between the 10% and 90% points on the output waveform
§ Measured between the 3 V and −3 V points on the output waveform (EIA/TIA-232-E conditions), all unused inputs tied either high or low

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: t_w = 25 µs, PRR = 20 kHZ, Z_O = 50 Ω, $t_r = t_f \leq 50$ ns.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

VOLTAGE TRANSFER CHARACTERISTICS

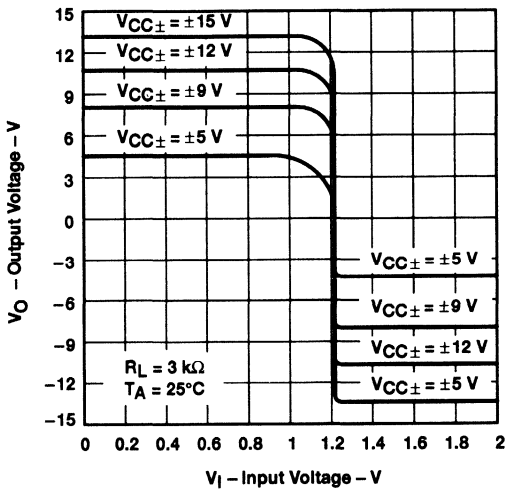


Figure 2

OUTPUT CURRENT vs OUTPUT VOLTAGE

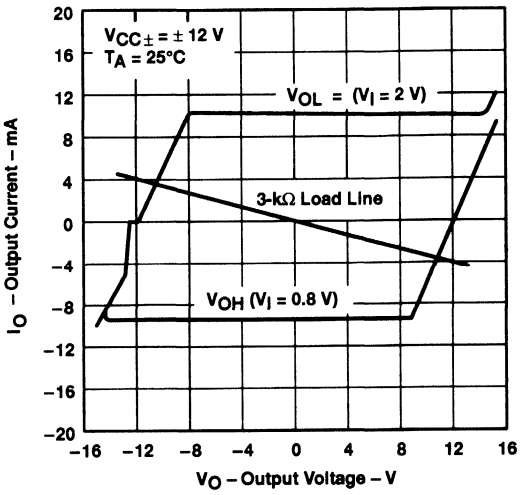


Figure 3

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE†

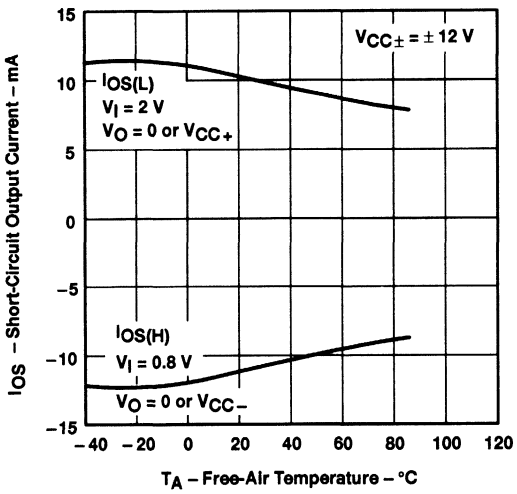


Figure 4

OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE†

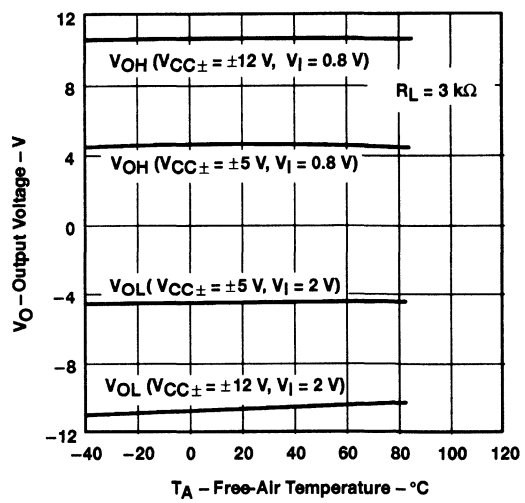


Figure 5

† Only the 0°C to 70°C portion of the curves applies to the SN75C188.

TYPICAL CHARACTERISTICS

INPUT CURRENT vs FREE-AIR TEMPERATURE†

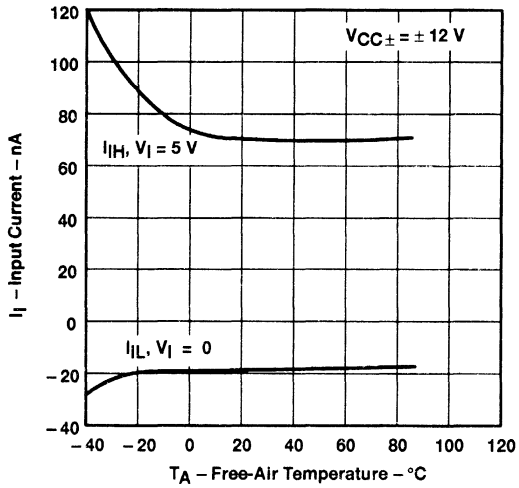


Figure 6

POWER-OFF OUTPUT RESISTANCE vs FREE-AIR TEMPERATURE†

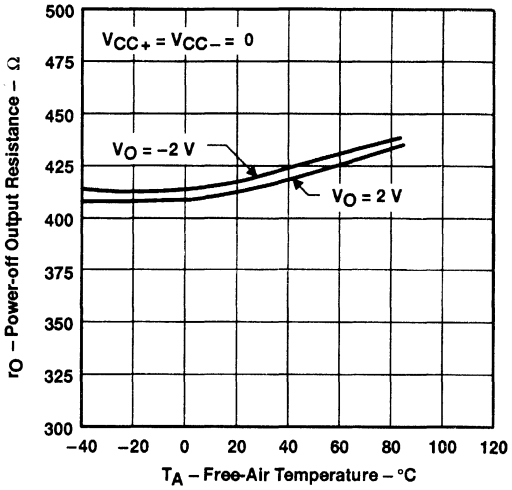


Figure 7

SUPPLY CURRENT vs FREE-AIR TEMPERATURE†

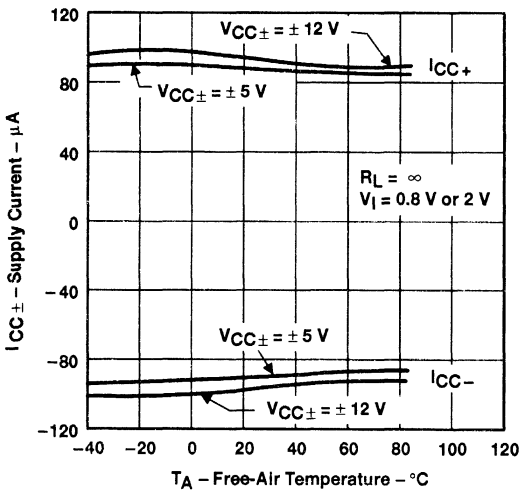


Figure 8

OUTPUT SLEW RATE vs FREE-AIR TEMPERATURE†

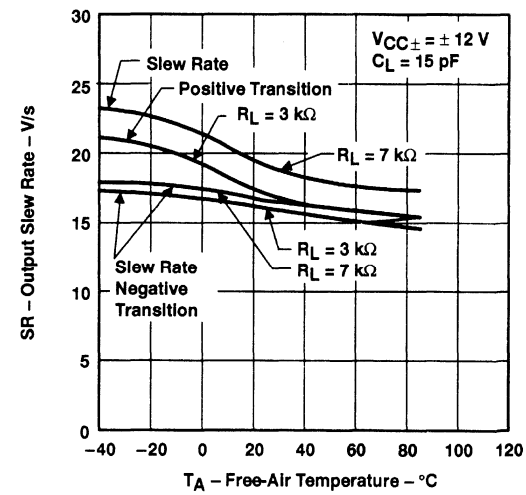


Figure 9

† Only the 0°C to 70°C portion of the curves applies to the SN75C188.

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE†

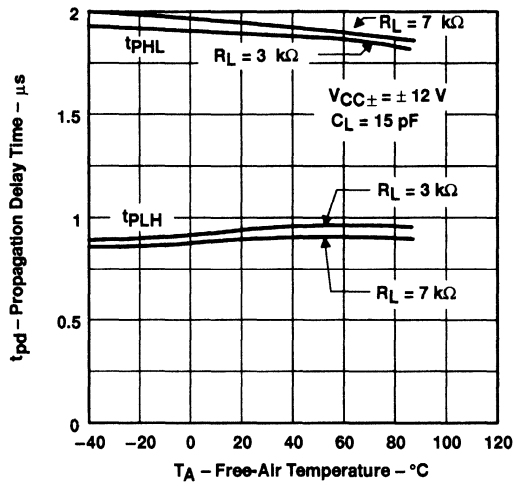


Figure 10

OUTPUT TRANSITION TIME
vs
FREE-AIR TEMPERATURE†

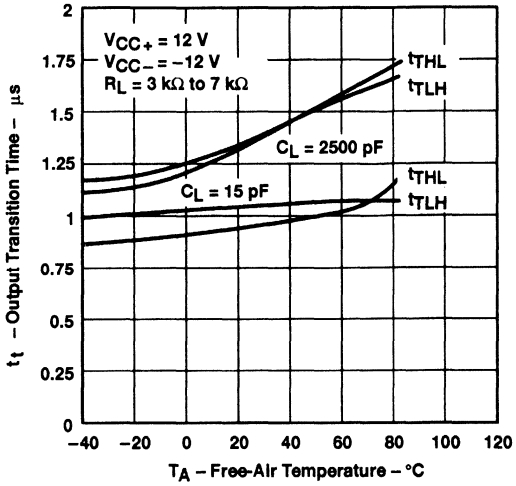


Figure 11

† Only the 0°C to 70°C portion of the curves applies to the SN75C188.

APPLICATION INFORMATION

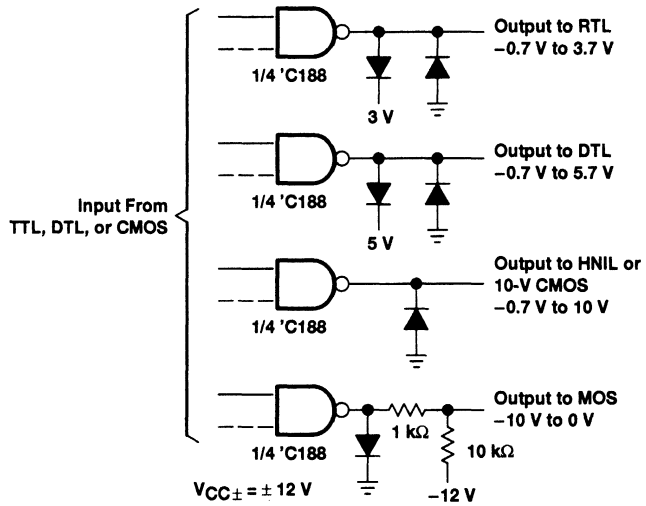
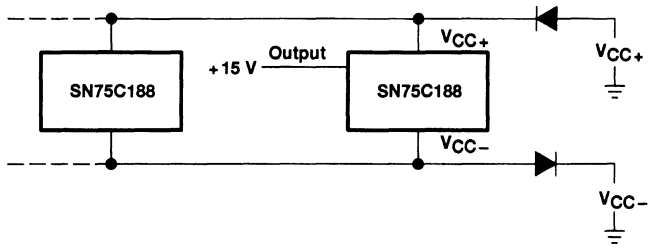


Figure 12. Logic Translator Applications

APPLICATION INFORMATION



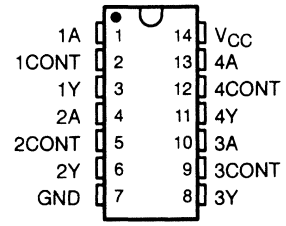
NOTE A: External diodes placed in series with the V_{CC+} and V_{CC-} leads will protect the SN75C188 in the fault condition where the device outputs are shorted to ±15 V and the power supplies are at low voltage and provide low-impedance paths to GND.

Figure 13. Power Supply Protection to Meet Power-Off Fault Conditions of Standard EIA/TIA-232-E

SLLS095B – SEPTEMPER 1973 – REVISED MAY 1995

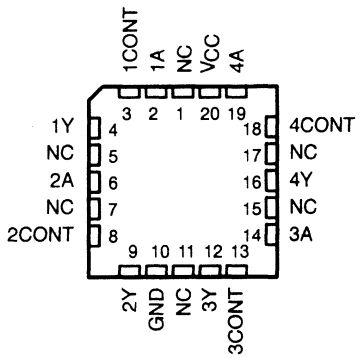
- **Input Resistance . . . 3 kΩ to 7 kΩ**
- **Input Signal Range . . . ±30 V**
- **Operate From Single 5-V Supply**
- **Built-In Input Hysteresis (Double Thresholds)**
- **Have Response Control that Provides:**
  Input Threshold Shifting
  Input Noise Filtering
- **Meet or Exceed the Requirements of ANSI EIA/TIA-232-E and ITU Recommendation V.28**
- **Fully Interchangeable With Motorola™ MC1489 and MC1489A**

SN55189, SN55189A . . . J OR W PACKAGE
MC1489, MC1489A, SN75189, SN75189A
D, N, OR NS† PACKAGE
(TOP VIEW)



† The NS package is only available left-end taped and reeled. For SN75189, i.e., order SN75189NSLE.

SN55189, SN55189A . . . FK PACKAGE
(TOP VIEW)



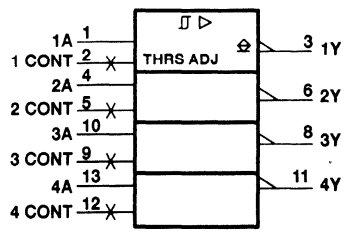
NC – No internal connection

description

These devices are monolithic low-power Schottky quadruple line receivers designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by ANSI EIA/TIA-232-E. A separate response control terminal is provided for each receiver. A resistor or a resistor and bias voltage source can be connected between this terminal and ground to shift the input threshold levels. An external capacitor can be connected between this terminal and ground to provide input noise filtering.

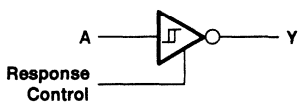
The SN55189 and SN55189A are characterized for operation over the full military temperature range of −55°C to 125°C. The MC1489, MC1489A, SN75189, and SN75189A are characterized for operation from 0°C to 70°C.

logic symbol‡



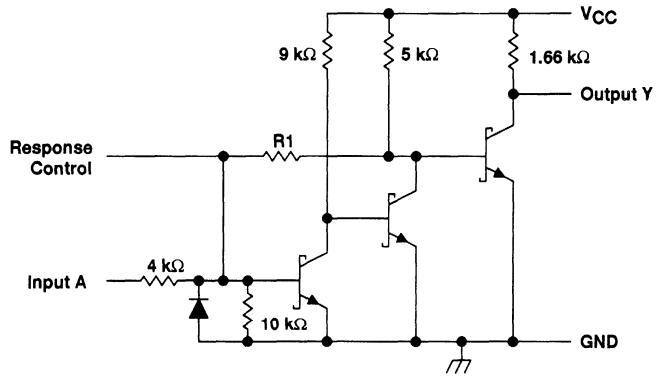
‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, NS, and W packages.

logic diagram (positive logic)



Motorola is a trademark of Motorola, Incorporated.

schematic (each receiver)



	MC1489 SN55189 SN75189	MC1489A SN55189A SN75189A
R1	8.4 kΩ	1.84 kΩ

Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

	SN55189 SN55189A	MC1489, MC1498A SN75189 SN75189A	UNIT
Supply voltage, V_{CC} (see Note 1)	10	10	V
Input voltage, V_I	±30	±30	V
Output current, I_O	20	20	mA
Continuous total power dissipation	See Dissipation Rating Table		
Operating temperature range, T_A	−55 to 125	0 to 70	°C
Storage temperature range, T_{stg}	−65 to 150	−65 t0 150	°C
Case temperature for 60 seconds: FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or NS package		260	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminals.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J†	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	N/A
NS	625 mW	4.0 mW/°C	445 mW	N/A
W	1000 mW	8.0 mW/°C	640 mW	200 mW

† In the J package, SN55189 and SN55189A chips are either silver glass or alloy mounted.

electrical characteristics over operating free-air temperature range, V_{CC} = 5 V ± 1% (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SN55189 SN55189A			MC1489, MC1489A SN75189 SN75189A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IT+}	Positive-going input threshold voltage	1	'89	T_A = 25°C	1	1.3	1.5	1	1.3	1.5	V
				T_A = 0°C to 70°C				0.9		1.6	
				T_A = −55°C to 125°C	0.6		1.9				
			'89A	T_A = 25°C	1.75	1.9	2.25	1.75	1.9	2.25	
				T_A = 0°C to 70°C				1.55		2.25	
				T_A = −55°C to 125°C	1.30		2.65				
V_{IT-}	Negative-going input threshold voltage	1	'89, '89A	T_A = 25°C	0.75	1.0	1.25	0.75	1.0	1.25	V
				T_A = 0°C to 70°C				0.65		1.25	
				T_A = −55°C to 125°C	0.35		1.6				
V_{OH}	High-level output voltage	1	V_I = 0.75 V,	I_{OH} = −0.5 mA	2.6	4	5	2.6	4	5	V
			Input open,	I_{OH} = −0.5 mA	2.6	4	5	2.6	4	5	
V_{OL}	Low-level output voltage	1	V_I = 3 V,	I_{OL} = 10 mA		0.2	0.45		0.2	0.45	V
I_{IH}	High-level input current	2	V_I = 25 V		3.6		8.3	3.6		8.3	mA
			V_I = 3 V		0.43			0.43			
I_{IL}	Low-level input current	2	V_I = −25 V		−3.6		−8.3	−3.6		−8.3	mA
			V_I = −3 V		−0.43			−0.43			
I_{OS}	Short-circuit output current	3				−3			−3		mA
I_{CC}	Supply current	2	V_I = 5 V,	Outputs open		20	26		20	26	mA

† All characteristics are measured with the response control terminal open.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	4	R_L = 3.9 kΩ		25	85	ns
t_{PHL}	Propagation delay time, high- to low-level output		R_L = 390 Ω		25	50	
t_{TLH}	Transition time, low- to high-level output		R_L = 3.9 kΩ		120	175	ns
t_{THL}	Transition time, high- to low-level output		R_L = 390 Ω		10	20	

PARAMETER MEASUREMENT INFORMATION†

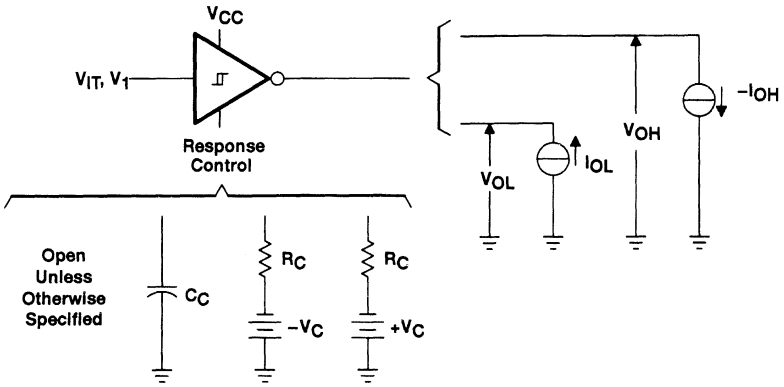
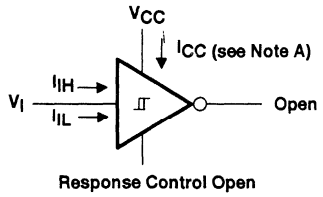


Figure 1. V_{IT+}, V_{IT-}, V_{OH}, V_{OL}



NOTE A. I_{CC} is tested for all four receivers simultaneously.

Figure 2. I_{IH}, I_{IL}, I_{CC}

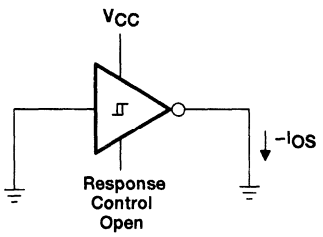
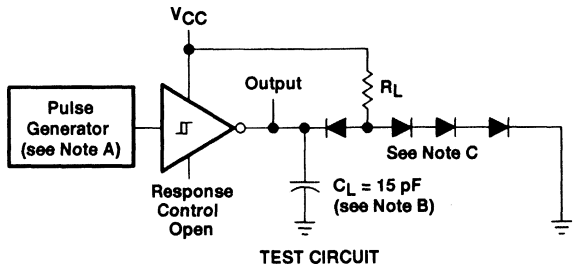


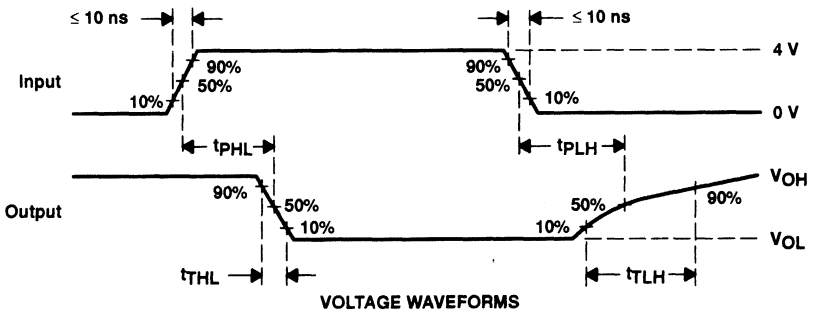
Figure 3. I_{OS}

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: B. The pulse generator has the following characteristics: Z_O = 50 Ω, t_w = 500 ns.
C. C_L includes probe and jig capacitances.
D. All diodes are 1N3064 or equivalent.

Figure 4. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

SN65189, SN75189
OUTPUT VOLTAGE
vs
INPUT VOLTAGE

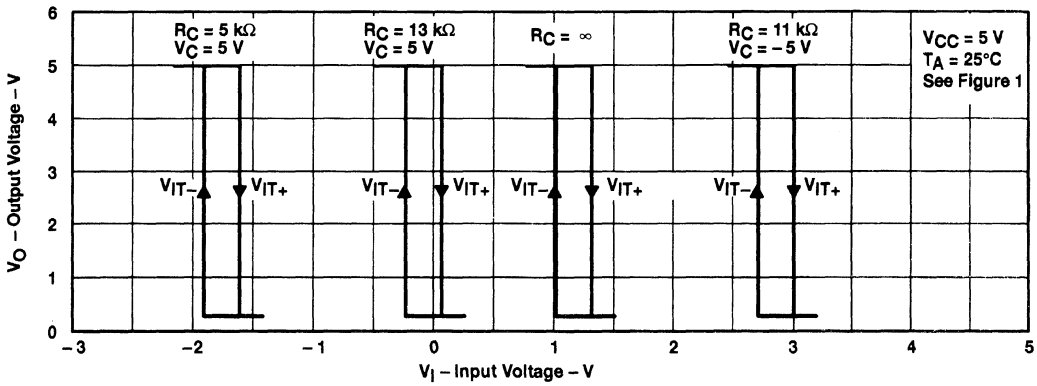


Figure 5

SN65189A, SN75189A
OUTPUT VOLTAGE
vs
INPUT VOLTAGE

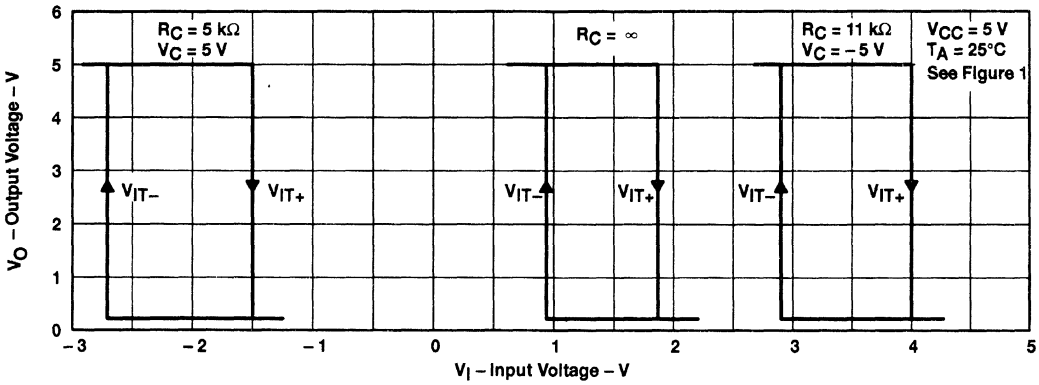


Figure 6

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS†

INPUT THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

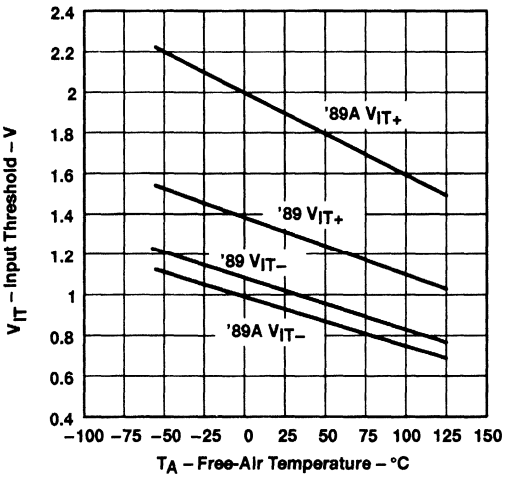


Figure 7

INPUT THRESHOLD VOLTAGE
vs
SUPPLY VOLTAGE

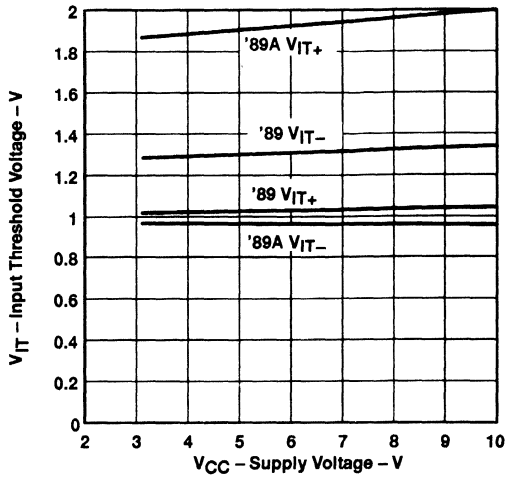


Figure 8

SN75189
NOISE REJECTION

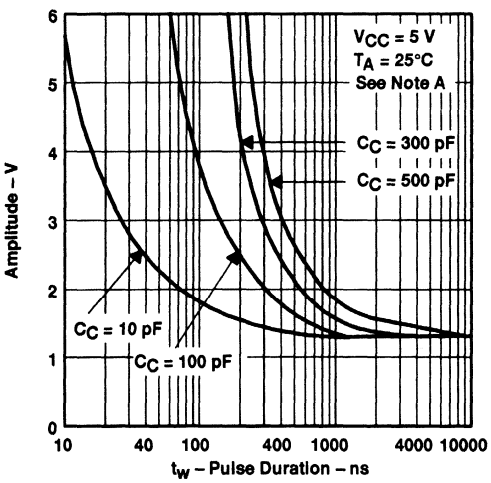


Figure 9

SN75189A
NOISE REJECTION

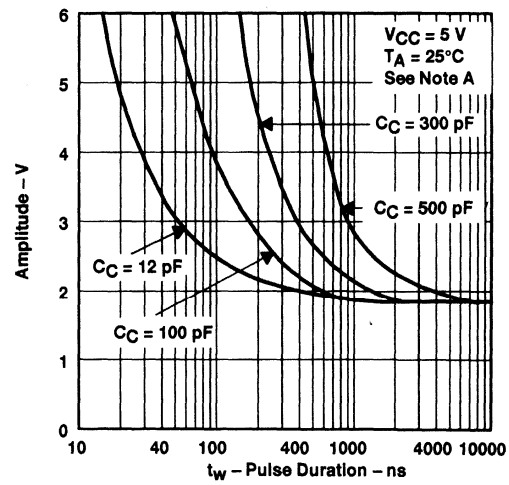


Figure 10

NOTE A: These figures shows the maximum amplitude of a positive-going pulse that, starting from 0 V, will not cause a change of the output level.

† Data for free-air temperatures below 0°C and above 70°C are applicable to SN55189 and SN55189A circuits only.

TYPICAL CHARACTERISTICS

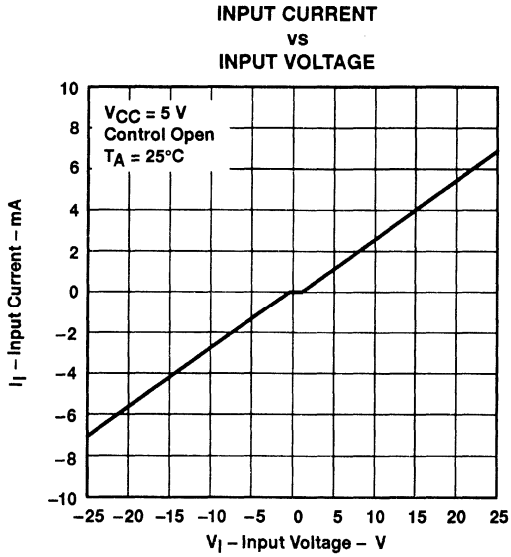
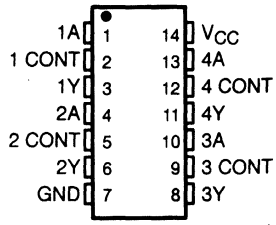


Figure 11

SLLS041D – OCTOBER 1988 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of ANSI EIA/TIA-232-E and ITU Recommendation V.28**
- **Low Supply Current . . . 420 μA Typ**
- **Preset On-Chip Input Noise Filter**
- **Built-In Input Hysteresis**
- **Response and Threshold Control Inputs**
- **Push-Pull Outputs**
- **Functionally Interchangeable and Pin Compatible With Texas Instruments SN75189/SN75189A, Motorola MC1489/MC1489A, and National Semiconductor DS14C88A**

D, DB†, N, OR NS† PACKAGE
(TOP VIEW)



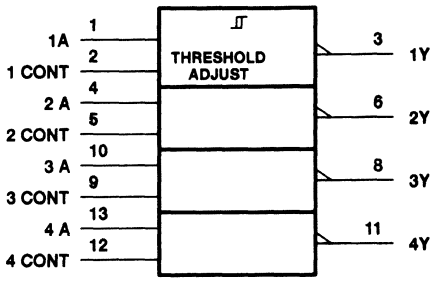
† The DB and NS packages are only available left-end taped and reeled, i.e., order SN75C189ADBLE or SN75C189ANSLE.

description

The SN65C189, SN65C189A, SN75C189, and SN75C189A are low-power bipolar quadruple line receivers that are used to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). These devices have been designed to conform with ANSI Standard EIA/TIA-232-E.

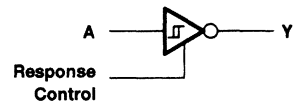
The SN65C189 and SN75C189 have a 0.33 V typical hysteresis compared with 0.97 V for the SN65C189A and SN75C189A. Each receiver has provision for adjustment of the overall input threshold levels. This is achieved by choosing external series resistors and voltages to provide bias levels for the response control pins. The output is in the high logic state if the input is left open circuited or shorted to ground.

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (each receiver)

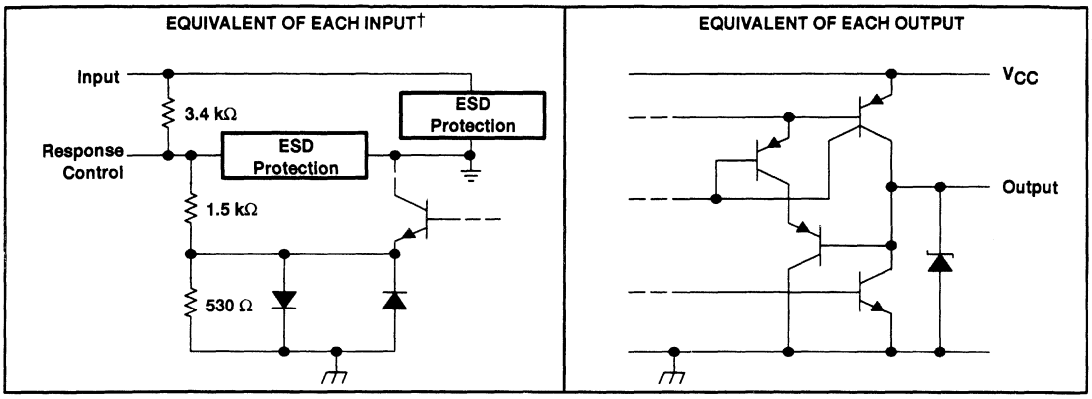


These devices have an on-chip filter that rejects input pulses of shorter than 1-μs minimum duration. An external capacitor may be connected from the control pins to ground to provide further input noise filtering for each receiver.

The SN65C189, SN75C189, SN65C189A, and SN75C189A have been designed using low-power techniques in a bipolar technology. In most applications, these receivers will interface to single inputs of peripheral devices such as UARTs, ACEs, or microprocessors. By using sampling, such peripheral devices are usually insensitive to the transition times of the input signals. If this is not the case or for other uses, it is recommended that the SN65C189, SN75C189, SN65C189A, and SN75C189A outputs be buffered by single Schmitt input gates or single gates of the HCMOS, ALS, or 74F logic families.

The SN65C189 and SN65C189A are characterized for operation from −40°C to 85°C. The SN75C189 and SN75C189A are characterized for operation from 0°C to 70°C.

schematic of inputs and outputs



† All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage range, V_I ..... −30 V to 30 V
Output voltage range, V_O ..... −0.3 V to V_{CC}+ 0.3 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65C189, SN65C189A ..... −40°C to 85°C
SN75C189, SN75C189A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
DB	525 mW	4.2 mW/°C	336 mW	273 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW
NS	500 mW	4.0 mW/°C	320 mW	260 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	6	V
Input voltage, V_I (see Note 2)		−25		25	V
High-level output current, I_{OH}				−3.2	mA
Low-level output current, I_{OL}				3.2	mA
Response control current				±1	mA
Operating free-air temperature, T_A	SN65C189, SN65C189A	−40		85	°C
	SN75C189, SN75C189A	0		70	

NOTE 2: The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if −10 V is a maximum, the typical value is a more negative voltage.

electrical characteristics over recommended free-air temperature range, V_{CC} = 5 V ±10% (unless otherwise noted) (see Note 3)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	'C189	See Figure 1		1		1.5	V
		'C189A			1.6		2.25	
V_{IT-}	Negative-going input threshold voltage	'C189	See Figure 1		0.75		1.25	V
		'C189A			0.75	1	1.25	
V_{hys}	Input hysteresis voltage ($V_{IT+} - V_{IT-}$)	'C189	See Figure 1		0.15	0.33		V
		'C189A			0.65	0.97		
V_{OH}	High-level output voltage		V_{CC} = 4.5 V to 6 V, I_{OH} = −20 μA	V_I = 0.75 V,	3.5			V
			V_{CC} = 4.5 V to 6 V, I_{OH} = −3.2 mA	V_I = 0.75 V,	2.5			
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V to 6 V, I_{OL} = 3.2 mA	V_I = 3 V,			0.4	V
I_{IH}	High-level input current		See Figure 2	V_I = 25 V	3.6		8.3	mA
				V_I = 3 V	0.43		1	
I_{IL}	Low-level input current		See Figure 2	V_I = −25 V	−3.6		−8.3	mA
				V_I = −3 V	−0.43		−1	
I_{OS}	Short-circuit output current		See Figure 3				−35	mA
I_{CC}	Supply current		V_I = 5 V, See Figure 2	No load,		420	700	μA

† All typical values are at T_A = 25°C.
NOTE 3: All characteristics are measured with response control terminal open.

switching characteristics, V_{CC} = 5 V ±10%, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 5 kΩ, C_L = 50 pF, See Figure 4			6	μs
t_{PHL}	Propagation delay time, high- to low-level output				6	μs
t_{TLH}	Transition time, low- to high-level output‡				500	ns
t_{THL}	Transition time, high- to low-level output‡				300	ns
$t_{w(N)}$	Duration of longest pulse rejected as noise§		1		6	μs

‡ Measured between 10% and 90% points of output waveform.
§ The receiver ignores any positive- or negative-going pulse that is less than the minimum value of $t_{w(N)}$ and accepts any postive- or negative-going pulse greater than the maximum of $t_{w(N)}$.

PARAMETER MEASUREMENT INFORMATION†

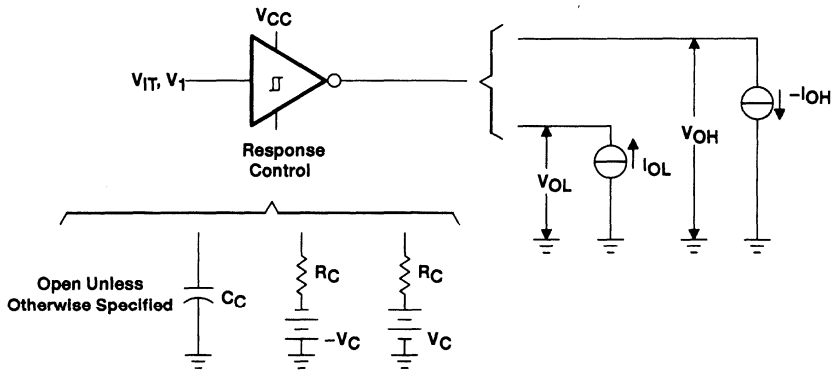


Figure 1. V_{T+}, V_{IT-}, V_{OH}, V_{OL}

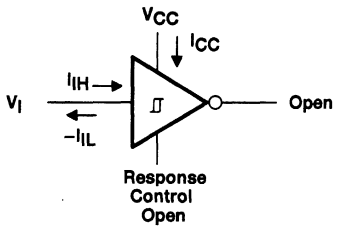


Figure 2. I_{IH}, I_{IL}, I_{CC}

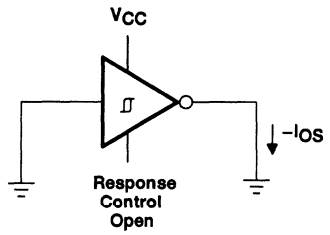


Figure 3. I_{OS}

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

TEXAS INSTRUMENTS
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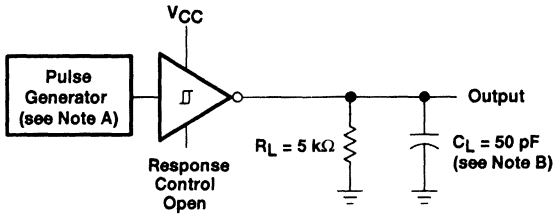
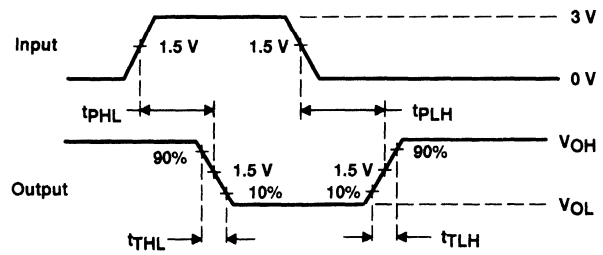
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, t_w = 25 μs.
B. C_L includes probe and jig capacitances.

Figure 4. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

SN75C189
INPUT THRESHOLD VOLTAGE (POSITIVE-GOING)
vs
FREE-AIR TEMPERATURE†

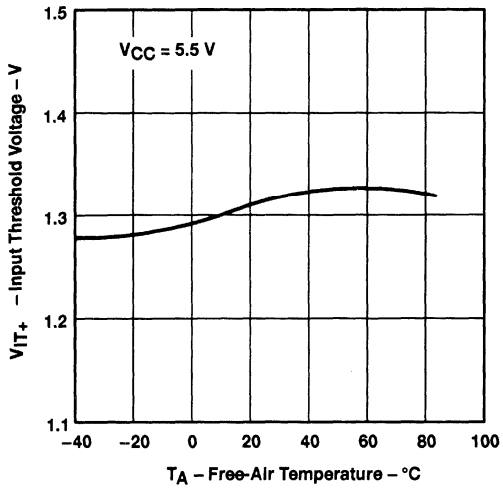


Figure 5

SN75C189A
INPUT THRESHOLD VOLTAGE (POSITIVE-GOING)
vs
FREE-AIR TEMPERATURE†

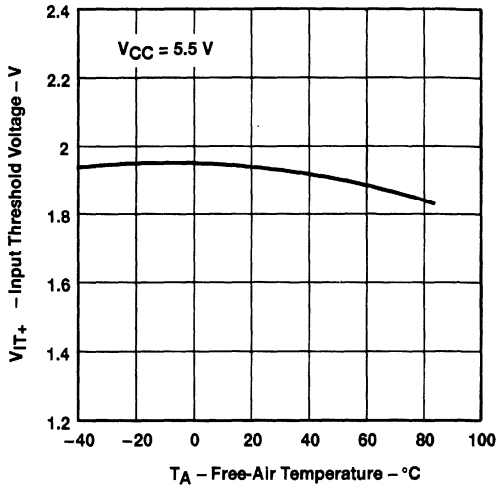


Figure 6

SN75C189
INPUT THRESHOLD VOLTAGE (NEGATIVE-GOING)
vs
FREE-AIR TEMPERATURE†

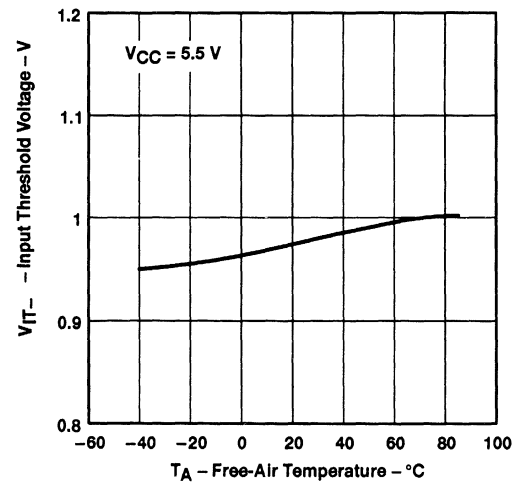


Figure 7

SN75C189A
INPUT THRESHOLD VOLTAGE (NEGATIVE-GOING)
vs
FREE-AIR TEMPERATURE†

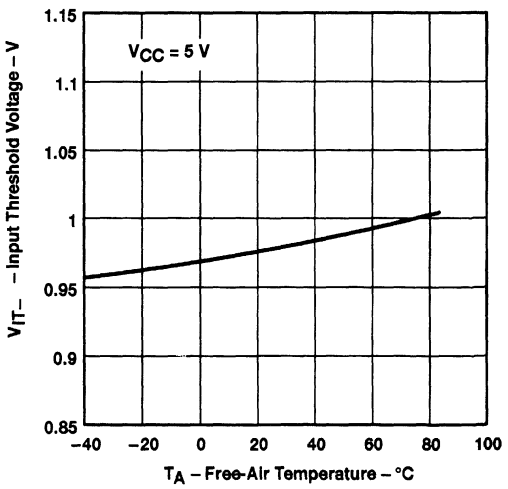


Figure 8

† Only the 0°C to 70°C portion of the curves applies to the SN75'.

TYPICAL CHARACTERISTICS

SN75C189
INPUT HYSTERESIS
vs
FREE-AIR TEMPERATURE†

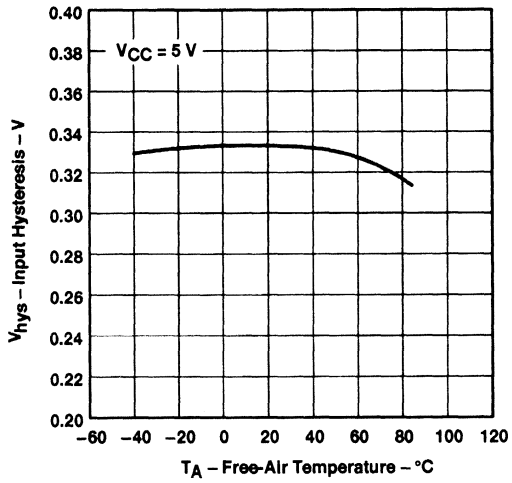


Figure 9

SN75C189A
INPUT HYSTERESIS
vs
FREE-AIR TEMPERATURE†

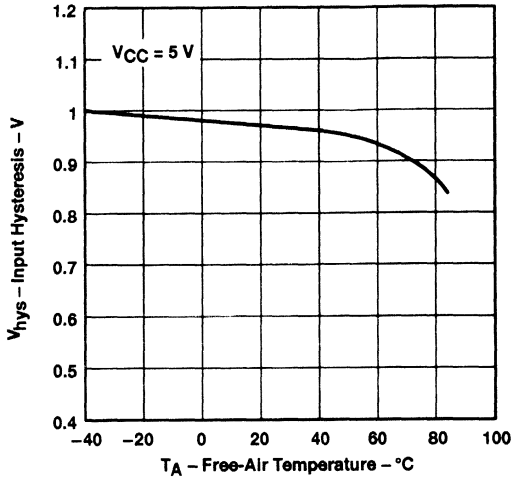


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE†

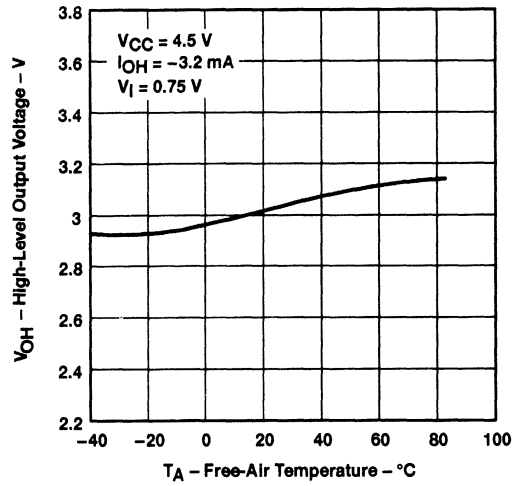


Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE†

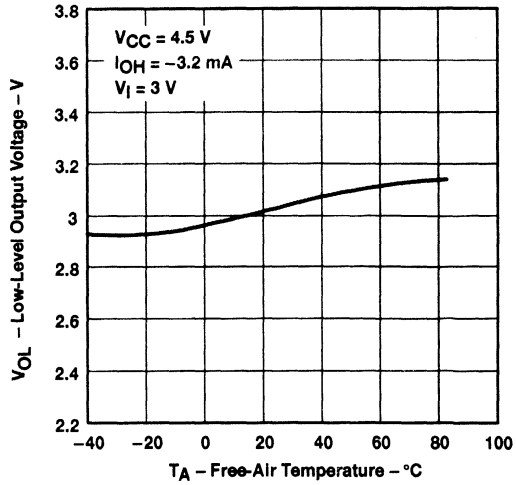


Figure 12

† Only the 0°C to 70°C portion of the curves applies to the SN75'.

TYPICAL CHARACTERISTICS

SN75C189
HIGH-LEVEL INPUT CURRENT
vs
FREE-AIR TEMPERATURE†

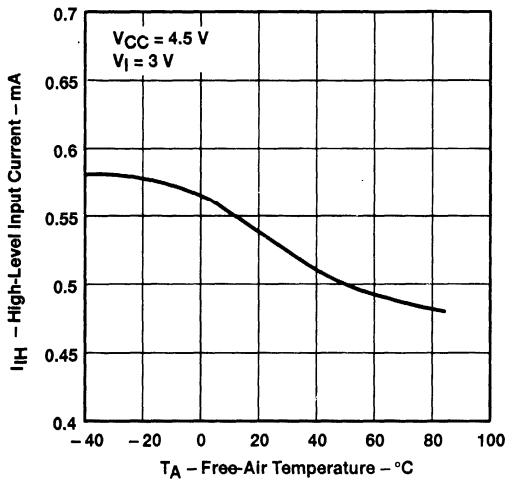


Figure 13

SN75C189A
HIGH-LEVEL INPUT CURRENT
vs
FREE-AIR TEMPERATURE†

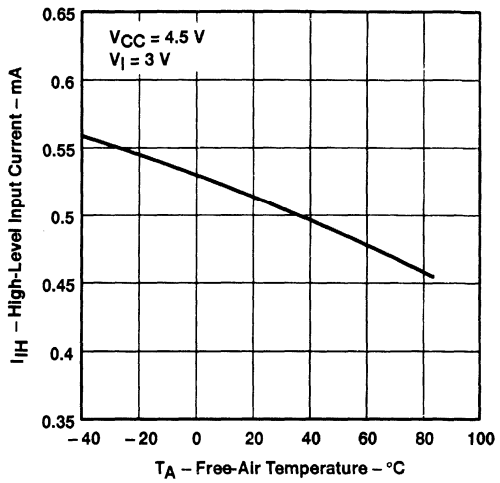


Figure 14

SN75C189
LOW-LEVEL INPUT CURRENT
vs
FREE-AIR TEMPERATURE†

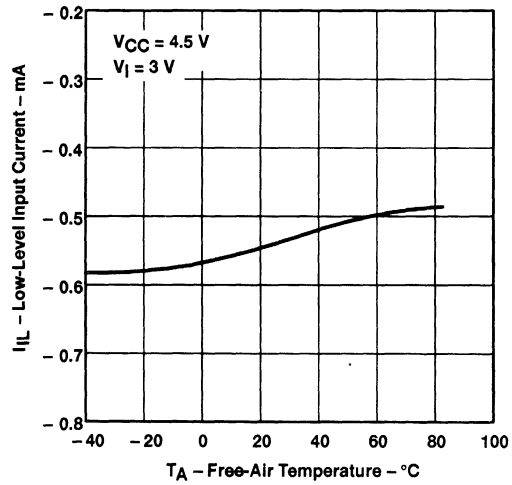


Figure 15

SN75C189A
LOW-LEVEL INPUT CURRENT
vs
FREE-AIR TEMPERATURE†

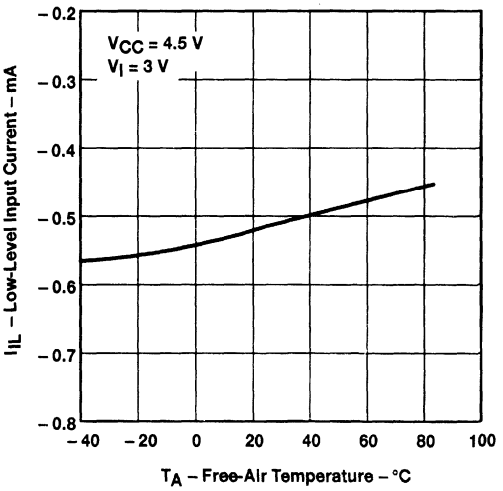


Figure 16

† Only the 0°C to 70°C portion of the curves applies to the SN75'.

TYPICAL CHARACTERISTICS

HIGH-LEVEL SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE†

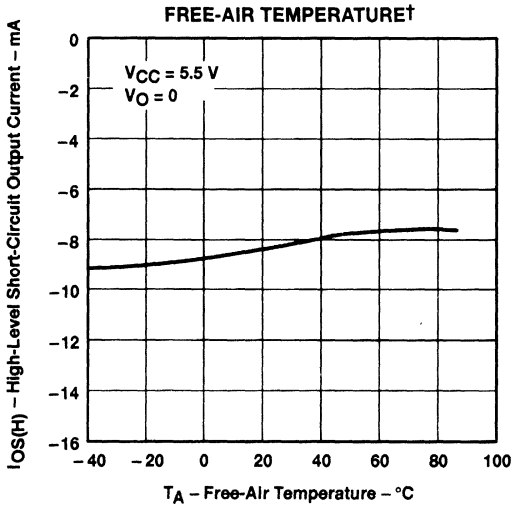


Figure 17

LOW-LEVEL SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE†

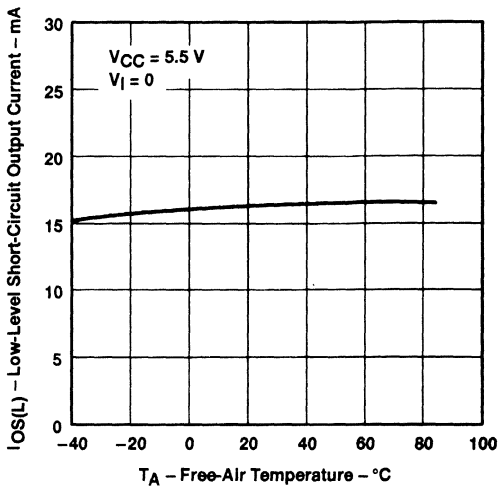


Figure 18

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE†

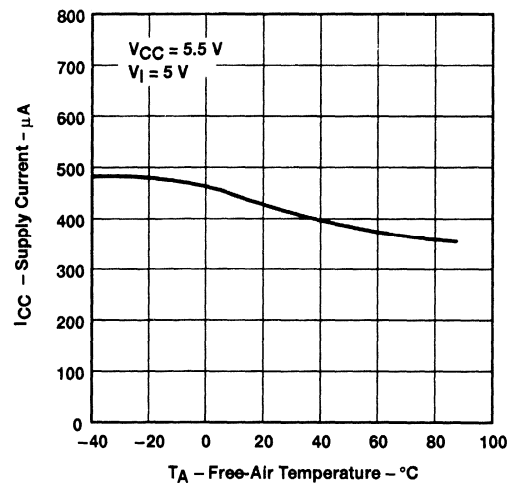


Figure 19

PROPAGATION DELAY TIME,
LOW-TO-HIGH LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE†

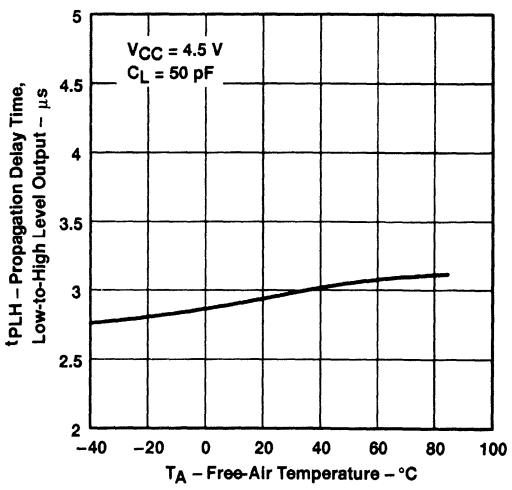


Figure 20

† Only the 0°C to 70°C portion of the curves applies to the SN75'.

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE†

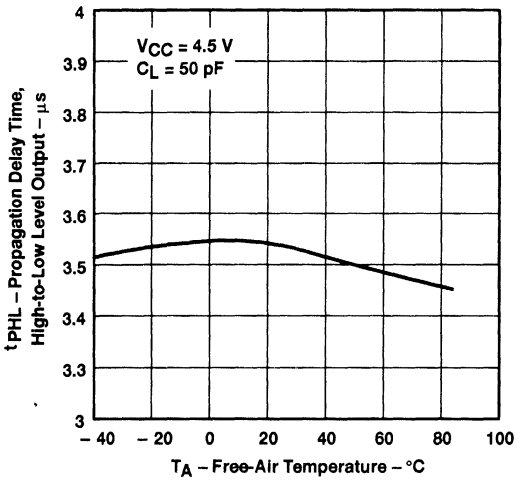


Figure 21

TRANSITION TIME,
LOW-TO-HIGH-LEVEL
vs
FREE-AIR TEMPERATURE†

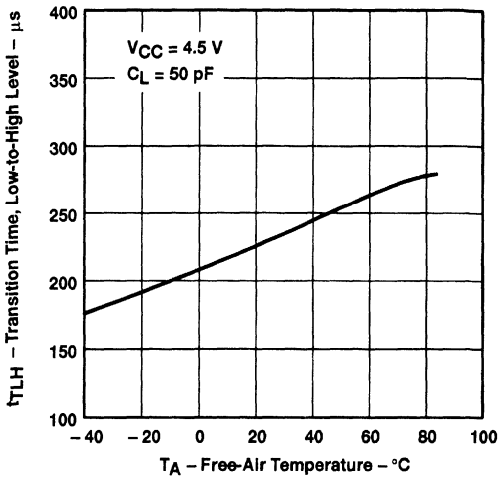


Figure 22

TRANSITION TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE†

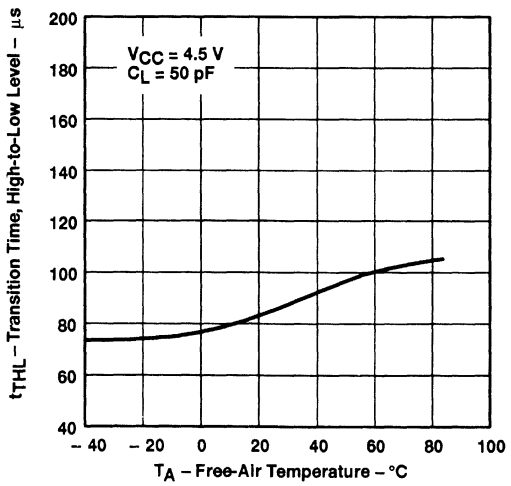


Figure 23

† Only the 0°C to 70°C portion of the curves applies to the SN75'.

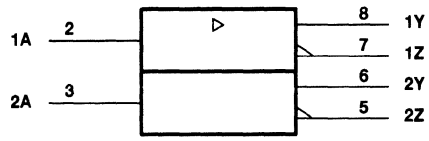
- **Meets or Exceeds the Requirements of ANSI Standard EIA/TIA-422-B and ITU Recommendation V.11**
- **Designed to Operate at 20 Mbaud or Higher**
- **TTL-and CMOS-Input Compatibility**
- **Single 5-V Supply Operation**
- **Output Short-Circuit Protection**
- **Improved Replacement for the μA9638**

description

The SN75ALS191 is a dual, high-speed, differential line driver designed to meet ANSI Standard EIA/TIA-422-B and ITU Recommendation V.11. The inputs are TTL- and CMOS-compatible and have input clamp diodes. Schottky-diode-clamped transistors minimizes propagation delay time. This device operates from a single 5-V power supply and is supplied in 8-pin packages.

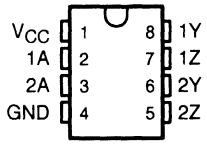
The SN75ALS191 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

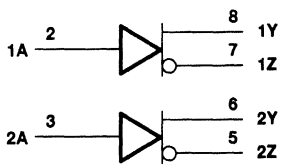
D OR P PACKAGE
(TOP VIEW)



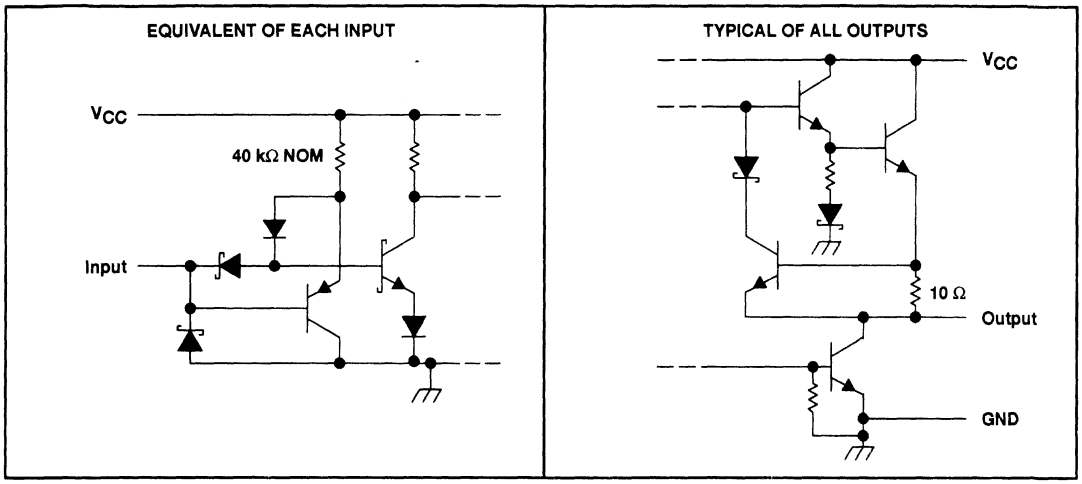
FUNCTION TABLE
(each driver)

INPUT	OUTPUTS	
A	Y	Z
H	H	L
L	L	H

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 7 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values except differential output voltage (V_{OD}) are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−50	mA
Low-level output current, I_{OL}			50	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V,	I_I = −18 mA			−1	−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, V_{IL} = 0.8 V	V_{IH} = 2 V,	I_{OH} = −10 mA	2.5	3.3		V
				I_{OH} = −40 mA	2			
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, I_{OL} = 40 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,			0.5	V
$\lvert V_{OD1}\rvert$	Differential output voltage	V_{CC} = 5.25 V,	I_O = 0				2 V_{OD2}	V
$\lvert V_{OD2}\rvert$	Differential output voltage	V_{CC} = 4.75 V to 5.25 V, See Figure 1		R_L = 100 Ω,	2			V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage‡						±0.4	V
V_{OC}	Common-mode output voltage§						3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage‡						±0.4	V
I_O	Output current with power off	V_{CC} = 0		V_O = 6 V		0.1	100	µA
				V_O = −0.25 V		−0.1	−100	
				V_O = −0.25 V to 6 V			±100	
I_I	Input current	V_{CC} = 5.25 V,	V_I = 5.5 V				50	µA
I_{IH}	High-level input current	V_{CC} = 5.25 V,	V_I = 2.7 V				25	µA
I_{IL}	Low-level input current	V_{CC} = 5.25 V,	V_I = 0.5 V				200	µA
I_{OS}	Short-circuit output current¶	V_{CC} = 5.25 V,	V_O = 0		−50		−150	mA
I_{CC}	Supply current (all drivers)	V_{CC} = 5.25 V,	No load,	All inputs at 0 V		32	40	mA

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ $\lvert V_{OD}\rvert$ and $\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
§ In ANSI Standard EIA/TIA-422-B, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
¶ Only one output at a time should be shorted, and duration of the short circuit should not exceed one second.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS	MIN	TYP#	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	C_L = 15 pF, R_L = 100 Ω, See Figure 2		3.5	7	ns
$t_{t(OD)}$	Differential-output transition time			3.5	7	ns
	Skew			1.5	4	ns

Typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

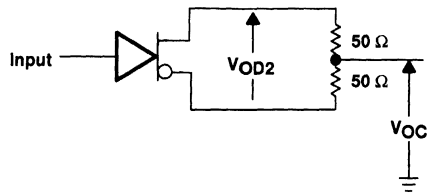
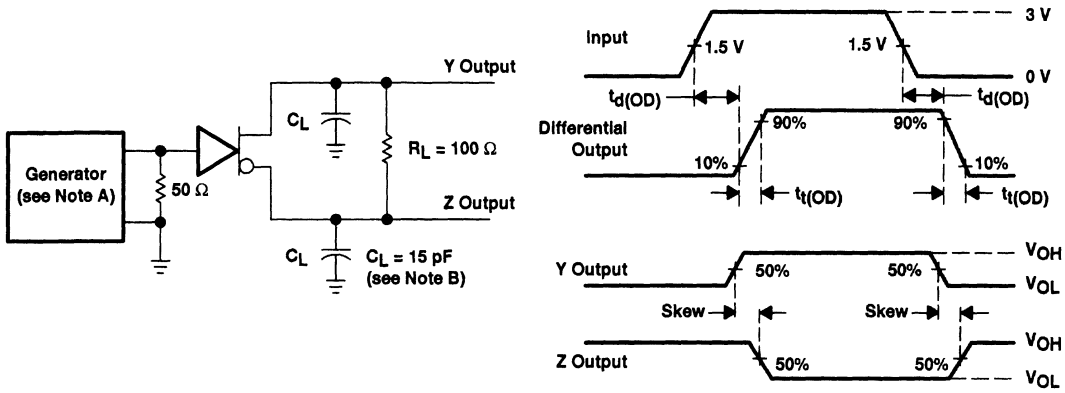


Figure 1. Differential and Common-Mode Output Voltages



TEST CIRCUIT **VOLTAGE WAVEFORMS**

NOTES: A. The input pulse generator has the following characteristics: Z_O = 50 Ω, PRR ≤ 500 kHz, t_w = 100 ns, t_r = ≤ 5 ns.
B. C_L includes probe and jig capacitance.

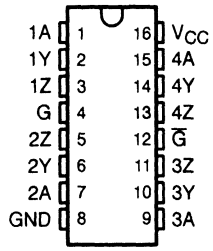
Figure 2. Test Circuit and Voltage Waveforms

SN55ALS192, SN75ALS192
QUADRUPLE DIFFERENTIAL LINE DRIVERS

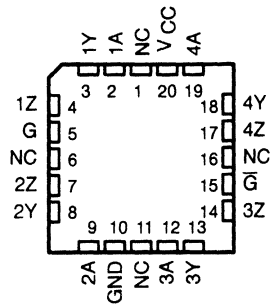
SLLS007C – JULY 1985 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of ANSI Standard EIA/TIA-422-B and ITU Recommendation V.11**
- **Designed to Operate Up to 20 Mbaud**
- **3-State TTL Compatible**
- **Single 5-V Supply Operation**
- **High Output Impedance in Power-Off Condition**
- **Complementary Output Enable Inputs**
- **Improved Replacement for the AM26LS31**

SN55ALS192 . . . J OR W PACKAGE
SN75ALS192 . . . D OR N PACKAGE
(TOP VIEW)



SN55ALS192 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These four differential line drivers are designed for data transmission over twisted-pair or parallel-wire transmission lines. They meet the requirements of ANSI Standard EIA/TIA-422-B and ITU Recommendations V.11 and are compatible with 3-state TTL circuits. Advanced low-power Schottky technology provides high speed without the usual power penalties. Standby supply current is typically only 26 mA, while typical propagation delay time is less than 10 ns.

High-impedance inputs maintain low input currents, less than 1 μA for a high level and less than 100 μA for a low level. Complementary enable inputs, G and $\overline{G}$, allow these devices to be enabled at either a high input level or low input level. The SN75ALS192 is capable of data rates in excess of 20 megabits per second and is designed to operate with the SN75ALS193 quadruple line receiver. The SN55ALS192 is also capable of data rates in excess of 20 megabits per second and designed to operate with the SN55ALS193; however, it may be limited to a lower bit rate based on the temperature (refer to the dissipation rating table and Figure 15).

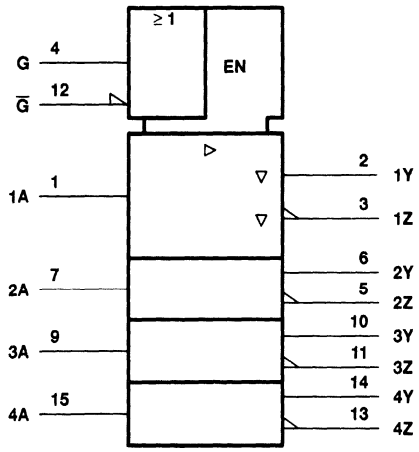
The SN55ALS192 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN75ALS192 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each driver)

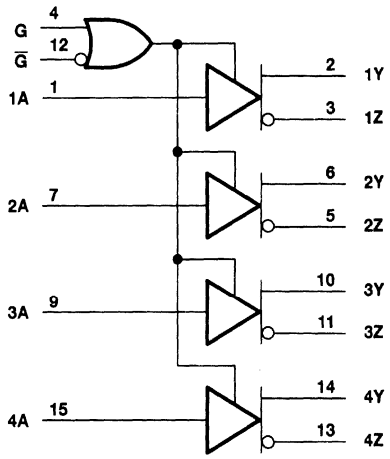
INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	$\overline{Z}$
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H = high level, L = low level,
Z = high impedance (off), X = irrelevant

logic symbol†

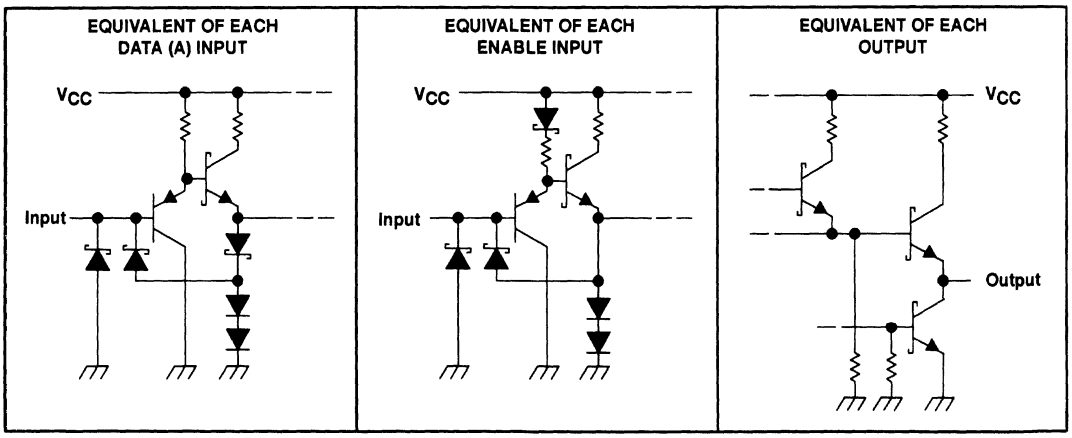


logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

schematics of inputs and outputs



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 7 V
Off-state output voltage ..... 6 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN55ALS192 ..... – 55°C to 125°C
SN75ALS192 ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... – 65°C to 150°C
Case temperature for 60 seconds, T_C: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or W package ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values except differential output voltage, V_{OD}, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J†	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	N/A
W	1000 mW	8.0 mW/°C	640 mW	200 mW

† In the J package, the SN55ALS192 chips are either alloy or silver glass mounted.

recommended operating conditions

	SN55ALS192			SN75ALS192			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
High-level output current, I_{OH}			– 20			– 20	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	– 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN55ALS192			SN75ALS192			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = –18 mA			–1.5			–1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN,	I_{OH} = – 20 mA	2.4			2.5			V
V_{OL}	Low-level output voltage	V_{CC} = MIN,	I_{OL} = 20 mA			0.5			0.5	V
V_O	Output voltage	V_{CC} = MAX,	I_O = 0	0		6	0		6	V
$\lvert V_{OD1}\rvert$	Differential output voltage	V_{CC} = MIN,	I_O = 0	1.5		6	1.5		6	V
$\lvert V_{OD2}\rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 1	1/2 V_{OD1} or 2§			1/2 V_{OD1} or 2§			V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage¶	R_L = 100 Ω,	See Figure 1			±0.2			±0.2	V
V_{OC}	Common-mode output voltage#	R_L = 100 Ω,	See Figure 1			±3			±3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage¶	R_L = 100 Ω,	See Figure 1			±0.2			±0.2	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V			100			100	µA
			V_O = – 0.25 V			–100			–100	
I_{OZ}	Off-state (high-impedance state) output current	V_{CC} = MAX	V_O = 0.5 V			–20			–20	µA
			V_O = 2.5 V			20			20	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V			100			100	µA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			20			20	µA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			– 200			– 200	µA
I_{OS}	Short-circuit output current‖	V_{CC} = MAX		– 30		–150	– 30		– 150	mA
I_{CC}	Supply current (all drivers)	V_{CC} = MAX, All outputs disabled			26	45		26	45	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.
§ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
¶ $\lvert V_{OD}\rvert$ and $\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
# In ANSI Standard EIA/TIA-422-B, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
‖ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	S1 and S2 open,	C_L = 30 pF		6	13	ns
t_{PHL}	Propagation delay time, high-to-low-level output	S1 and S2 open,	C_L = 30 pF		9	14	ns
	Output-to-output skew	S1 and S2 open,	C_L = 30 pF		3	6	ns
t_{PZH}	Output enable time to high level	S1 open and S2 closed			11	15	ns
t_{PZL}	Output enable time to low level	S1 closed and S2 open			16	20	ns
t_{PHZ}	Output disable time from high level	S1 open and S2 closed,	C_L = 10 pF		8	15	ns
t_{PLZ}	Output disable time from low level	S1 and S2 closed,	C_L = 10 pF		18	20	ns

PARAMETER MEASUREMENT INFORMATION

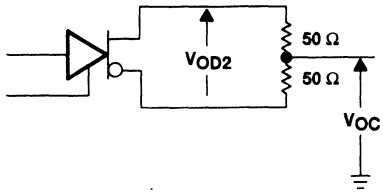
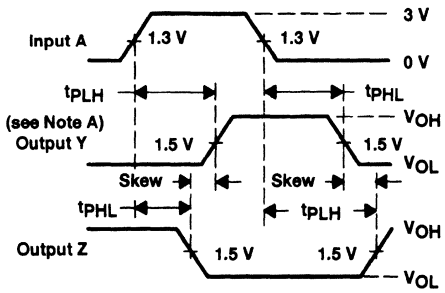
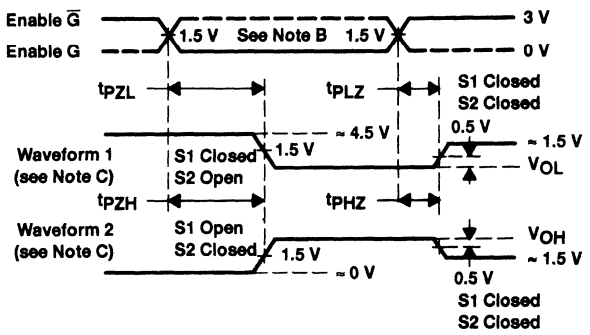


Figure 1. Differential and Common-Mode Output Voltages

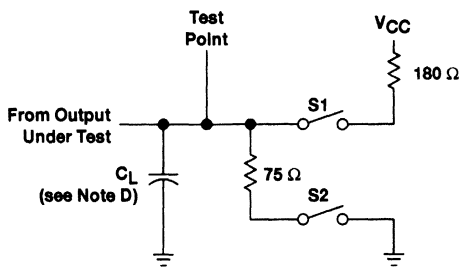


PROPAGATION DELAY TIMES AND SKEW



ENABLE AND DISABLE TIMES

VOLTAGE WAVEFORMS



TEST CIRCUIT

NOTES: A. When measuring propagation delay times and skew, switches S1 and S2 are open.
B. Each enable is tested separately.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. C_L includes probe and jig capacitance.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\ \Omega$, $t_r \leq 15$ ns, and $t_f \leq 6$ ns.

Figure 2. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

Y OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

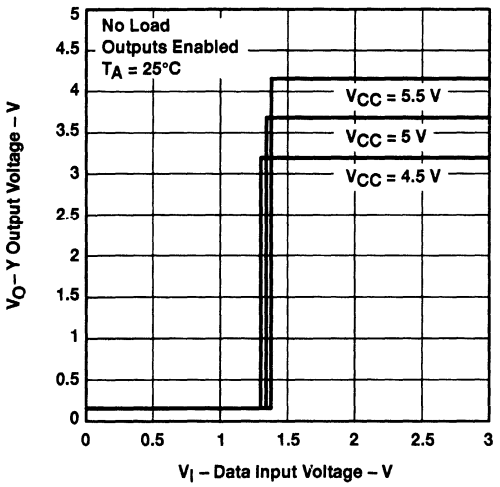


Figure 3

Y OUTPUT VOLTAGE
vs
DATA INPUT VOLTAGE

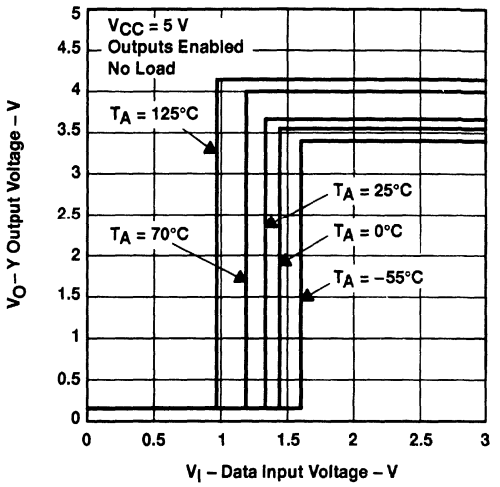


Figure 4

Y OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

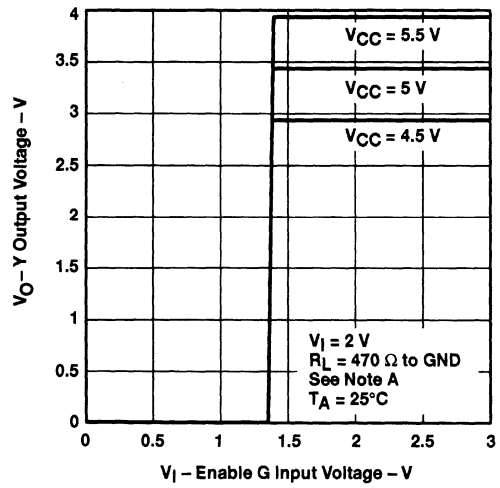


Figure 5

Y OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

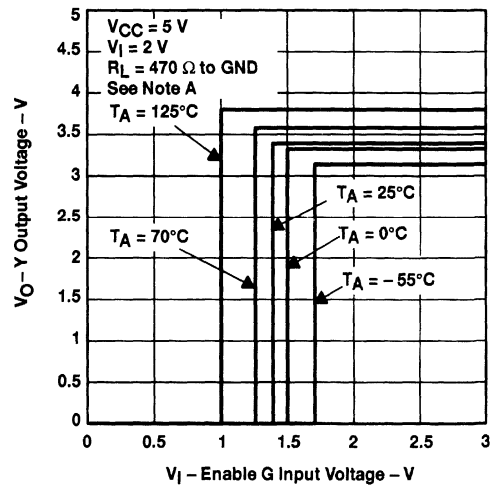


Figure 6

NOTE A: The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.

† Data for temperatures below 0°C and above 70°C and below 4.75 V and above 5.25 V are applicable to SN55ALS192 circuits only.

TYPICAL CHARACTERISTICS†

Z OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

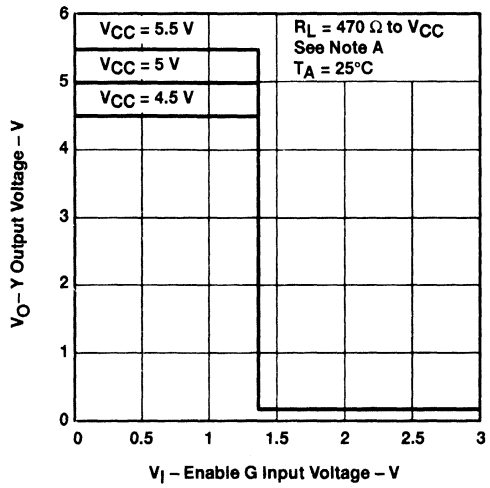


Figure 7

Z OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

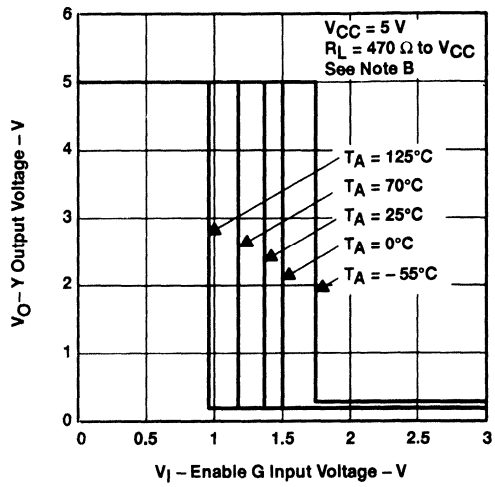


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

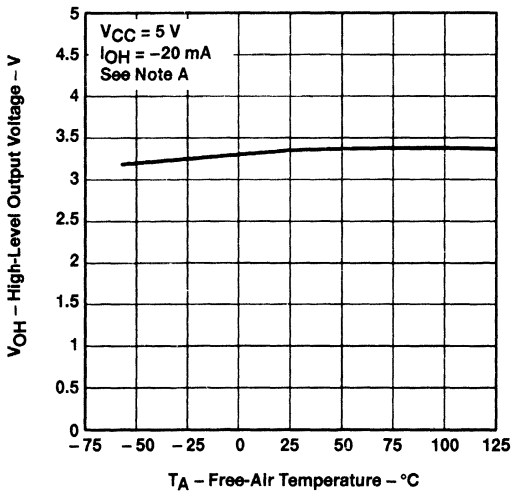


Figure 9

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

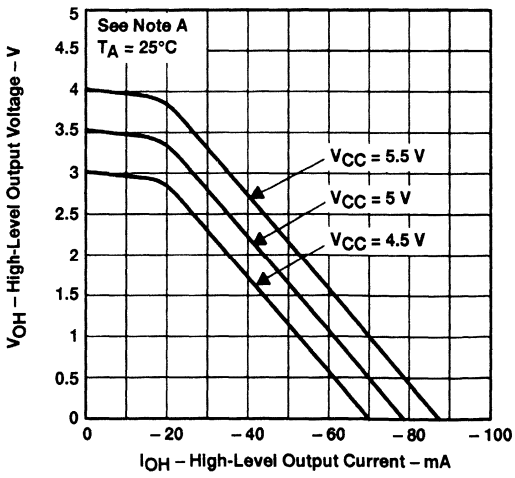


Figure 10

† Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS192 circuits only.

NOTES: A. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.
B. The A input is connected to GND during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

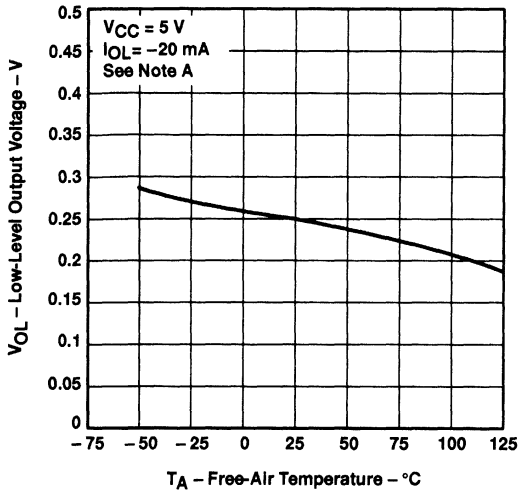


Figure 11

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

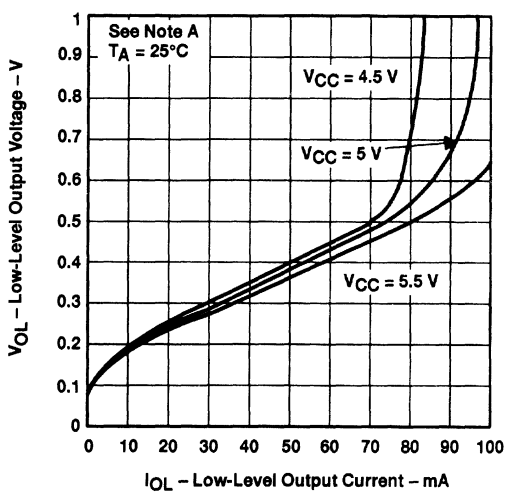


Figure 12

NOTE A: The A input is connected to GND during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

SUPPLY CURRENT vs SUPPLY VOLTAGE

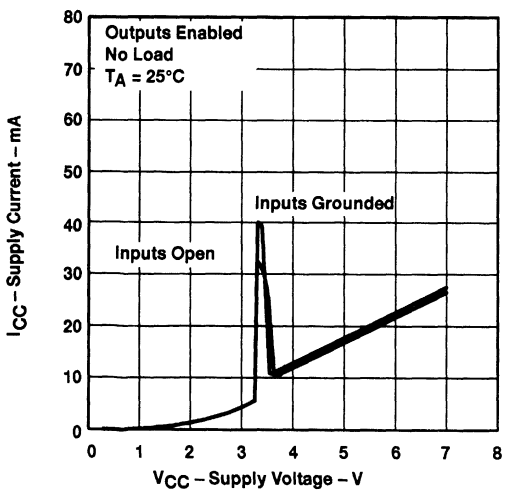


Figure 13

SUPPLY CURRENT vs SUPPLY VOLTAGE

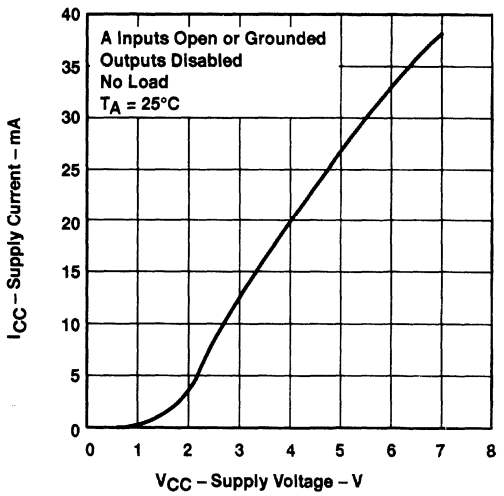


Figure 14

† Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS192 circuits only.

TYPICAL CHARACTERISTICS

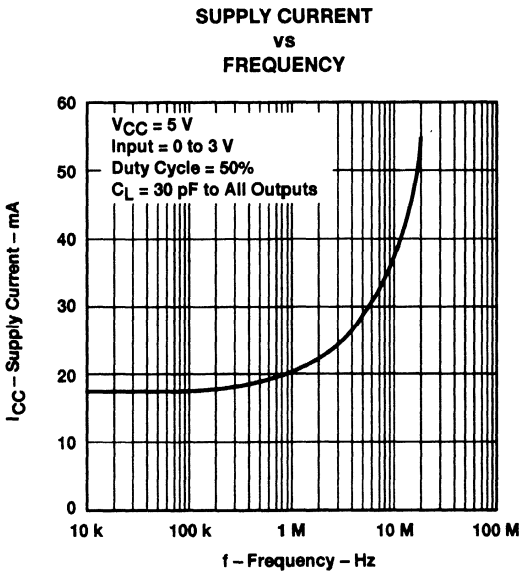
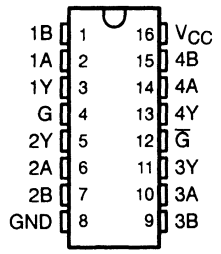


Figure 15

SLLS008D – JUNE 1986 – REVISED MAY 1995

- **Meets or Exceeds ANSI Standard EIA/TIA-422-B and EIA/TIA-423-A and ITU Recommendations V.10 and V.11**
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments**
- **3-State Outputs**
- **Common-Mode Input Voltage Range −7 V to 7 V**
- **Input Sensitivity . . . ±200 mV**
- **Input Hysteresis . . . 120 mV Typ**
- **High Input Impedance . . . 12 kΩ Min**
- **Operates from Single 5-V Supply**
- **Low Supply Current Requirement 35 mA Max**
- **Improved Speed and Power Version of the AM26LS32A**

SN75ALS193 . . . D, J OR N PACKAGE
(TOP VIEW)



description

The SN75ALS193 is a monolithic quadruple line receiver with 3-state outputs designed using advanced low-power Schottky technology. This technology provides combined improvements in bar design, tooling production, and wafer fabrication. This, in turn, provides significantly less power requirements and permits much higher data throughput than other designs. These devices meet the specifications of ANSI Standards EIA/TIA-422-B and EIA/TIA-423-A and ITU Recommendations V.10 and V.11. It features 3-state outputs that permit direct connection to a bus-organized system with a fail-safe design that ensures the outputs will always be high if the inputs are open.

The device is optimized for balanced multipoint bus transmission at rates up to 20 megabits per second. The input features high input impedance, input hysteresis for increased noise immunity, and an input sensitivity of ± 200 mV over a common-mode input voltage range of −7 to 7 V. It also features active-high and active-low enable functions that are common to the four channels. The SN75ALS193 is designed for optimum performance when used with the 'ALS192 quadruple differential line driver.

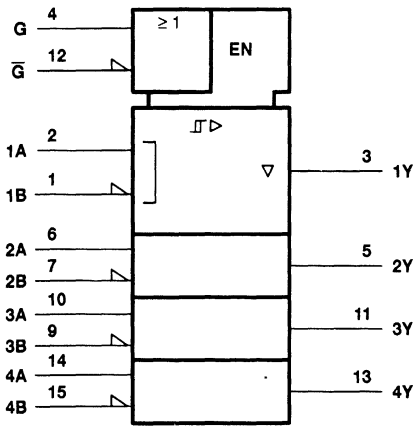
The SN75ALS193 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS	ENABLES		OUTPUT
A – B	G	$\overline{G}$	Y
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
$-0.2\text{ V} < V_{ID} < 0.2$ V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
X	L	H	Z
Open	H	X	H
	X	L	H

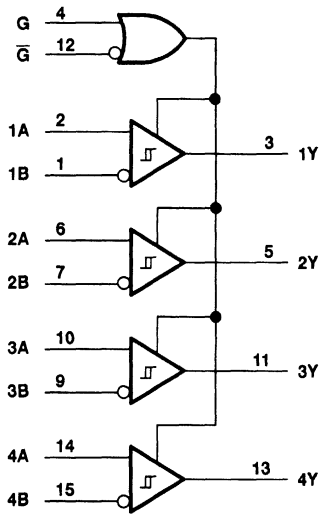
H = high level, L = low level, X = irrelevant, ? = indeterminate
Z = high impedance (off)

logic symbol†

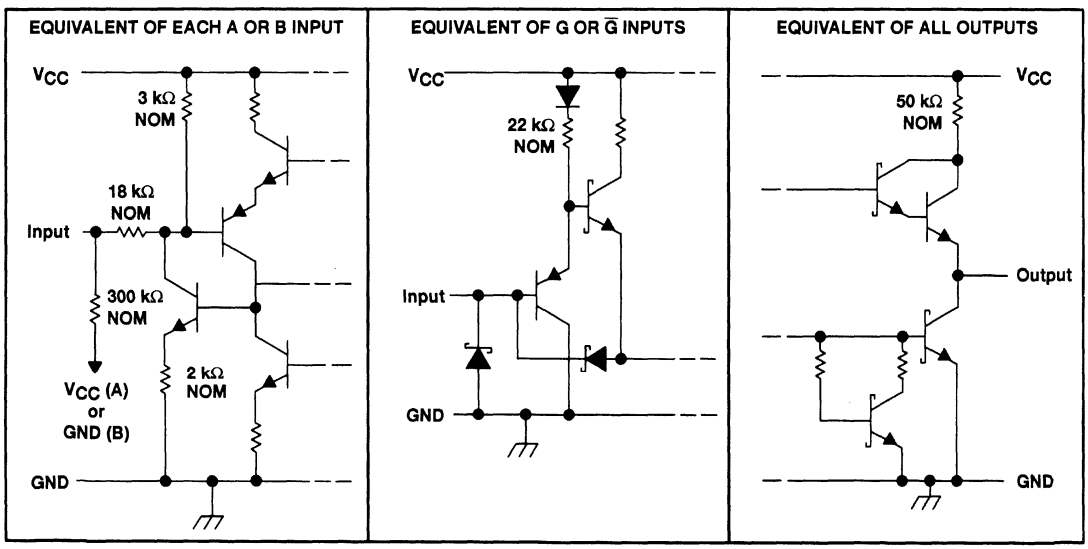


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I (A or B) ..... ±15 V
Differential input voltage, V_{ID} (see Note 2) ..... ±15 V
Enable input voltage, V_I ..... 7 V
Low-level output current, I_{OL} ..... 50 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds ..... 300°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditons is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
J	1025 mW	8.2 mW/°C	656 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Differential input voltage, V_{ID}			±12	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−400	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended range of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage					200	mV
V_{IT-}	Negative-going input threshold voltage			−200§			mV
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)				120		mV
V_{IK}	Enable-input clamp voltage	V_{CC} = MIN,	I_I = − 18 mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = −400 μA,	V_{ID} = 200 mV, See Figure 1	2.5	3.6		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{ID} = −200 mV, See Figure 1	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	V_{CC} = MAX	V_O = 2.4 V			20	μA
			V_O = 0.4 V			−20	
I_I	Line input current	Other input at 0, See Note 3	V_{CC} = MIN, V_I = 15 V		0.7	1.2	mA
			V_{CC} = MIN, V_I = −15 V		−1.0	−1.7	
I_{IH}	High-level enable-input current	V_{CC} = MAX	V_{IH} = 2.7 V			20	μA
			V_{IH} = MAX			100	
I_{IL}	Low-level enable-input current	V_{CC} = MAX,	V_{IL} = 0.4 V			−100	μA
	Input resistance			12	18		kΩ
I_{OS}	Short-circuit output current	V_{CC} = MAX, V_O = 0,	V_{ID} = 3 V, See Note 4	−15	−78	−130	mA
I_{CC}	Supply current	V_{CC} = MAX,	Outputs disabled		22	35	mA

† For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.
NOTES: 3. Refer to ANSI Standard EIA/TIA-422-B and EIA/TIA-423-A for exact conditions.
4. Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −2.5 V to 2.5 V, C_L = 15 pF, See Figure 2		15	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output			15	22	
t_{PZH}	Output enable time to high level	C_L = 15 pF, See Figure 3		13	25	
t_{PZL}	Output enable time to low level			11	25	
t_{PHZ}	Output disable time from high level	C_L = 5 pF, See Figure 3		13	25	
t_{PLZ}	Output disable time from low level			15	22	

PARAMETER MEASUREMENT INFORMATION

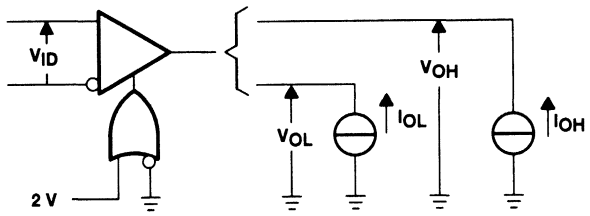
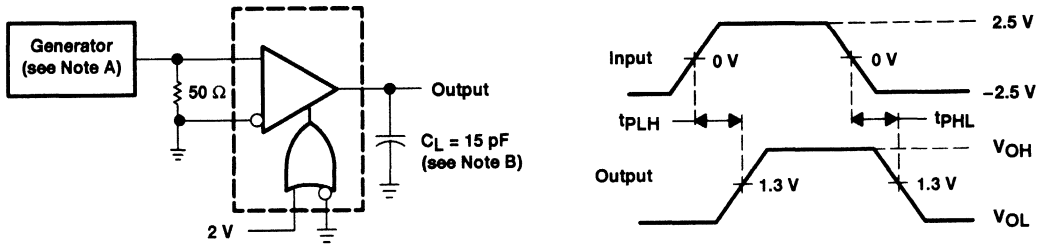


Figure 1. V_{OH}, V_{OL}

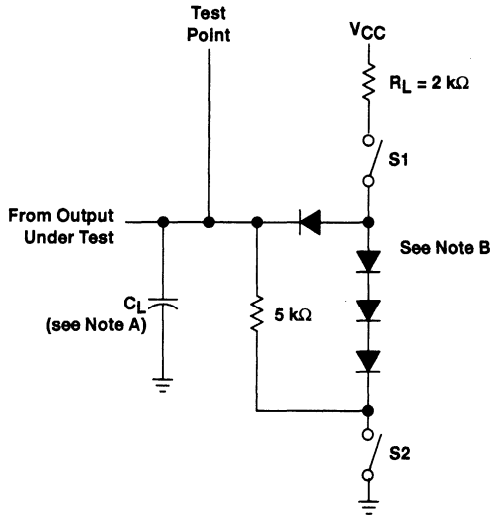


TEST CIRCUIT **VOLTAGE WAVEFORMS**

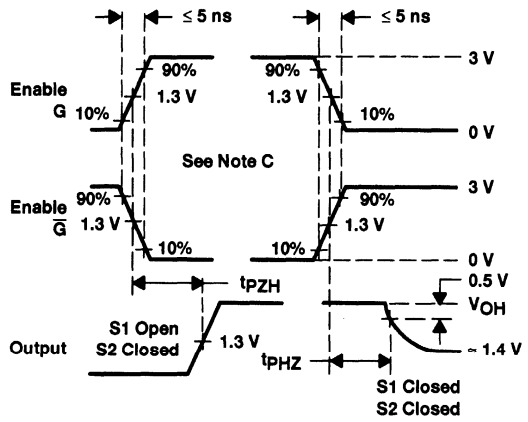
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms

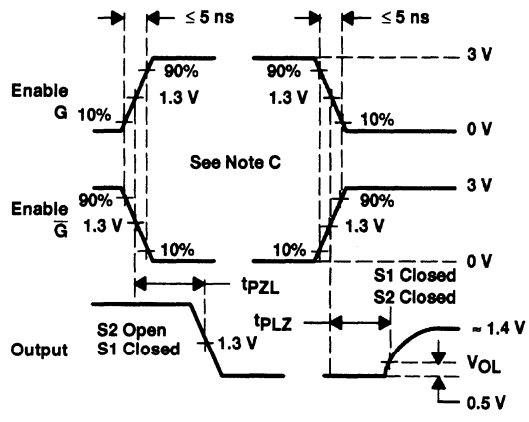
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS FOR t_{PHZ}, t_{PZH}



VOLTAGE WAVEFORMS FOR t_{PLZ}, t_{PZL}

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Enable G is tested with $\overline{G}$ high; $\overline{G}$ is tested with G low.

Figure 3. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

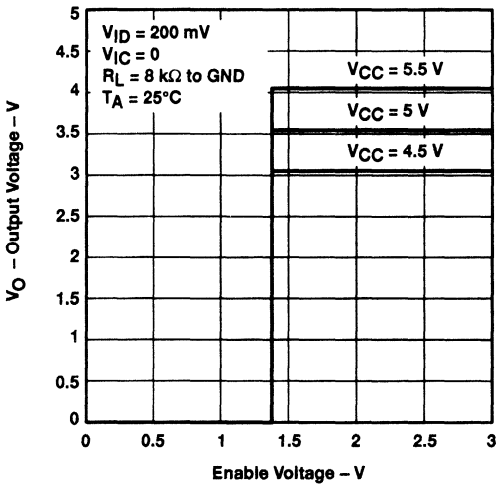


Figure 4

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

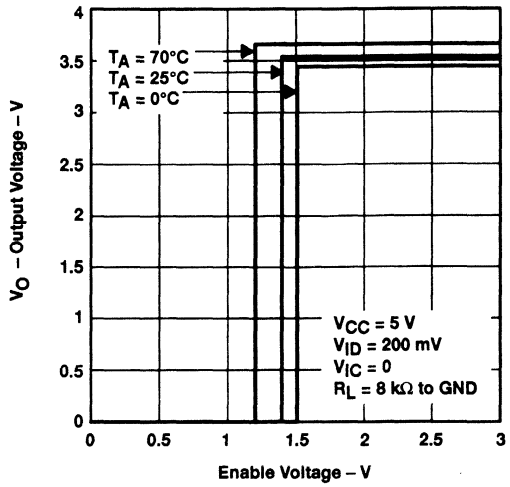


Figure 5

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

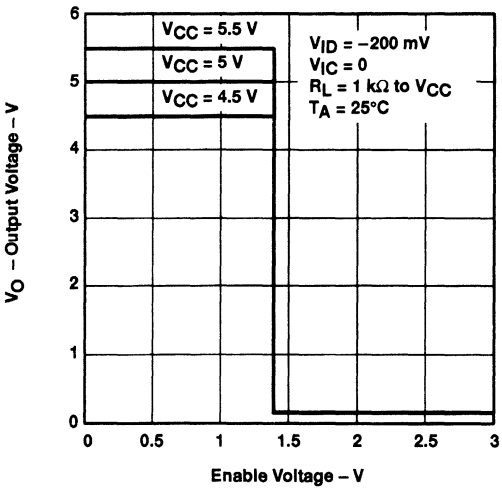


Figure 6

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

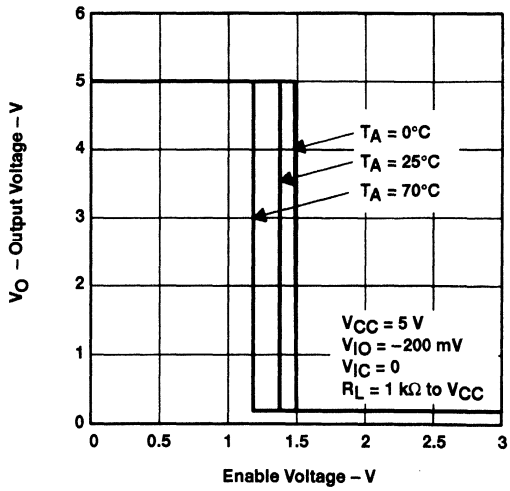


Figure 7

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

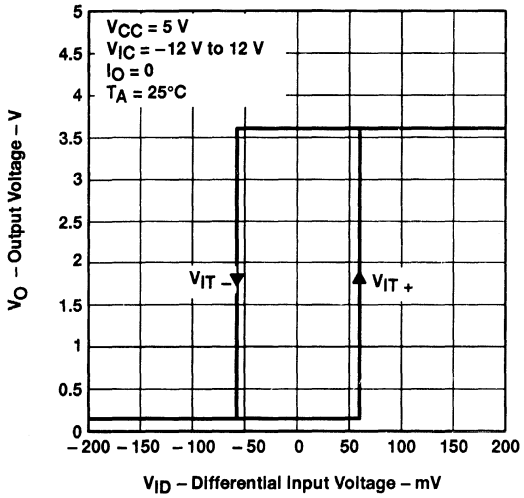


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

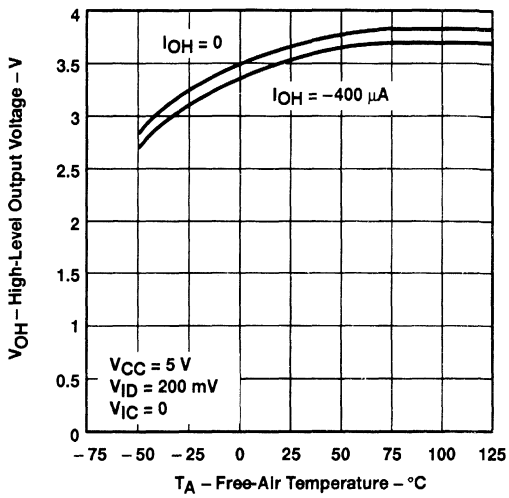


Figure 9

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

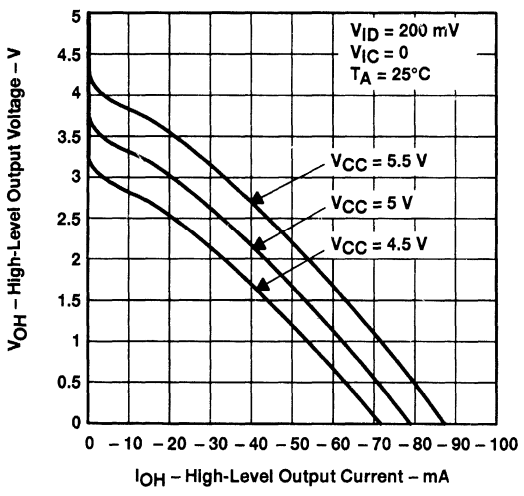


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

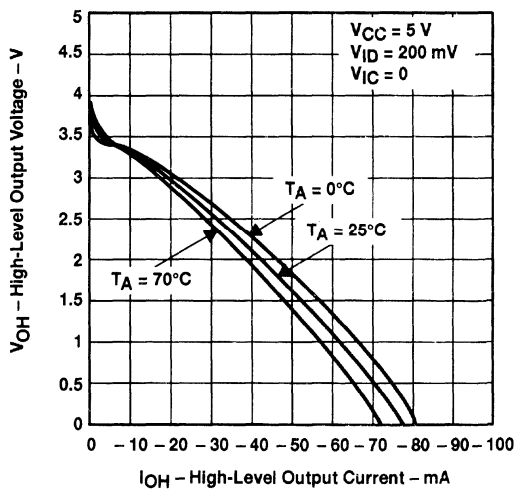


Figure 11

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

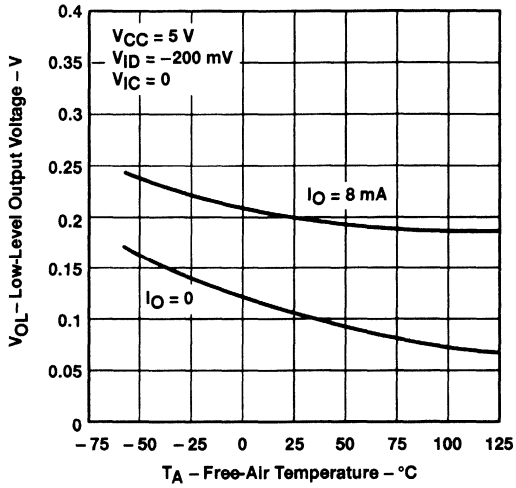


Figure 12

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

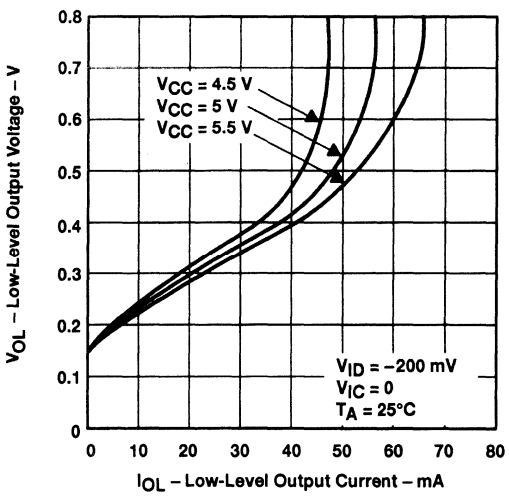


Figure 13

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

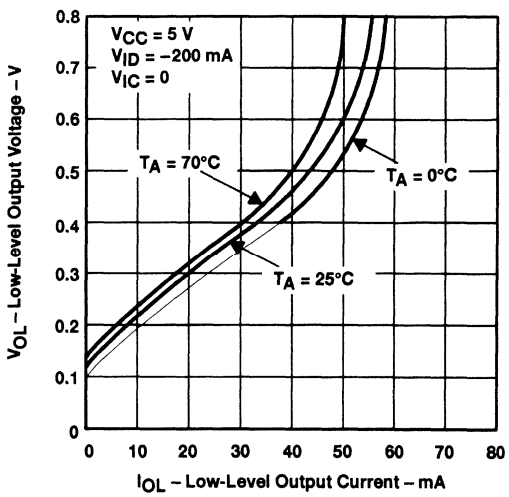


Figure 14

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

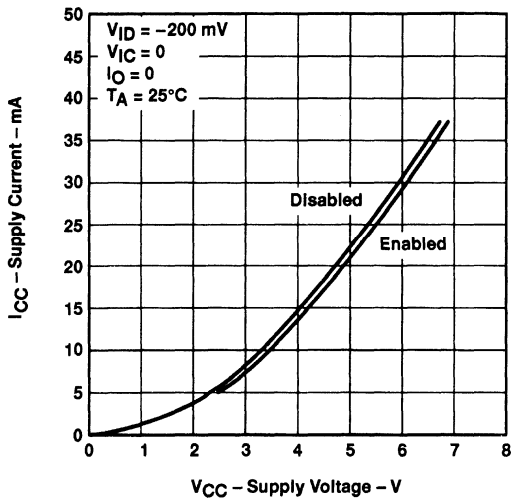


Figure 15

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

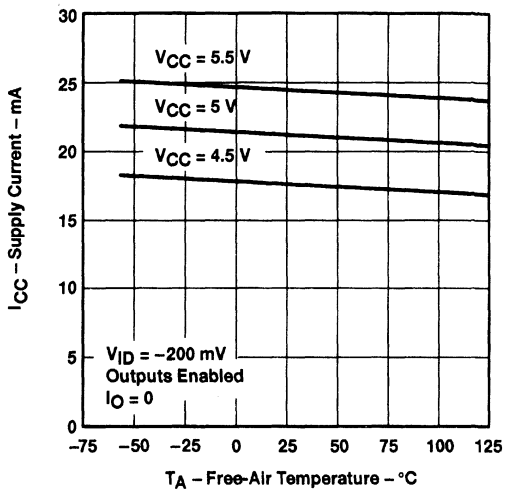


Figure 16

SUPPLY CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

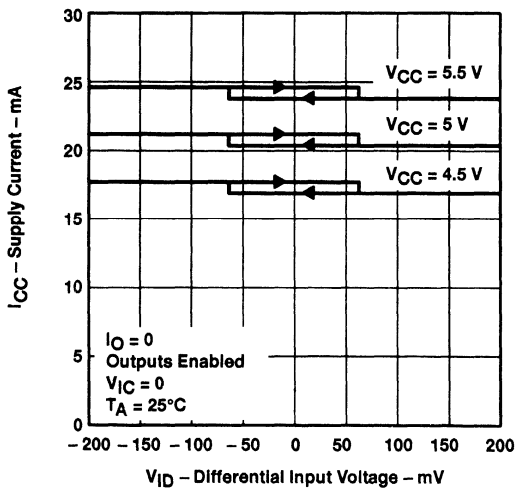


Figure 17

SUPPLY CURRENT
vs
FREQUENCY

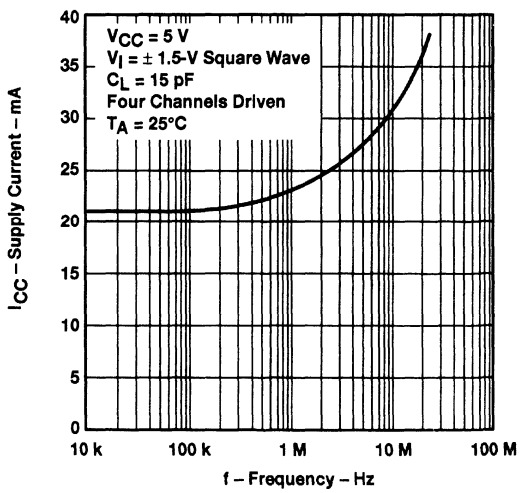


Figure 18

TYPICAL CHARACTERISTICS

INPUT RESISTANCE vs FREE-AIR TEMPERATURE

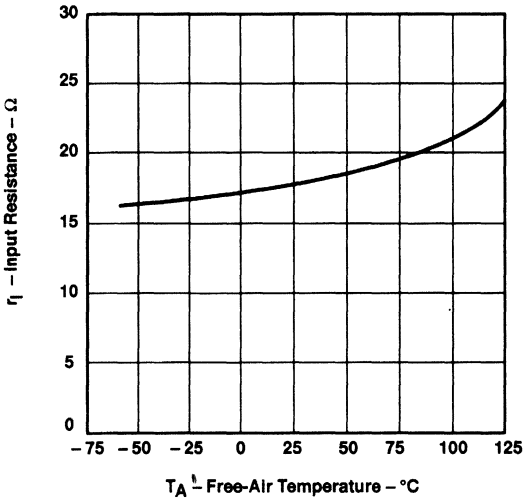


Figure 19

INPUT CURRENT vs INPUT VOLTAGE TO GND

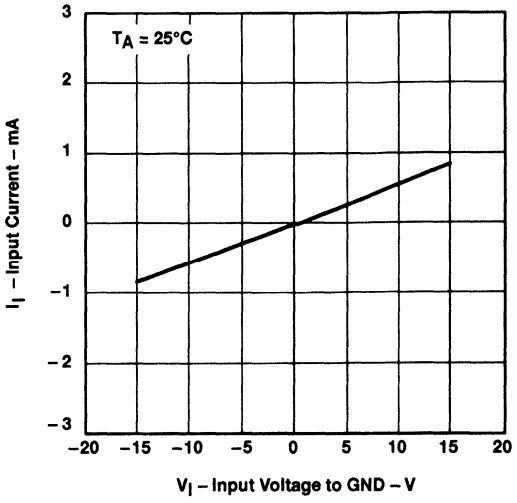


Figure 20

SWITCHING TIME vs FREE-AIR TEMPERATURE

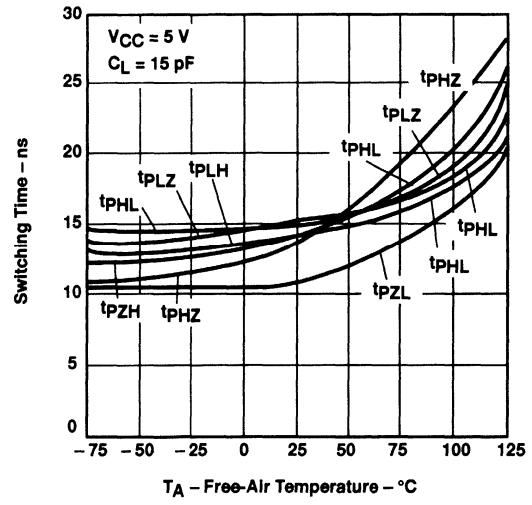


Figure 21

PROPAGATION DELAY TIME vs SUPPLY VOLTAGE

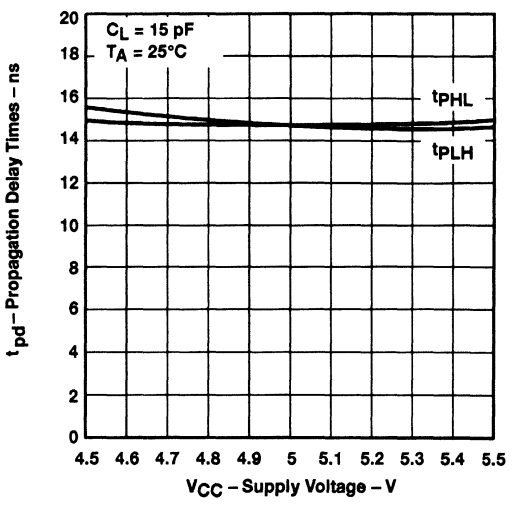


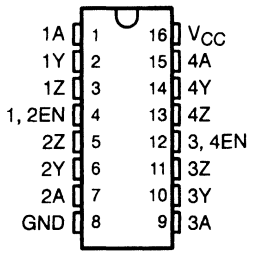
Figure 22

SN55ALS194, SN75ALS194
QUADRUPLE DIFFERENTIAL LINE DRIVER

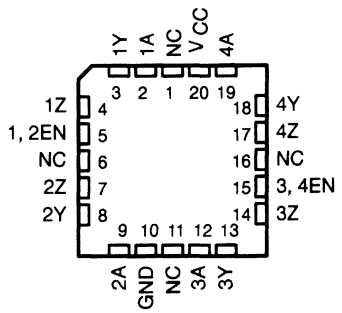
SLLS009D – OCTOBER 1985 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of ANSI Standard EIA/TIA-422-B and ITU Recommendation V.11**
- **Designed to Operate Up to 20 Mbaud**
- **3-State TTL-Compatible Outputs**
- **Single 5-V Supply Operation**
- **High Output Impedance in Power-Off Condition**
- **Two Pairs of Drivers, Independently Enabled**
- **Designed as Improved Replacements for the MC3487**

SN55ALS194 . . . J OR W PACKAGE
SN75ALS194 . . . D OR N PACKAGE
(TOP VIEW)



SN55ALS194 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These four differential line drivers are designed for data transmission over twisted-pair or parallel-wire transmission lines. They meet the requirements of ANSI Standard EIA/TIA-422-B and ITU Recommendation V.11 and are compatible with 3-state TTL circuits. Advanced low-power Schottky technology provides high speed without the usual power penalty. Standby supply current is typically only 26 mA. Typical propagation delay time is less than 10 ns, and enable/disable times are typically less than 16 ns.

High-impedance inputs keep input currents low: less than 1 μA for a high level and less than 100 μA for a low level. The driver circuits can be enabled in pairs by separate active-high enable inputs. The SN55ALS194 and SN75ALS194 are capable of data rates in excess of 20 megabits per second and are designed to operate with the SN55ALS195 and SN75ALS195 quadruple line receivers.

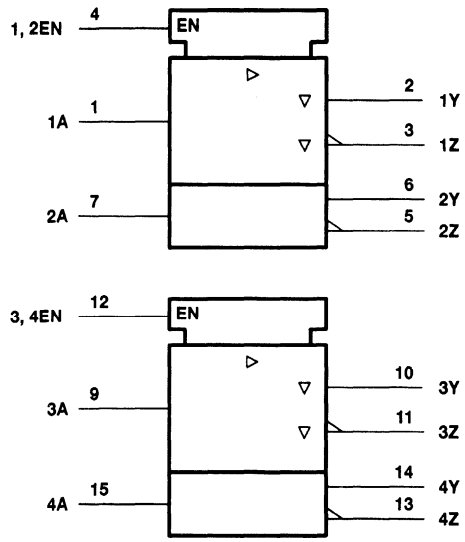
The SN55ALS194 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN75ALS194 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each driver)

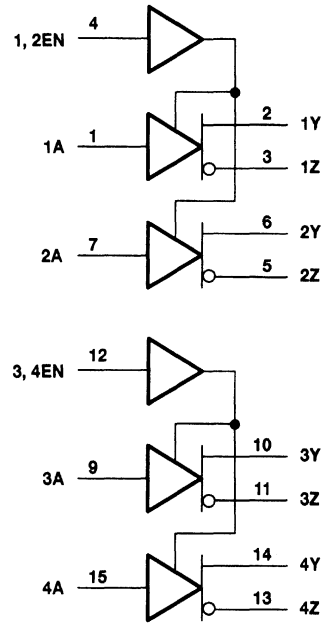
INPUT	OUTPUT	OUTPUTS	
A	EN	Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = high level, L = low level, X = irrelevant, Z = high impedance

logic symbol†

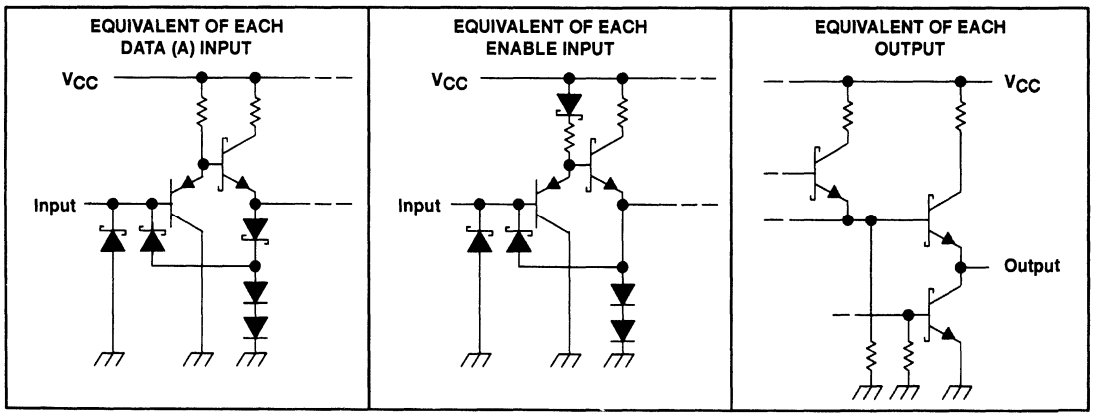


logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

schematics of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 5.5 V
Output voltage, V_O ..... 7 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN55ALS194 ..... – 55°C to 125°C
SN75ALS194 ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... – 65°C to 150°C
Case temperature for 60 seconds, T_C: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or W package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	N/A
W	1000 mW	8.0 mW/°C	640 mW	200 mW

recommended operating conditions‡

		SN55ALS194			SN75ALS194			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	All inputs, T_A = 25°C	2			2			V
	A inputs, T_A = Full range	2			2			
	EN inputs, T_A = Full range	2.1			2			
Low-level input voltage, V_{IL}				0.8			0.8	V
High-level output current, I_{OH}				– 20			– 20	mA
Low-level output current, I_{OL}	T_A = 25°C			48			48	mA
	T_A = Full range			20			48	
Operating free-air temperature, T_A		– 55		125	0		70	°C

‡ Full range is T_A = – 55°C to 125°C for SN55ALS194 and T_A = 0°C to 70°C for SN75ALS194.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = –18 mA			–1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = –20 mA	SN55ALS194	2.4			V
			SN75ALS194	2.5			
V_{OL}	Low-level output voltage	V_{CC} = MIN,	I_{OL} = MAX			0.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω,	See Figure 1	1/2 V_{OD1} or 2§			V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage¶					±0.4	V
V_{OC}	Common-mode output voltage					±3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage¶					±0.4	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V			100	µA
			V_O = –0.25 V			–100	
I_{OZ}	High-impedance-state output current	V_{CC} = MAX, Output enables at 0.8 V	V_O = 2.7 V			100	µA
			V_O = 0.5 V			–100	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			100	µA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			50	µA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V			–200	µA
I_{OS}	Short-circuit output current#	V_{CC} = MAX,	V_I = 2 V	–40		–140	mA
I_{CC}	Supply current (all drivers)	V_{CC} = MAX,	All outputs disabled		26	45	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, TA = 25°C.
§ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
¶ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
# Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN55ALS194			SN75ALS194			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 15 pF, See Figure 2		6	13		6	13	ns
t_{PHL}	Propagation delay time, high- to low-level output			9	14		9	14	ns
	Output-to-output skew			3.5	6		3.5	6	ns
$t_{t(OD)}$	Differential output transition time	C_L = 15 pF, See Figure 3		8	14		8	14	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF, See Figure 4		9	12		9	12	ns
t_{PZL}	Output enable time to low level			12	20		12	20	ns
t_{PHZ}	Output disable time from high level			9	15		9	14	ns
t_{PLZ}	Output disable time from low level			12	15		12	15	ns

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	EIA/TIA-422-B
V_O	V_{oa}, V_{ob}
$\lvert V_{OD1} \rvert$	V_o
$\lvert V_{OD2} \rvert$	V_t (R_L = 100 Ω)
$\Delta \lvert V_{OD} \rvert$	$\lvert \lvert V_t \rvert - \lvert \overline{V}_t \rvert \rvert$
V_{OC}	$\lvert V_{os} \rvert$
$\Delta \lvert V_{OC} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$
I_{OS}	$\lvert I_{sa} \rvert$, $\lvert I_{sb} \rvert$
I_O	$\lvert I_{xa} \rvert$, $\lvert I_{xb} \rvert$

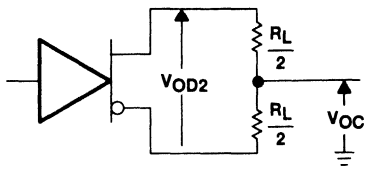


Figure 1. Driver V_{OD} and V_{OC}

PARAMETER MEASUREMENT INFORMATION

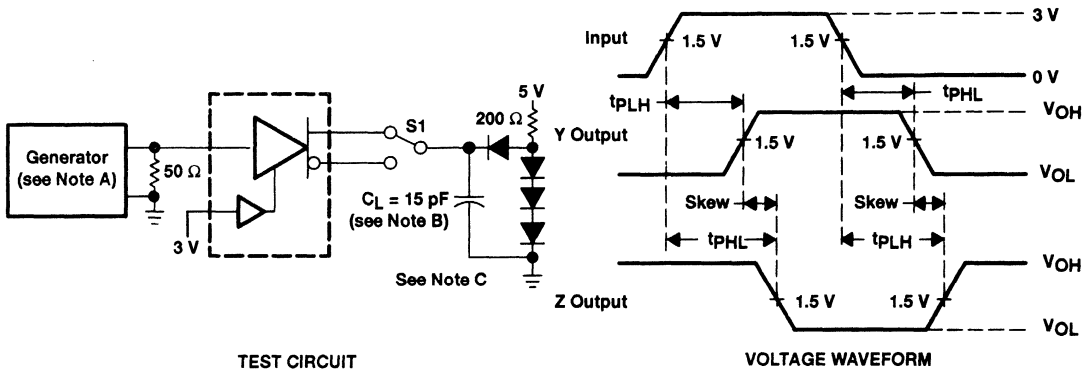


Figure 2. Test Circuit and Voltage Waveform

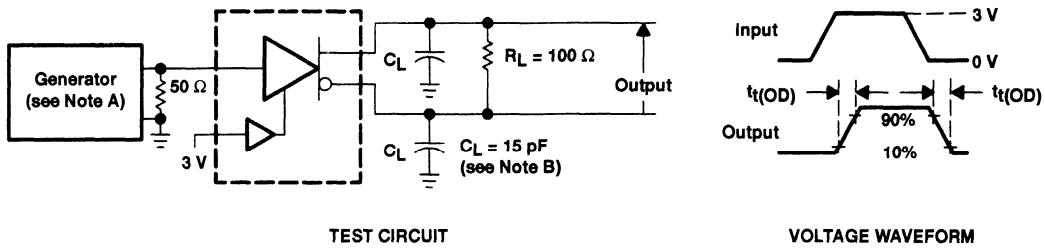
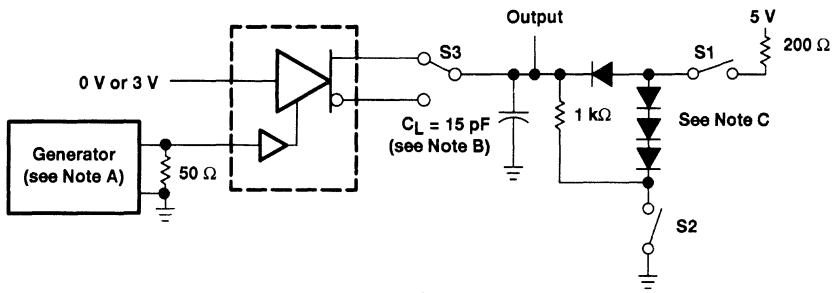


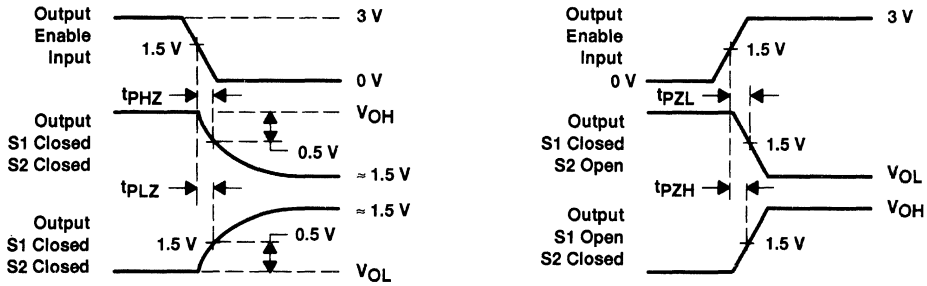
Figure 3. Differential-Output Test Circuit and Voltage Waveform

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \le 5$ ns, $t_f \le 5$ ns, PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_O \approx 50\ \Omega$.
B. C_L includes probe and stray capacitance.
C. All diodes are 1N916 or 1N3064.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_O \approx 50\ \Omega$.
B. C_L includes probe and stray capacitance.
C. All diodes are 1N916 or 1N3064.

Figure 4. Driver Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

Y OUTPUT VOLTAGE vs DATA INPUT VOLTAGE

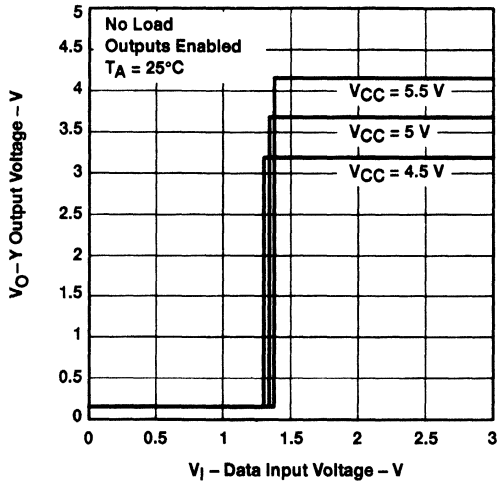


Figure 5

Y OUTPUT VOLTAGE vs DATA INPUT VOLTAGE

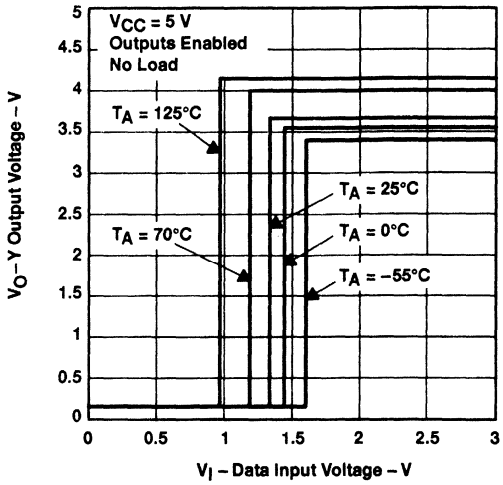


Figure 6

Y OUTPUT VOLTAGE vs ENABLE G INPUT VOLTAGE

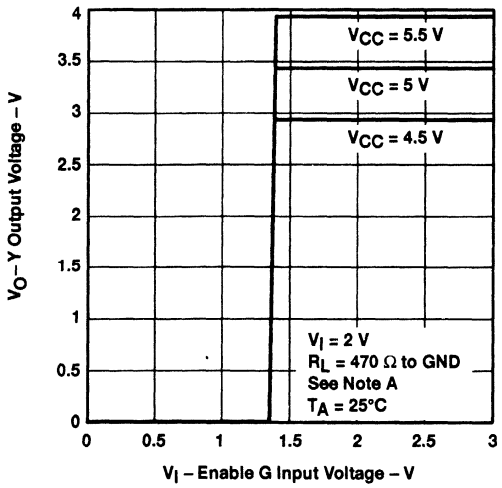


Figure 7

Y OUTPUT VOLTAGE vs ENABLE G INPUT VOLTAGE

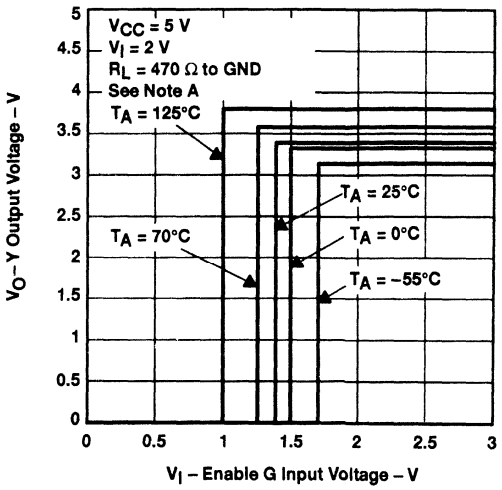


Figure 8

NOTE A: The A input is connected to V_{CC} during the testing of the Y outputs and to GND during the testing of the Z outputs.

† Data for temperatures below 0°C and above 70°C are applicable to the SN55ALS194 circuits only.

TYPICAL CHARACTERISTICS†

Z OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

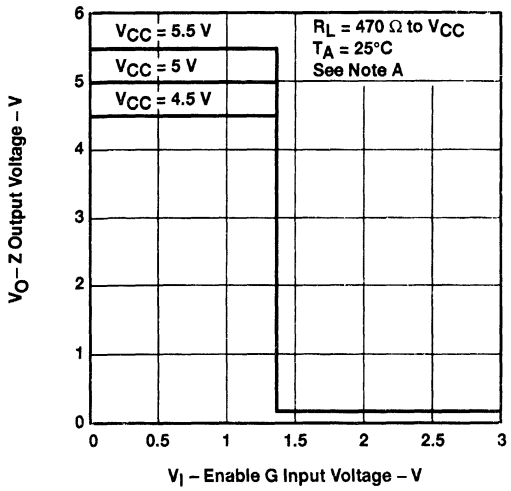


Figure 9

Z OUTPUT VOLTAGE
vs
ENABLE G INPUT VOLTAGE

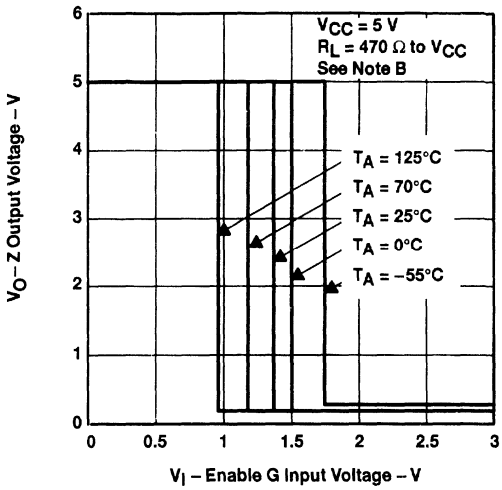


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

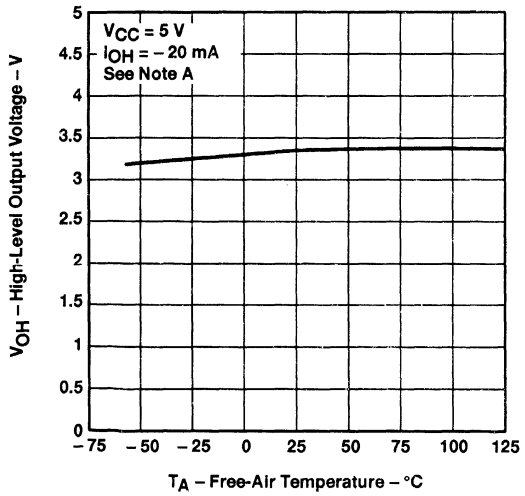


Figure 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

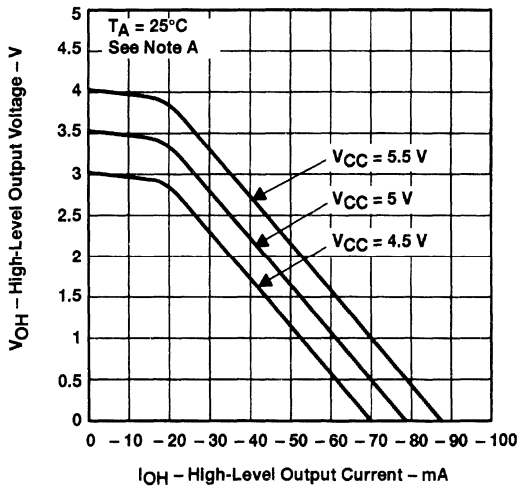


Figure 12

† Data for temperatures below 0°C and above 70°C are applicable to the SN55ALS194 circuits only.

NOTES: A. The A input is connected to V_{CC} during the testing of the Y outputs and to GND during the testing of the Z outputs.
B. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

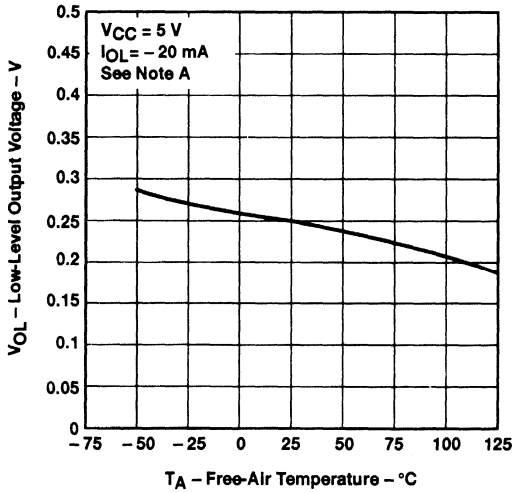


Figure 13

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

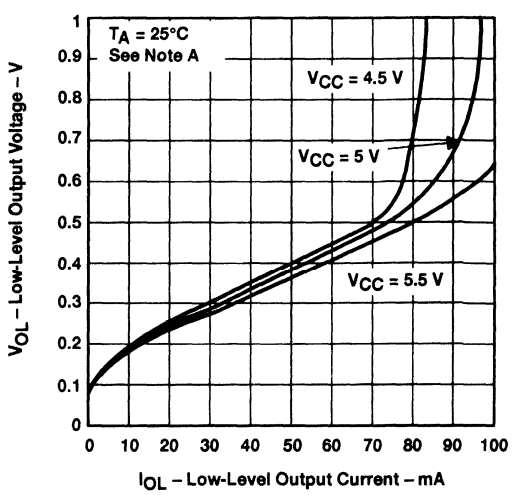


Figure 14

NOTE A: The A input is connected to GND during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

SUPPLY CURRENT vs SUPPLY VOLTAGE

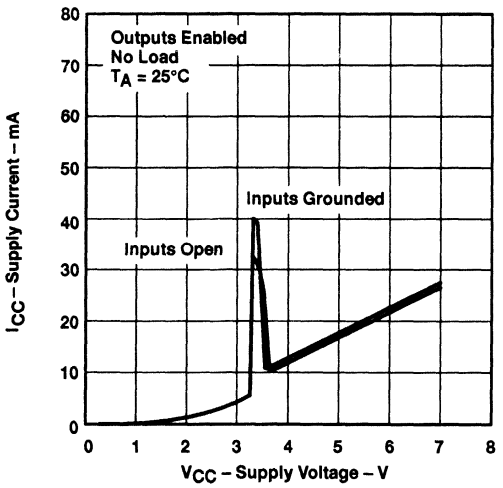


Figure 15

SUPPLY CURRENT vs SUPPLY VOLTAGE

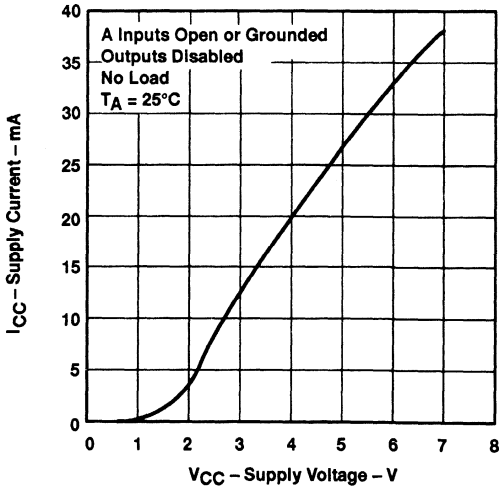


Figure 16

† Data for temperatures below 0°C and above 70°C are applicable to the SN55ALS194 circuits only.

TYPICAL CHARACTERISTICS

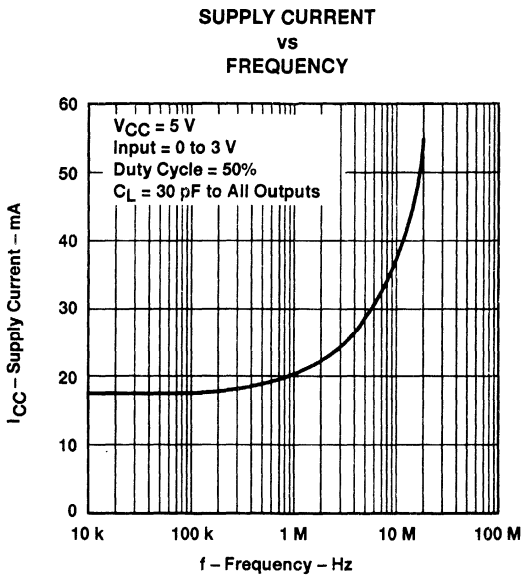


Figure 17

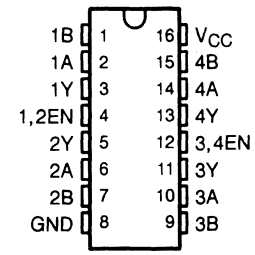
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN55ALS195, SN75ALS195
QUADRUPLE DIFFERENTIAL LINE RECEIVERS

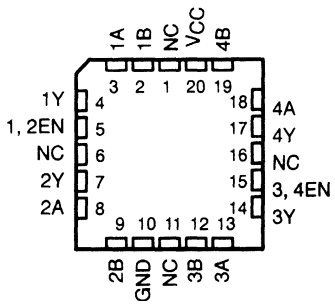
SLLS010D – JUNE 1986 – REVISED MAY 1995

- **Meet or Exceed the Requirements of ANSI Standards EIA/TIA-422-B and EIA/TIA-423-A**
- **Meets ITU Recommendations V.10 and V.11**
- **Designed to Operate Up to 20 Mbaud**
- **–7 V to 7 V Common-Mode Input Voltage Range With 200-mV Sensitivity**
- **3-State TTL-Compatible Outputs**
- **High Input Impedance . . . 12 kΩ Min**
- **Input Hysteresis . . . 120 mV Typ**
- **Single 5-V Supply Operation**
- **Low Supply Current Requirement 35 mA Max**
- **Improved Speed and Power Consumption Compared to MC3486**

SN55ALS195 . . . J OR W PACKAGE
SN75ALS195 . . . J OR N PACKAGE†
(TOP VIEW)



SN55ALS195 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection
† For surface-mount package, see the SN75ALS199.

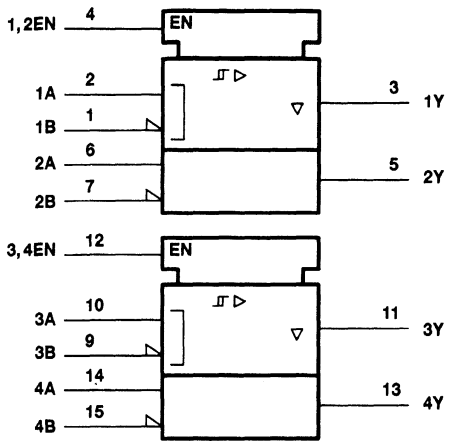
description

The SN55ALS195 and SN75ALS195 are four differential line receivers with 3-state outputs designed using advanced low-power Schottky technology. This technology provides combined improvements in die design, tooling production, and wafer fabrication, which in turn, provide lower power consumption and permit much higher data throughput than other designs. The devices meet the specifications of ANSI Standards EIA/TIA-422-B and EIA/TIA-423-A and ITU Recommendations V.10 and V.11. The 3-state outputs permit direct connection to a bus-organized system with a fail-safe design that ensures the outputs will always be high if the inputs are open.

The devices are optimized for balanced multipoint bus transmission at rates up to 20 megabits per second. The input features high input impedance, input hysteresis for increased noise immunity, and an input sensitivity of ±200 mV over a common-mode input voltage range of ±7 V. The devices also feature an active-high enable function for each of two receiver pairs. The SN55ALS195 and SN75ALS195 are designed for optimum performance when used with the SN55ALS194 and SN75ALS194 quadruple differential line drivers.

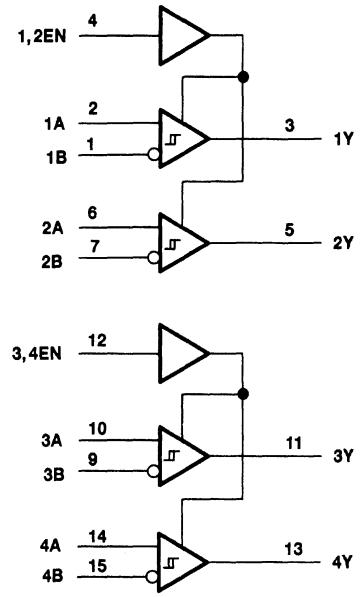
The SN55ALS195 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN75ALS195 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



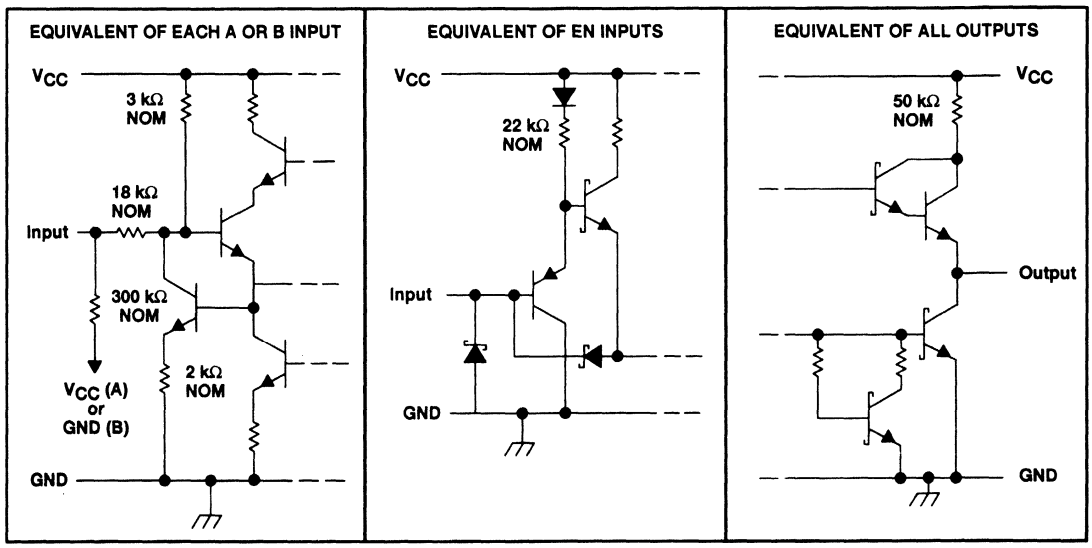
Pin numbers shown are for the J, N, and W packages.

FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A–B	ENABLE EN	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	H
-0.2 V $< V_{ID} <$ 0.2 V	H	?
$V_{ID} \leq -0.2$ V	H	L
X	L	Z
Open	H	H

H = high level, L = low level, X = irrelevant, ? = indeterminate, Z = high impedance (off)

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, A or B inputs, V_I ..... ±15 V
Differential input voltage, V_{ID} (see Note 2) ..... ±15 V
Enable input voltage, V_I ..... 7 V
Low-level output current, I_{OL} ..... 50 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN55ALS195 ..... – 55°C to 125°C
SN75ALS195 ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... – 65°C to 150°C
Case temperature for 60 seconds, T_C: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J, N, or W package ..... 300°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditons is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
FK	1375 mW	11.0mW/°C	880 mW	275 mW
J (SN55ALS195)	1375 mW	11.0mW/°C	880 mW	275 mW
J (SN75ALS195)	1025 mW	8.2mW/°C	656 mW	N/A
N	1150 mW	9.2mW°C	736 mW	N/A
W	1000 mW	8.0mW/°C	640 mW	200 mW

recommended operating conditions

	SN55ALS195			SN75ALS195			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7			±7	V
Differential input voltage, V_{ID}			±12			±12	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage						200	mV
V_{IT-}	Negative-going input threshold voltage				−200§			mV
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)					120		mV
V_{IK}	Enable-input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, See Figure 1	V_{ID} = 200 mV,	I_{OH} = −400 μA,	2.5	3.6		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{ID} = −200 mV, See Figure 1	I_{OL} = 8 mA				0.45	V
			I_{OL} = 16 mA				0.5	
I_{OZ}	High-impedance-state output current	V_{CC} = MAX, V_O = 2.7 V	V_{IL} = 0.8 V,	V_{ID} = −3 V,			20	μA
		V_{CC} = MAX, V_O = 0.5 V	V_{IL} = 0.8 V,	V_{ID} = 3 V,			−20	
I_I	Line input current	Other input at 0 V, See Note 3	V_{CC} = MIN,	V_I = 15 V		0.7	1.2	mA
			V_{CC} = MAX,	V_I = −15 V		−1	−1.7	
I_{IH}	High-level enable-input current	V_{CC} = MAX	V_{IH} = 2.7 V				20	μA
			V_{IH} = 5.25 V				100	
I_{IL}	Low-level enable-input current	V_{CC} = MAX,	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance				12	18		kΩ
I_{OS}	Short-circuit output current	V_{CC} = MAX, See Note 4	V_{ID} = 3 V,	V_O = 0,	−15	−78	−130	mA
I_{CC}	Supply current	V_{CC} = MAX,	Outputs disabled			22	35	mA

† For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.
NOTES: 3. Refer to ANSI Standards EIA/TIA-422-B and EIA/TIA-423-A for exact conditions.
4. Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_{ID} = 0 to 3 V, See Figure 2		15	22	ns
t_{PHL}	Propagation delay time, high- to low-level output			15	22	ns
t_{PZH}	Output enable time to high level	See Figure 3		13	25	ns
t_{PZL}	Output enable time to low level			10	25	
t_{PHZ}	Output disable time from high level	See Figure 3		19	25	ns
t_{PLZ}	Output disable time from low level			17	22	

PARAMETER MEASUREMENT INFORMATION

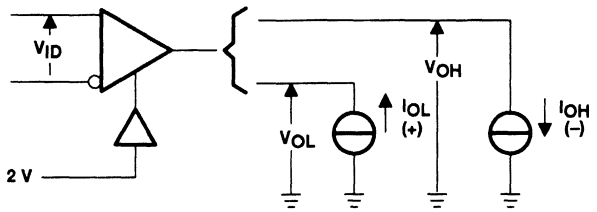
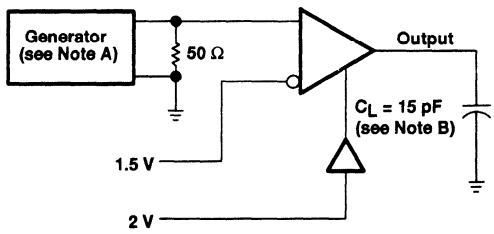
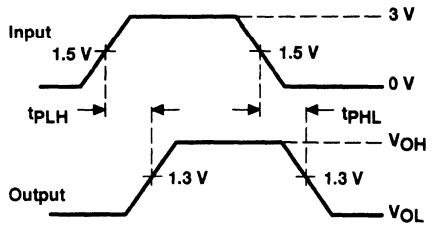


Figure 1. V_{OH}, V_{OL}



TEST CIRCUIT

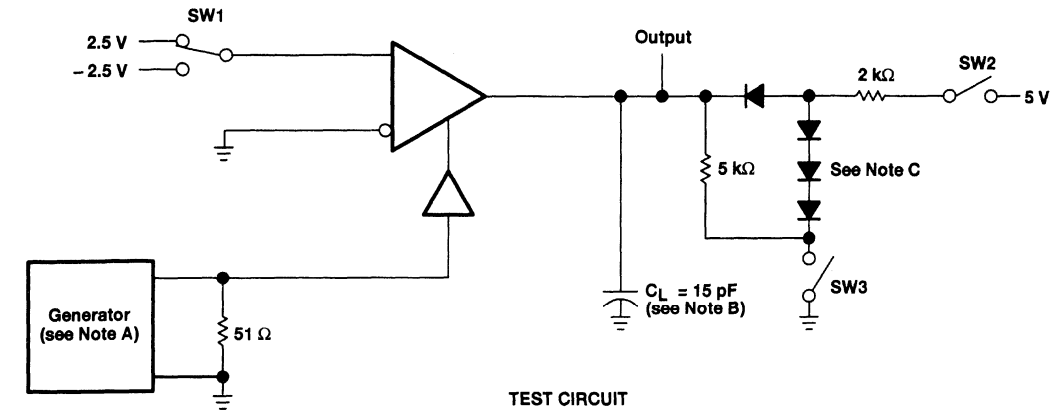


VOLTAGE WAVEFORMS

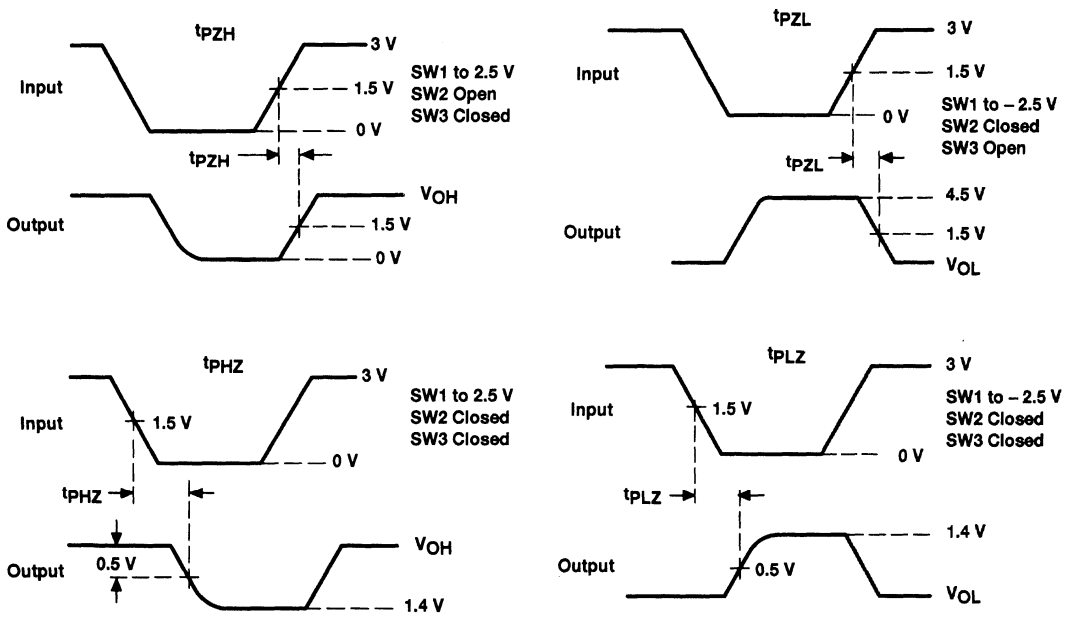
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

Figure 3. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

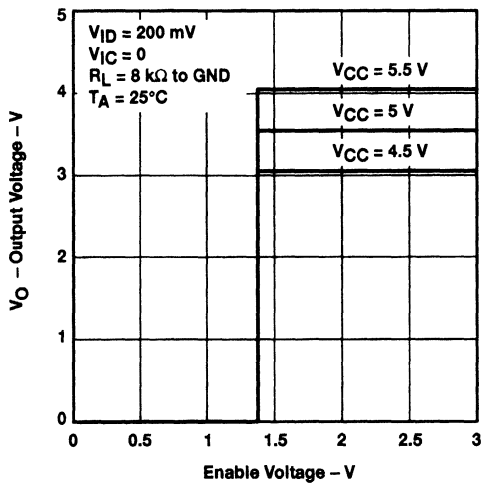


Figure 4

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

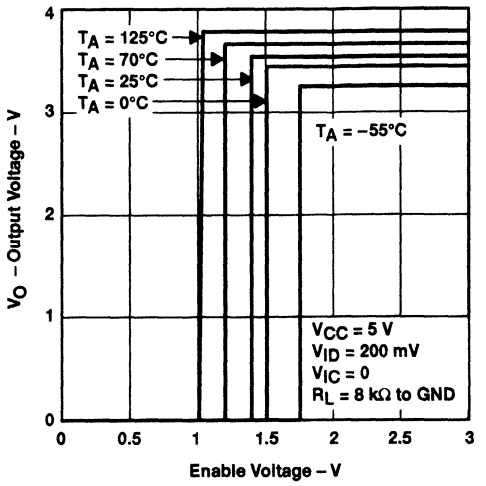


Figure 5

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

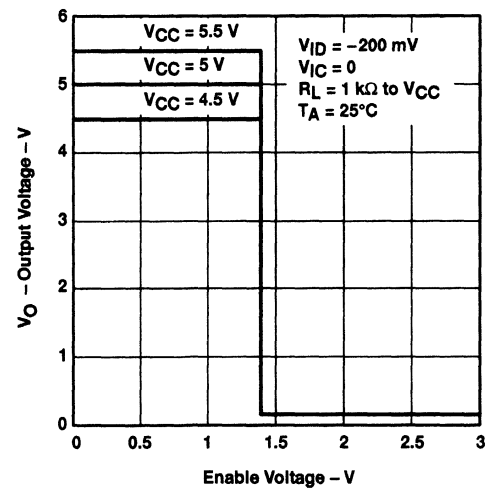


Figure 6

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

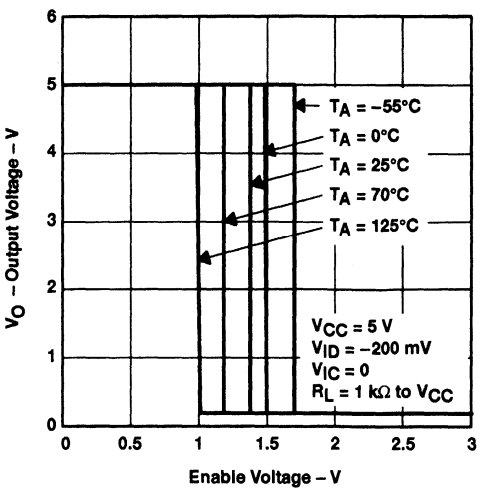


Figure 7

† Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

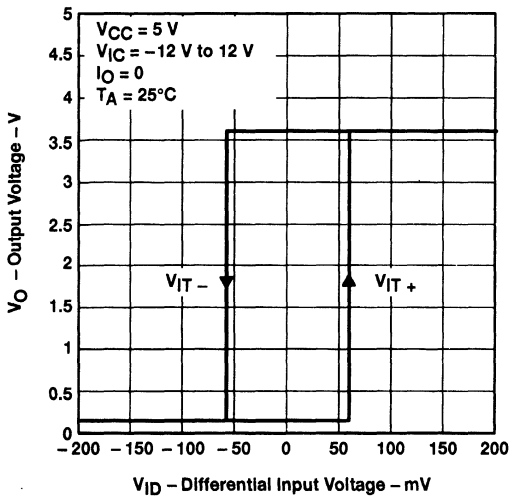


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

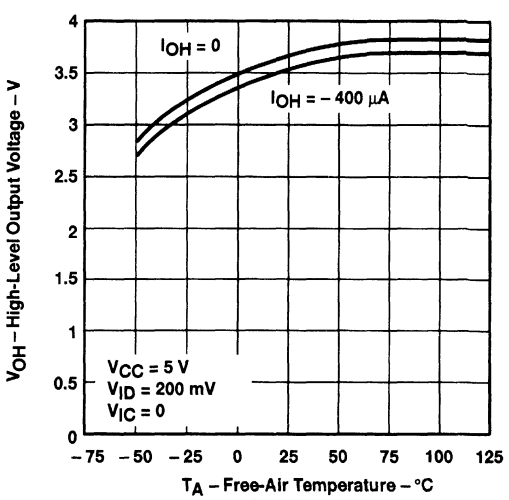


Figure 9

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

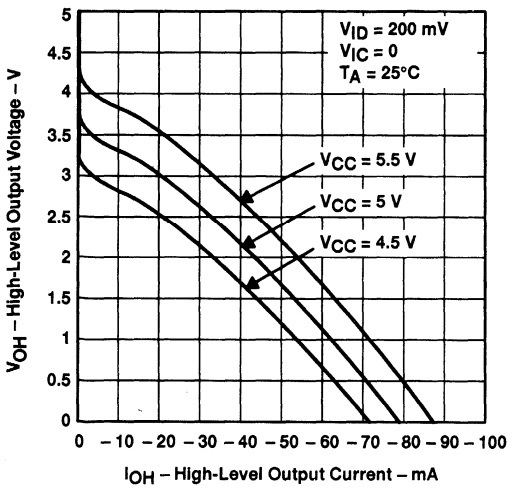


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

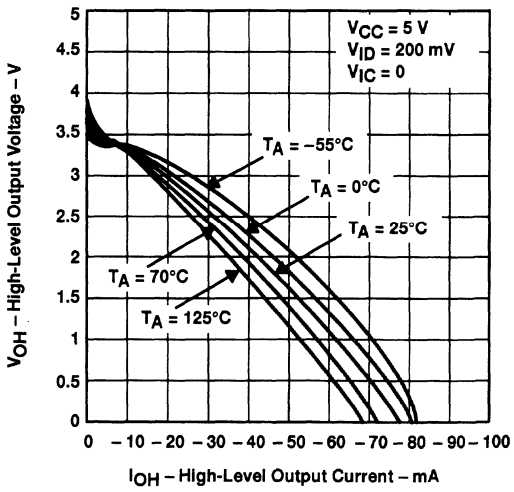


Figure 11

† Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

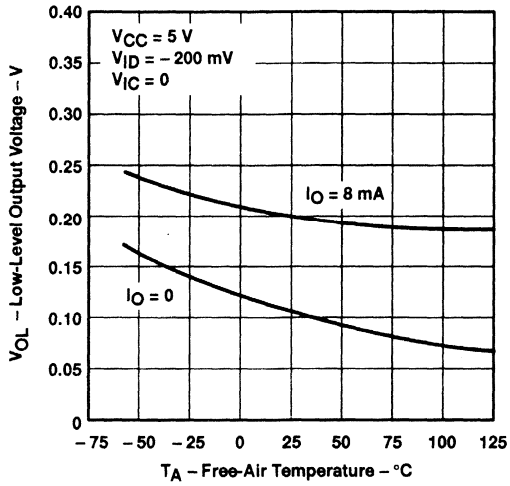


Figure 12

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

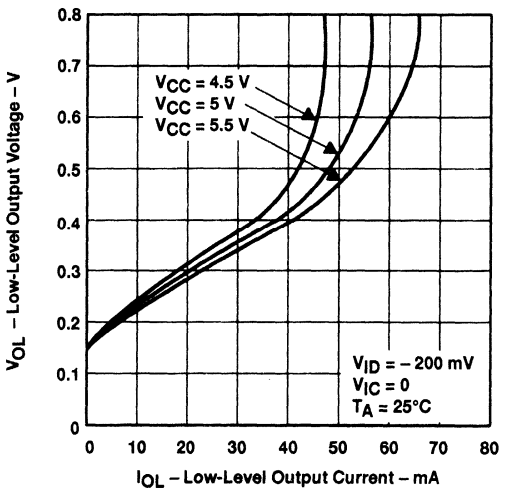


Figure 13

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

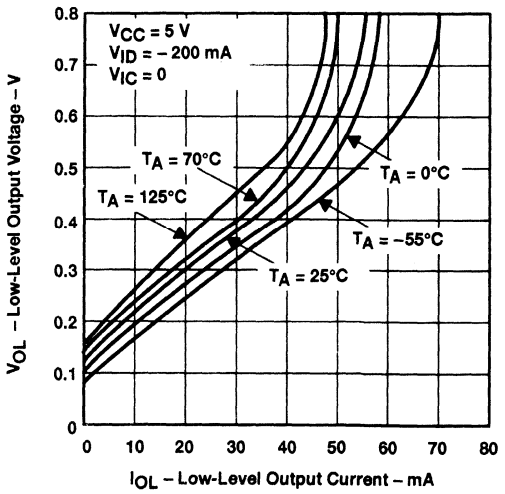


Figure 14

† Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

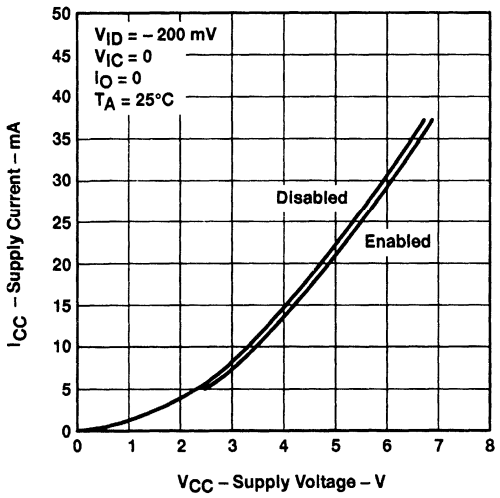


Figure 15

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

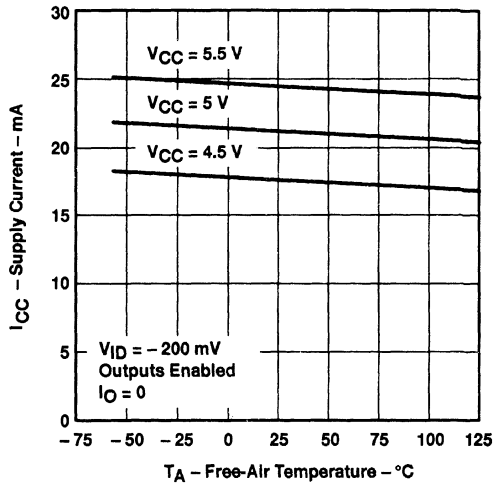


Figure 16

SUPPLY CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

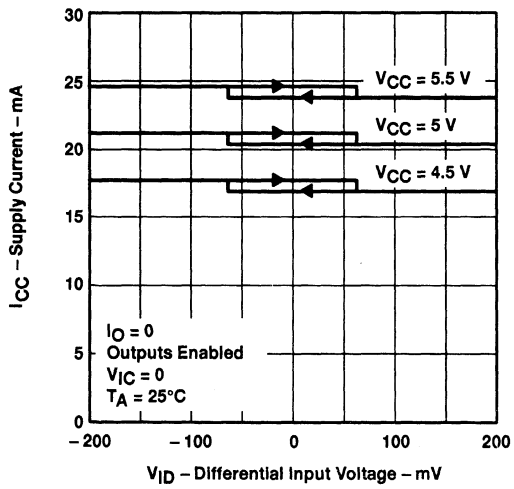


Figure 17

SUPPLY CURRENT
vs
FREQUENCY

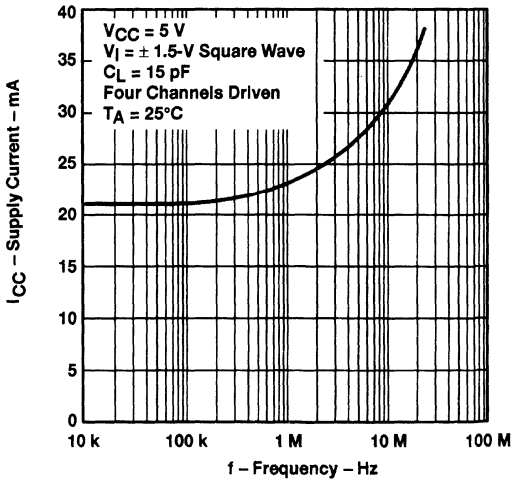


Figure 18

† Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

TYPICAL CHARACTERISTICS†

INPUT RESISTANCE
vs
FREE-AIR TEMPERATURE

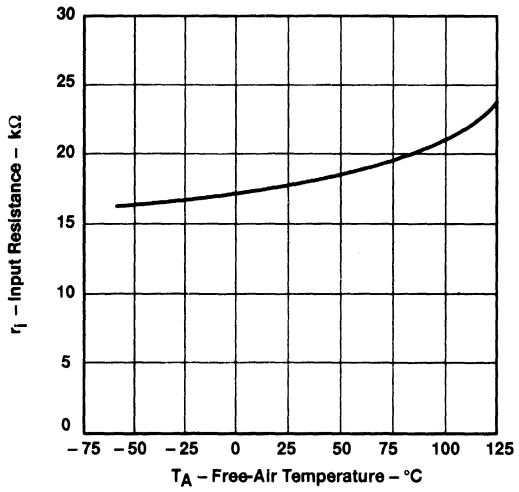


Figure 19

INPUT CURRENT
vs
INPUT VOLTAGE TO GND

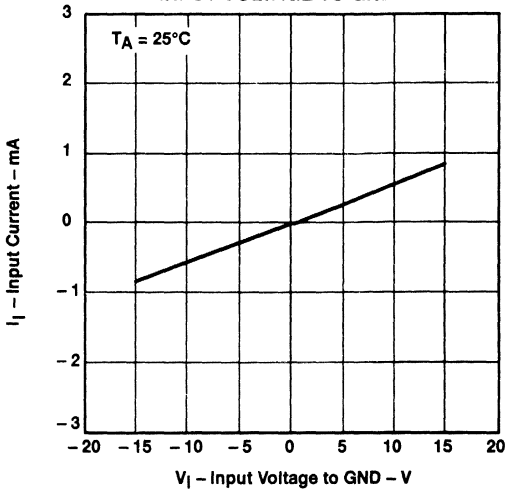


Figure 20

SWITCHING TIME
vs
FREE-AIR TEMPERATURE

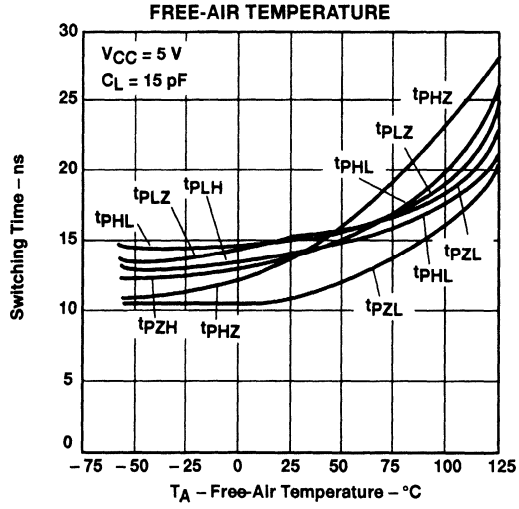


Figure 21

PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

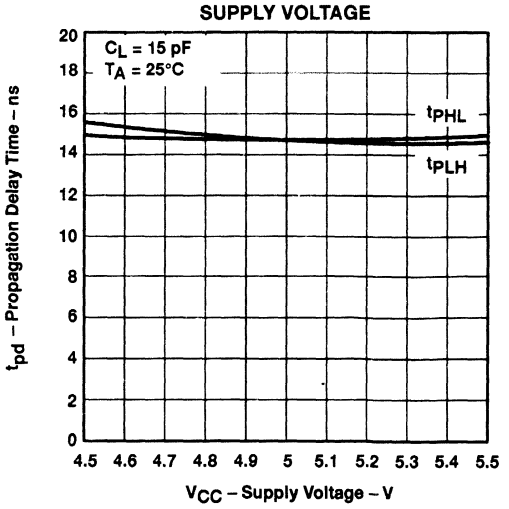


Figure 22

† Data for temperatures below 0°C and above 70°C, and below 4.75 V and above 5.25 V, are applicable to SN55ALS195 circuits only.

SLLS188 – MAY 1995

- **Single Chip With Easy Interface Between UART and Serial-Port Connector of an External Modem or Other Computer Peripheral**
- **Five Drivers and Three Receivers Meet or Exceed the Requirements of ANSI EIA/TIA-232-E and ITU Recommendation V.28 Standards**
- **Designed to Support Data Rates Up To 120 kbps**
- **ESD Protection Meets Or Exceeds 10 kV on RS-232 Pins and 5 kV on All Other Pins (Human-Body Model)**
- **Complement to the SN75185**
- **Pin-to-Pin Replacement for the Goldstar GD75323**
- **Functional Replacement for the MC145405**

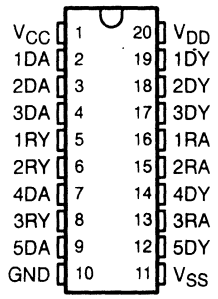
description

The SN75196 combines five drivers and three receivers from the trade-standard SN75188 and SN75189 bipolar quadruple drivers and receivers, respectively. The flow-through design of the SN75196 decreases the part count, reduces the board space required, and allows easy interconnection of the UART and serial-port connector. The all-bipolar circuits and processing of the SN75196 provide a rugged, low-cost solution for this function.

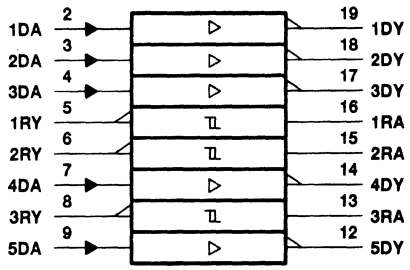
The SN75196 complies with the requirements of the ANSI EIA/TIA 232-E and ITU (formerly CCITT) V.28 standards. These standards are for data interchange between a host computer and peripheral at signal rates of up to 20 kbps. The switching speeds of the SN75196 are fast enough to support rates of up to 120 kbps with lower capacitive loads (shorter cables). Interoperability at the higher signaling rates cannot be assured unless the designer has design control of the cable and the interface circuits at both ends. For interoperability at signaling rates to 120 kbps, use of EIA/TIA-423-B (ITU V.10) and EIA/TIA-422-B (ITU V.11) standards are recommended.

The SN75196 is characterized for operation over a temperature range of 0°C to 70°C.

DW OR N PACKAGE
(TOP VIEW)

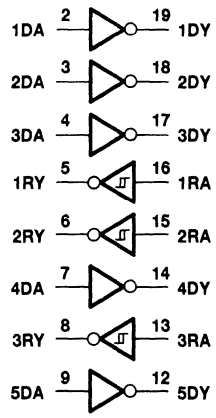


logic symbol†

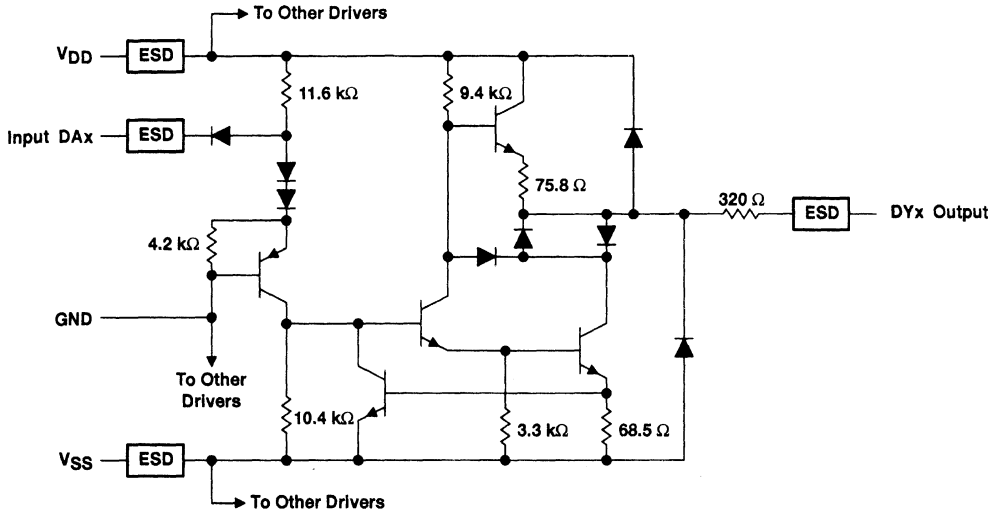


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

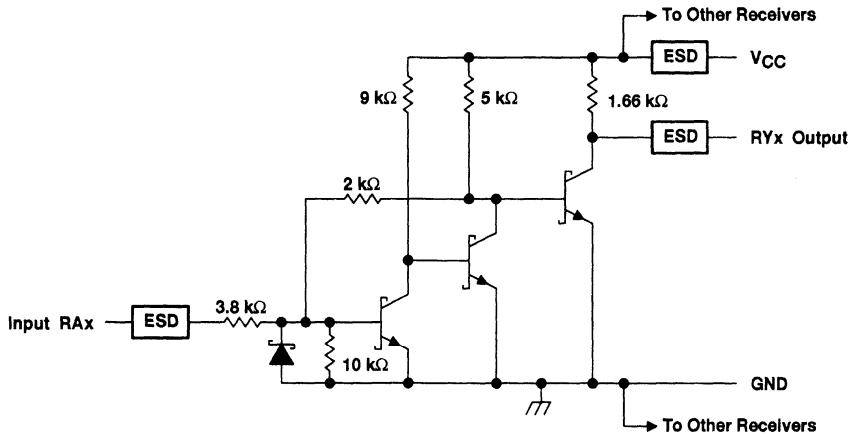


schematic of each driver



Resistor values shown are nominal.

schematic of each receiver



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 10 V
Supply voltage, V_{DD} (see Note 1) ..... 15 V
Supply voltage, V_{SS} (see Note 1) ..... −15 V
Input voltage range, V_I: Driver ..... −15 V to 7 V
Receiver ..... −30 V to 30 V
Output voltage range, V_O (Driver) ..... − 15 V to 15 V
Low-level output current, I_{OL} (Receiver) ..... 20 mA
Continuous total dissipation ..... See Dissipation Rating Table
Electrostatic discharge: DY and RA to GND (see Note 2) ..... Class 3, A: 10 kV, B: 500 V
All pins (see Note 2) ..... Class 3, A: 5 kV, B: 300 V
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to the network ground terminal.
2. Per MIL-STD-883C, Method 3015.7

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
N	1150 mW	9.2 mW/°C	736 mW

‡ This is the inverse of the traditional junction-to-case thermal resistance ($R_{\theta JA}$).

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		7.5	9	13.5	V
Supply voltage, V_{SS}		−7.5	−9	−13.5	V
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level input voltage, V_{IH}	Driver	1.9			V
Low-level input voltage, V_{IL}	Driver			0.8	V
High-level output current, I_{OH}	Driver			−6	mA
	Receiver			−0.5	
High-level output current, I_{OL}	Driver			6	mA
	Receiver			16	
Operating free-air temperature, T_A		0		70	°C

supply currents over operating free-air temperature range

PARAMETER		TEST CONDITIONS				MIN	MAX	UNIT
I_{DD}	Supply current from V_{DD}	All inputs at 1.9 V,	No load	V_{DD} = 9 V,	V_{SS} = −9 V		25	mA
				V_{DD} = 12 V,	V_{SS} = −12 V		32	
		All inputs at 0.8 V,	No load	V_{DD} = 9 V,	V_{SS} = −9 V		7.5	mA
				V_{DD} = 12 V,	V_{SS} = −12 V		9.5	
I_{SS}	Supply current from V_{SS}	All inputs at 1.9 V,	No load	V_{DD} = 9 V,	V_{SS} = −9 V		−25	mA
				V_{DD} = 12 V,	V_{SS} = −12 V		−32	mA
		All inputs at 0.8 V,	No load	V_{DD} = 9 V,	V_{SS} = −9 V		−5.3	mA
				V_{DD} = 12 V,	V_{SS} = −12 V		−5.3	mA
I_{CC}	Supply current from V_{CC}	V_{CC} = 5 V,	All inputs at 5 V,		No load		20	mA

DRIVER SECTION

electrical characteristics over operating free-air temperature range, V_{DD} = 9 V, V_{SS} = −9 V, V_{CC} = 5 V, (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_{IL} = 0.8 V,	R_L = 3 kΩ,	See Figure 1	6	7.5		V
V_{OL}	Low-level output voltage (see Note 2)	V_{IH} = 1.9 V,	R_L = 3 kΩ,	See Figure 1		−7.5	−6	V
I_{IH}	High-level input current	V_I = 5 V,	See Figure 2				10	μA
I_{IL}	Low-level input current	V_I = 0,	See Figure 2				−1.6	mA
$I_{OS(H)}$	High-level short-circuit output current (see Note 4)	V_{IL} = 0.8 V,	V_O = 0,	See Figure 1	−4.5	−9	−19.5	mA
$I_{OS(L)}$	Low-level short-circuit output current (see Note 4)	V_{IH} = 2 V,	V_O = 0,	See Figure 1	4.5	9	19.5	mA
r_o	Output resistance (see Note 5)	V_{CC} = V_{DD} = V_{SS} = 0,		V_O = −2 V to 2 V	300			Ω

NOTES: 3. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if −10 V is a maximum, the typical value is a more negative voltage.
4. Output short-circuit conditions must maintain the total power dissipation below absolute maximum ratings.
5. Test conditions are those specified by EIA/TIA-232-E and as listed above.

switching characteristics, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ±10%, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 3 kΩ to 7 kΩ,	C_L = 15 pF, See Figure 3		315	500	ns
t_{PHL}	Propagation delay time, high- to low-level output				75	175	ns
t_{TLH}	Transition time, low- to high-level output	R_L = 3 kΩ to 7 kΩ, See Figure 3	C_L = 15 pF,		60	100	ns
		R_L = 3 kΩ to 7 kΩ, See Figure 3 and Note 6	C_L = 2500 pF,		1.7	2.5	μs
t_{THL}	Transition time, high- to low-level output (see Note 6)	R_L = 3 kΩ to 7 kΩ, See Figure 3	C_L = 15 pF,		40	75	ns
		R_L = 3 kΩ to 7 kΩ, See Figure 3 and Note 7	C_L = 2500 pF,		1.5	2.5	μs

NOTES: 6. Measured between −3-V and 3-V points of the output waveform (EIA/TIA-232-E conditions), all unused inputs are tied either high or low.
7. Measured between 3-V and −3-V points of the output waveform (EIA/TIA-232-E conditions), all unused inputs are tied either high or low.

RECEIVER SECTION

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going threshold voltage	See Figure 5	T_A = 25°C	1.75	1.9	2.3	V
			T_A = 0°C to 70 °C	1.55		2.3	
V_{IT-}	Negative-going threshold voltage	See Figure 5		0.75	0.97	1.25	
V_{hys}	Input hysteresis ($V_{IT+} - V_{IT-}$)			0.5			
V_{OH}	High-level output voltage	I_{OH} = −0.5 mA	V_{IH} = 0.75 V	2.6	4	5	V
			Inputs open	2.6			
V_{OL}	Low-level input voltage	I_{OL} = 10 mA,	V_I = 3 V		0.2	0.45	V
I_{IH}	High-level input current	V_I = 25 V,	See Figure 5	3.6		8.3	mA
		V_I = 3 V,	See Figure 5	0.43			
I_{IL}	Low-level output current	V_I = −25 V,	See Figure 5	−3.6		−8.3	mA
		V_I = −3 V,	See Figure 5	−0.43			
I_{OS}	Short-circuit output current	See Figure 4			−3.4	−12	mA

† All typical values are at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 9 V, and V_{SS} = −9 V.

switching characteristics, V_{CC} = 5 V, V_{DD} = 12 V, V_{SS} = −12 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 50 pF, R_L = 5 kΩ, See Figure 6		107	500	ns
t_{PHL}	Propagation delay time, high- to low-level output			42	150	ns
t_{TLH}	Transition time, low- to high-level output			175	525	ns
t_{THL}	Transition time, high- to low-level output			16	60	ns

PARAMETER MEASUREMENT INFORMATION

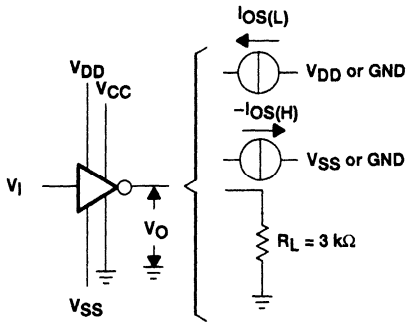


Figure 1. Driver Test Circuit for V_{OH}, V_{OL}, $I_{OS(H)}$, and $I_{OS(L)}$

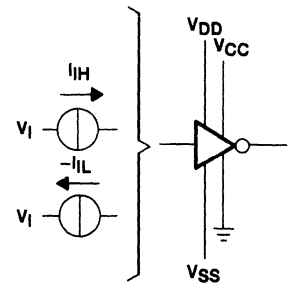
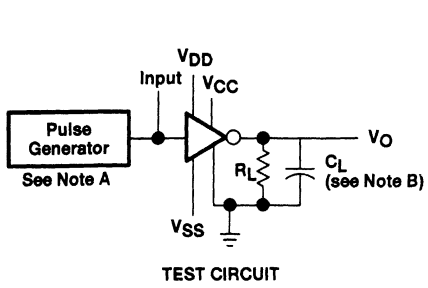
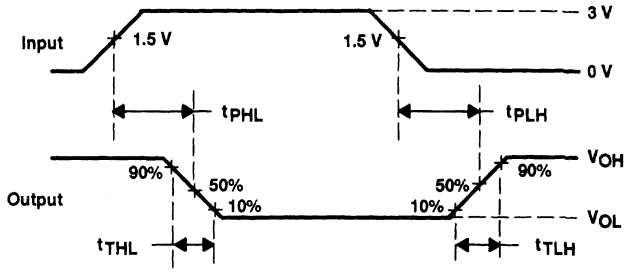


Figure 2. Driver Test Circuit for I_{IH} and I_{IL}

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: t_w = 25 µs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

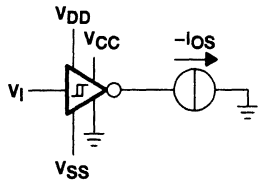


Figure 4. Receiver Test Circuit for I_{OS}

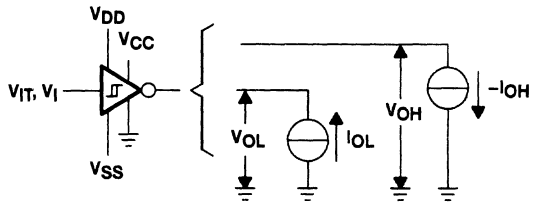
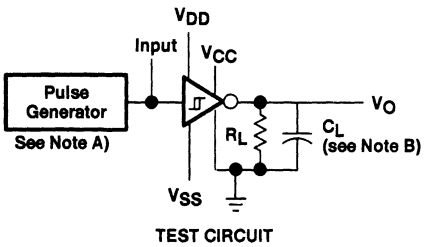
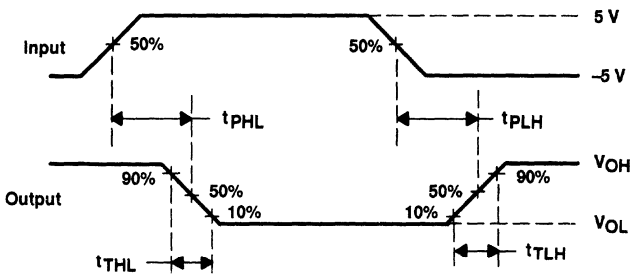


Figure 5. Receiver Test Circuit for V_{IT}, V_{OH}, and V_{OL}



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: t_w = 25 µs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.
B. C_L includes probe and jig capacitance.

Figure 6. Receiver Propagation and Transition Times

TYPICAL CHARACTERISTICS

DRIVER SECTION

VOLTAGE TRANSFER CHARACTERISTICS

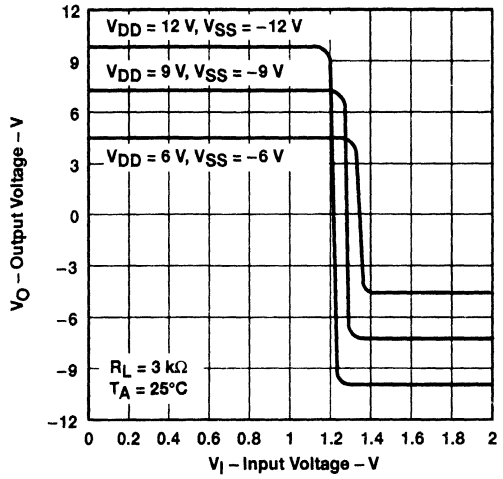


Figure 7

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

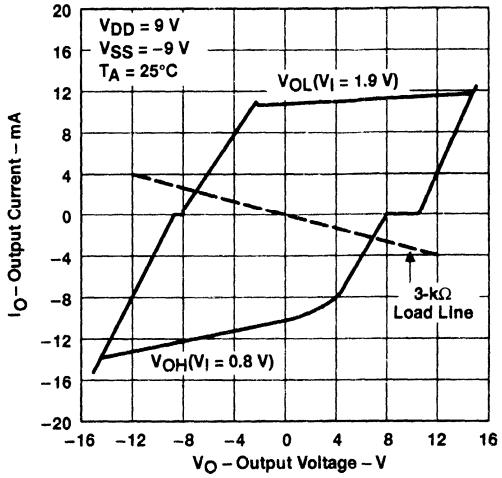


Figure 8

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

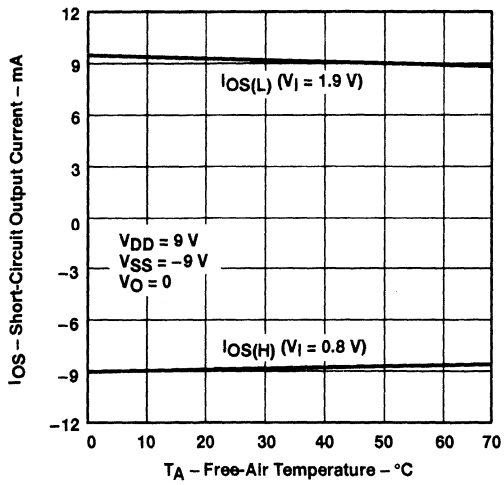


Figure 9

SLEW RATE
vs
LOAD CAPACITANCE

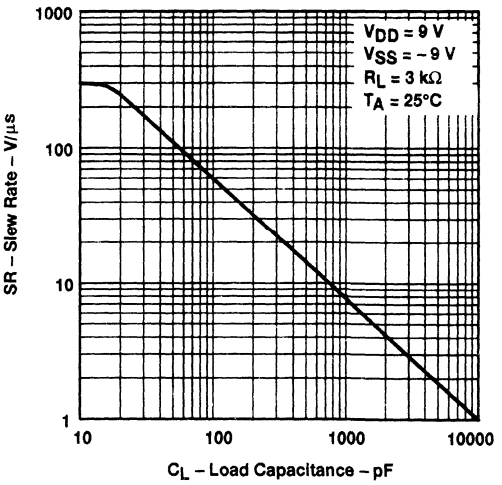


Figure 10

TYPICAL CHARACTERISTICS

RECEIVER SECTION

INPUT THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

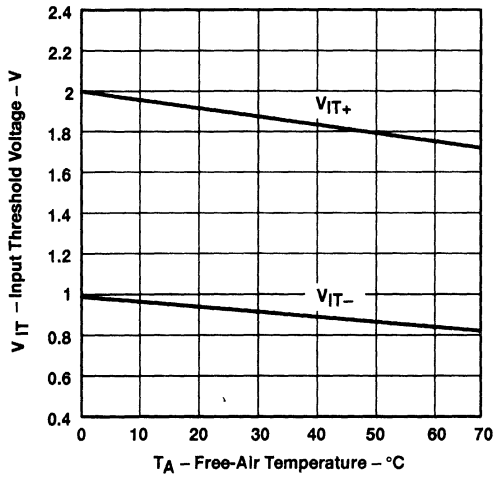


Figure 11

INPUT THRESHOLD VOLTAGE vs SUPPLY VOLTAGE

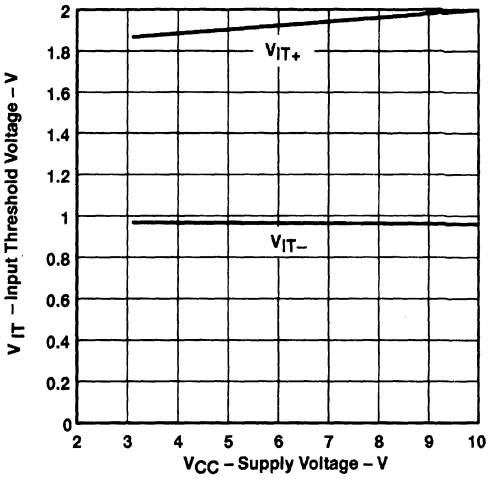
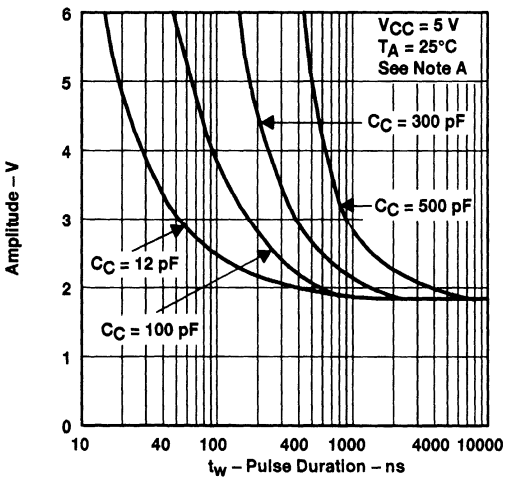


Figure 12

NOISE REJECTION



NOTE A: This figure shows the maximum amplitude of a positive-going pulse that, starting from 0 V, will not cause a change of the output level.

Figure 13

MAXIMUM SUPPLY VOLTAGE vs FREE-AIR TEMPERATURE

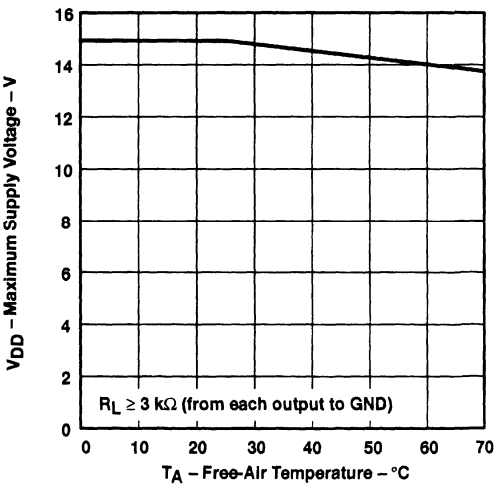


Figure 14

APPLICATION INFORMATION

Diodes placed in series with the V_{DD} and V_{SS} pins protect the SN75196 in the fault condition in which the device outputs are shorted to V_{DD} or V_{SS} and the power supplies are at low and provide low-impedance paths to ground (see Figure 15).

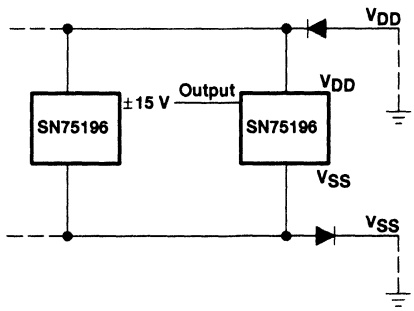
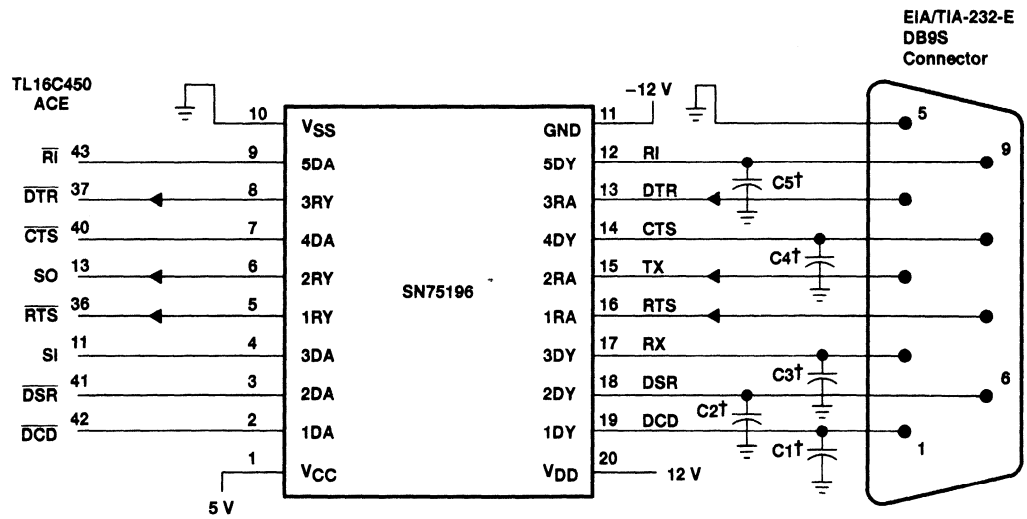


Figure 15. Power-Supply Protection to Meet Power-Off Fault Conditions of EIA/TIA-232-E



† See Figure 10 to select the correct values for the loading capacitors (C1, C2, C3, C4 and C5), which may be required to meet the RS-232 maximum slew-rate requirement of 30 V/μs. The value of the loading capacitors required depends upon the line length and desired slew rate, but is typically 330 pF.

NOTE C. To use the receivers only, V_{DD} and V_{SS} must both be powered or tied to ground.

Figure 16. Typical Connection

SLLS045B – JANUARY 1989 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of ITU Recommendations V.10, V.11, X.26, and X.27**
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments**
- **Designed to Operate Up To 20 Mbaud**
- **3-State Outputs**
- **Common-Mode Input Voltage Range −7 V to 7 V**
- **Input Sensitivity . . . ± 300 mV**
- **Input Hysteresis . . . 120 mV Typ**
- **High-Input Impedance . . . 12 kΩ Min**
- **Operates from Single 5-V Supply**
- **Low Supply Current Requirement 35 mA Max**
- **Improved Speed and Power Consumption Compared to AM26LS32A**

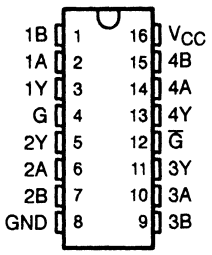
description

The SN75ALSI97 is a monolithic, quadruple line receiver with 3-state outputs designed using advanced, low-power, Schottky technology. This technology provides combined improvements in bar design, tooling production, and wafer fabrication. This, in turn, provides significantly less power requirements and permits much higher data throughput than other designs. The device meets the specifications of ITU Recommendations V.10, V.11, X.26, and X.27. It features 3-state outputs that permit direct connection to a bus-organized system with a fail-safe design that ensures the outputs will always be high if the inputs are open.

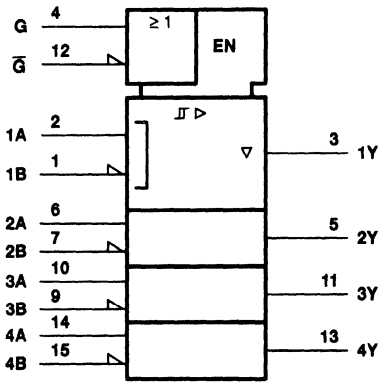
The device is optimized for balanced, multipoint bus transmission at rates up to 20 megabits per second. The input features high-input impedance, input hysteresis for increased noise immunity, and an input sensitivity of ±300 mV over a common-mode input voltage range of −7 V to 7 V. It also features active-high and active-low enable functions that are common to the four channels. The SN75ALS197 is designed for optimum performance when used with the SN75ALS192 quadruple differential line driver.

The SN75ALS197 is characterized for operation from 0°C to 70°C.

D OR N PACKAGE
(TOP VIEW)

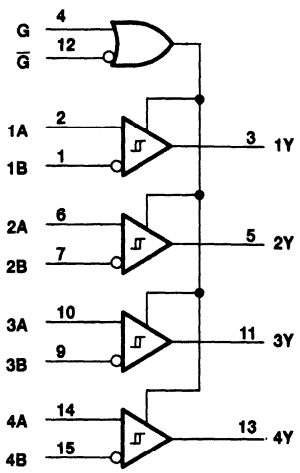


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

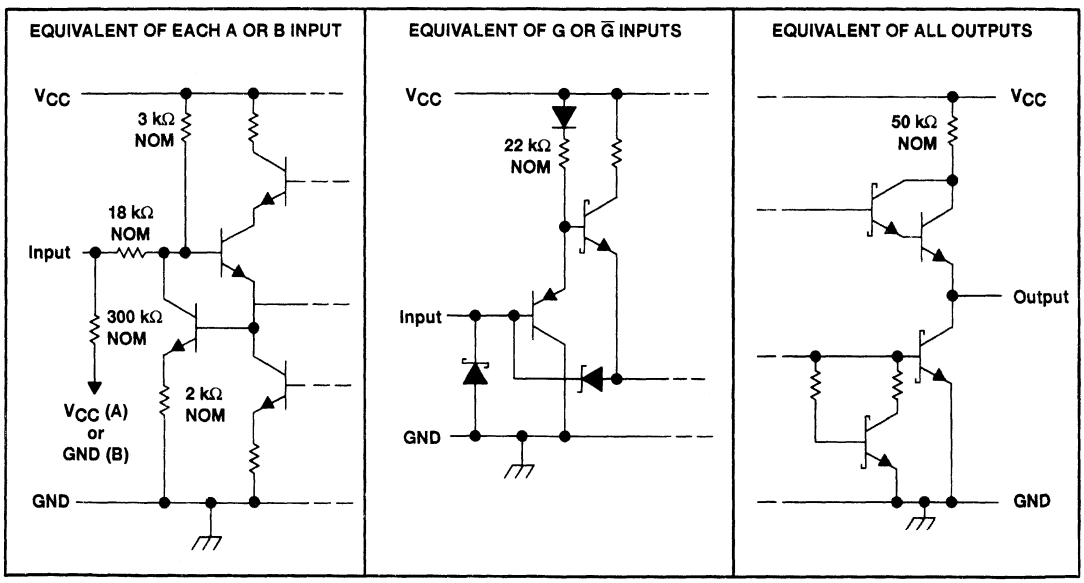


FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A–B	ENABLES G	ENABLES $\overline{G}$	OUTPUT Y
$V_{ID} \geq 0.3$ V	H	X	H
	X	L	H
-0.3 V $< V_{ID} <$ 0.3 V	H	X	?
	X	L	?
$V_{ID} \leq -0.3$ V	H	X	L
	X	L	L
X	L	H	Z
Open	H	X	H
	X	L	H

H = high level, L = low level, X = irrelevant, ? = indeterminate,
Z = high impedance (off)

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I (A or B inputs) ..... ±15 V
Differential input voltage, V_{ID} (see Note 2) ..... ±15 V
Enable input voltage, V_I ..... 7 V
Low-level output current, I_{OL} ..... 50 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the, corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Differential input voltage, V_{ID}			±12	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			– 400	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended range of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage					300	mV
V_{IT-}	Negative-going input threshold voltage			−300‡			mV
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)	See Figure 4			120		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 300 mV,	I_{OH} = − 400 µA	2.7	3.6		V
V_{OL}	Low-level output voltage	V_{ID} = − 300 mV	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	V_{CC} = 5.25 V	V_O = 2.4 V			20	µA
			V_{OH} = 0.4 V			−20	
I_I	Line input current	Other input at 0 V, See Note 3	V_I = 15 V		0.7	1.2	mA
			V_I = −15 V		−1.0	−1.7	
I_H	High-level enable-input current		V_{IH} = 2.7 V			20	µA
			V_{IH} = 5.25 V			100	
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	µA
	Input resistance			12	18		kΩ
I_{OS}	Short-circuit output current§	V_{ID} = 3 V,	V_O = 0	−15	−78	−130	mA
I_{CC}	Supply current	Outputs disabled			22	35	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 3: Refer to ANSI Standard EIA/TIA-422-B and EIA/TIA-423-B for exact conditions.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_{ID} = − 2.5 V to 2.5 V, See Figure 2	C_L = 15 pF,		15	22	ns
t_{PHL}	Propagation delay time, high- to low-level output				15	22	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 3		13	25	ns
t_{PZL}	Output enable time to low level				11	25	
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 3		13	25	ns
t_{PLZ}	Output disable time from low level				15	22	

PARAMETER MEASUREMENT INFORMATION

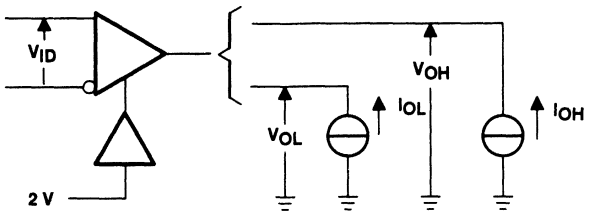
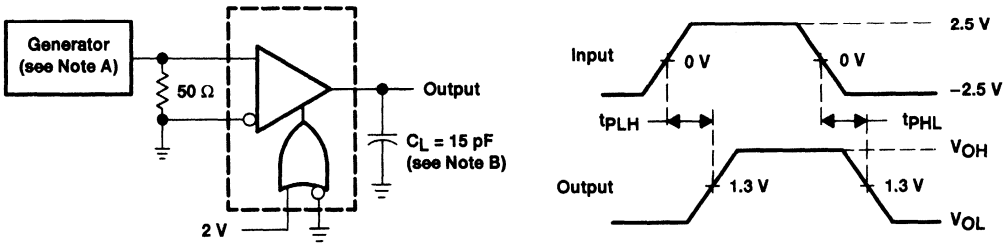


Figure 1. V_{OH} and V_{OL} Test Circuit

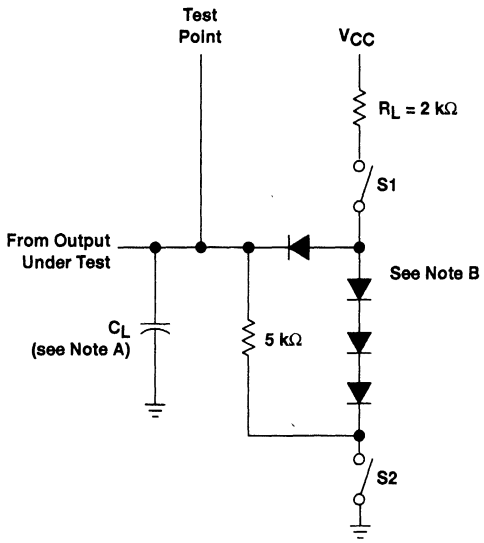


TEST CIRCUIT **VOLTAGE WAVEFORMS**

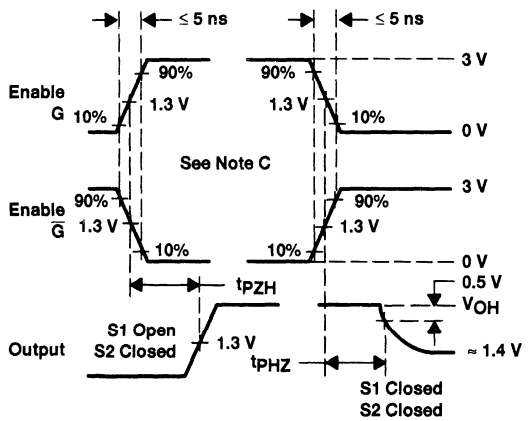
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.

Figure 2. t_{PLH} and t_{PHL} Test Circuit and Voltage Waveforms

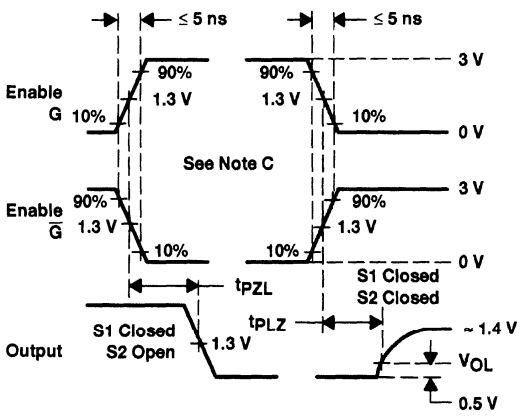
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS FOR t_{PHZ} and t_{PZH}



VOLTAGE WAVEFORMS FOR t_{PLZ} and t_{PZL}

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Enable G is tested with $\overline{G}$ high; $\overline{G}$ is tested with G low.

Figure 3. t_{PHZ}, t_{PZH}, t_{PLZ}, and t_{PZL} Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

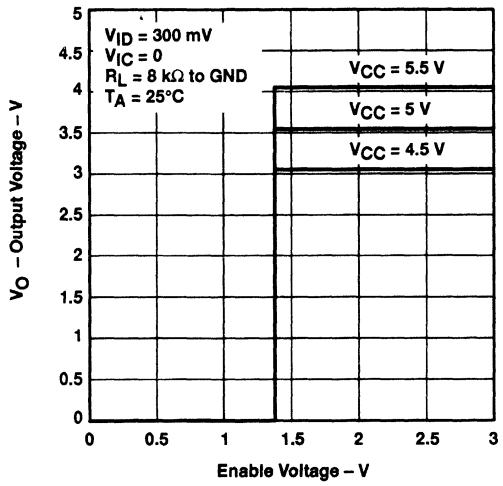


Figure 4

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

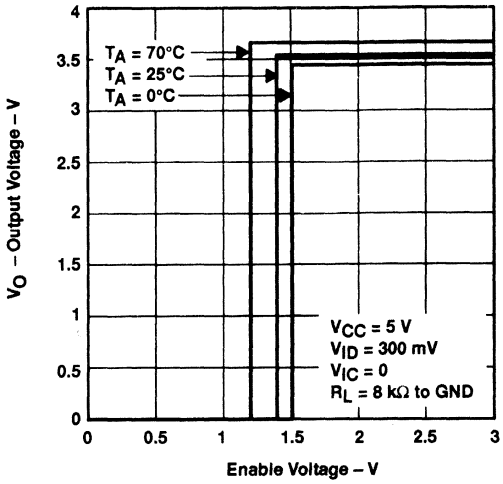


Figure 5

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

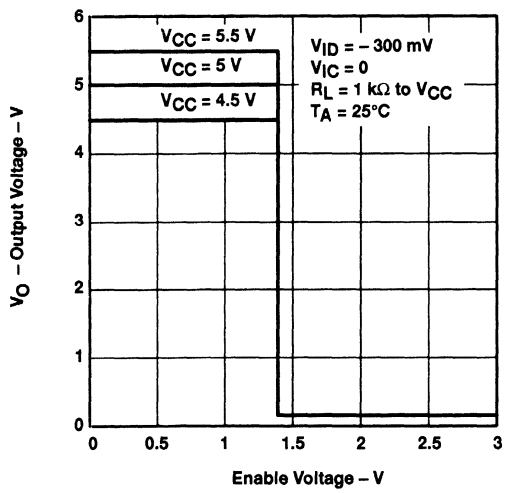


Figure 6

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

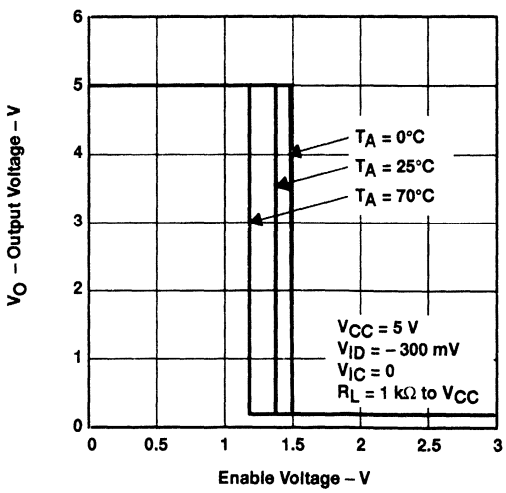


Figure 7

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

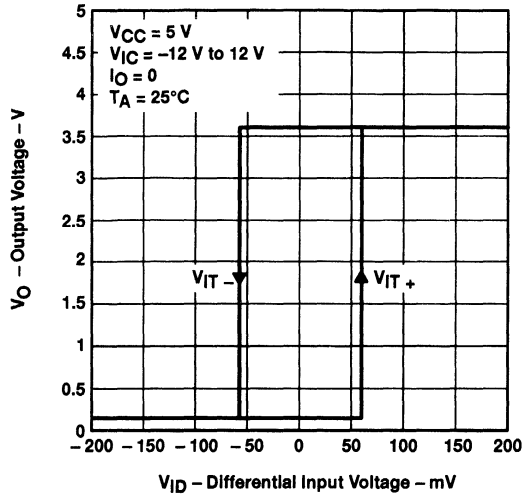


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

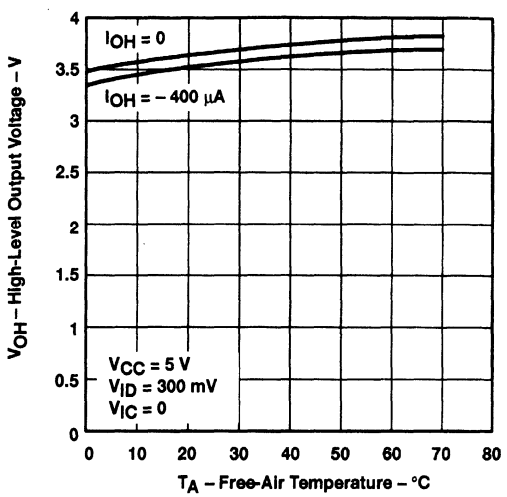


Figure 9

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

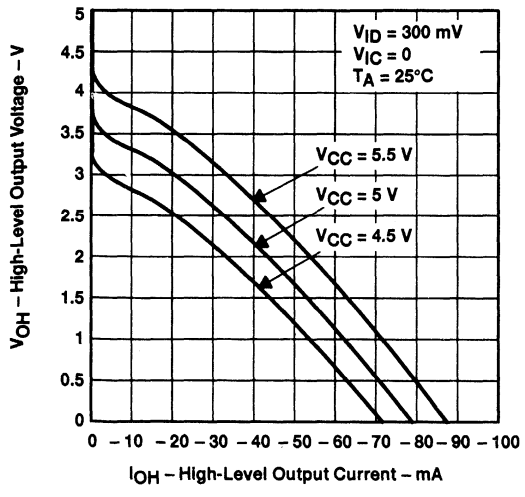


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

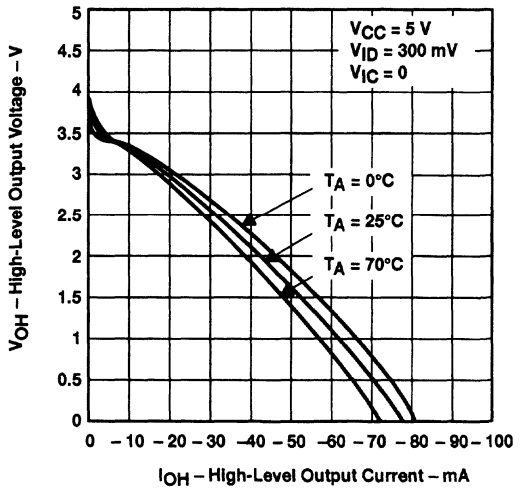


Figure 11

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

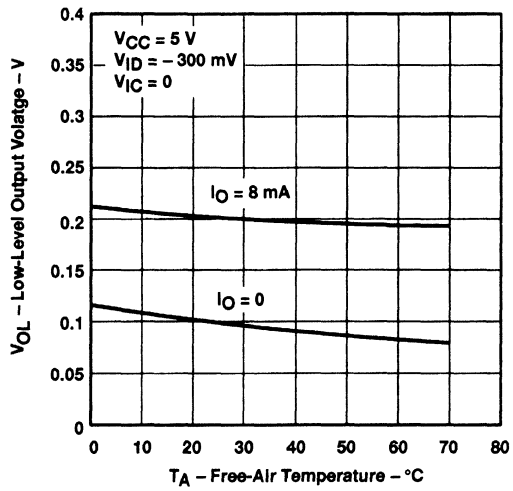


Figure 12

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

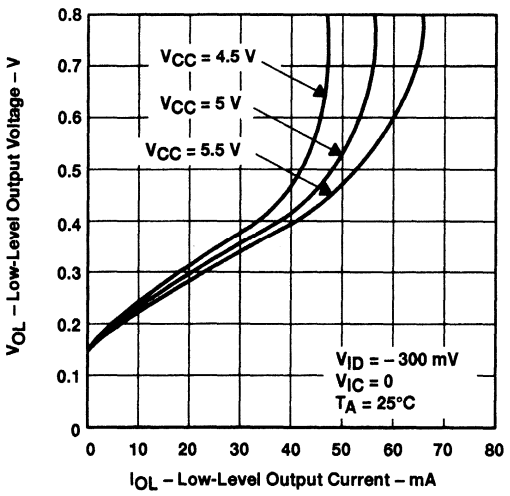


Figure 13

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

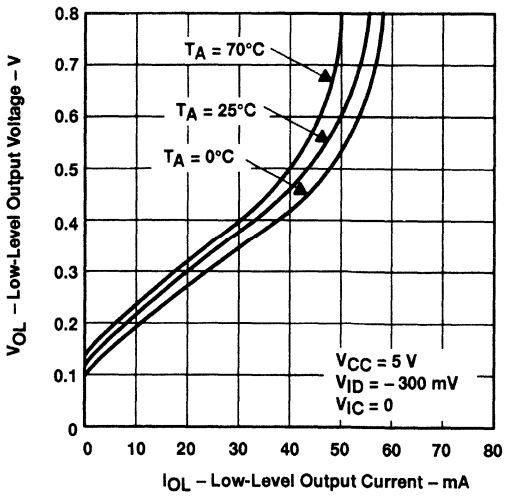


Figure 14

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

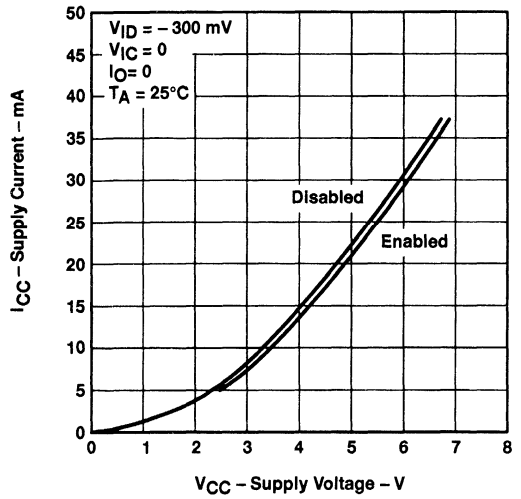


Figure 15

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

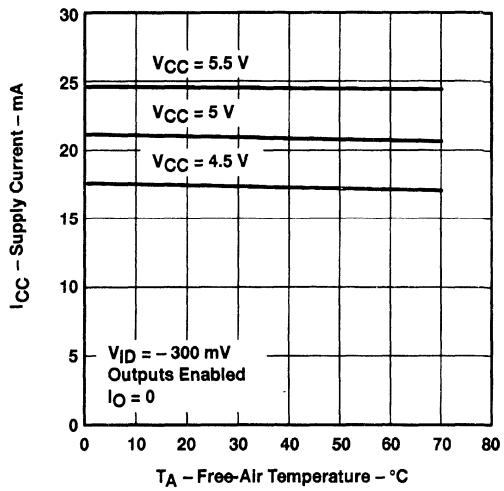


Figure 16

SUPPLY CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

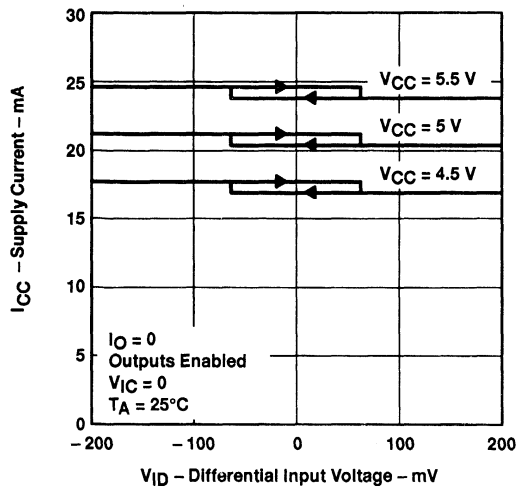


Figure 17

SUPPLY CURRENT
vs
FREQUENCY

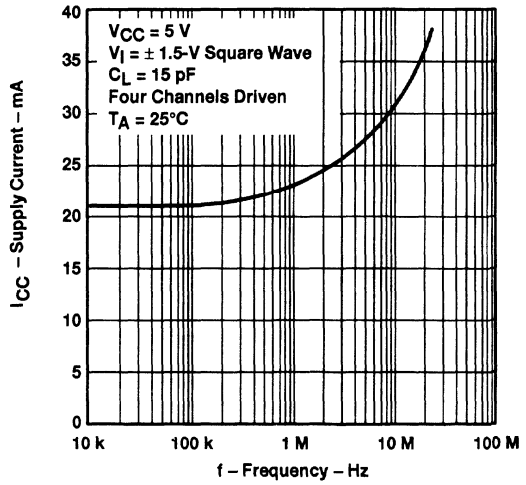


Figure 18

TYPICAL CHARACTERISTICS

INPUT RESISTANCE vs FREE-AIR TEMPERATURE

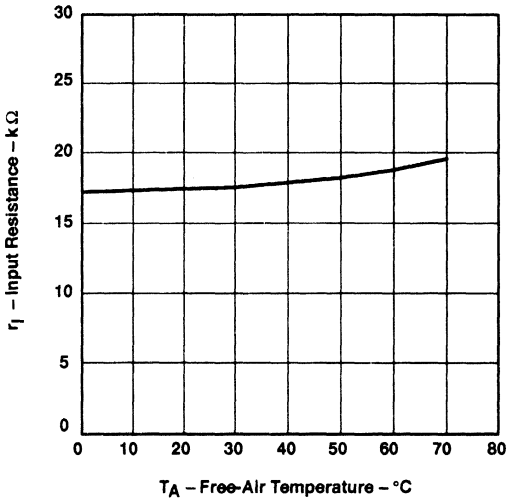


Figure 19

INPUT CURRENT vs INPUT VOLTAGE TO GND

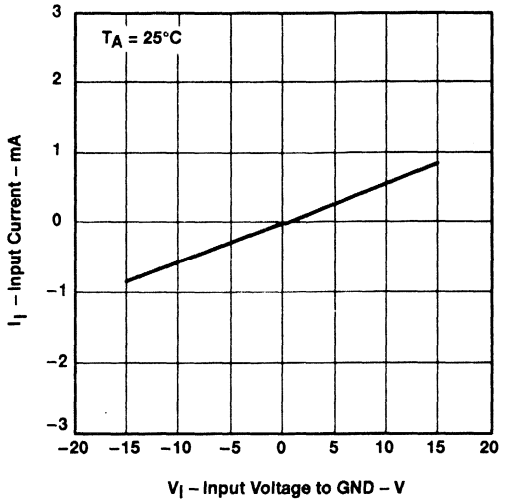


Figure 20

SWITCHING TIME vs FREE-AIR TEMPERATURE

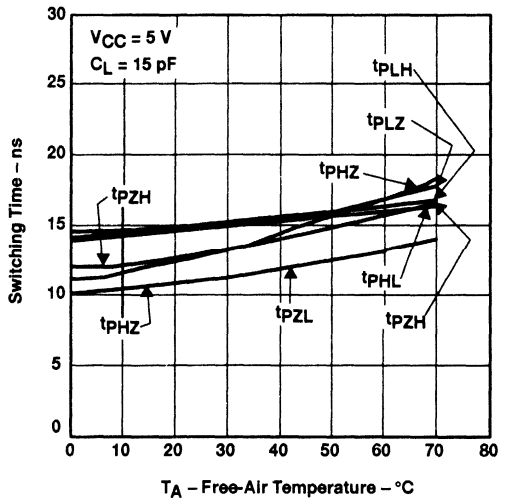


Figure 21

PROPAGATION DELAY TIME vs SUPPLY VOLTAGE

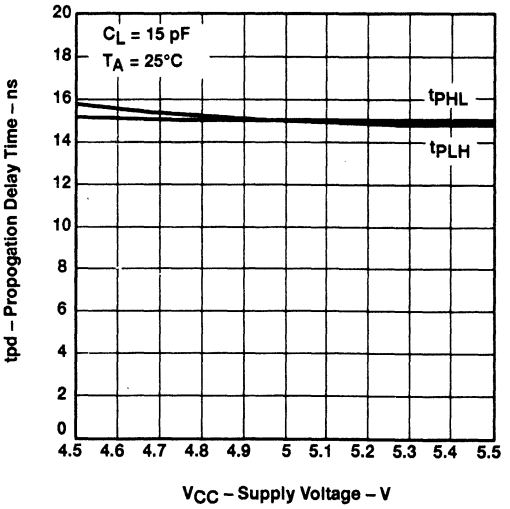


Figure 22

- **Meets ANSI EIA/TIA-232-E and ITU Recommendation V.28**
- **Very Low Supply Current**
- **Sleep Mode:**
  3-State Outputs In High-Impedance State
  Ultra-Low Supply Current . . . 17 μA Typ
- **Improved Functional Replacement for:**
  SN75188,
  Motorola MC1488,
  National Semiconductor DS14C88, and
  DS1488
- **CMOS- and TTL-Compatible Data Inputs**
- **On-Chip Slew-Rate Limit . . . 30 V/μs**
- **Output Current Limit . . . 10 mA Typ**
- **Wide Supply Voltage Range . . . ±4.5 V to ±15 V**

description

The SN65C198 and SN75C198 are monolithic low-power BI-MOS quadruple low-power line drivers designed to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE) in conformance with the specifications of ANSI EIA/TIA-232-E. The drivers of the SN65C198 and SN75C198 are similar to those of the SN75C188 quadruple driver. The drivers have a controlled-output slew rate that is limited to a maximum of 30 V/μs. This feature eliminates the need for external components.

The sleep-mode input, $\overline{SM}$, can switch the outputs to high impedance, which avoids the transmission of corrupted data during power-up and allows significant system power savings during data-off periods.

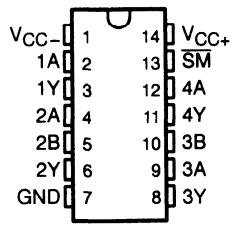
The SN65C198 is characterized for operation from −40°C to 85°C. The SN75C198 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

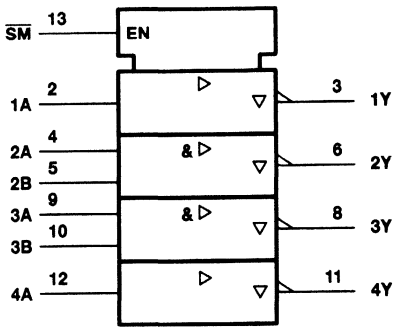
INPUTS			OUTPUT
$\overline{SM}$	A	B	Y
H	H	H	L
H	L	X	H
H	X	L	H
L	X	X	Z

H = high level, L = low level,
X = irrelevant, Z= high impedance

D OR N PACKAGE
(TOP VIEW)

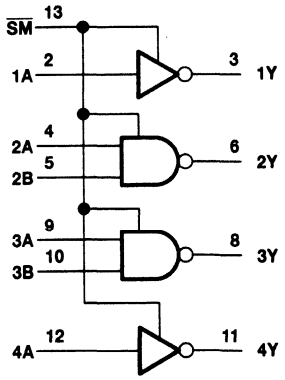


logic symbol†

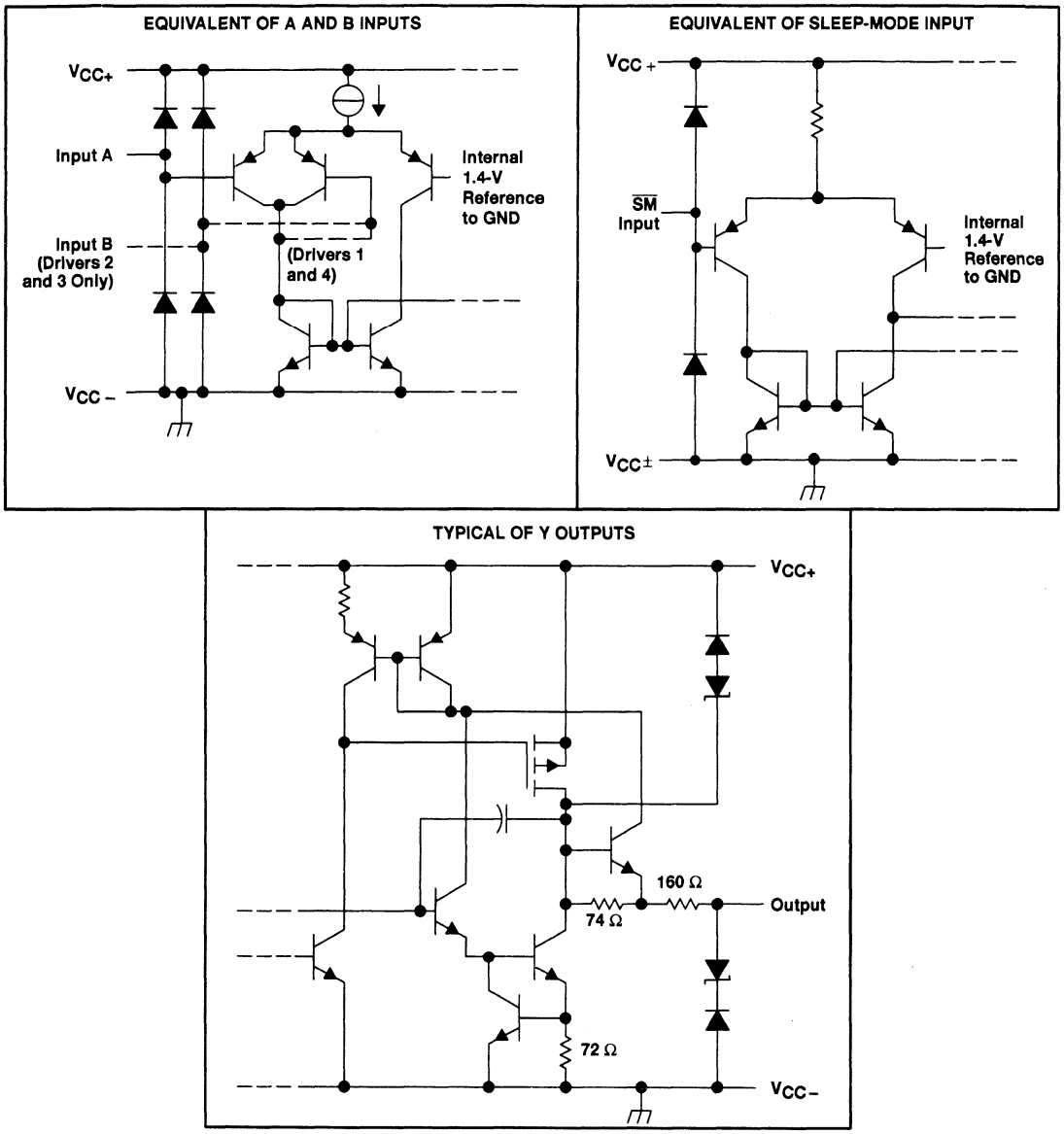


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) ..... 15 V
Supply voltage, V_{CC-} ..... −15 V
Input voltage range, V_I ..... −15 V to 15 V
Output voltage range, V_O ..... V_{CC-} −6 V to V_{CC+} + 6 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65C198 ..... −40°C to 85°C
SN75C198 ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	494 mW
N	1150 mW	9.2 mW/°C	598 mW

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}			4.5	12	15	V
Supply voltage, V_{CC-}			−4.5	−12	−15	V
Input voltage, V_I (see Figure 2)			V_{CC-}+2		V_{CC+}	V
High-level input voltage, V_{IH}			2			V
Low-level input voltage, V_{IL}	A and B inputs				0.8	V
	$\overline{SM}$ input				0.6	
Operating free-air temperature, T_A		SN65C198	−40		85	°C
		SN75C198	0		70	

electrical characteristics over recommended operating free-air temperature range, $V_{CC\pm}$ = ±12 V, $\overline{SM}$ at 2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{IH} = 0.8 V, R_L = 3 kΩ		$V_{CC\pm}$ = ±5 V	4			V
				$V_{CC\pm}$ = ±12 V	10			
V_{OL}	Low-level output voltage (see Note 2)	V_{IH} = 2 V, R_L = 3 kΩ		$V_{CC\pm}$ = ±5 V			−4	V
				$V_{CC\pm}$ = ±12 V			−10	
I_{IH}	High-level input current	V_I = 5 V					10	μA
I_{IL}	Low-level input current	V_I = 0 V					−10	μA
I_{OZ}	High-impedance-state output current	$\overline{SM}$ at 0.6 V		V_O = 12 V, $V_{CC\pm}$ = ±12 V			100	μA
				V_O = −12 V, $V_{CC\pm}$ = ±12 V			−100	
$I_{OS(H)}$	High-level short-circuit output current‡	V_I = 0.8 V,	V_O = 0 or V_{CC-}		−4.5	−10	−19.5	mA
$I_{OS(L)}$	Low-level short-circuit output current‡	V_I = 2 V,	V_O = 0 or V_{CC+}		4.5	10	19.5	mA
r_o	Output resistance	$V_{CC\pm}$ = 0,	V_O = −2 V to 2 V		300			Ω
I_{CC+}	Supply current from V_{CC+}	A and B inputs at 0.8 V or 2 V, No load		$V_{CC\pm}$ = ±5 V		90	160	μA
				$V_{CC\pm}$ = ±12 V		95	160	
		A and B inputs at 0.8 V or 2 V, R_L = 3 kΩ, $\overline{SM}$ at 0.6 V		$V_{CC\pm}$ = ±5 V		40		
				$V_{CC\pm}$ = ±12 V		40		
I_{CC-}	Supply current from V_{CC-}	A and B inputs at 0.8 V or 2 V, No load		$V_{CC\pm}$ = ±5 V		−90	−160	μA
				$V_{CC\pm}$ = ±12 V		−95	−160	
		A and B inputs at 0.8 V or 2 V, R_L = 3 kΩ, $\overline{SM}$ at 0.6 V		$V_{CC\pm}$ = ±5 V		−40		
				$V_{CC\pm}$ = ±12 V		−40		

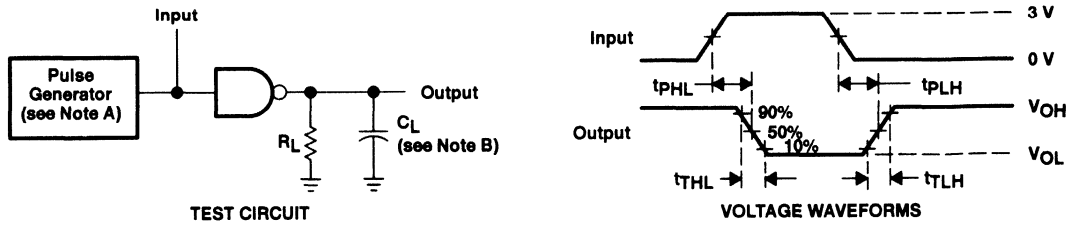
† All typical values are at T_A = 25°C.
‡ Not more than one output should be shorted at a time.
NOTE 2: The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if −10 V is a maximum, the typical value is a more negative voltage.

switching characteristics over recommended operating free-air temperature range, $V_{CC\pm}$ = ±12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output§	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 1			3	μs
t_{PHL}	Propagation delay time, high- to low-level output§				3.5	μs
t_{TLH}	Transition time, low- to high-level output¶		0.53	1	3.2	μs
t_{THL}	Transition time, high- to low-level output¶		0.53	1	3.2	μs
t_{TLH}	Transition time, low- to high-level output#	R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF, See Figure 2		1.5		μs
t_{THL}	Transition time, high- to low-level output#			1.5		μs
t_{PZH}	Output enable time to high level	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 3			50	μs
t_{PHZ}	Output disable time from high level				10	μs
t_{PZL}	Output enable time to low level	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 4			15	μs
t_{PLZ}	Output disable time from low level				10	μs
SR	Output slew rate#	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF	6	15	30	V/μs

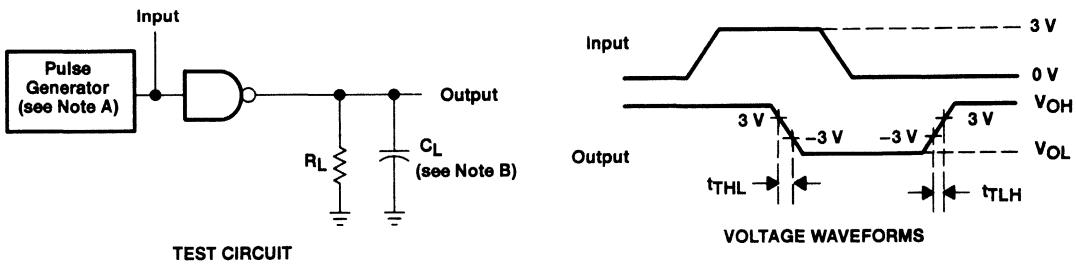
† All typical values are at T_A = 25°C.
§ t_{PHL} and t_{PLH} include the additional time due to on-chip slew rate and are measured at the 50% points.
¶ Measured between 10% and 90% points of output waveform
# Measured between 3-V and −3-V points of output waveform

PARAMETER MEASUREMENT INFORMATION



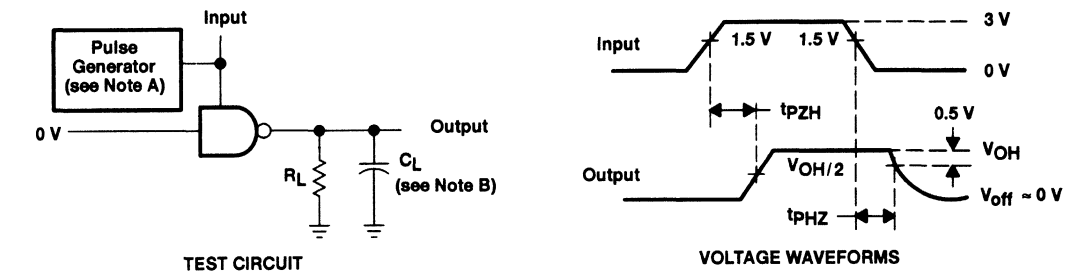
NOTES: A. The pulse generator has the following characteristics: t_w = 25 μs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f \leq 50$ ns.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms, Propagation and Transition Times



NOTES: A. The pulse generator has the following characteristics: t_w = 25 μs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f \leq 50$ ns.
B. C_L includes probe and jig capacitance.

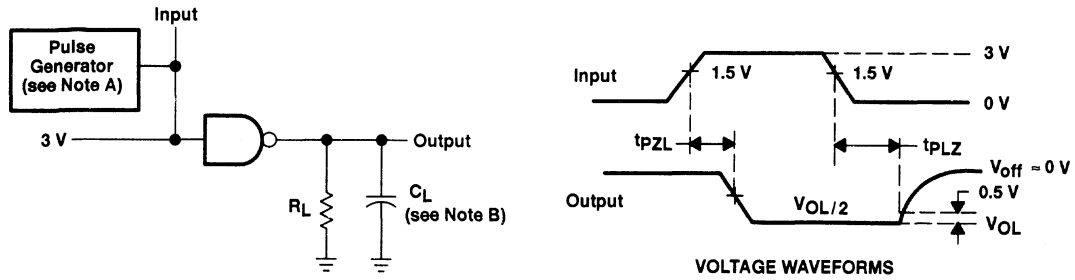
Figure 2. Test Circuit and Voltage Waveforms, Transition Times



NOTES: A. The pulse generator has the following characteristics: t_w = 25 μs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f \leq 50$ ns.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: t_w = 25 μs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f \leq 50$ ns.
B. C_L includes probe and jig capacitance.

Figure 4. Driver Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

VOLTAGE TRANSFER CHARACTERISTICS

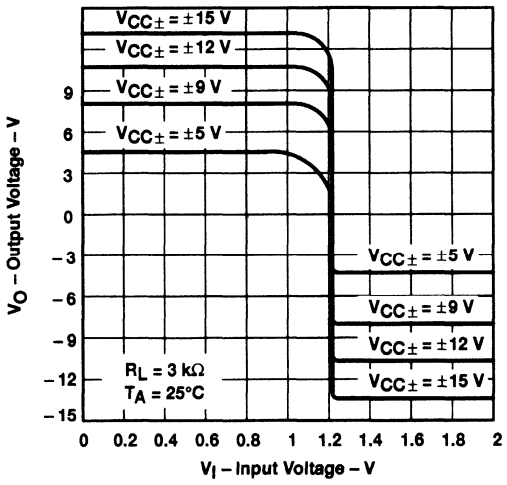


Figure 5

OUTPUT CURRENT vs OUTPUT VOLTAGE

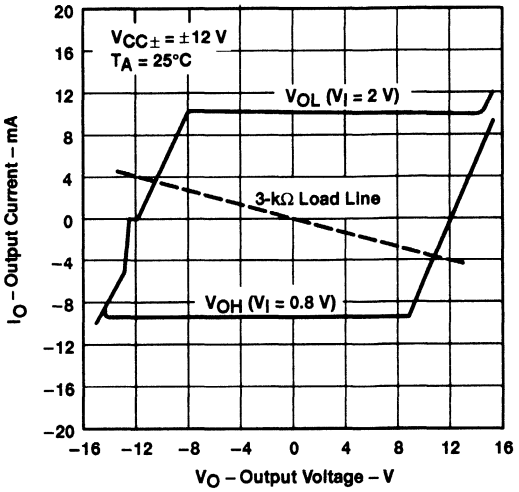


Figure 6

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE†

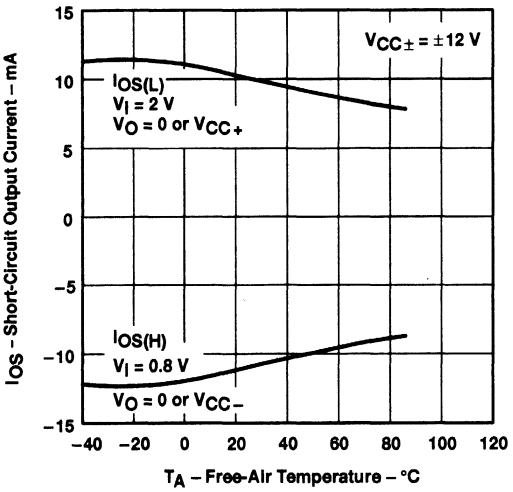


Figure 7

OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE†

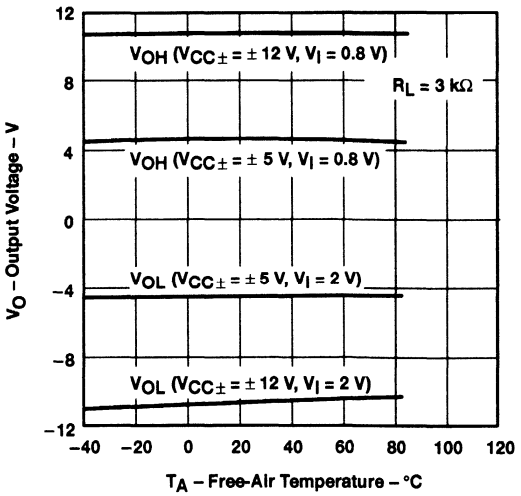


Figure 8

† Only the 0°C to 70°C portion of the curves applies to the SN75C198.

TYPICAL CHARACTERISTICS

INPUT CURRENT vs FREE-AIR TEMPERATURE†

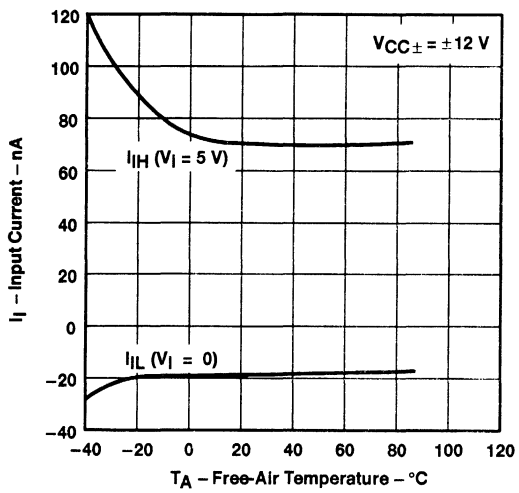


Figure 9

POWER-OFF OUTPUT RESISTANCE vs FREE-AIR TEMPERATURE†

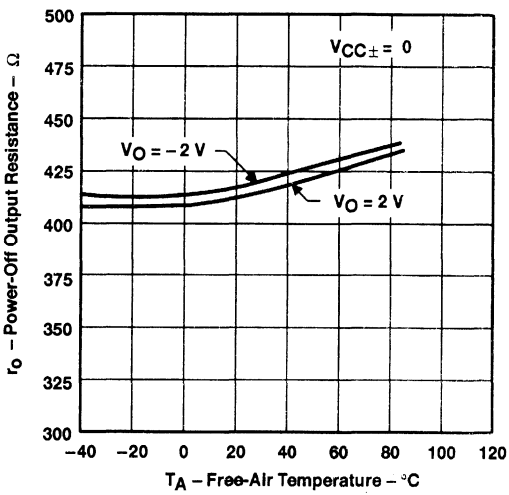


Figure 10

SUPPLY CURRENT vs FREE-AIR TEMPERATURE†

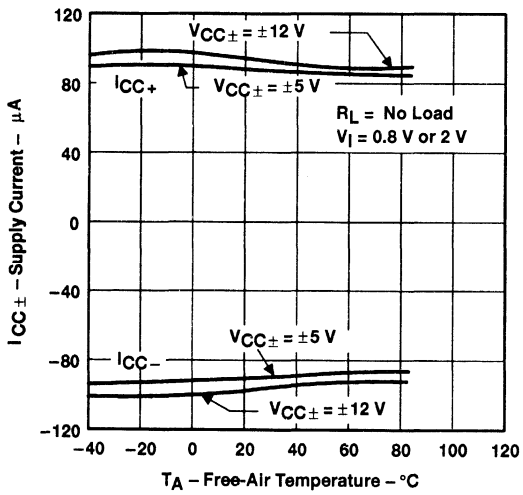


Figure 11

OUTPUT SLEW RATE vs FREE-AIR TEMPERATURE†

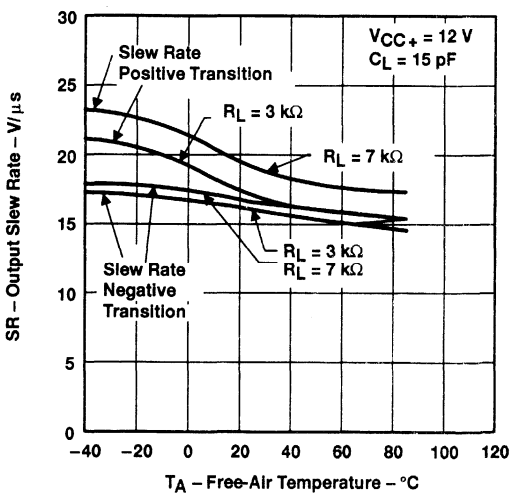


Figure 12

† Only the 0°C to 70°C portion of the curves applies to the SN75C198.

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE†

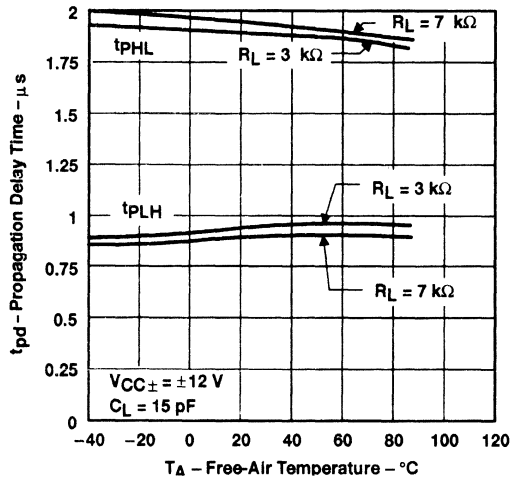


Figure 13

OUTPUT TRANSITION TIME vs FREE-AIR TEMPERATURE†

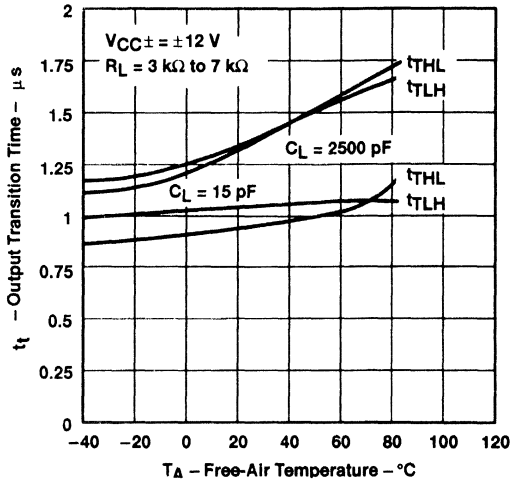


Figure 14

OUTPUT ENABLE TIME TO HIGH LEVEL vs FREE-AIR TEMPERATURE†

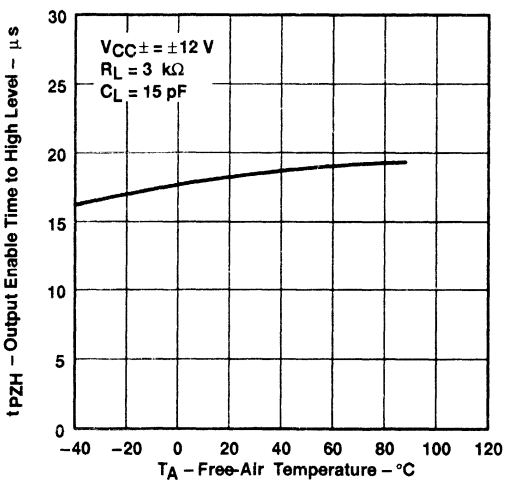


Figure 15

OUTPUT DISABLE TIME FROM HIGH LEVEL vs FREE-AIR TEMPERATURE†

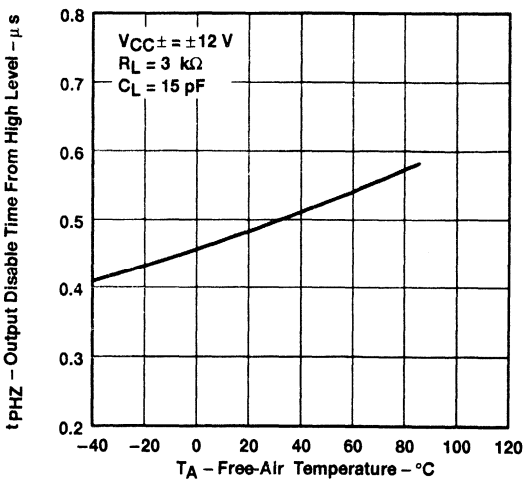


Figure 16

† Only the 0°C to 70°C portion of the curves applies to the SN75C198.

TYPICAL CHARACTERISTICS

OUTPUT ENABLE TIME TO LOW LEVEL vs FREE-AIR TEMPERATURE†

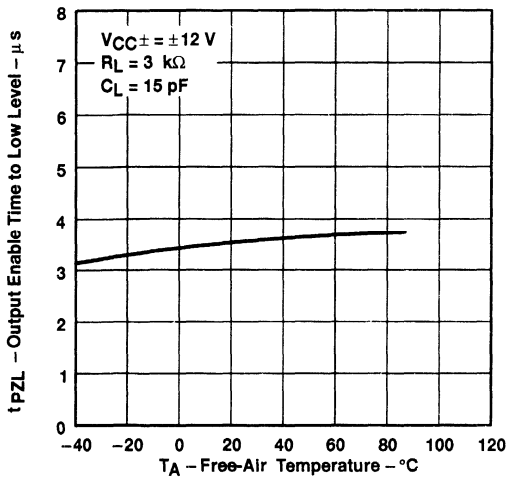


Figure 17

OUTPUT DISABLE TIME FROM LOW LEVEL vs FREE-AIR TEMPERATURE†

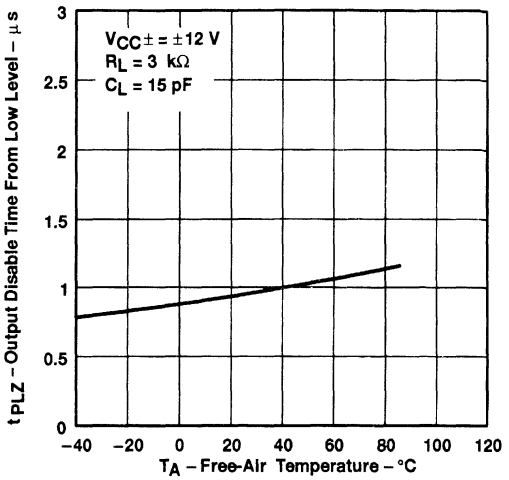


Figure 18

† Only the 0°C to 70°C portion of the curves applies to the SN75C198.

SLLS046C – JANUARY 1989 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of ITU Recommendations V.10, V.11, X.26, and X.27**
- **Designed to Operate Up To 20 Mbaud**
- **–7 V to 7 V Common-Mode Input Voltage Range With 300-mV Sensitivity**
- **3-State TTL-Compatible Outputs**
- **High Input Impedance . . . 12 kΩ Min**
- **Input Hysteresis . . . 120 mV Typ**
- **Single 5-V Supply Operation**
- **Low Supply Current Requirement 35 mA Max**
- **Improved Speed and Power Consumption Compared to MC3486**

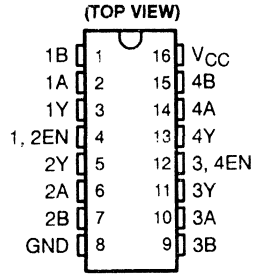
description

The SN75ALS199 is a monolithic, quadruple line receiver with 3-state outputs designed using advanced, low-power, Schottky technology. This technology provides combined improvements in bar design, tooling production, and wafer fabrication, providing significantly less power consumption and permitting much higher data throughput than other designs. The device meets the specification of ITU Recommendations V.10, V.11, X.26, and X.27.

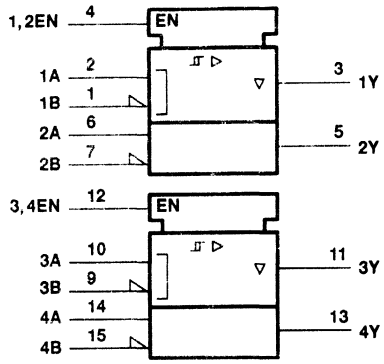
The SN75ALS199 features 3-state outputs that permit direct connection to a bus-organized system with a fail-safe design that ensures the ouptuts will always be high if the inputs are open. The device is optimized for balanced multipoint bus transmission at rates up to 20 megabits per second. The input features high-input impedance, input hysteresis for increased noise immunity, and an input sensitivity of ±300 mV over a common-mode input voltage range of ±7 V. It also features an active-high enable function for each of two receiver pairs. The SN75ALS199 is designed for optimum performance when used with the SN75ALS194 quadruple, differential line driver.

The SN75ALS199 is characterized for operation from 0°C to 70°C.

D OR N PACKAGE
(TOP VIEW)

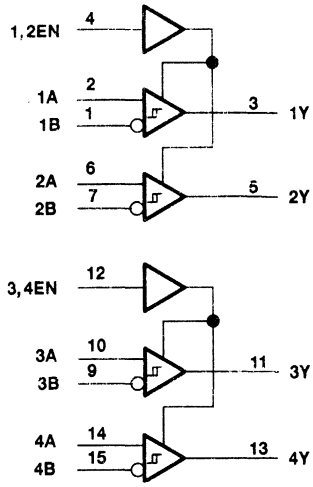


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram

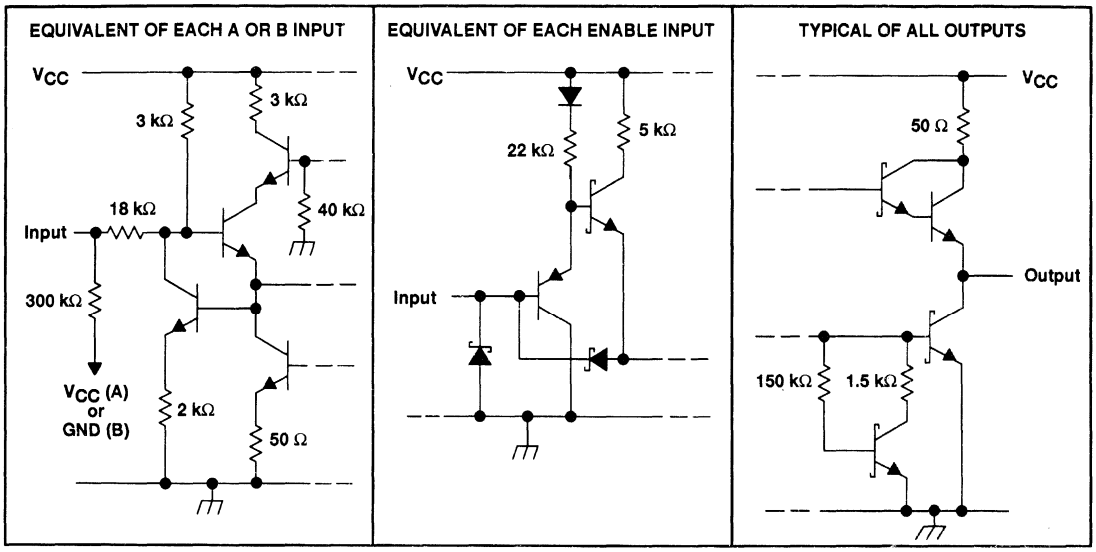


FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A–B	EN	OUTPUT Y
$V_{ID} \geq 0.3$ V	H	H
-0.3 V $< V_{ID} < 0.3$ V	H	?
$V_{ID} \leq -0.3$ V	H	L
X	L	Z
Open	H	H

H = high level, L = low level, X = irrelevant,
? = indeterminate, Z = high impedance (off)

schematics of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I (A or B inputs) ..... ±15 V
Differential input voltage, V_{ID} (see Note 2) ..... ±15 V
Enable input voltage, V_I ..... 7 V
Low-level output current, I_{OL} ..... 50 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Differential input voltage, V_{ID}			±12	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			– 400	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage					300	mV
V_{IT-}	Negative-going input threshold voltage			−300‡			mV
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)				120		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 300 mV,	I_{OH} = −400 µA	2.7	3.6		V
V_{OL}	Low-level output voltage	V_{ID} = −300 mV	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	V_{IL} = 0.8 V, V_{ID} = −3 V,	V_O = 2.7 V			20	µA
		V_{IL} = 0.8 V, V_{ID} = 3 V,	V_O = 0.5 V			−20	
I_I	Line input current	Other input at 0 V, See Note 3	V_I = 15 V		0.7	1.2	mA
			V_I = −15 V		−1	−1.7	
I_{IH}	High-level enable-input current		V_{IH} = 2.7 V			20	µA
			V_{IH} = 5.25 V			100	
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	µA
	Input resistance			12	18		kΩ
I_{OS}	Short-circuit output current§	V_{ID} = 3 V,	V_O = 0	−15	−78	−130	mA
I_{CC}	Supply current	Outputs disabled			22	35	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 3: Refer to ITU Recommendations V.10 and V.11 for exact conditions.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_{ID} = 0 V to 3 V, See Figure 2	C_L = 15 pF,		15	22	ns
t_{PHL}	Propagation delay time, high- to low-level output				15	22	
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 3		13	25	ns
t_{PZL}	Output enable time to low level				11	25	
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 3		13	25	ns
t_{PLZ}	Output disable time from low level				15	22	

PARAMETER MEASUREMENT INFORMATION

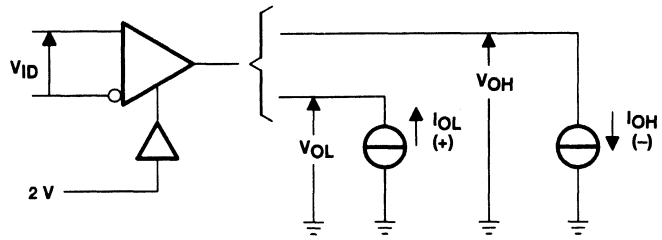
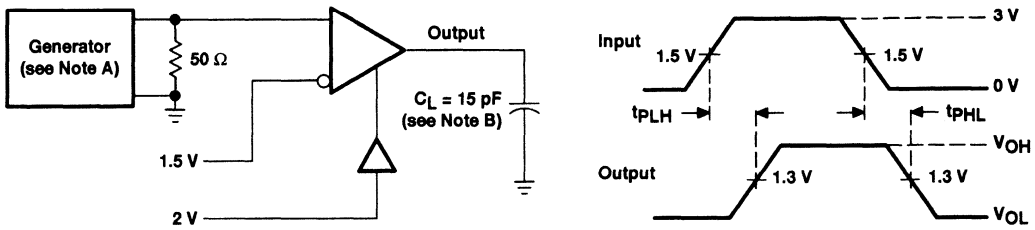


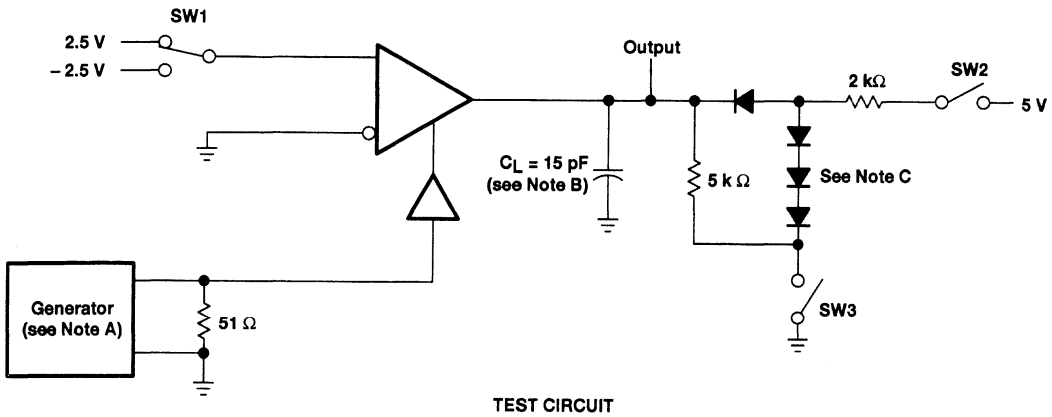
Figure 1. V_{OH} and V_{OL} Test Circuit



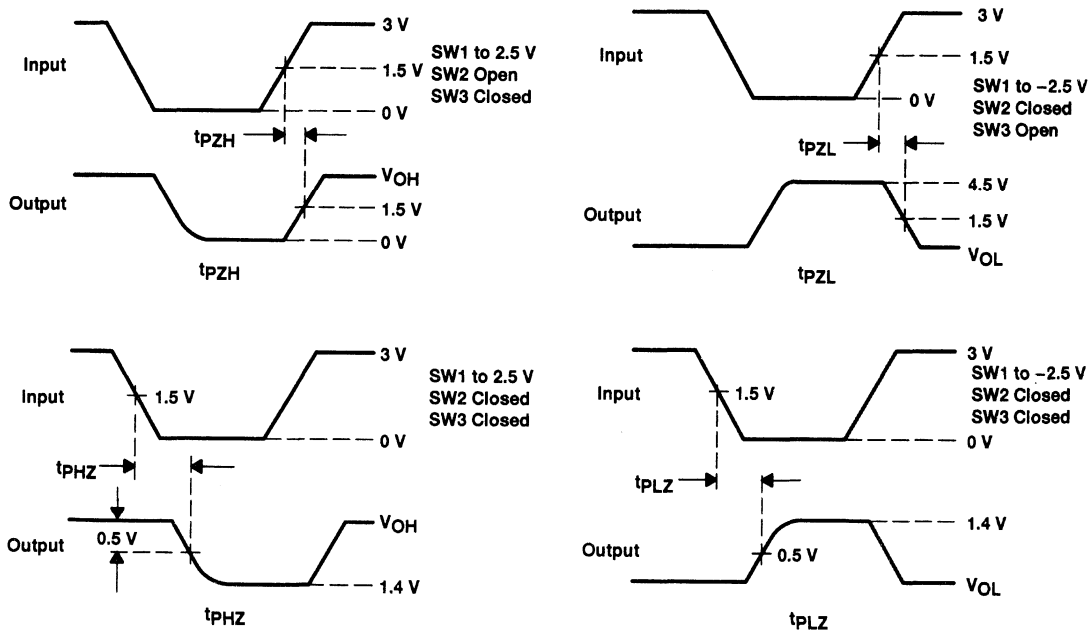
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

Figure 3. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

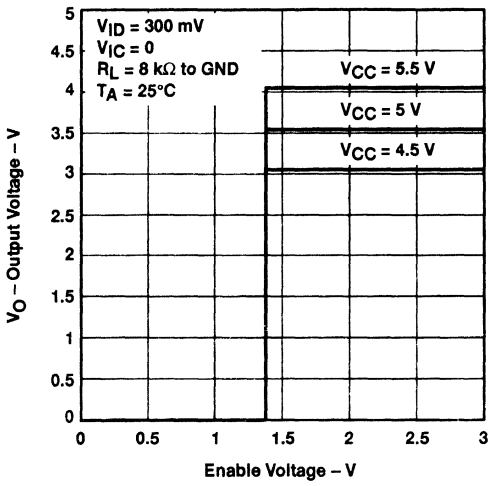


Figure 4

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

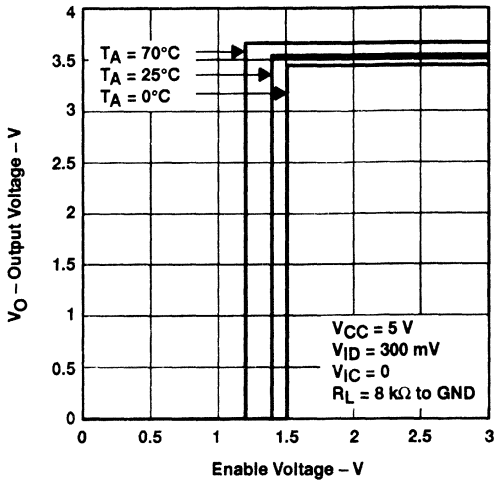


Figure 5

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

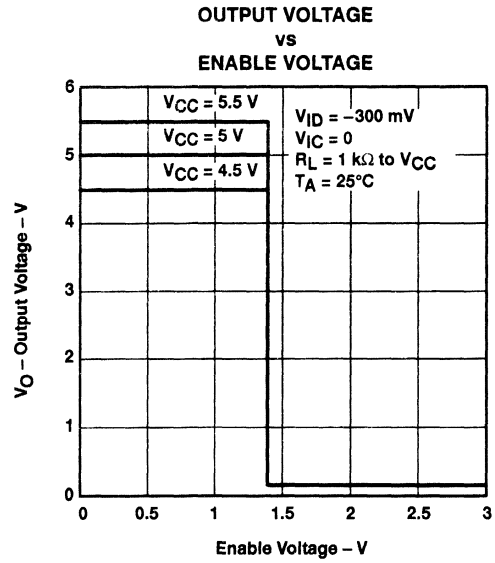


Figure 6

OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

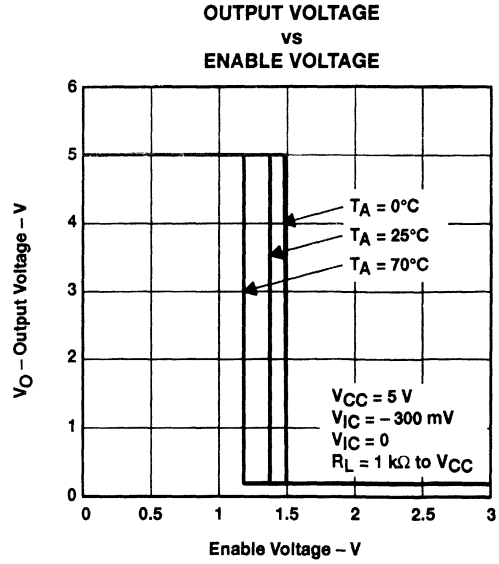


Figure 7

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

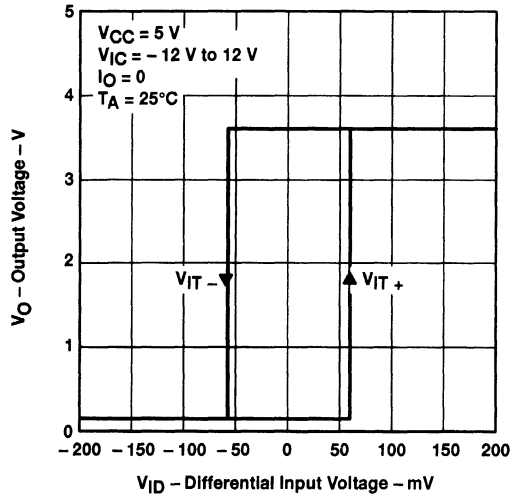


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

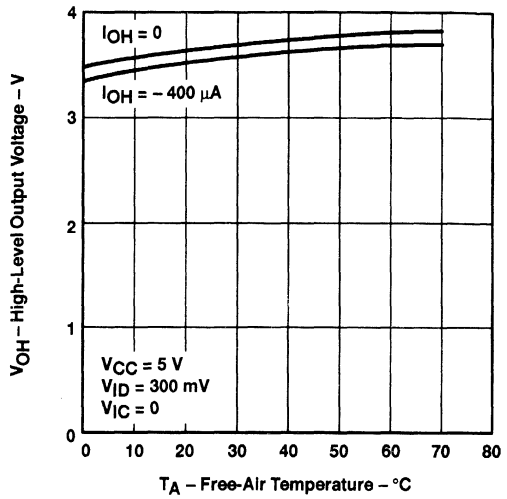


Figure 9

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

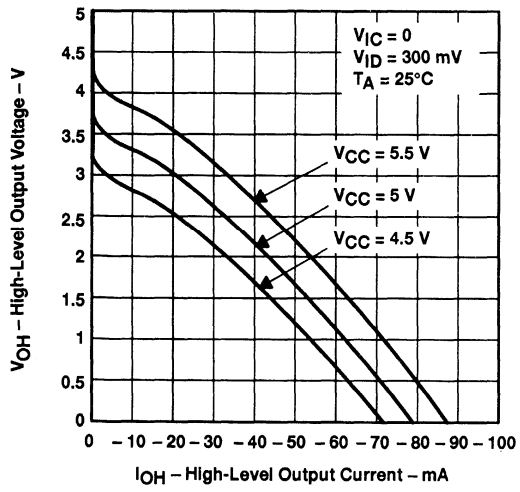


Figure 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

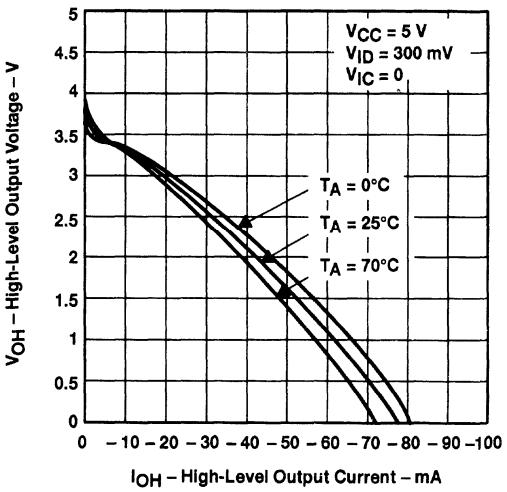


Figure 11

TYPICAL CHARACTERISTICS

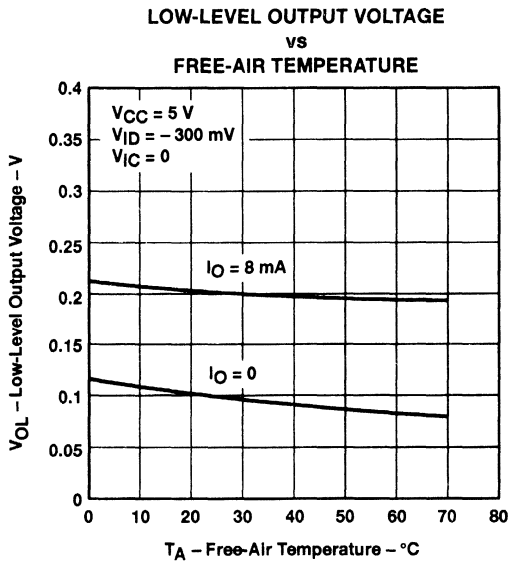


Figure 12

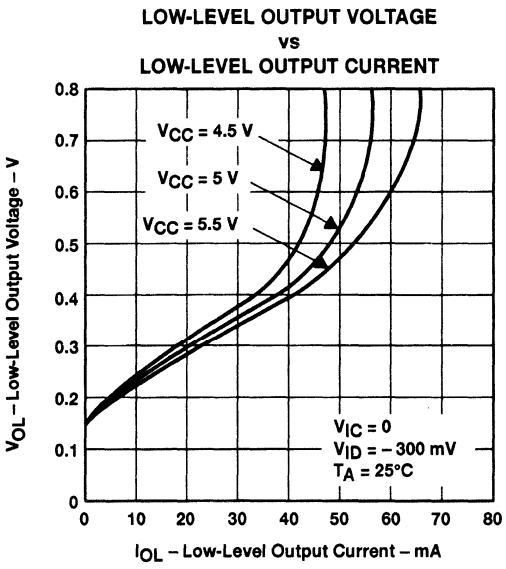


Figure 13

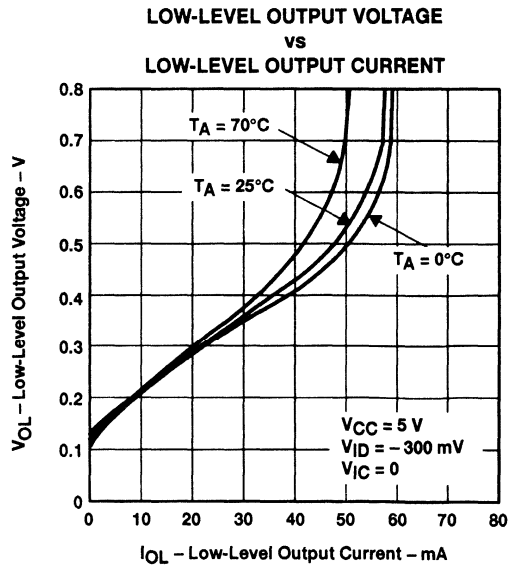


Figure 14

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

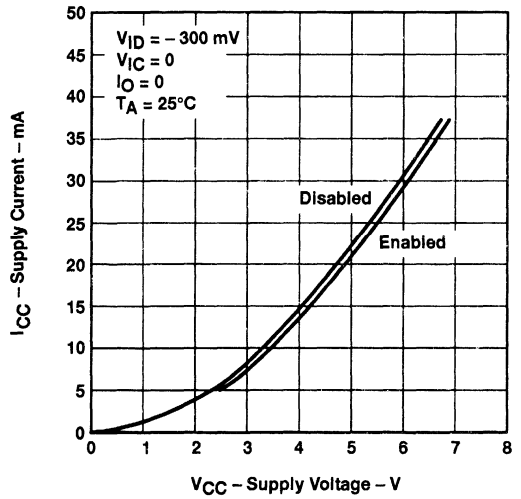


Figure 15

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

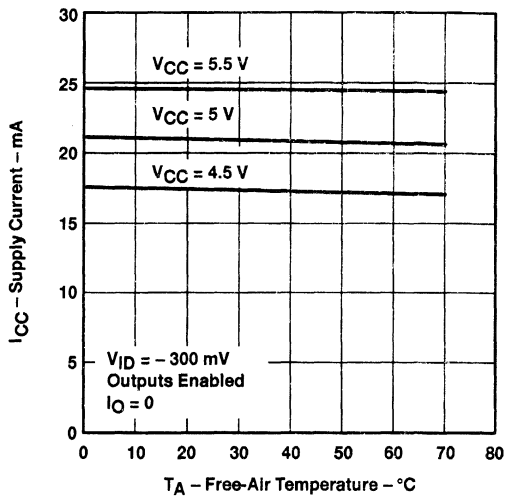


Figure 16

SUPPLY CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

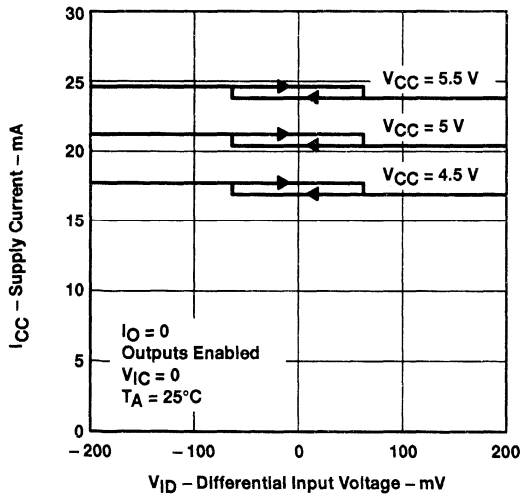


Figure 17

SUPPLY CURRENT
vs
FREQUENCY

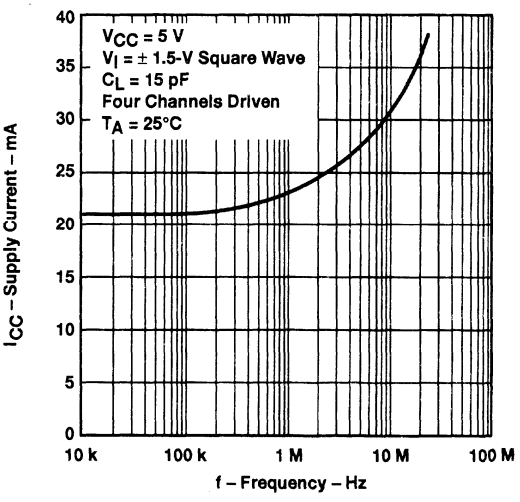


Figure 18

TYPICAL CHARACTERISTICS

INPUT RESISTANCE vs FREE-AIR TEMPERATURE

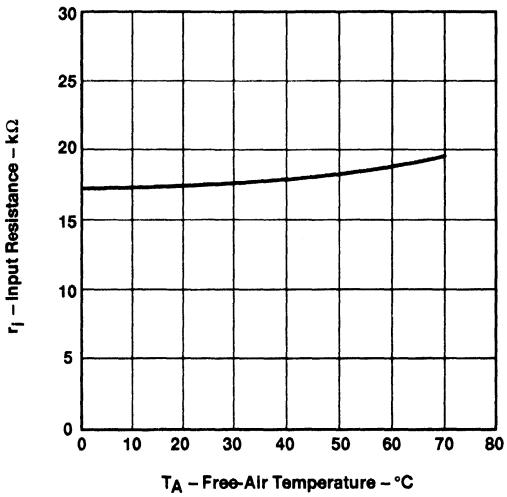


Figure 19

INPUT CURRENT vs INPUT VOLTAGE TO GND

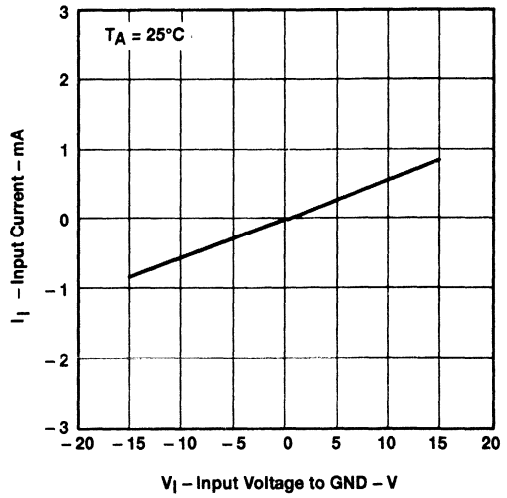


Figure 20

SWITCHING TIME vs FREE-AIR TEMPERATURE

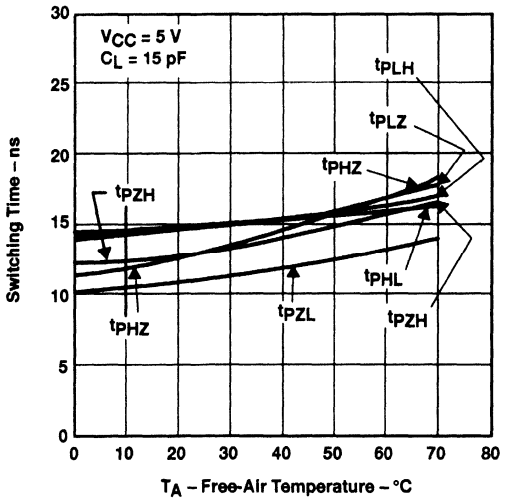


Figure 21

PROPAGATION DELAY TIME vs SUPPLY VOLTAGE

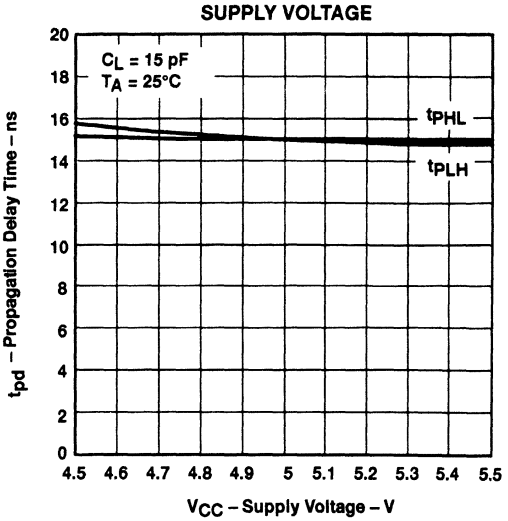


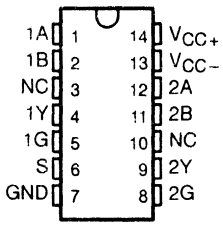
Figure 22

SN75207, SN75207B
DUAL SENSE AMPLIFIER FOR MOS MEMORIES OR DUAL HIGH-SENSITIVITY LINE RECEIVERS

SLLS096B – JULY 1973 – REVISED MAY 1995

- **Plug-In Replacement for SN75107A and SN75107B With Improved Characteristics**
- **±10-mV Input Sensitivity**
- **TTL-Compatible Circuitry**
- **Standard Supply Voltages . . . ±5 V**
- **Differential Input Common-Mode Voltage Range of ±3 V**
- **Strobe Inputs for Channel Selection**
- **Totem-Pole Outputs**
- **SN75207B Has Diode-Protected Input Stage for Power-Off Condition**
- **Sense Amplifier for MOS Memories**
- **Dual Comparator**
- **High-Sensitivity Line Receiver**

D OR N PACKAGE
(TOP VIEW)



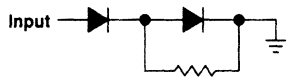
NC – No internal connection

THE SN75207 IS NOT RECOMMENDED FOR NEW DESIGNS.

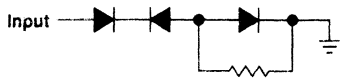
description

The SN75207 and SN75207B are terminal-for-terminal replacements for the SN75107A and SN75107B, respectively. The improved input sensitivity makes them more suitable for MOS memory sense amplifiers and can result in faster memory cycles. Improved sensitivity also makes them more useful in line-receiver applications by allowing use of longer transmission line lengths. The '207 and '207B each features a TTL-compatible, active-pullup output.

The essential difference between the SN75207 and SN75207B can be seen in the schematics. Input protection diodes are in series with the collectors of the differential-input transistors of the SN75207B. These diodes are useful in certain party-line systems that may have multiple V_{CC+} power supplies and may be operated with some of the V_{CC+} supplies turned off. In such a system, if a supply is turned off and allowed to go to ground, the equivalent input circuit connected to that supply would be as follows:



SN75207



SN75207B

This would be a problem in specific systems that might have the transmission lines biased to some potential greater than 1.4 V.

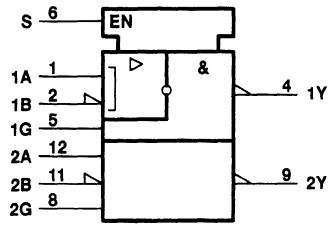
These devices are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

DIFFERENTIAL INPUTS A-B	STROBES G	STROBES S	OUTPUT Y
$V_{ID} \geq 10$ mV	X	X	H
-10 mV $< V_{ID} < 10$ mV	X	L	H
	L	X	H
	H	H	Indeterminate
$V_{ID} \leq -10$ mV	X	L	H
	L	X	H
	H	H	L

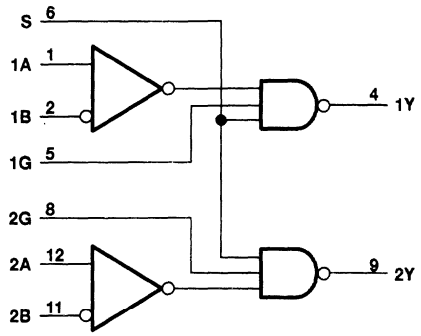
H = high level, L = low level, X = irrelevant

logic symbol†

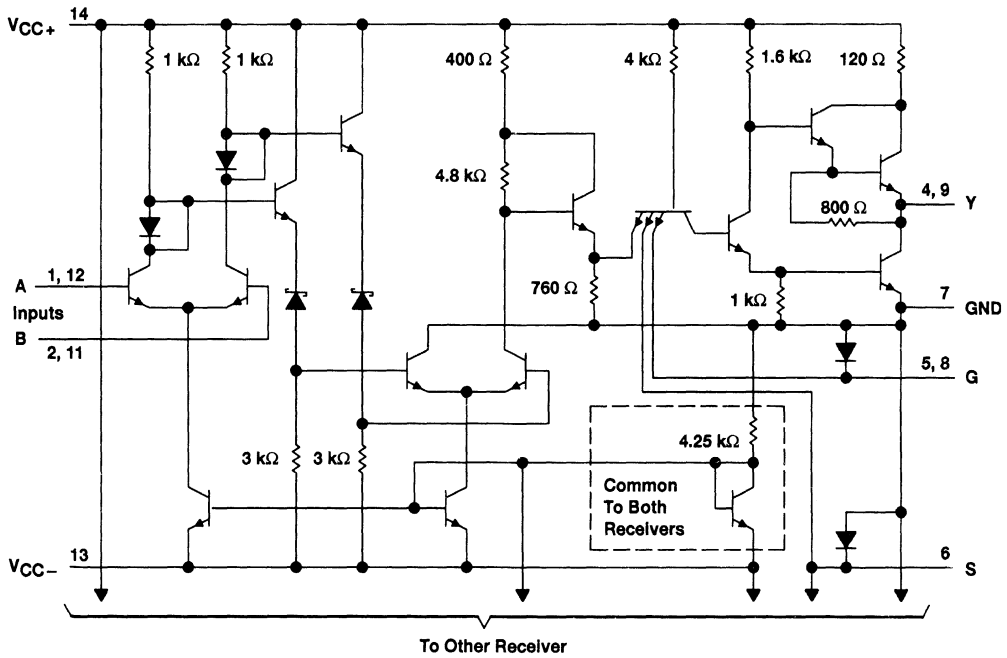


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic (each receiver)



Resistor values shown are normal.

design characteristics

The '207 and '207B line receivers/sense amplifiers are TTL-compatible, dual circuits intended for use in high-speed, data-transmission systems or MOS memory systems. They are designed to detect low-level differential signals in the presence of common-mode noise and variations of temperature and supplies. The dc specifications reflect worst-case conditions of temperature, supply voltages, and input voltages.

The input common-mode voltage range is ±3 V. This is adequate for application in most systems. In systems with requirements for greater common-mode voltage range, input attenuators may be used to decrease the noise to an acceptable level at the receiver-input terminals.

The circuits feature individual strobe inputs for each channel and a strobe input common to both channels for logic versatility. The strobe inputs are tested to ensure 400 mV of dc noise margin when interfaced with Series 54/74 TTL.

The circuits feature high input impedance and low input currents, which induce very little loading on the transmission line. This makes these devices especially useful in party-line systems. The excellent input sensitivity (3 mV typical) is particularly important when data is to be detected at the end of a long transmission line and the amplitude of the data has deteriorated due to cable losses. The circuits are designed to detect input signals of 10-mV (or greater) amplitude and convert the polarity of the signal into appropriate TTL-compatible output logic levels.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1) ..... 7 V
Supply voltage, V_{CC-} (see Note 1) ..... −7 V
Differential input voltage, V_{ID} (see Note 2) ..... ±6 V
Common-mode input voltage, V_{IC} (see Note 3) ..... ±5 V
Strobe input voltage ..... 5.5 V
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to GND terminal.
2. Differential input voltage values are at the noninverting (A) terminal with respect to the inverting (B) terminal.
3. Common-mode input voltage is the average of the voltages at the A and B inputs.

DISSIPATION RATING TABLE

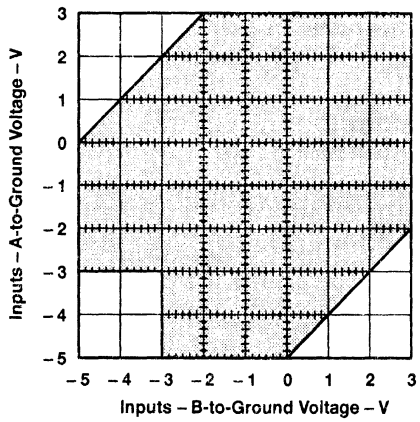
PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1050 mW	9.2 mW/°C	636 mW

recommended operating conditions (see Note 4)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	4.75	5	5.25	V
Supply voltage, V_{CC-}	−4.75	−5	−5.25	V
High-level differential input voltage, $V_{ID(H)}$ (see Note 5)	0.01		5	V
Low-level differential input voltage, $V_{ID(L)}$	−5†		−0.01	V
Common-mode input voltage, V_{IC} (see Notes 5 and 6)	−3†		3	V
Input voltage, any differential input to ground (see Note 5)	−5†		3	V
High-level input voltage at strobe inputs, $V_{IH(S)}$	2		5.5	V
Low-level input voltage at strobe inputs, $V_{IL(S)}$	0		0.8	V
Low-level output current, I_{OL}			−16	mA
Operating free-air temperature, T_A	0		70	°C

† The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

NOTES: 4. When using only one channel of the line receiver, the strobe G of the unused channel should be grounded and at least one of the differential inputs of the unused receiver should be terminated at some voltage between −3 V and 3 V.
5. The recommended combinations of input voltages fall within the shaded area of the figure shown.
6. The common-mode voltage may be as low as −4 V provided that the more positive of the two inputs is not more negative than −3 V.



electrical characteristics over recommended free-air temperature range (unless otherwise noted)

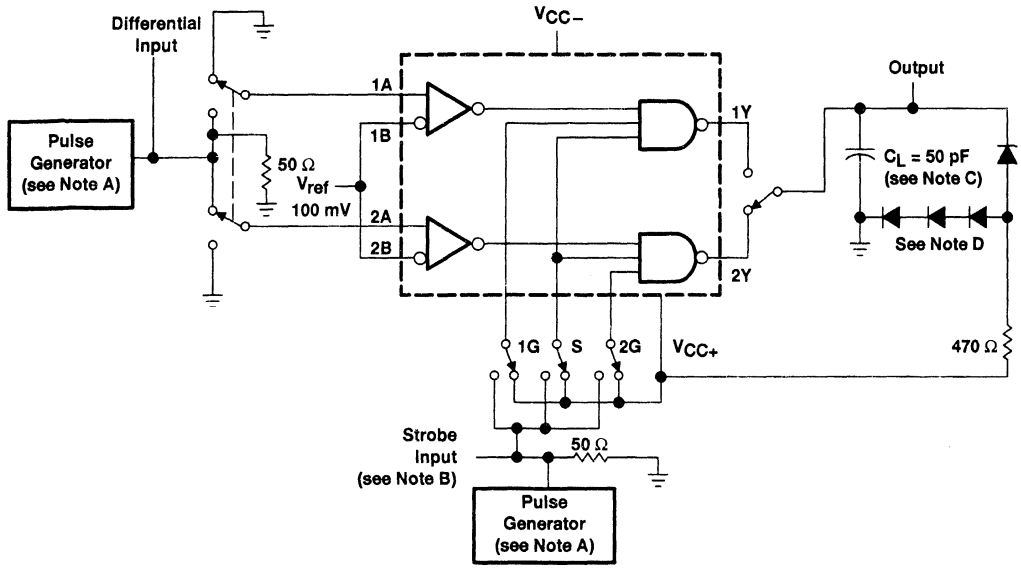
PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
I_{IH}	High-level input current	'207	$V_{CC\pm}$ = ±5.25 V		V_{ID} = 5 V		30	75	µA
		'207B			V_{ID} = −5 V		30	75	
I_{IL}	Low-level input current	'207	$V_{CC\pm}$ = ±5.25 V		V_{ID} = −5 V			−10	µA
		'207B			V_{ID} = 5 V			−10	
I_{IH}	High-level input current into 1G or 2G		$V_{CC\pm}$ = ±5.25 V,	$V_{IH(S)}$ = 2.4 V				40	µA
			$V_{CC\pm}$ = ±5.25 V,	$V_{IH(S)}$ = ±5.25 V				1	mA
I_{IL}	Low-level input current into 1G or 2G		$V_{CC\pm}$ = ±5.25 V,	$V_{IL(S)}$ = 0.4 V				−1.6	mA
I_{IH}	High-level input current into S		$V_{CC\pm}$ = ±5.25 V,	$V_{IH(S)}$ = 2.4 V				80	µA
			$V_{CC\pm}$ = ±5.25 V,	$V_{IH(S)}$ = ±5.25 V				2	mA
I_{IL}	Low-level input current into S		$V_{CC\pm}$ = ±5.25 V,	$V_{IL(S)}$ = 0.4 V				−3.2	mA
V_{OH}	High-level output voltage		$V_{CC\pm}$ = ±4.75 V, I_{OH} = −400 µA,	$V_{IL(S)}$ = 0.8 V, V_{IC} = −3 V to 3 V	$V_{ID(H)}$ = 10 mV,	2.4			V
V_{OL}	Low-level output voltage		$V_{CC\pm}$ = ±4.75 V, I_{OL} = 16 mA,	$V_{IH(S)}$ = 2 V, V_{IC} = −3 V to 3 V	$V_{ID(L)}$ = −10 mV,			0.4	V
I_{OH}	High-level output current		$V_{CC\pm}$ = ±4.75 V,	V_{OH} = ±5.25 V				400	µA
I_{OS}	Short-circuit output current‡		$V_{CC\pm}$ = ±5.25 V			−18		−70	mA
I_{CC+}	Supply current from V_{CC+}		$V_{CC\pm}$ = ±5.25 V,	T_A = 25°C,	Outputs high		18	30	mA
I_{CC-}	Supply current from V_{CC-}		$V_{CC\pm}$ = ±5.25 V,	T_A = 25°C,	Outputs high		−8.4	−15	mA

† All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time.

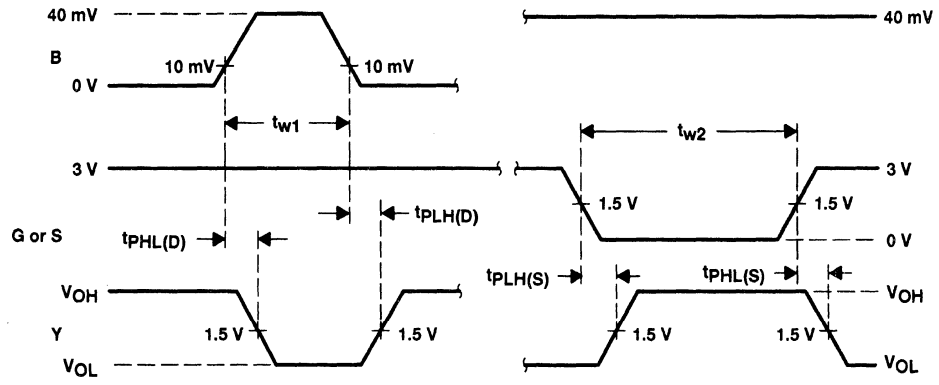
switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{PLH(D)}$	Propagation delay time, low- to high-level output, from differential inputs A and B	R_L = 470 Ω, C_L = 50 pF, See Figure 1		35	ns
$t_{PHL(D)}$	Propagation delay time, high- to low-level output, from differential inputs A and B			20	ns
$t_{PLH(S)}$	Propagation delay time, low- to high-level output, from strobe input G or S			17	ns
$t_{PHL(S)}$	Propagation delay time, high- to low-level output, from strobe input G or S			17	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: $Z_O = 50\ \Omega$, $t_r \leq 5$ ns, $t_f \leq 5$ ns, $t_{w1} = 500$ ns with PRR = 1 MHz, $t_{w2} = 1\ \mu s$ with PRR = 500 kHz.
B. Strobe input pulse is applied to Strobe 1G when inputs 1A-1B are being tested, to Strobe S when inputs 1A-1B or 2A-2B are being tested, and to Strobe 2G when inputs 2A-2B are being tested.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N916.

Figure 1. Test Circuit and Voltage Waveforms

APPLICATION INFORMATION

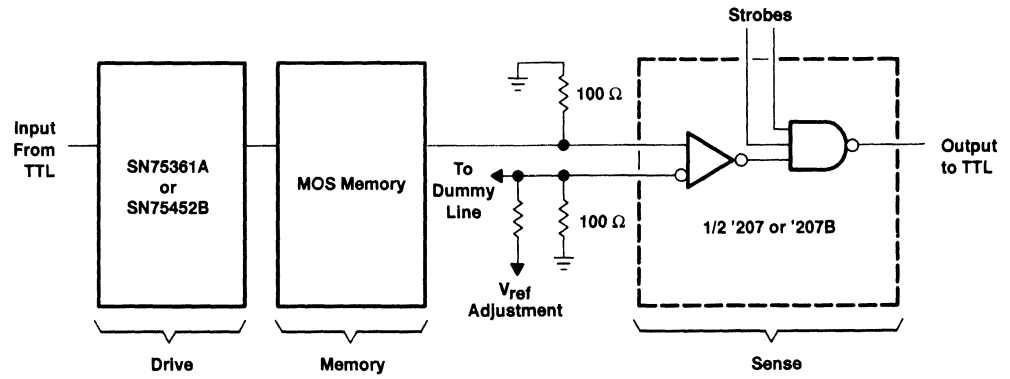
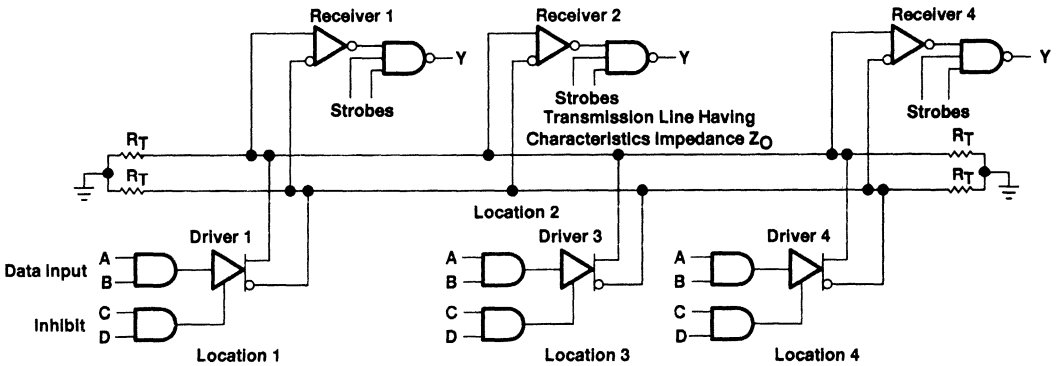


Figure 2. Mos Memory Sense Amplifier



Receivers are '207 or '207B; drivers are SN55109A, SN75109A, SN55110A, SN75110A, or SN75112.

Figure 3. Data-Bus or Parity-Line System

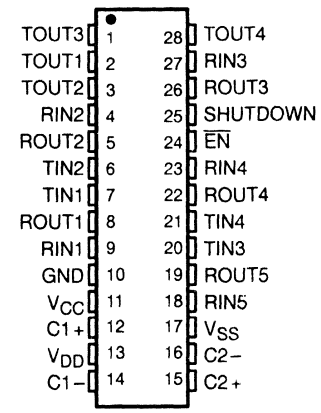
PRECAUTIONS: When only one receiver in a package is being used, at least one of the differential inputs of the unused receiver should be terminated at some voltage between –3 V and 3 V, preferably at GND. Failure to do so will cause improper operation of the unit being used because of common bias circuitry for the current sources of the two receivers. Strobe G of the unused channel should be grounded.

LOW-POWER LinBiCMOS™ MULTIPLE DRIVERS AND RECEIVERS

SLLS137D – MAY 1992 – REVISED MAY 1995

- **Operates With Single 5-V Power Supply**
- **Meets or Exceeds the Requirements of ANSI Standard EIA/TIA-232-E and ITU Recommendation V.28**
- **Improved Performance Replacement for MAX241**
- **Operate at Data Rates Up to 100 kbs Over a 3-Meter Cable**
- **Low-Power Shutdown Mode: ≤1 μA Typ**
- **LinBiCMOS™ Process Technology**
- **Four Drivers and Five Receivers**
- **±30-V Input Levels**
- **3-State TTL/CMOS Receiver Outputs**
- **±9-V Output Swing With a 5-V Supply**
- **Applications**
  - **EIA/TIA-232-E Interface**
  - **Battery-Powered Systems**
  - **Terminals**
  - **Modems**
  - **Computers**

DW PACKAGE
(TOP VIEW)



description

The SN75LBC241† is a low-power LinBiCMOS™ line interface device containing four independent drivers and five receivers. It is designed to provide a plug-in replacement for the Maxim MAX241. The SN75LBC241 provides a capacitive charge-pump voltage generator to produce EIA/TIA-232 voltage levels from a 5-V supply. The charge-pump oscillator frequency is 20 kHz. Each receiver converts EIA/TIA-232 inputs to 5-V TTL/CMOS levels. The receivers have a typical threshold of 1.2 V and a typical hysteresis of 0.5 V, and can accept ±30-V inputs. Each driver converts TTL/CMOS input levels into EIA/TIA-232 levels.

The SN75LBC241 includes a receiver, 3-state control line and a low-power shutdown control line. Whenever the $\overline{EN}$ line is high, the receiver outputs are placed in a high-impedance state. When $\overline{EN}$ is low, normal operation is enabled.

The shutdown mode reduces power dissipation to less than 5 μW typically. In this mode, receiver outputs have high impedance, driver outputs are turned off, and the charge-pump circuit is turned off. When SHUTDOWN is high, the shutdown mode is enabled. When SHUTDOWN is low, normal operation is enabled.

This device has been designed to conform to ANSI Standard EIA/TIA-232-E and ITU Recommendation V.28 specifications.

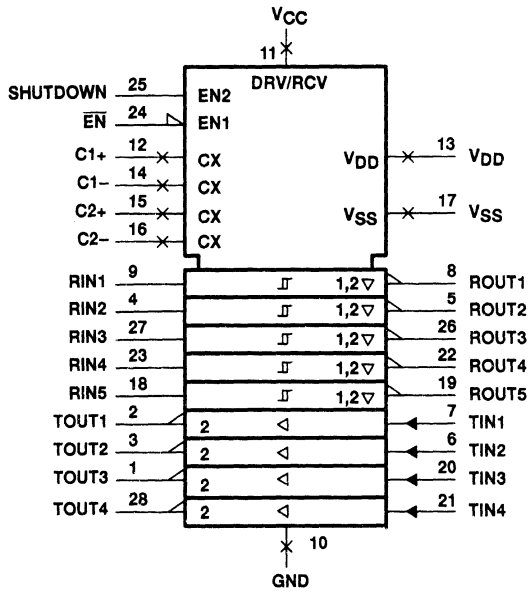
The SN75LBC241 has been designed using LinBiCMOS™ technology and cells contained in the TI's LinASIC™ library. Use of LinBiCMOS™ circuitry increases latch-up immunity in this device over an all-CMOS design.

The SN75LBC241 is characterized for operation from 0°C to 70°C.

† Patent pending

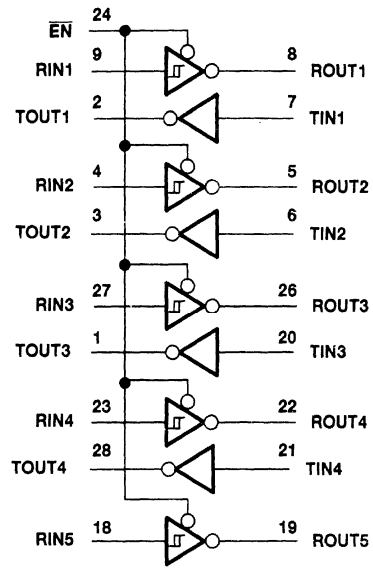
LinBiCMOS and LinASIC are trademarks of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input supply voltage range, V_{CC} (see Note 1) ..... −0.3 V to 6 V
Positive output supply voltage range, V_{DD} ..... V_{CC} − 0.3 V to 15 V
Negative output supply voltage range, V_{SS} ..... 0.3 V to −15 V
Input voltage range, V_I: Driver ..... −0.3 V to V_{CC} + 0.3 V
Receiver ..... ±30 V
Output voltage range, V_O: TOUT ..... V_{SS} − 0.3 V to V_{DD} + 0.3 V
ROUT ..... −0.3 V to V_{CC} + 0.3 V
Short-circuit duration: TOUT ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1348 mW	10.8 mW/°C	862 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level input voltage, V_{IH}	TIN	2			V
	$\overline{EN}$, SHUTDOWN	2.4			
Low-level input voltage, V_{IL}	TIN, $\overline{EN}$, SHUTDOWN			0.8	V
External charge-pump capacitor	C1 – C4 (see Figure 1)	1			μF
External charge-pump capacitor voltage rating	C1, C3 (see Figure 1)	6.3			V
	C2, C4 (see Figure 1)	16			
Receiver input voltage, V_I				±30	V
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	TOUT	R_L = 3 kΩ to GND,	See Note 2	5	9		V
		ROUT	I_{OH} = –1 mA		3.5			
V_{OL}	Low-level output voltage	TOUT	R_L = 3 kΩ to GND,	See Note 3		–9‡	–5	V
		ROUT	I_{OL} = 3.2 mA				0.4	
V_{IT+}	Receiver positive-going input threshold voltage	RIN	V_{CC} = 5 V,	T_A = 25°C		1.7	2.4	V
V_{IT-}	Receiver negative-going input threshold voltage	RIN	V_{CC} = 5 V,	T_A = 25°C	0.8	1.2		V
V_{hys}	Input hysteresis voltage ($V_{IT+} - V_{IT-}$)	RIN	V_{CC} = 5 V			0.5	1	V
r_i	Receiver input resistance	RIN	V_{CC} = 5 V,	T_A = 25°C	3	5	7	kΩ
r_o	Output resistance	TOUT	$V_{DD} = V_{SS} = V_{CC}$ = 0,	V_O = ±2 V	300			Ω
I_{OS}	Short circuit output current§	TOUT	V_{CC} = 5.5 V,	V_O = 0		±10		mA
I_{IS}	Short circuit input current	TIN	V_I = 0				200	μA
I_{CC}	Supply current		V_{CC} = 5.5 V, All output open	T_A = 25°C,		4	8	mA
			All outputs open, Shutdown terminal high	T_A = 25°C,		1	10	μA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.
§ Not more than one output should be shorted at one time.
NOTES: 2. Total I_{OH} drawn from TOUT1, TOUT2, TOUT3, TOUT4 and V_{DD} terminal should not exceed 12 mA.
3. Total I_{OL} drawn from TOUT1, TOUT2, TOUT3, TOUT4 and V_{SS} terminal should not exceed – 12 mA.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{PLH(R)}$	Receiver propagation delay time, low- to high-level output	See Figure 2			500		ns
$t_{PHL(R)}$	Receiver propagation delay time, high- to low-level output	See Figure 2			500		ns
t_{PZH}	Receiver output enable time to high level	See Figure 5			100		ns
t_{PZL}	Receiver output enable time to low level	See Figure 5			100		ns
t_{PHZ}	Receiver output disable time from high level	See Figure 5			50		ns
t_{PLZ}	Receiver output disable time from low level	See Figure 5			50		ns
SR	Driver slew rate	R_L = 3 kΩ to 7 kΩ,	See Figure 4			30	V/μs
$SR_{(tr)}$	Driver transition region slew rate	C_L = 2500 pF,	See Figure 4	4	6		V/μs

APPLICATION INFORMATION

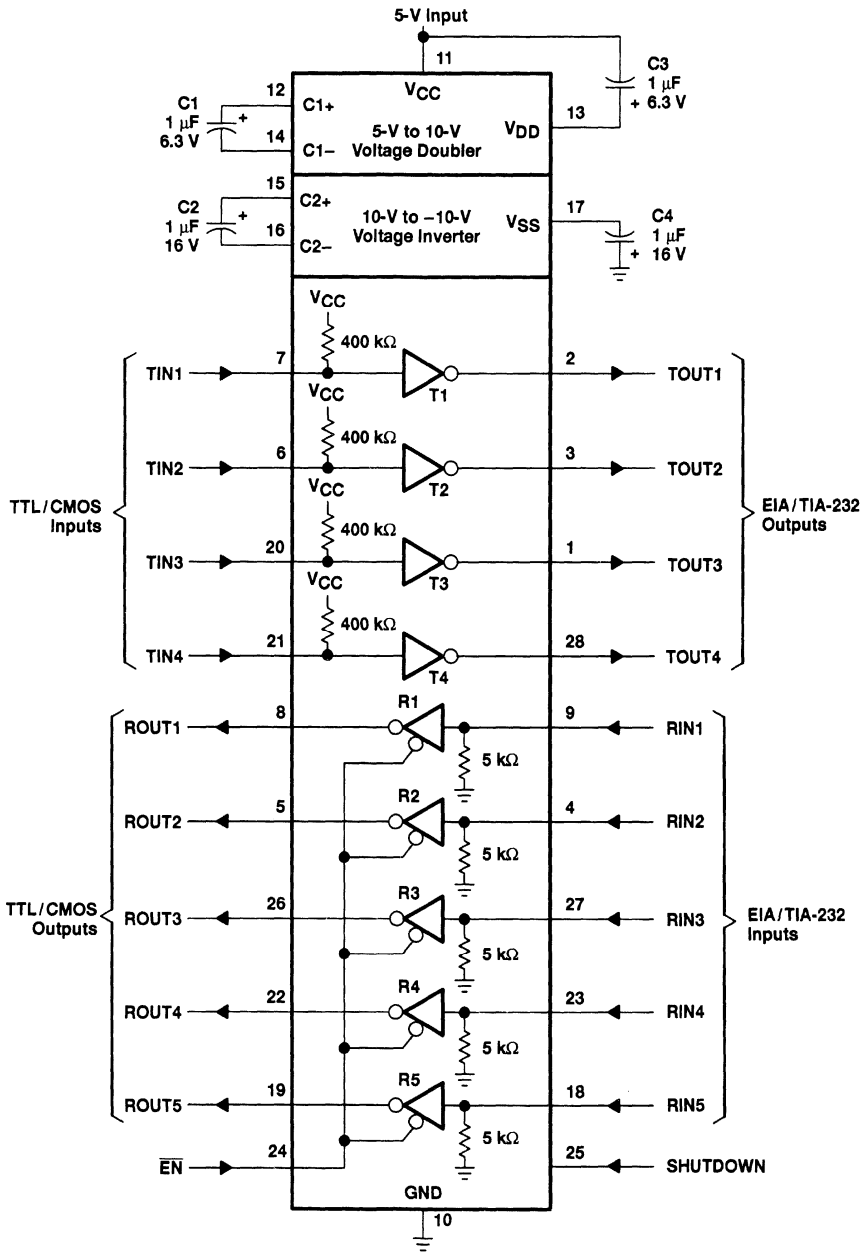


Figure 1. Typical Operating Circuit

PARAMETER MEASUREMENT INFORMATION

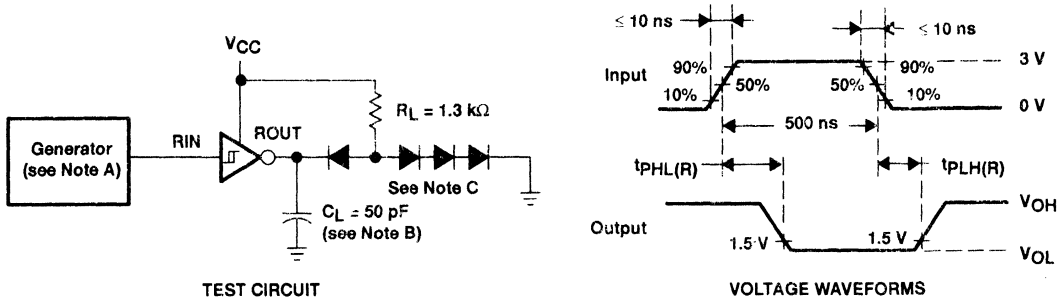


Figure 2. Receiver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurement

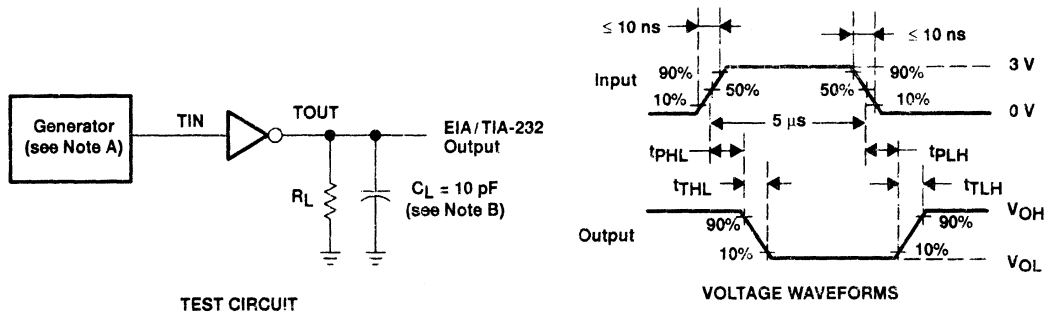
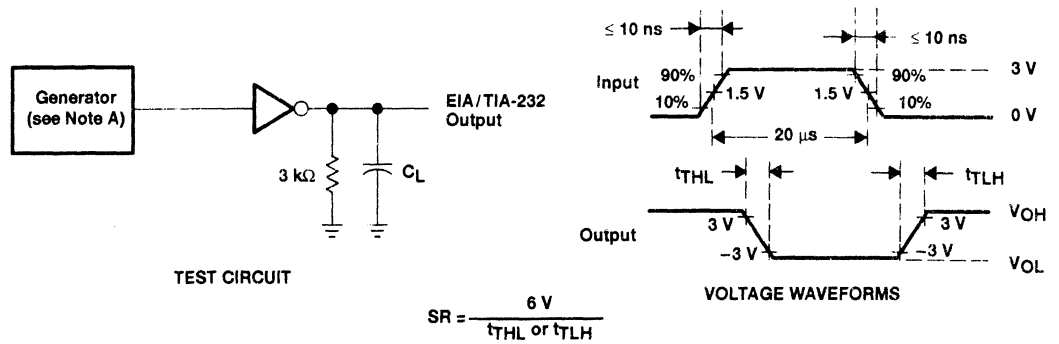


Figure 3. Driver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurement (5-µs Input)



$$SR = \frac{6\ V}{t_{THL}\ or\ t_{TLH}}$$

Figure 4. Test Circuit and Waveforms for t_{THL} and t_{TLH} Measurement (20-µs Input)

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, duty cycle ≤ 50%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

PARAMETER MEASUREMENT INFORMATION

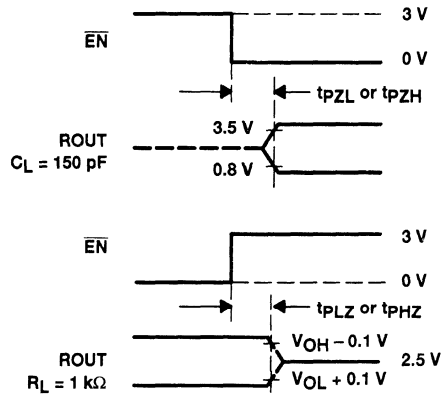


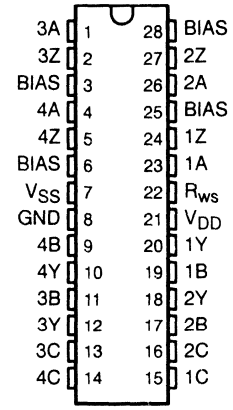
Figure 5. Receiver Output Enable and Disable Timing

SN75LBC784
QUADRUPLE RS-423-B DRIVER/RECEIVER

SLLS187A – NOVEMBER 1994 – REVISED AUGUST 1995

- **Four Independent Drivers and Receivers**
- **Driver Slew Rate Controlled by a Single Resistor**
- **Fast Driver Transition Times Down to 1.5 μs and Receiver Transition Times of 20 ns Typ**
- **Internal Thermal-Overload Protection**
- **RS-423-B Inputs and Outputs Designed to Withstand ±25 V**
- **ESD Protection Exceeds 2000 V Per MIL-STD-833C Method 3015**
- **LinBICMOS™ Process Technology**

DW PACKAGE
(TOP VIEW)



description

The SN75LBC784 performs as four independent RS-423-B driver/receiver pairs designed to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE) at rates up to 120 kbps and distances to 1.2 km. The SN75LBC784 provides an upgrade to the RS-232 serial interface and can be backward compatible with existing serial ports while offering the higher performance required by new faster peripherals, such as v.34 (v.fast) modems. The RS-232 standard, and subsequent revisions, only support data rates up to 20 kbps over about 15 meters of cable. For RS-423-B the data rate is increased to 120 kbps and transmission distance to 1.2 km by reducing the maximum output signal swing, increasing the driver output current, and reducing the receiver input voltage thresholds.

FUNCTION TABLE

INPUTS			OUTPUTS	
A	B	C	Z	Y
L	L	H	H	H
H	L	H	H	L
L	H	L	L	H
H	H	L	L	L
L	L	L	?	H
H	L	L	?	L
L	H	H	?	H
H	H	H	?	L

H = high level, L = low level,
X = irrelevant, Z = high impedance (off)
? = indeterminate

The receivers consist of differential comparators with hysteresis and resistive attenuation on the inputs. The resistive attenuation improves the input common mode range and also provides additional protection from ESD and over-voltage stress. The differential and common mode input impedances are sufficiently high to meet RS-423-B. When a differential voltage input of 500 mV is applied across the entire common mode range (see Figure 5), the receiver characteristics and bias voltage allow the receiver to remain in its intended binary state.

The drivers meet all RS-423-B specifications with built-in current limits and thermal-overload protection. Slew-rate controlling circuitry is included in the design, which is adjusted to suit the application by means of an external resistor (R_{WS}). The slew rate controlling circuitry also has a default mode – if the R_{WS} pin is shorted to 5 V externally, the transistion time defaults to approximately 1.5 ms. The BIAS input, when shorted to 5 V externally, provides the internal node voltages. The receiver is compatible to RS-232 with the use of external input resistors to meet the RS-232 input resistance specification of 3 kΩ to 7 kΩ.

The SN75LBC784 is characterized for operation over the temperature range of 0°C to 70°C.

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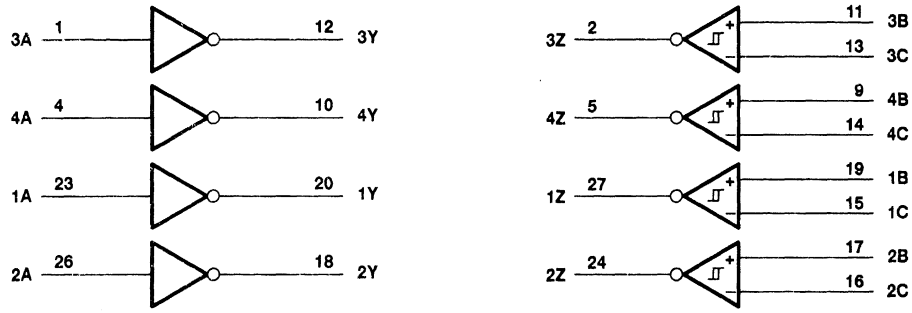
logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Positive supply voltage, V_{DD} (see Note 1) ..... 14 V
Negative supply voltage, V_{SS} ..... −14 V
Bias voltage, V_{bias} ..... 5.75 V
Receiver input voltage range ..... −30 V to 30 V
Driver input voltage range ..... −0.5 V to 5.75 V
Driver output voltage range (supplies at 0 V) ..... −30 V to 30 V
Driver output voltage range (supplies at ±12 V) ..... −25 V to 25 V
Continuous power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR† ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1348 mW	10.8 mW/°C	862 mW

† Derating factors are the inverse of the junction-to-ambient thermal resistance when board-mounted with no air flow.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		10.8	12	13.2	V
Supply voltage, V_{SS}		−10.8	−12	−13.2	V
Bias voltage, V_{bias}		2	5	5.5	V
High-level input voltage, V_{IH}	Driver	2			V
Low-level input voltage, V_{IL}	Driver			0.8	V
High-level output current, I_{OH}	Receiver			−4	mA
Low-level output current, I_{OL}	Receiver			4	mA
Rws slew rate control resistor		20	82	820	kΩ
Operating free-air temperature, T_A		0		70	°C

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{DD} = 10.8 V to 13.2 V, V_{SS} = −10.8 V to −13.2 V, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	Open circuit or R_L = 450 Ω		4	5.5	6	V
V_{OL}	Low-level output voltage	Open circuit or R_L = 450 Ω		−6	−5.5	−4	V
I_{IH}	High-level input current	V_I = 2.4 V to 5.5 V				100	µA
I_{IL}	Low-level input current	V_I = 0 V to 0.8 V		−100			µA
I_O	Output leakage current	V_{DD} = V_{SS} = 0,	V_O = ±6 V	−100		100	µA
$I_{OS(H)}$	High-level short circuit output current	V_I = 5 V,	V_O = 0	15		45	mA
$I_{OS(L)}$	Low-level short circuit output current	V_I = 0,	V_O = 0	−45		−15	mA
I_{DD}	Supply current	No load			10	12	mA
		R_L = 450 Ω			60	70	
I_{SS}	Supply current	No load			−10	−12	mA
		R_L = 450 Ω			−60	−70	
I_{bias}	Bias current					400	µA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{DD} = 10.8 V to 13.2 V, V_{SS} = −10.8 V to −13.2 V, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{TLH}	Transition time, low-to-high level (see Figure 1)	R_L = 450 Ω, C_L = 50 pF, V_{WS} = 5 V	R_{WS} = 0 kΩ		1.5		µs
			R_{WS} = 20 kΩ	1.5	2.1	2.7	
			R_{WS} = 82 kΩ	5	8	11	
			R_{WS} = 820 kΩ		80		
t_{THL}	Transition time, high-to-low level (see Figure 1)		R_{WS} = 0 kΩ		1.5		µs
			R_{WS} = 20 kΩ	1.5	2.1	2.7	
			R_{WS} = 82 kΩ	5	8	11	
			R_{WS} = 820 kΩ		80		
SR	Output slew rate		Rws = 20 kΩ			15	V/µs
t_{sk}	Output skew (see Figure 4) $\lvert t_{PHL} - t_{PLH} \rvert$		R_{WS} = 82 kΩ			1	µs

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature, V_{DD} = 10.8 V to 13.2 V, V_{SS} = −10.8 V to −13.2 V, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IT+}	Positive input threshold voltage					200	mV
		With 500 Ω series resistor				400	
V_{IT-}	Negative input threshold voltage					−200	mV
		With 500 Ω series resistor				−400	
I_I	Input current	V_I = 10 V	Other input to GND		1.3	3.25	mA
		V_I = −10 V		−3.25	−1.3		
V_{hys}	Hysteresis ($V_{IT+} - V_{IT-}$)			20	40	150	mV
V_{OH}	High-level output voltage (see Note 2)	I_O = −20 μA		3.5		5	V
		I_O = −4 mA		2.4		5	
V_{OL}	Low-level output voltage	I_O = 20 μA to 4 mA				0.4	V
I_{RX}	RX short circuit current					50	mA
V_{ID}	Differential input voltage	Receiver inputs open circuit		1.6	2.1	2.6	V
V_{ofs}	Fail safe output voltage	See Note 3		3.5			V

NOTES: 2. Device has an internal RX supply regulator. Maximum RX logic output voltage under no load is thus defined by an internal voltage value. This is nominally set to 4.5 V with a tolerance of ±5%.
3. One input at ground, other input open circuit, I_O = −20 μA, or both open circuit.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

test conditions: V_{DD} = 10.8 V to 13.2 V, V_{SS} = −10.8 V to −13.2 V, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{PLH}	Propagation Delay time low-to-high (see Figure 2)	C_L = 50 pF		0.15	1	μs
t_{PHL}	Propagation delay time high-to-low (see Figure 2)					
t_{THL}	Transition time high-to-low (see Figure 3)			20	200	ns
t_{TLH}	Transition time low-to-high (see Figure 3)					

PARAMETER MEASUREMENT INFORMATION

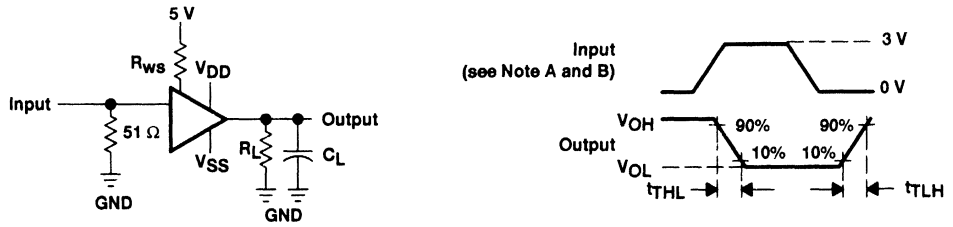


Figure 1. Driver Transition Times

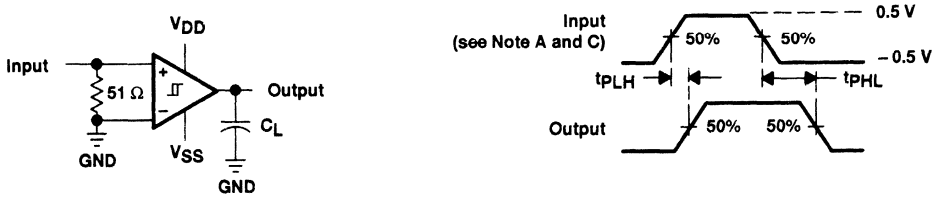


Figure 2. Receiver Propagation Delay Times

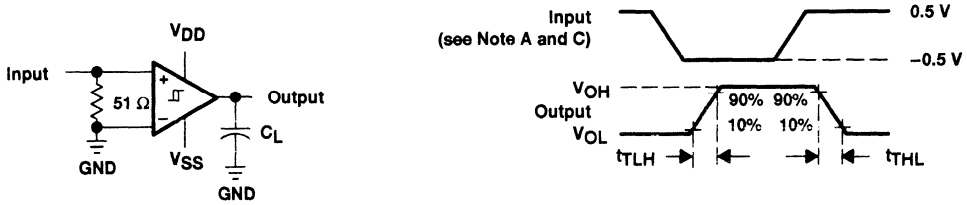


Figure 3. Receiver Transition Times

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 10$ nS, $t_f < 10$ nS, $Z_O = 50\ \Omega$, PRR ≥ 5 kHz, duty cycle 50%, $V_{max} = 3$ V, $V_{min} = 0$ V.
C. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 10$ nS, $t_f < 10$ nS, $Z_O = 50\ \Omega$, PRR ≥ 5 kHz, duty cycle 50%, $V_{max} = 0.5$ V, $V_{min} = -0.5$ V.

PARAMETER MEASUREMENT INFORMATION

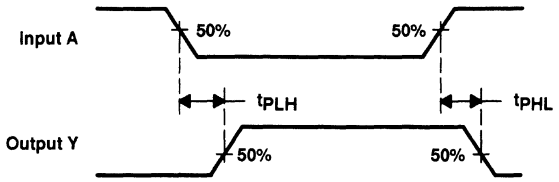


Figure 4. Skew Definition Times

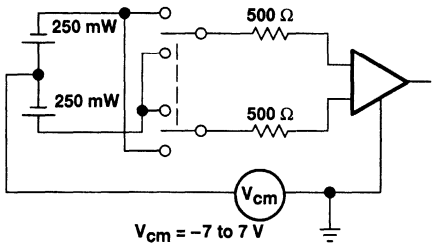
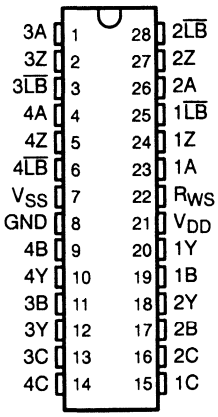


Figure 5. Receiver Input Balance Test

SLLS184 – NOVEMBER 1994

- **Four Independent Drivers and Receivers**
- **Loopback Mode Functionally Self Tests Drivers and Receivers Without Disconnection From Line**
- **Driver Slew Rate Controlled by a Single Resistor**
- **Internal Thermal-Overload Protection**
- **RS-423-B Inputs and Outputs Designed to Withstand ±25 V**
- **ESD Protection Exceeds 2000 V Per MIL-STD-833C Method 3015**
- **LinBiCMOS™ Process Technology**

DW PACKAGE
(TOP VIEW)



description

The SN75LBC786 is a monolithic quadruple RS-423-B driver and receiver with integrated-loopback function. The operation of the SN75LBC786 is closely based on that of the SN75186. In normal operation, the device performs as four independent RS-423-B driver/receiver pairs designed to interface data-terminal equipment (DTE) with data circuit-terminating equipment (DCE). In loopback mode, the signal from each driver output is fed back via special circuitry into its associated receiver input, removing the need to locally disconnect cables and install a loopback connector. The receiver output signal is the same as the driver input signal.

The SN75LBC786 is characterized for operation over the temperature range of 0°C to 70°C.

FUNCTION TABLE

LOOPBACK LB	INPUTS			OUTPUTS	
	A	B	C	Z	Y
H	L	L	H	H	H
H	H	L	H	H	L
H	L	H	L	L	H
H	H	H	L	L	L
H	L	L	L	?	H
H	H	L	L	?	L
H	L	H	H	?	H
H	H	H	H	?	L
L	L	X	X	L	L
L	H	X	X	H	L

H = high level, L = low level, X = irrelevant, ? = indeterminate

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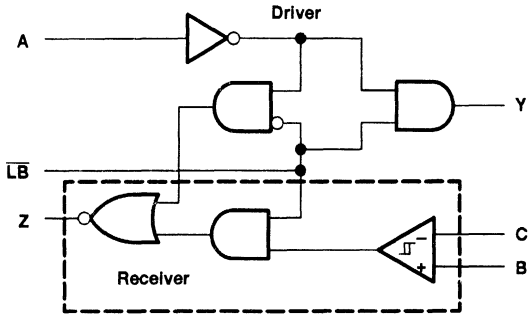
logic diagram (positive logic) (each transceiver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Positive supply voltage, V_{DD} (see Note 1) ..... 14 V
Negative supply voltage, V_{SS} ..... −14 V
Receiver input voltage range ..... −30 V to 30 V
Driver input voltage range ..... −0.5 V to 5.75 V
Loopback input voltage range ..... −0.5 V to 5.75 V
Driver output voltage range (supplies at 0 V) ..... −30 V to 30 V
Driver output voltage range (supplies at ±12 V) ..... −25 V to 25 V
Continuous power dissipation at (or below) T_A= 70°C ..... 800 mW
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Case temperature for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		10.8	12	13.2	V
Supply voltage, V_{SS}		−10.8	−12	−13.2	V
High-level input voltage, V_{IH}	Driver and loopback	2			V
Low-level input voltage, V_{IL}	Driver and loopback			0.8	V
High-level output current, I_{OH}	Receiver			−4	mA
Low-level output current, I_{OL}	Receiver			4	mA
Slew rate control resistor, R_{WS}		20	82	820	kΩ
Operating free-air temperature, T_A		0		70	°C

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	Open circuit or RI = 450 Ω		4	5.5	6	V
V_{OL}	Low-level output voltage	Open circuit or RI = 450 Ω		−6	−5.5	−4	V
I_{IH}	High-level input current	V_I = 2.4 V – 5.5 V				100	μA
I_{IL}	Low-level input current	V_I = 0 V – 0.8 V		−100			μA
I_{IKG}	Output leakage current	V_{DD} = V_{SS} = 0 V,	V_O = ±6 V	−100		100	μA
$I_{OS(H)}$	High-level short-circuit output current	V_I = high,	V_O = 0 V	15		45	mA
$I_{OS(L)}$	Low-level short-circuit output current	V_I = low,	V_O = 0 V	−45		−15	mA
I_{DD}	Supply current (loopback off)	No load,	$\overline{LB}$ at 2 V		10	12	mA
		RI = 450 Ω,	$\overline{LB}$ at 2 V		60	70	
$I_{DD(LB)}$	Supply current with loopback on	No load,	$\overline{LB}$ at 0.8 V		13	16	mA
I_{SS}	Supply current (loopback off)	No load,	$\overline{LB}$ at 2 V		−10	−12	mA
		RI = 450 Ω,	$\overline{LB}$ at 2 V		−60	−70	
I_{DD}	Supply current with loopback on	No load,	$\overline{LB}$ at 0.8 V		−13	−16	mA
LOOPBACK MODE							
	Output voltage (input either high or low)	RI = >450 Ω,	V_{LB} = low	−6	−5.5	−4	V

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{TLH}	Transition time, low-to-high level output (see Figure 1)	RI = 450 Ω, V_{WS} = 5 V	C_L = 50 pF,	R_{WS} = 0 kΩ		1.5		μs
				R_{WS} = 20 kΩ	1.5	2.1	2.7	
				R_{WS} = 82 kΩ	5	8	11	
				R_{WS} = 820 kΩ		80		
t_{THL}	Transition time, high-to-low level output (see Figure 1)			R_{WS} = 0 kΩ		1.5		μs
				R_{WS} = 20 kΩ	1.5	2.1	2.7	
				R_{WS} = 82 kΩ	5	8	11	
				R_{WS} = 820 kΩ		80		
SR	Output slew rate			R_{WS} = 20 kΩ			15	V/μs
t_{sk}	Output skew, $\lvert t_{PHL} - t_{PLH} \rvert$ (see Figure 4)			R_{WS} = 82 kΩ			1	μs

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

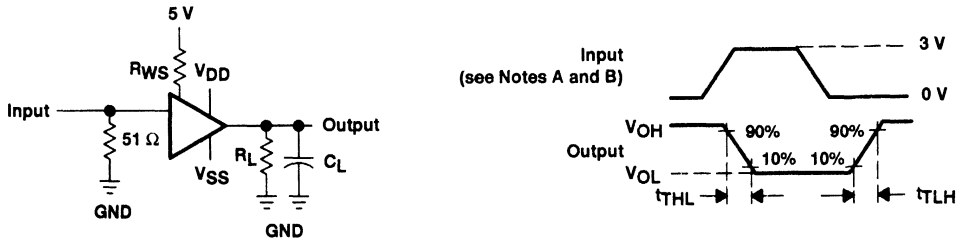
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IT}	Receiver input threshold voltage (see Figure 5)	$V_{IT} = (V_{I+} - V_{I-})$		−200		200	mV
		$V_{IT} = (V_{I+} - V_{I-})$ with 500-Ω series resistor		−400		400	
I_I	Input current	V_I = 10 V	Other input to GND		1.3	3.25	mA
		V_I = −10 V		−3.25	−1.3		
V_{hys}	Hysteresis voltage			20	40	150	mV
V_{OH}	High-level output voltage (see Note 2)	I_O = −20 μA		3.5		5	V
		I_O = −4 mA		2.4		5	
V_{OL}	Low-level output voltage	I_O = 20 μA to 4 mA				0.4	V
I_{OS}	RX short circuit current					50	mA
V_{ID}	Differential input voltage	Receiver inputs open circuit		1.6	2.1	2.6	V
V_{ofs}	Fail safe output voltage	See Note 3		3.5			V

NOTES: 2. Device has an internal RX supply regulator. Maximum RX logic output voltage under no load is thus defined by an internal voltage value. This is nominally set to 4.5 V with a tolerance of ±5%.
3. One input at ground, other input open circuit, I_O = −20 μA, or both open circuit.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

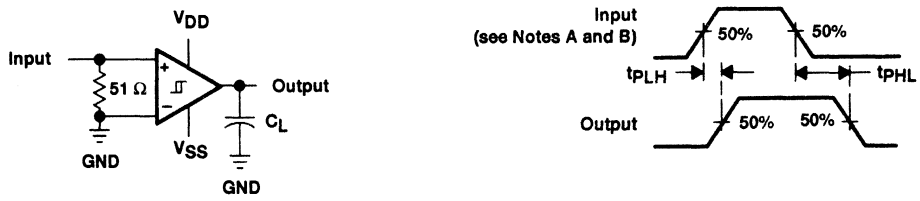
PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high (see Figure 2)	C_L = 50 pF		0.15	1	μs
t_{PHL}	Propagation delay time, high-to-low (see Figure 2)					
t_{THL}	Transition time, high-to-low (see Figure 3)			20	200	ns
t_{TLH}	Transition time, low-to-high (see Figure 3)					

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 10$ nS, $t_f < 10$ nS, $Z_O = 50\ \Omega$, PRR ≥ 5 kHz, duty cycle = 50%, $V_{max} = 3$ V, $V_{min} = 0$ V.

Figure 1. Driver Transition Times



NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 10$ nS, $t_f < 10$ nS, $Z_O = 50\ \Omega$, PRR ≥ 5 kHz, duty cycle = 50%, $V_{max} = 0.5$ V, $V_{min} = -0.5$ V.

Figure 2. Receiver Propagation Delay Times

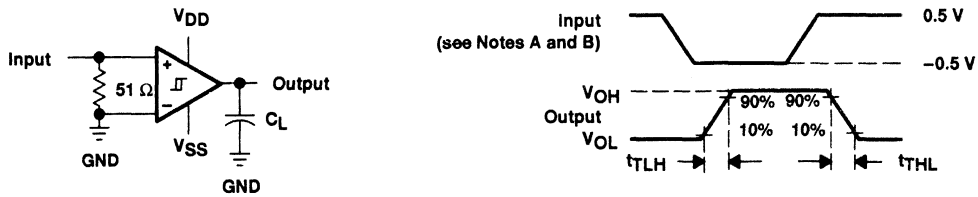


Figure 3. Receiver Transition Times

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 10$ nS, $t_f < 10$ nS, $Z_O = 50\ \Omega$, PRR ≥ 5 kHz, duty cycle = 50%, $V_{max} = 0.5$ V, $V_{min} = -0.5$ V.

PARAMETER MEASUREMENT INFORMATION

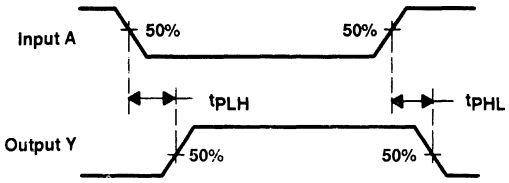


Figure 4. Skew Definition Times

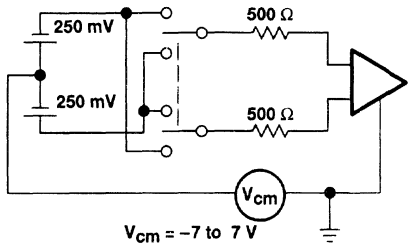


Figure 5. Input Balance Test

PRINCIPLES OF OPERATION

In normal operation, the SN75LBC786 functions as four independent drivers and receivers. The loopback mode is disabled by maintaining a high logic level on the $\overline{LB}$ input. The receivers consist of differential comparators with hysteresis and resistive attenuation on the inputs. The resistive attenuation improves the input common-mode range and also provides additional protection from ESD and over-voltage stress. The differential and common-mode input impedance are sufficiently high to meet RS-423-B. The balance of the receiver input voltage current characteristics and bias voltage is such that the receiver remains in the intended binary state when a differential voltage of 500 mV is applied to the inputs through 500 Ω across the entire common-mode range (see Figure 5).

The drivers meet all RS-423-B specifications. In normal operation, the drivers have built-in current limits and thermal overload protection. Slew-rate controlling circuitry is included into the design that is adjusted to suit the application by means of an external resistor. The slew-rate controlling circuitry also has a default mode. If R_{WS} is shorted to 5 V externally, the transition time defaults to approximately 1.5 µs. The receiver is compatible to the RS-232 with the use of external input resistors to meet the RS-232 input-resistance specification of 3 kΩ to 7 kΩ.

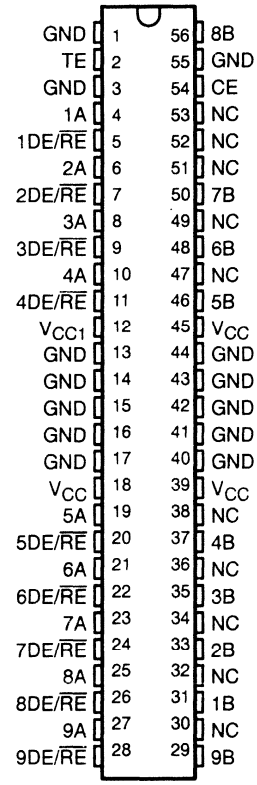
Taking an individual $\overline{LB}$ input low activates the loopback mode in the corresponding driver/receiver pair. This causes the output from that driver to be fed back to the input of its receiver through dedicated internal-loopback circuitry. Data from the receiver output can then be compared, by a communication system, with the data transmitted to the driver to determine if the functional operation of the driver and receiver together is correct.

In the loopback mode, external data at the input of the receiver is ignored and the driver does not transmit data onto the line. Extraneous data is prevented internally from being sent by the driver in the loopback mode by clamping its output to a level below the maximum interface voltage, −5 V, or the EIA-423-B marking state. Below this marking level, a reduced 1.5-V output amplitude is used at the driver output. This signal is detected by an on-chip loopback comparator and fed to the input stage of the receiver to complete the loop.

Line faults external to the SN75LBC786 are detected in addition to device failures. These line faults include short circuits to ground and to external supply voltages. The loopback mode should be entered only when the driver output is low, that is, the marking condition. It is recommended that loopback not be entered when the driver output is in a high state as this may cause a low-level, nondamaging oscillation at the driver output.

- **Nine Single-Ended SCSI Transceiver Channels With Active Termination**
- **Programmable Drivers Provide Active Negation (Totem Pole) or Wired-OR (Open Drain) Outputs**
- **24-mA Current-Mode Active Termination With Common Nine-Channel Bus Enable**
- **Low Output Capacitance Presented to SCSI Bus, 13.5 pF Typ**
- **3.3 V Compatible Logic Inputs Provide Bridge from 3 V Controllers to 5 V SCSI Bus**
- **Designed to Operate at 10-Million Data Transfers Per Second (Fast-SCSI)**
- **Controlled Driver Rise and Fall Times 5 ns Min**
- **High-Receiver Input-Voltage Hysteresis 500 mV Typ**
- **Receiver Input-Noise Pulse Filter 5 ns Typ**
- **Each Driver and Receiver Meets ANSI X3.131-1994 (SCSI-2) and the Proposed SCSI-3 Standards**
- **Power-Up/Power-Down Glitch Protection**
- **High Impedance Driver With V_{CC} at 0 V**

DL PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN75LBC968 is a nine-channel transceiver with active termination that drives and receives the signals from the single-ended, parallel data buses such as the Small Computer-Systems Interface (SCSI) bus. The features of the line drivers, receivers, and active-termination circuits provide the optimum signal-to-noise ratios for reliable data transmission. Integration of the termination and transceivers in the LinBiCMOS™ process provides the necessary analog-circuit performance, has low quiescent power, and reduces the capacitance presented to the bus over separate termination and I/O circuits.

The transceivers of the SN75LBC968 can be enabled to function as totem-pole or open-drain outputs. The open-drain mode drives the wired-OR lines of SCSI (BSY, SEL, and RST) by inputting the data to the direction control input DE/RE instead of the A input. When driving the data through the A input, the outputs become totem poles and provide active signal negation for a higher voltage level on low-to-high signal transitions on heavily loaded buses. In either mode, the turn-on and turn-off output transition times are limited to minimize crosstalk through capacitive coupling to adjacent lines and RF emissions from the cable. The receivers are also designed for optimum analog performance by precisely controlling the input-voltage thresholds, providing wide input-voltage hysteresis and including an input-noise filter. These features significantly increase the likelihood of detecting only the desired data signal and rejecting noise.

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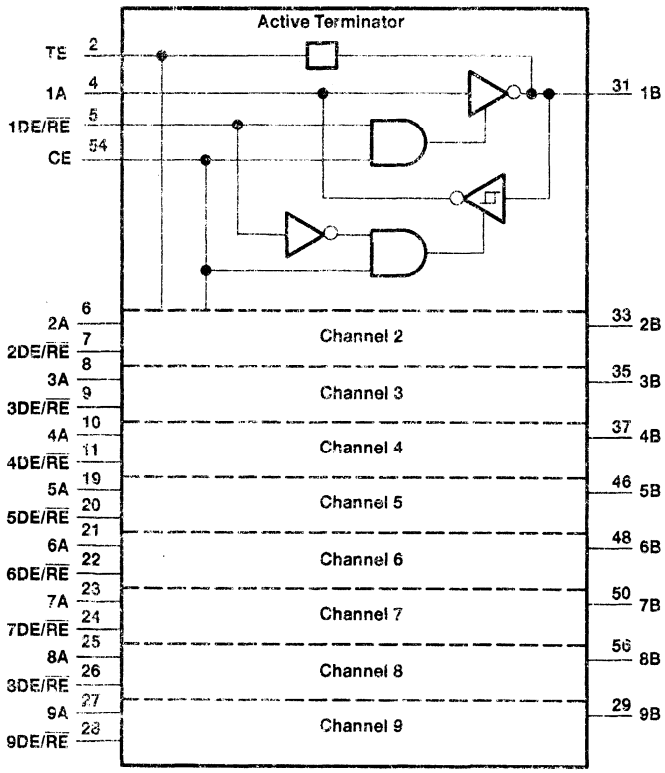
description (continued)

The communication between the SN75LBC968 and the controller can be accomplished at 3.3-V logic levels provided that the V_{CC1} input connects to the same supply rail as the controller. This provides a bridge from the lower-voltage circuit and the 5-V SCSI bus. The SN75LBC968 also removes the need for special I/O buffers (and associated power dissipation) on the controller itself. The SN75LBC968 must be used with a SCSI controller with support for Differential SCSI.

The integrated, current-mode, active termination supplies a constant 24 mA of current (TERMPWR) to the bus when the bus voltage falls below 2.5 V. This makes the next low-to-high (negation) signal transition independent of the low-level (asserted) bus voltage, unlike voltage-mode terminators. The termination current is provided through the TE input and from TERMPWR and can be disabled by letting the TE input float or by connecting it to ground. The termination circuitry is independent from the line drivers and receivers and V_{CC} or V_{CC1}. Operational termination is present as long as TERMPWR is applied.

The switching speeds of the SN75LBC968 are sufficient to transfer data over the data bus at ten million transfers per second (Fast-SCSI). The specification, $t_{sk(lim)}$, is for system skew budgeting and maintenance of bus set-up and hold times. The device is available in the space-efficient shrink-small-outline package (SSOP) with 25-mil lead pitch. The SN75LBC968 meets or exceeds the requirements of ANSI X3.131–1994 (SCSI-2) and the proposed SPI (SCSI-3) standards, and is characterized for operation from 0°C to 70°C.

logic diagram (positive logic)



Function Tables

TRANSCEIVER FUNCTIONS

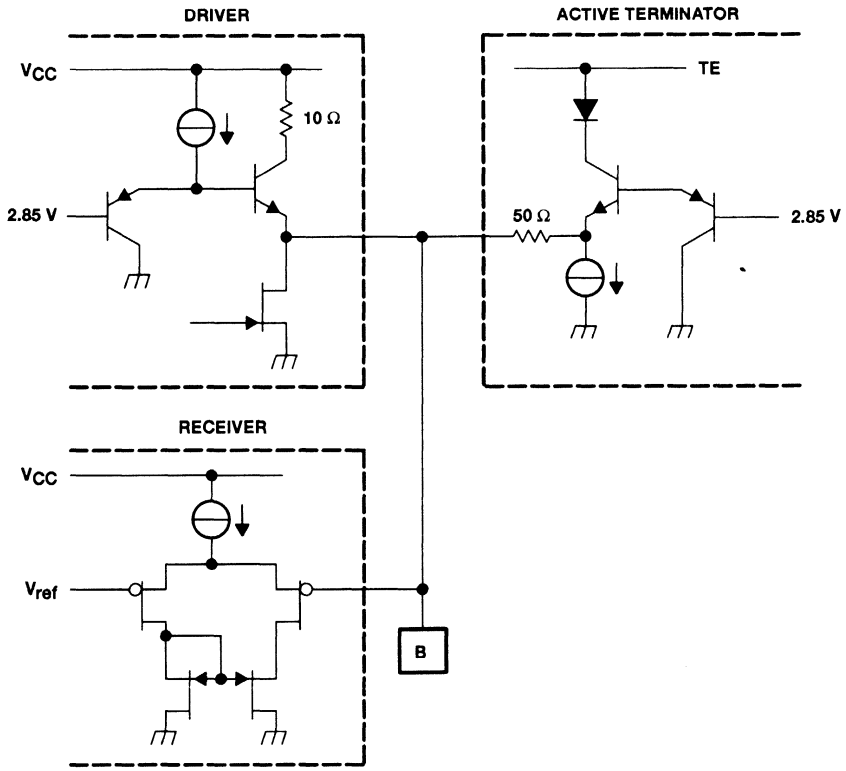
INPUTS				OUTPUTS	
CE	DE/RE	A	B	A	B
L	X	X	X	Z	Z
H	L	X	L	H	Z
H	L	X	H	L	Z
H	H	L	X	Z	H
H	H	H	X	Z	L
H	L	X	Open	H	Z
H	H	Open	X	Z	L

H = high level L = low level
X = irrelevant Z = high impedance

TERMINATION FUNCTION

INPUT TE	OUTPUT B
GND	Z
V_{TE}	24-mA source
Open	Z

schematics



absolute maximum ratings†

Supply voltage range, V_{CC}, V_{CC1}, V_{TE} (see Note 1)	−0.5 V to 7 V
Input voltage range, V_I (A-side)	V_{CC1} + 0.3 V
Bus voltage range (B-side)	−0.5 V to 7 V
Data I/O and control (A-side) voltage range	−0.5 V to 7 V
Continuous power dissipation (see Note 2)	internally limited
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. The maximum operating-junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR† ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DL	2500 mW	20 mW/°C	1600 mW

† Derating factors are the inverse of the junction-to-ambient thermal resistance when board-mounted with no air flow.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Supply voltage, V_{CC1} (see Note 3)		3		5.25	V
Termination voltage, V_{TE}		4.25		5.25	V
High-level input voltage, V_{IH}	DE/$\overline{RE}$, CE, A, B	2			V
Low-level input voltage, V_{IL}	DE/$\overline{RE}$, CE, A, B			0.8	V
High-level output current, I_{OH}	A			−8	mA
Low-level output current, I_{OL}	B			48	mA
	A			8	
Operating free-air temperature, T_A		0		70	°C

NOTE 3: All electrical characteristics are measured with $V_{CC1} = V_{CC}$ unless otherwise noted.

driver electrical characteristics over recommended operating conditions (unless otherwise noted) (see Figure 1)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -20$ mA		2		V
V_{OL}	Low-level output voltage	$I_{OL} = 48$ mA			0.5	V
I_{IH}	High-level input current	$V_{IH} = 2$ V,	$V_{CC} = V_{CC1} = 5.25$ V		−100	μA
I_{IL}	Low-level input current, A	$V_{IL} = 0.5$ V,	$V_{CC} = V_{CC1} = 5.25$ V		−100	μA
I_{OZ}	High-impedance-state output current	$V_O = 5.25$ V,	$V_{CC} = V_{CC1} = 5.25$ V		−100	μA
		$V_O = 0$ V,	$V_{CC} = V_{CC1} = 5.25$ V		−100	

termination electrical characteristics over recommended operating conditions (unless otherwise noted) (see Figure 2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{O(OC)}$	Open-circuit output voltage	$I_O = 0$ mA,	$V_{CC} = V_{CC1} = 0$ V	2.5	2.85	3.24	V
I_O	Output current	$V_O = 0$ V,	$V_{CC} = V_{CC1} = 0$ V			−24	mA
		$V_O = 0.5$ V,	$V_{CC} = V_{CC1} = 0$ V	−20		−24	mA
		$V_O = 3$ V,	$V_{CC} = V_{CC1} = 0$ V			100	μA
		$V_O = 4$ V,	$V_{CC} = V_{CC1} = 0$ V	20		100	mA

receiver electrical characteristics over recommended operating conditions (unless otherwise noted) (see Figure 3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −8 mA	2	2.5		V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			0.8	V
V_{IT+}	Positive-going input threshold voltage	$V_{CC} = V_{CC1}$	1.2	1.6	2	V
V_{IT-}	Negative-going input threshold voltage		0.8	1.1	1.4	V
V_{hys}	Input hysteresis voltage ($V_{IT+} - V_{IT-}$)		0.2	0.5		V
I_{IH}	High-level input current	V_{IH} = 2 V			100	µA
I_{IL}	Low-level input current	V_{IL} = 0.5 V			100	µA
I_{OZ}	High-impedance-state output current	V_O = 0 V			−100	µA
		V_O = 5.25 V			−100	

device electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{CC}	Supply current to V_{CC} and V_{CC1}	All drivers, receivers, and terminator disabled	All inputs at 0 V		1.3	3	mA
		All receivers enabled, termination and drivers disabled, No load	CE at V_{CC}, DE/$\overline{RE}$ at 0 V, TE at 0 V		14	21	
		All drivers enabled, termination and receivers disabled, No load	DE/$\overline{RE}$ and CE at V_{CC}, A and TE at 0 V		33	45	
			DE/$\overline{RE}$ and CE at V_{CC}, V_{TE} = 0 V, A at V_{CC1}		15	21	
I_{CC}	Supply current to TE	Termination and receivers enabled, No load	TE at V_{TE}, DE/$\overline{RE}$ at 0 V		33	45	
C_o	Bus port capacitance (see Note 4)				13.5	16.5	pF
I_{IH}	High-level input current	DE/$\overline{RE}$, CE	$V_{IH} = V_{CC}$ or 2 V			100	µA
I_{IL}	Low-level input current	DE/$\overline{RE}$, CE	V_{IL} = 0.5 V			100	µA

† All typical values are at $V_{CC} = V_{CC1}$ = 5 V, T_A = 25°C.
NOTE 4: Tested in accordance with Annex G X3T9.2/855D, revision 14

driver switching characteristics over recommended operating conditions (unless otherwise noted) (see Figure 4)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	C_L = 15 pF	10		35	ns
t_{PLH}	Propagation delay time, low- to high-level output		15		45	ns
$t_{sk(lim)}$	Skew limit‡, the maximum delay time – minimum delay time	V_{CC} = V_{CC1} = 5 V, T_A = 25°C, C_L = 15 pF			14	ns
		V_{CC} = V_{CC1} = 5 V, T_A = 70°C, C_L = 15 pF			14	ns
$t_{sk(p)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$	V_{CC} = V_{CC1} = 5 V, T_A = 25°C		8		ns
t_t	Output transition time, 10% to 90% or 90% to 10% of the steady-state output	15 pF < C_L < 100 pF	5		20	ns
t_{PLZ}	Propagation delay time, low-level to high-impedance output	From CE, C_L = 15 pF	5		150	ns
		From DE/$\overline{RE}$, C_L = 15 pF			45	
t_{PZL}	Propagation delay time, high-impedance to low-level output	From CE, C_L = 15 pF	5		150	ns
		From DE/$\overline{RE}$, C_L = 15 pF			45	

† All typical values are at V_{CC} = V_{CC1} = 5 V, T_A = 25°C.
‡ The value for this parameter was derived from the difference between the slowest and the fastest driver delay times measured on devices from four sample wafer lots.

receiver switching characteristics over recommended of operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	See Figure 5	5		20	ns
t_{PLH}	Propagation delay time, low- to high-level output		5		25	ns
$t_{sk(lim)}$	Skew limit‡, the maximum delay time – minimum delay time	V_{CC} = V_{CC1} = 5 V, T_A = 25°C, See Figure 5			8.5	ns
		V_{CC} = V_{CC1} = 5 V, T_A = 70°C, See Figure 5			8.5	ns
$t_{sk(p)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$	V_{CC} = V_{CC1} = 5 V, T_A = 25°C, See Figure 5		6		ns
t_{PLZ}	Propagation delay time, low-level to high-impedance output	From CE, See Figure 6	5		150	ns
		From DE/$\overline{RE}$, See Figure 6			45	
t_{PZL}	Propagation delay time, high-impedance to low-level output	From CE, See Figure 6	5		150	ns
		From DE/$\overline{RE}$, See Figure 6			80	
t_{PHZ}	Propagation delay time, high-level to high-impedance output	From CE, See Figure 7	5		150	ns
		From DE/$\overline{RE}$, See Figure 7			45	
t_{PZH}	Propagation delay time, high-impedance to high-level output	From CE, See Figure 7	5		150	ns
		From DE/$\overline{RE}$, See Figure 7			80	

† All typical values are at V_{CC} = V_{CC1} = 5 V, T_A = 25°C.
‡ The value for this parameter was derived from the difference between the slowest and the fastest driver delay times measured on devices from four sample wafer lots.

thermal characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	Board-mounted, no air flow		50		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance			12		°C/W
T_{JS}	Junction-shutdown temperature			180		°C

PARAMETER MEASUREMENT INFORMATION

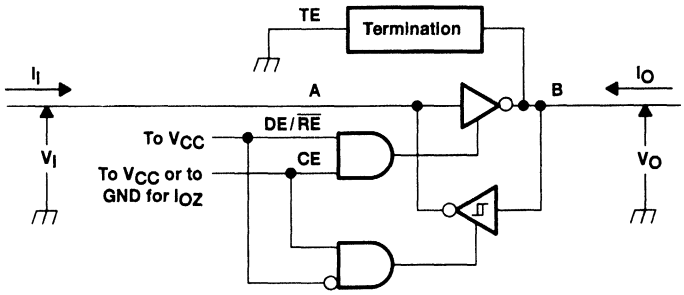


Figure 1. Driver Test Circuit Currents and Voltages.

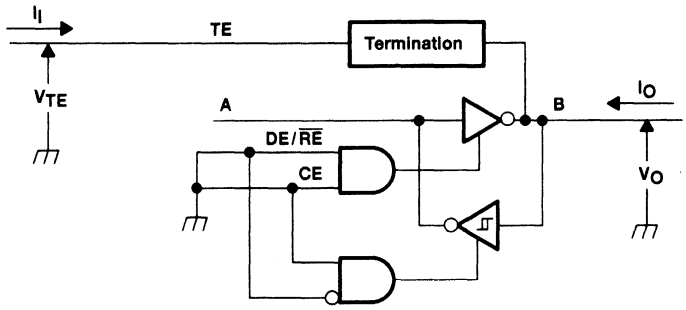


Figure 2. Active Termination Voltages, Currents, and Test Circuit.

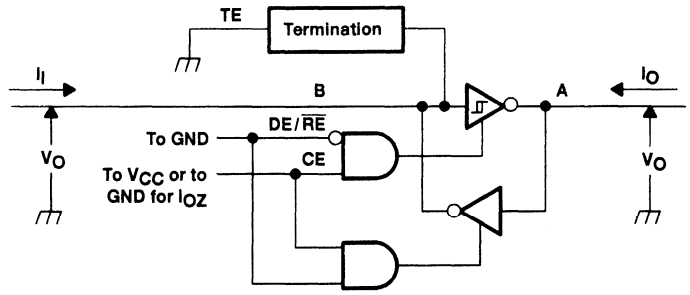


Figure 3. Receiver Voltages, Currents, and Test Circuit

NOTES: A. All input pulses are supplied by a generator having the following characteristics: $t_r \leq 6$ ns, $t_f \leq 6$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50\ \Omega$.
B. All resistances are in ohms and ±5%, unless otherwise indicated.
C. All capacitances are in picofarads and ±10%, unless otherwise indicated.
D. All indicated voltages are ±10 mV.

PARAMETER MEASUREMENT INFORMATION

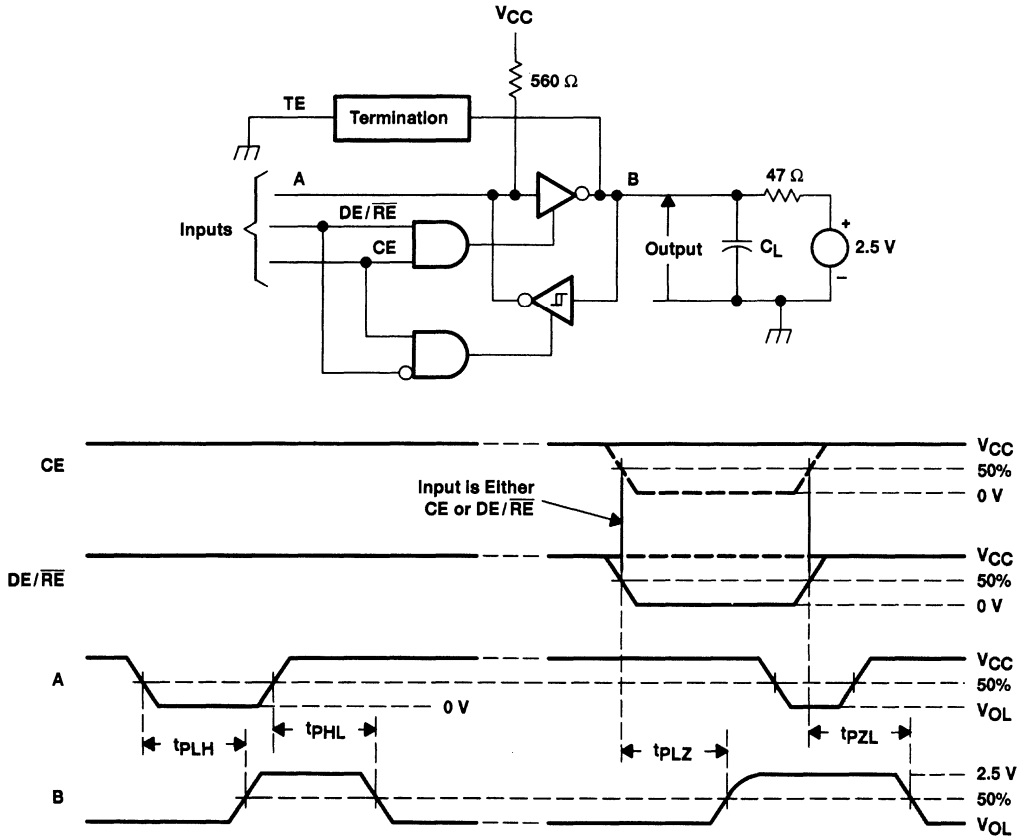


Figure 4. Driver Delay Time Test Circuit and Waveforms

NOTES: A. All input pulses are supplied by a generator having the following characteristics: $t_r \leq 6$ ns, $t_f \leq 6$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50\ \Omega$.
B. All resistances are in ohms and ±5%, unless otherwise indicated.
C. All capacitances are in picofarads and ±10%, unless otherwise indicated.
D. All indicated voltages are ±10 mV.

PARAMETER MEASUREMENT INFORMATION

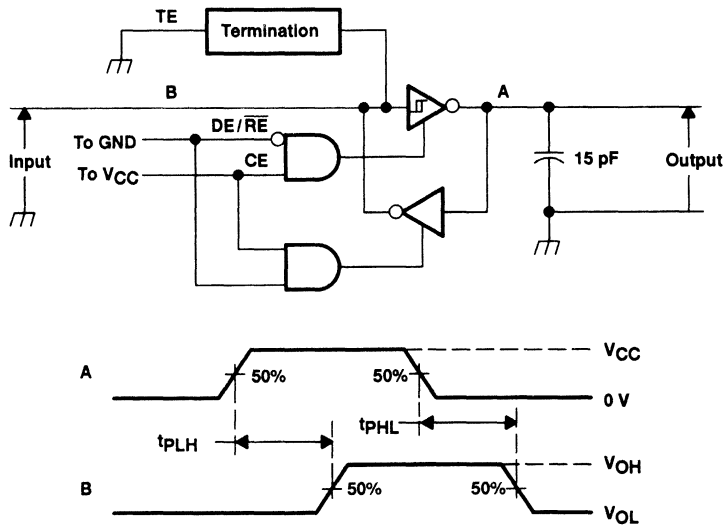


Figure 5. Receiver Propagation Delay Time Test Circuit and Waveforms

NOTES: A. All input pulses are supplied by a generator having the following characteristics: $t_r \leq 6$ ns, $t_f \leq 6$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50\ \Omega$.
B. All resistances are in ohms and ±5%, unless otherwise indicated.
C. All capacitances are in picofarads and ±10%, unless otherwise indicated.
D. All indicated voltages are ±10 mV.

PARAMETER MEASUREMENT INFORMATION

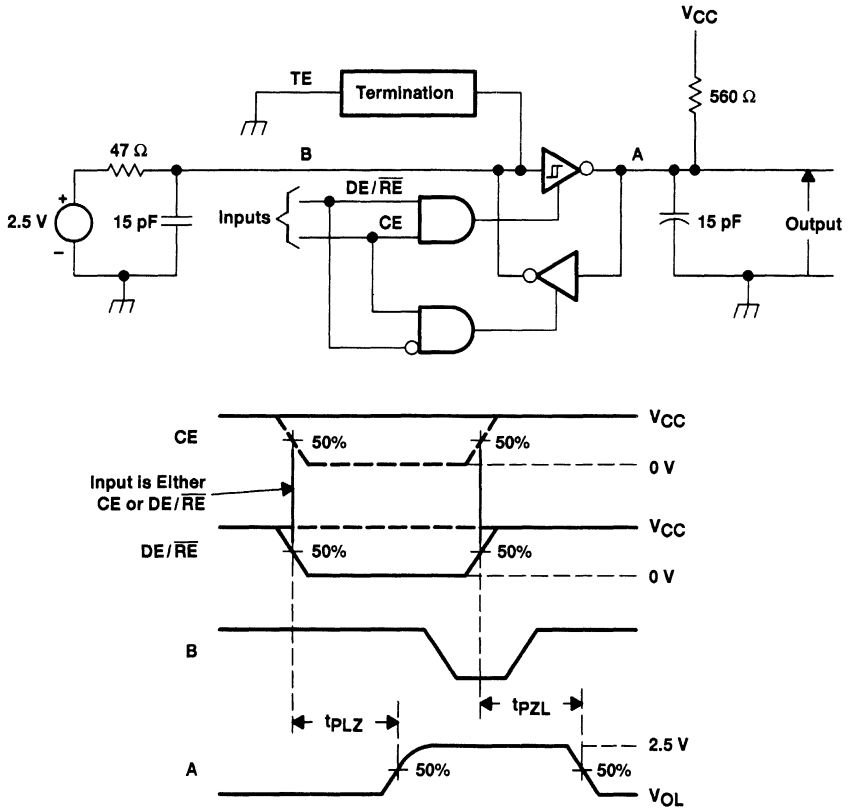


Figure 6. Receiver Enable and Disable Times to and From Low-Level Output Test Circuit and Waveforms

NOTES: A. All input pulses are supplied by a generator having the following characteristics: $t_r \leq 6$ ns, $t_f \leq 6$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50\ \Omega$.
B. All resistances are in ohms and ±5%, unless otherwise indicated.
C. All capacitances are in picofarads and ±10%, unless otherwise indicated.
D. All indicated voltages are ±10 mV.

PARAMETER MEASUREMENT INFORMATION

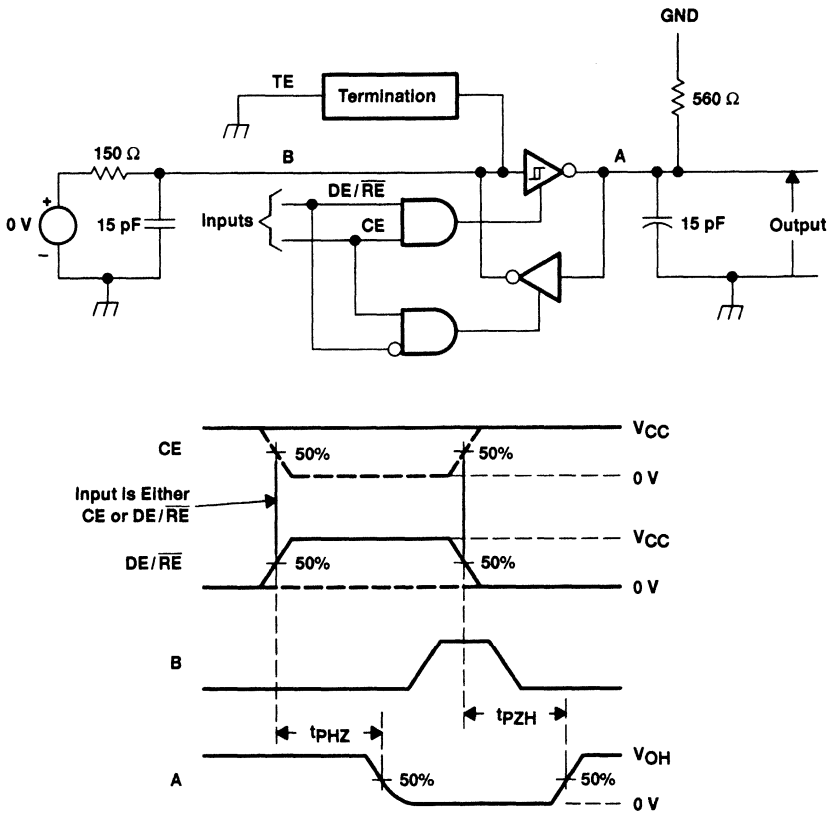


Figure 7. Receiver Enable and Disable Times to and From High-Level Output Test Circuit and Waveforms

NOTES: A. All input pulses are supplied by a generator having the following characteristics: $t_r \leq 6$ ns, $t_f \leq 6$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50\ \Omega$.
B. All resistances are in ohms and ±5%, unless otherwise indicated.
C. All capacitances are in picofarads and ±10%, unless otherwise indicated.
D. All indicated voltages are ±10 mV.

TYPICAL CHARACTERISTICS

DRIVER AND TERMINATION
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

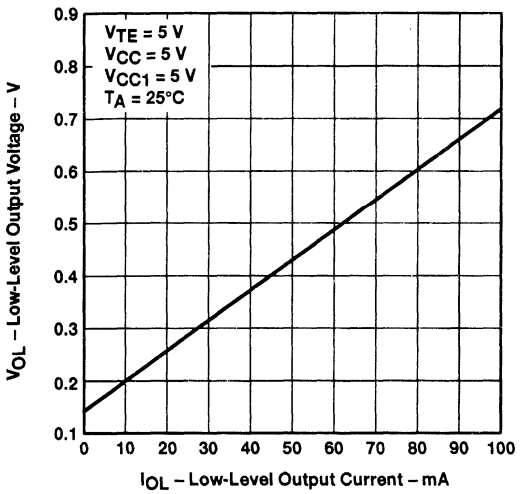


Figure 8

TERMINATION
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

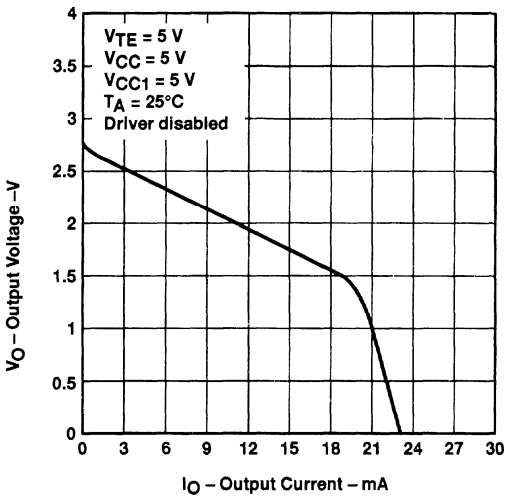


Figure 9

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

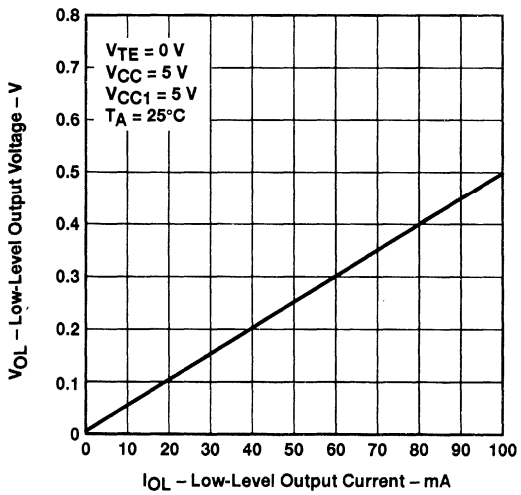


Figure 10

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

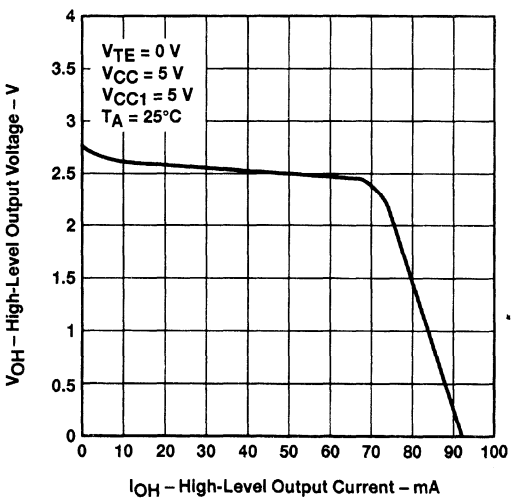


Figure 11

TYPICAL CHARACTERISTICS

DRIVER
PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

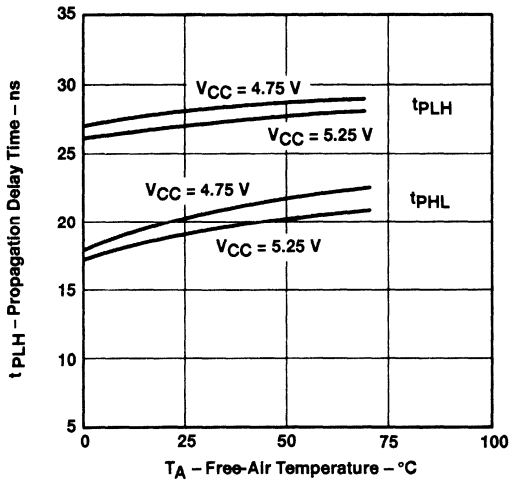


Figure 12

RECEIVER
PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

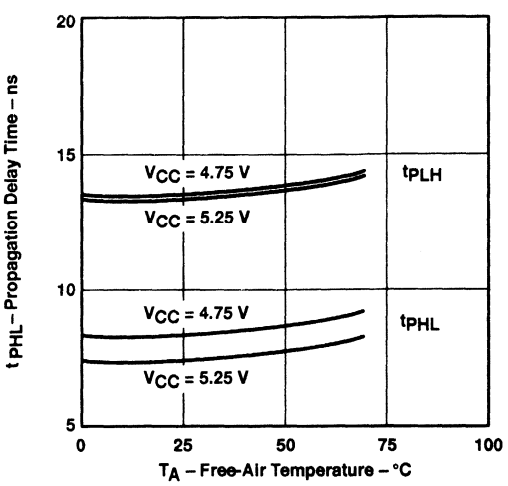
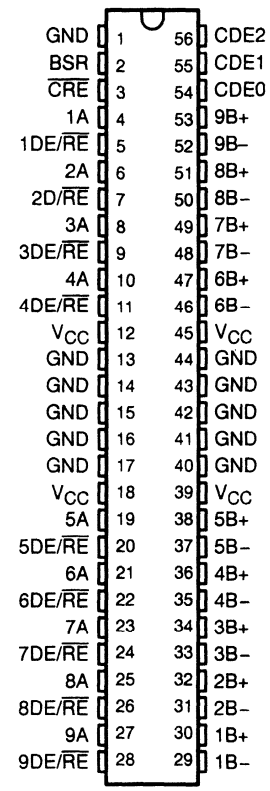


Figure 13

SLLS218 – MAY 1995

- **Improved Speed and Package Replacement for the SN75LBC976**
- **Designed to Operate at up to 20 Million Data Transfers per Second (Fast-20 SCSI)**
- **Nine Differential Channels for the Data and Control Paths of the Small Computer Systems Interface (SCSI) and Intelligent Peripheral Interface (IPI)**
- **Packaged in Shrink Small-Outline Package with 25-Mil Terminal Pitch and Thin Shrink Small-Outline Package with 20 Mil Terminal Pitch**
- **Two Skew Limits Available**
- **ESD Protection on Bus Terminals Exceeds 12 kV**
- **Low Disabled Supply Current 8 mA Typ**
- **Thermal Shutdown Protection**
- **Positive- and Negative-Current Limiting**
- **Power-Up/Down Glitch Protection**

SN75976A DL or DGG
(TOP VIEW)



Terminals 13 through 17 and 40 through 44 are connected together to the package lead frame and signal ground.

description

The SN75976A is an improved replacement for the industry's first 9-channel RS-485 transceiver — the SN75LBC976. The A version offers improved switching performance, a smaller package, and higher ESD protection. The SN75976A is offered in two versions. The '976A2 skew limits of 4 ns for the differential drivers and 5 ns for the differential receivers complies with the recommended skew budget of the proposed Fast-20 SCSI standard for data transfer rates up to 20 million transfers per second. The '976A1 supports the Fast SCSI skew budget for 10 million

AVAILABLE OPTIONS

Skew Limit (ns)		PACKAGE†	
Driver	Receiver	TSSOP (DGG)	SSOP (DL)
8	9	SN75976A1DGG SN75976A1DGGR	SN75976A1DL SN75976A1DLR
4	5	SN75976A2DGG SN75976A2DGGR	SN76976A2DL SN75976A2DLR

† The R suffix indicates taped and reeled packages.

description (continued)

transfers per second. The skew limit ensures that the propagation delay times, not only from channel-to-channel but from device-to-device, are closely matched for the tight skew budgets associated with high-speed parallel data buses.

The patented thermal enhancements made to the 56-pin shrink small-outline package (SSOP) of the '976 have been applied to the new, thin shrink, small-outline package (TSSOP). The TSSOP package offers even less board area requirements than the SSOP while reducing the package height to 1 mm. This provides more board area and allows component mounting to both sides of the printed circuit boards for low-profile, space-restricted applications such as small form-factor hard disk drives.

In addition to speed and package improvements, the '976A can withstand electrostatic discharges exceeding 12 kV per the human-body model, and 600 V per the machine model of MIL-STD-883C, Method 3015.7 on the RS-485 I/O terminals. This is six times the industry standard and provides protection from the noise that can be coupled into external cables. The other terminals of the device can withstand discharges exceeding 4 kV and 400 V respectively.

Each of the 9 channels of the '976A typically meet or exceed the requirements of EIA RS-485 (1983) and ISO 8482-1987/TIA TR30.2 referenced by American National Standard of Information (ANSI) Systems X3.131-1993 (SCSI-2) standard. This device also meets or exceeds the requirements of the proposed SCSI-3 Parallel Interface (SPI) ANSI X3T9.2/855D and X3T10/1071D SCSI-3 Fast-20 SCSI Working Drafts, and the Intelligent Peripheral Interface Physical Layer-ANSI X3.129-1986 standard.

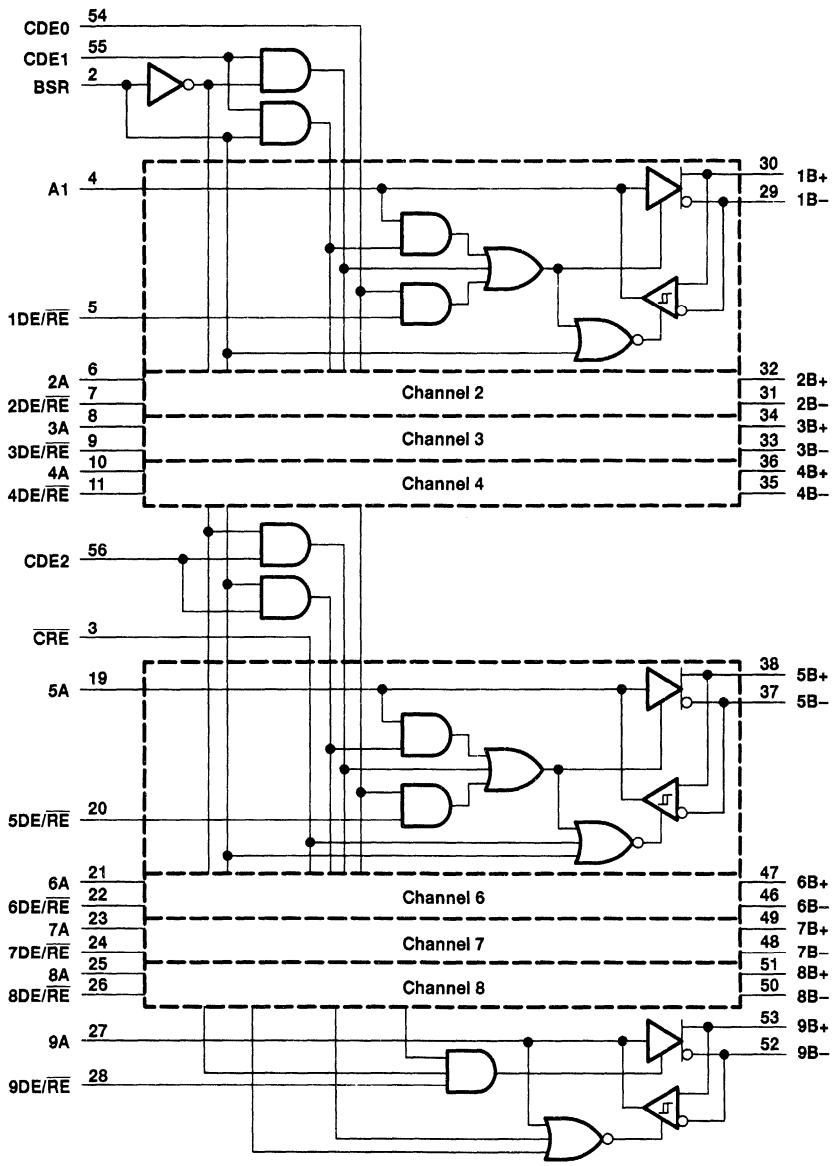
The SN75976A is characterized for operation over an ambient air temperature range of 0°C to 70°C

Terminal Functions

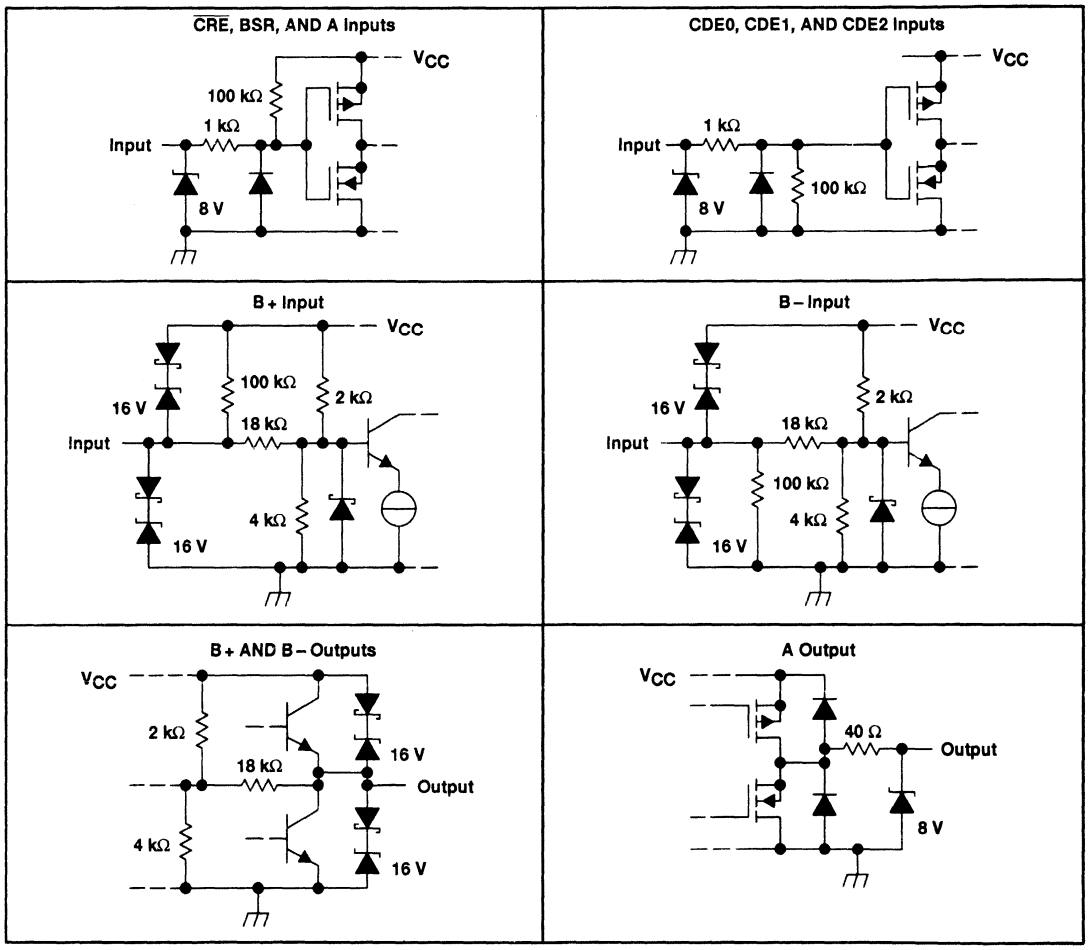
TERMINAL NAME	TERMINAL NO.	Logic Level	I/O	Termination	DESCRIPTION
1A to 9A	4,6,8,10, 19,21,23, 25,27	TTL	I/O	Pullup	1A to 9A carry data to and from the communication controller.
1B– to 9B–	29,31,33, 35,37,.46, 48,50,52	RS-485	I/O	Pulldown	1B– to 9B– are the inverted data signals of the balanced pair to/from the bus.
1B+ to 9B+	30,32,34, 36,38,47, 49,51,53	RS-485	I/O	Pullup	1B+ to 9B+ are the noninverted data signals of the balanced pair to/from the bus.
BSR	2	TTL	Input	Pullup	BSR is the bit significant response. It disables receivers 1 through 8 and enables wired-OR drivers when it and DE/$\overline{RE}$ and CDE1 or CDE2 are high. Channel 9 is placed in a high-impedance state with BSR high.
CDE0	54	TTL	Input	Pulldown	CDE0 is the common driver enable 0. Its input signal enables all drivers when it and 1DE/$\overline{RE}$ – 9DE/$\overline{RE}$ are high.
CDE1	55	TTL	Input	Pulldown	CDE1 is the common driver enable 1. Its input signal enables drivers 1 to 4 when it is high and BSR is low.
CDE2	56	TTL	Input	Pulldown	CDE2 is the common driver enable 2. Its input signal enables drivers 5 to 8 when high and BSR is low.
$\overline{CRE}$	3	TTL	Input	Pullup	$\overline{CRE}$ is the common receiver enable. It disables receiver channels 5 to 9 when high.
1DE/$\overline{RE}$ to 9DE/$\overline{RE}$	5,7,9,11, 20,22,24, 26,28	TTL	Input	Pullup	1DE/$\overline{RE}$–9DE/$\overline{RE}$ are direction controls that transmit data to the bus when it and CDE0 are high. Data is received from the bus when it and $\overline{CRE}$ and BSR are low and CDE1 and CDE2 are low.
GND	1,13,14, 15,16,17, 40,41,42, 43,44	NA	Power	NA	GND is the circuit ground. All terminals except terminal 1 are physically tied to the die pad for improved thermal conductivity.†
V_{CC}	12,18,39, 45	NA	Power	NA	Supply voltage

† Terminal 1 must be connected to signal ground for proper operation.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.3 V to 6 V
Bus voltage range ..... −10 V to 15 V
Data I/O and control (A side) voltage range ..... −0.3 V to V_{CC} +0.5 V
Electrostatic discharge: B side and GND, Class 3, A: (see Note 2) ..... 12 kV
B side and GND, Class 3, B: (see Note 2) ..... 400 V
All terminals, Class 3, A: ..... 4 kV
All terminals, Class 3, B: ..... 400 V
Continuous power dissipation (see Note 3) ..... internally limited
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the GND terminals.
2. This absolute maximum rating is tested in accordance with MIL-STD-883C, Method 3015.7.
3. The maximum operating junction temperature is internally limited. Use the Dissipation Rating Table to operate below this temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	OPERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DGG	2500 mW	20 mW/°C	1600 mW
DL	2500 mW	20 mW/°C	1600 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

package thermal characteristics

		MIN	NOM	MAX	UNIT
Junction-to-ambient thermal resistance, $R_{\theta JA}$	DGG, board-mounted, no air flow		50		°C/W
	DL, board-mounted, no air flow		50		°C/W
Junction-to-case thermal resistance, $R_{\theta JC}$	DGG		27		°C/W
	DL		12		°C/W
Thermal-shutdown junction temperature, T_{JS}			165		°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	Except nB+, nB–	2			V
Low-level input voltage, V_{IL}	Except nB+, nB–			0.8	V
Voltage at any bus terminal (separately or common-mode), V_O, V_I, or V_{IC}	nB+ or nB –			12	V
				−7	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−8	mA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	mA
Operating case temperature, T_C		0		125	°C
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{ODH}	Driver differential high-level output voltage	S1 to A, See Figure 1	V_T = 5 V,	1	1.8		V
		S1 to B, $T_C \geq 25°C$	V_T = 5 V, See Figure 1	1	1.4		V
		S1 to B, See Figure 1	V_T = 5 V,	0.8			V
V_{ODL}	Driver differential low-level output voltage	S1 to A, $T_C \geq 25°C$	V_T = 5 V, See Figure 1	−1	−1.4		V
		S1 to B, See Figure 1	V_T = 5 V,	−1	−1.8		V
		S1 to A, See Figure 1	V_T = 5 V,	−0.8	−1.4		V
V_{OH}	High-level output voltage	A side, I_{OH} = −8 mA	V_{ID} = 200 mV, See Figure 3	4	4.5		V
		B side, See Figure 1	V_T = 5 V		3		V
V_{OL}	Low-level output voltage	A side, I_{OH} = 8 mA	V_{ID} = −200 mV, See Figure 3		0.6	0.8	V
		A side, See Figure 1	V_T = 5 V		1		V
V_{IT+}	Receiver positive-going differential input threshold voltage	I_{OH} = −8 mA,	See Figure 3			0.2	V
V_{IT-}	Receiver negative-going differential input threshold voltage	I_{OL} = 8 mA,	See Figure 3			−0.2	V
V_{HYS}	Receiver input hysteresis (V_{IT+} − V_{IT-})	V_{CC} = 5 V,	T_A = 25°C	24	45		mV
I_I	Bus input current	V_{IH} = 12 V, Other input at 0 V	V_{CC} = 5 V,		0.4	1	mA
		V_{IH} = 12 V, Other input at 0 V	V_{CC} = 0 V,		0.5	1	mA
		V_{IH} = −7 V, Other input at 0 V	V_{CC} = 5 V,		−0.4	−0.8	mA
		V_{IH} = −7 V, Other input at 0 V	V_{CC} = 0 V,		−0.3	−0.8	mA
I_{IH}	High-level input current	A, BSR, DE/RE, and CRE,	V_{IH} = 2 V			−100	µA
		CDE0, CDE1, and CDE2,	V_{IH} = 2V			100	µA
I_{IL}	Low-level input current	A, BSR, DE/RE, and CRE,	V_{IL} = 0.8 V			−100	µA
		CDE1, CDE1, and CDE2,	V_{IL} = 0.8 V			100	µA
I_{OS}	Short circuit output current	nB+ or nB–				±260	mA
I_{OZ}	High-impedance-state output current	A		See I_{IH} and I_{IL}			
		nB+ or nB–		See I_I			
I_{CC}	Supply current	Disabled				10	mA
		All drivers enabled, no load				60	mA
		All receivers enabled, no load				45	mA
C_O	Output capacitance	nB+ or nB– to GND			18	25	pF
C_{pd}	Power dissipation capacitance (see Note 4)	Receiver			40		pF
		Driver			100		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 4: C_{pd} determines the no-load dynamic supply current consumption, $I_S = C_{PD} \times V_{CC} \times f + I_{CC}$

driver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{pd}	Propagation delay time, t_{PHL} or t_{PLH} (see Figures 1 and 2)	'976A1	V_T = 4.5 V	2.5		13.5	ns
			V_{CC} = 5 V, V_T = 4.5 V, T_C = 25°C	3		11	ns
			V_{CC} = 5 V, V_T = 4.5 V, T_C = 100°C	5		13	ns
		'976A2	V_T = 4.5 V	4.5		11.5	ns
			V_{CC} = 5 V, V_T = 4.5 V, T_C = 25°C	5		9	ns
			V_{CC} = 5 V, V_T = 4.5 V, T_C = 100°C	7		11	ns
$t_{sk(lim)}$	Skew limit, maximum t_{pd} – maximum t_{pd} (see Note 5)	'976A1				8	ns
		'976A2				4	ns
$t_{sk(p)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$					4	ns
t_f	Fall time		S1 to B, See Figure 2		4		ns
t_r	Rise time		See Figure 2		8		ns
t_{en}	Enable time, control inputs to active output					50	ns
t_{dis}	Disable time, control inputs to high-impedance output					100	ns
t_{PHZ}	Propagation delay time, high-level to high-impedance output		See Figures 5 and 6		17	100	ns
t_{PLZ}	Propagation delay time, low-level to high-impedance output				25	100	ns
t_{PZH}	Propagation delay time, high-impedance to high-level output				17	50	ns
t_{PZL}	Propagation delay time, high-impedance to low-level output				17	50	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 5: This parameter is applicable at one V_{CC} and operating temperature within the recommended operating conditions and to any two devices.

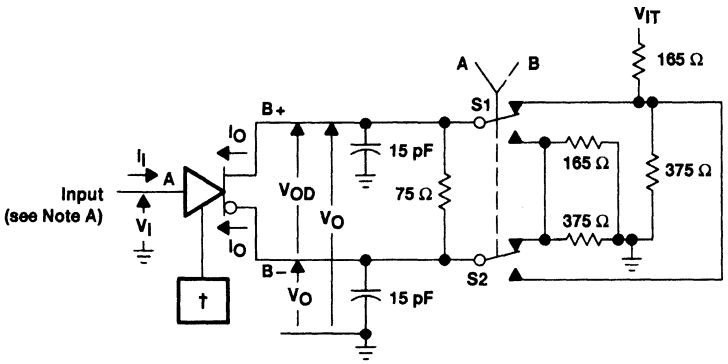
receiver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{pd}	Propagation delay time, t_{PHL} or t_{PLH} (see Figures 3 and 4)	'976A1		7.5		16.5	ns
		'976A2		8.5		14.5	ns
			V_{CC} = 5 V, T_C = 25°C	8.6		13.6	ns
			V_{CC} = 5 V, T_C = 100°C	9		14	ns
$t_{sk(lim)}$	Skew limit, maximum t_{pd} – minimum t_{pd} (see Note 5)	'976A1				9	ns
		'976A2				5	ns
$t_{sk(p)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$				0.6	4	ns
t_t	Transition time (t_r or t_f)		See Figure 4		2		ns
t_{en}	Enable time, control inputs to active output					50	ns
t_{dis}	Disable time, control inputs to high-impedance output					60	ns
t_{PHZ}	Propagation delay time, high-level to high-impedance output		See Figures 7 and 8			60	ns
t_{PLZ}	Propagation delay time, low-level to high-impedance output					50	ns
t_{PZH}	Propagation delay time, high-impedance to high-level output					50	ns
t_{PZL}	Propagation delay time, high-impedance to low-level output					50	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 5. This parameter is applicable at one V_{CC} and operating temperature within the recommended operating conditions and to any two devices.

PARAMETER MEASUREMENT INFORMATION



† CDE0 and DE/$\overline{RE}$ are at 2 V, BSR is at 0.8 V, and all others are open.
‡ All nine drivers are enabled, similarly loaded, and switching.

Figure 1. Driver Test Circuit, Currents, and Voltages‡

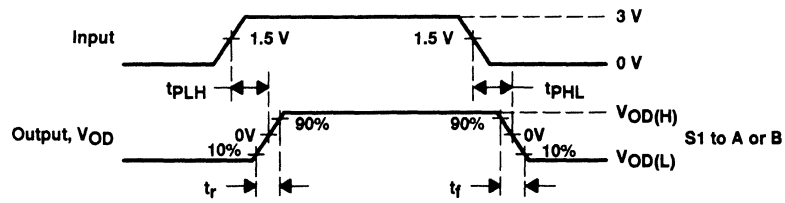
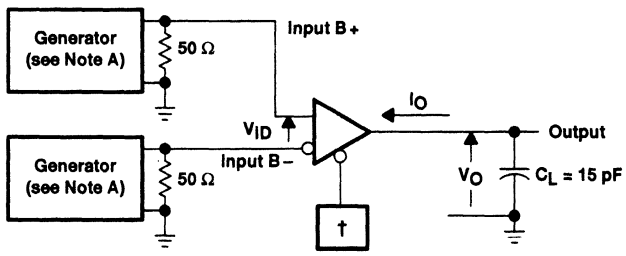


Figure 2. Driver Delay and Transition Time Test Waveforms



† CDE0, CDE1, CDE2, BSR, CRE, and DE/$\overline{RE}$ at 0.8 V
‡ All nine receivers are enabled and switching.

Figure 3. Receiver Propagation Delay and Transition Time Test Circuit‡

NOTES: A. All input pulses are supplied by a generator having the following characteristics: $t_r \leq 6$ ns, $t_f \leq 6$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50\ \Omega$.
B. All resistances are in Ω and ± 5%, unless otherwise indicated.
C. All capacitances are in pF and ± 10%, unless otherwise indicated.
D. All indicated voltages are ± 10 mV.

PARAMETER MEASUREMENT INFORMATION

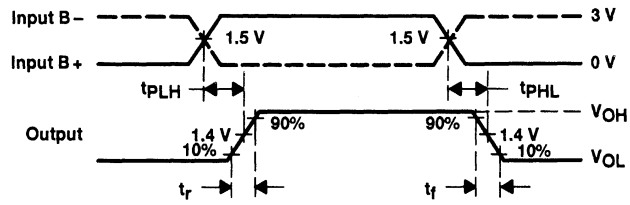
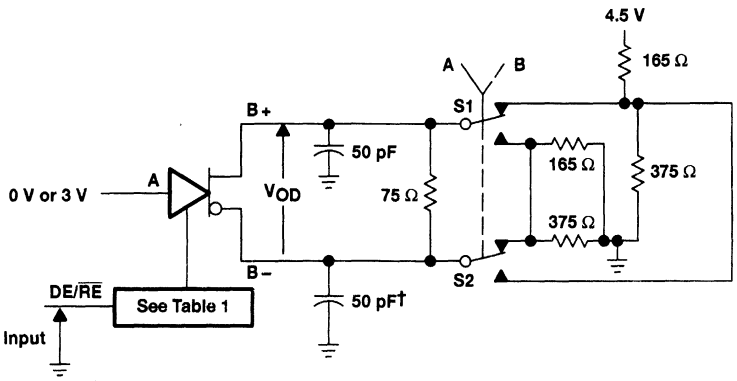


Figure 4. Receiver Delay and Transition Time Waveforms



† Includes probe and jig capacitance in two places.

Figure 5. Driver Enable and Disable Time Test Circuit

Table 1. Enabling For Driver Enable And Disable Time

DRIVER	BSR	CDE0	CDE1	CDE2	$\overline{CRE}$
1 – 8	H	H	L	L	X
9	L	H	H	H	H

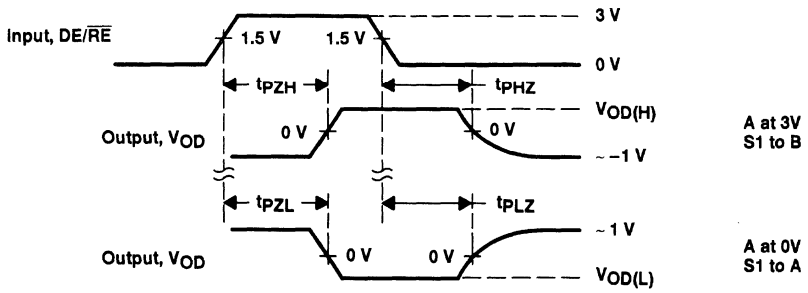
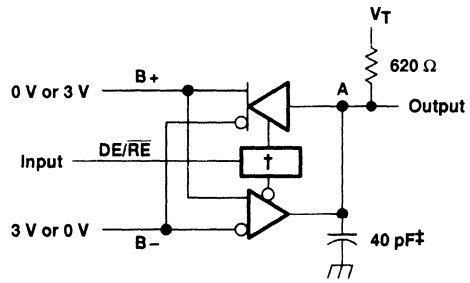


Figure 6. Driver Enable Time Waveforms

NOTES: A. All input pulses are supplied by a generator having the following characteristics: $t_r \le 6$ ns, $t_f \le 6$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50\ \Omega$.
B. All resistances are in Ω and ± 5%, unless otherwise indicated.
C. All capacitances are in pF and ± 10%, unless otherwise indicated.
D. All indicated voltages are ± 10 mV.

PARAMETER MEASUREMENT INFORMATION



† CDE0 is high, CDE1, CDE2, BSR, and $\overline{CRE}$ are low, and all others are open.
‡ Includes probe and jig capacitance.

Figure 7. Receiver Enable and Disable Time Test Circuit

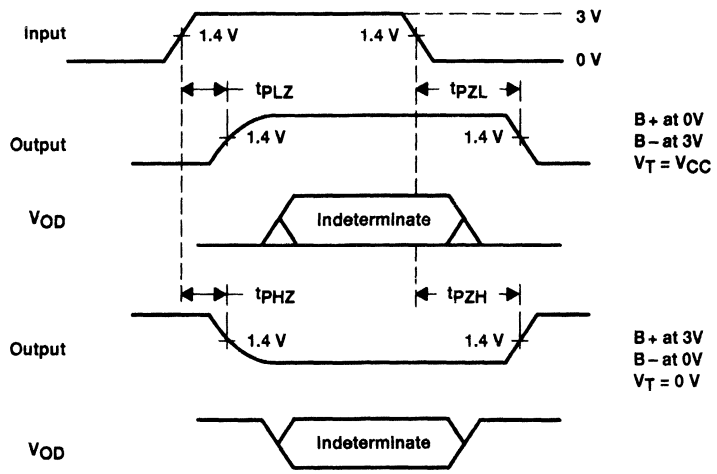


Figure 8. Receiver Enable and Disable Time Waveforms

NOTES: A. All input pulses are supplied by a generator having the following characteristics: $t_r \leq 6$ ns, $t_f \leq 6$ ns, PRR ≤ 1 MHz, duty cycle = 50%, $Z_O = 50\ \Omega$.
B. All resistances are in Ω and ± 5%, unless otherwise indicated.
C. All capacitances are in pF and ± 10%, unless otherwise indicated.
D. All indicated voltages are ± 10 mV.

TYPICAL CHARACTERISTICS

AVERAGE SUPPLY CURRENT
vs
FREQUENCY

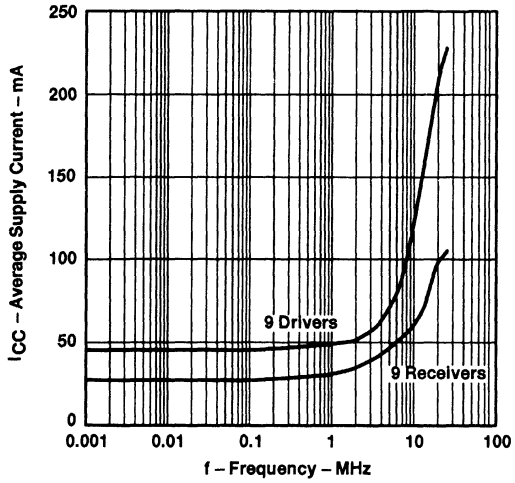


Figure 9

LOGIC INPUT CURRENT
vs
INPUT VOLTAGE

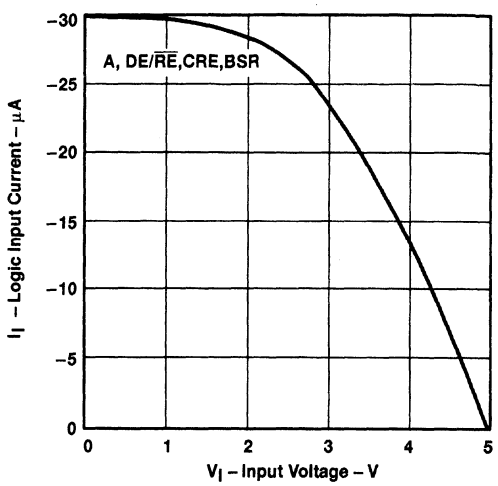


Figure 10

BUS
INPUT CURRENT
vs
INPUT VOLTAGE

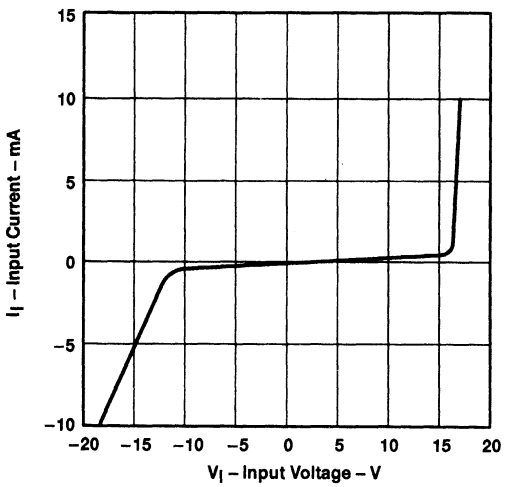


Figure 11

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

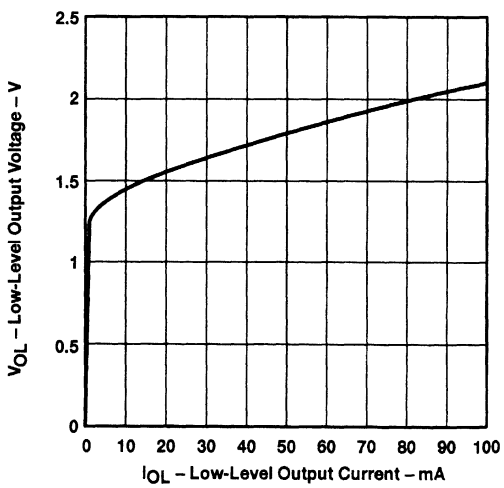


Figure 12

TYPICAL CHARACTERISTICS

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

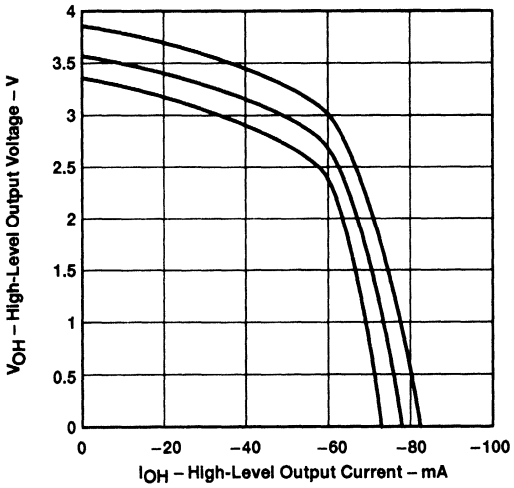


Figure 13

DRIVER
AVERAGE DIFFERENTIAL OUTPUT VOLTAGE
vs
AVERAGE CASE TEMPERATURE

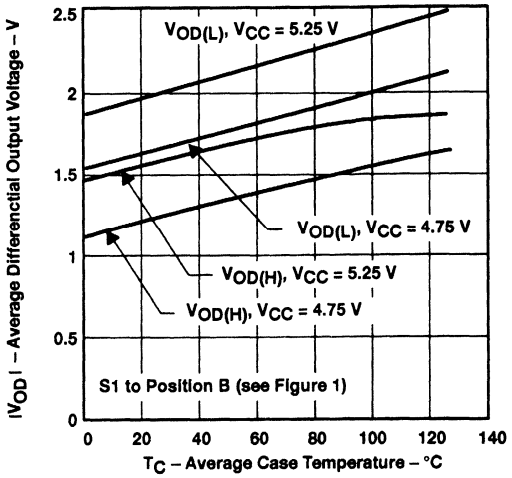


Figure 14

RECEIVER
PROPAGATION DELAY TIME
vs
CASE TEMPERATURE

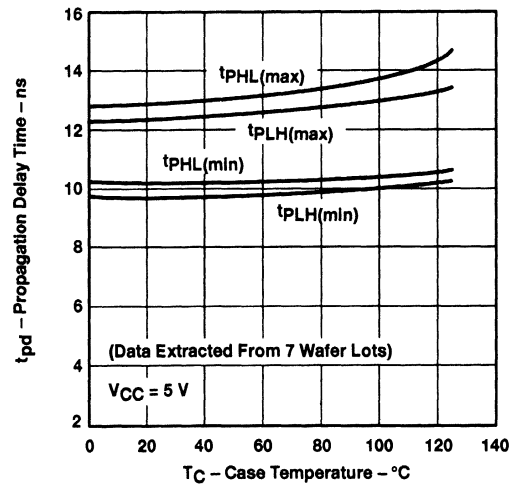


Figure 15

DRIVER
PROPAGATION DELAY TIME
vs
CASE TEMPERATURE

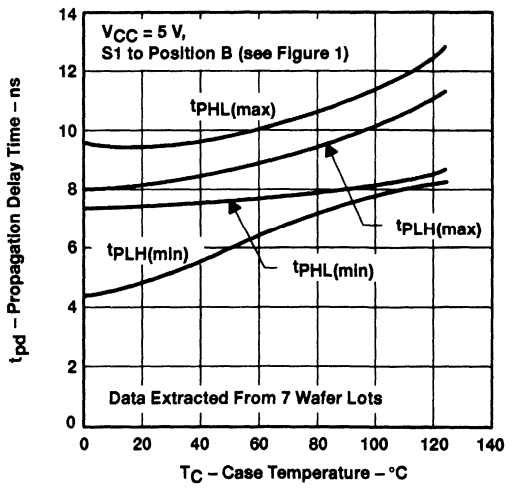


Figure 16

TYPICAL CHARACTERISTICS

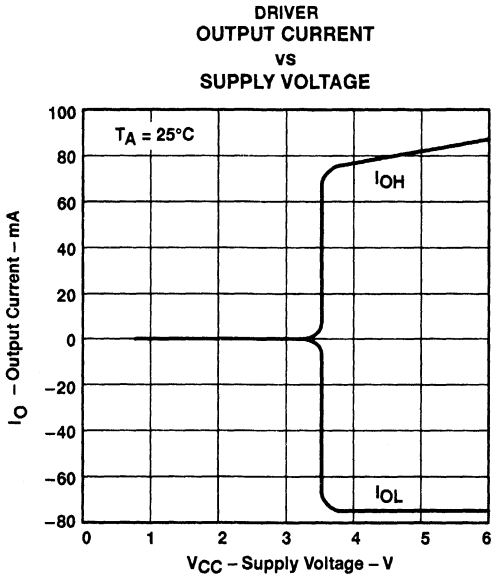


Figure 17

APPLICATION INFORMATION

Table 2. Typical Signal and Terminal Assignments

SIGNAL	TERMINAL	SCSI DATA	SCSI CONTROL	IPI DATA	IPI CONTROL
CDE0	54	DIFFSENSE	DIFFSENSE	V_{CC}	V_{CC}
CDE1	55	GND	GND	XMTA, XMTB	GND
CDE2	56	GND	GND	XMTA, XMTB	SLAVE/MASTER
BSR	2	GND	GND	GND, BSR	GND
$\overline{CRE}$	3	GND	GND	GND	V_{CC}
1A	4	DB0, DB8	ATN	AD7, BD7	NOT USED
1DE/$\overline{RE}$	5	DBE0, DBE8	INIT EN	GND	GND
2A	6	DB1, DB9	BSY	AD6, BD6	NOT USED
2DE/$\overline{RE}$	7	DBE1, DBE9	BSY EN	GND	GND
3A	8	DB2, DB10	ACK	AD5, BD5	SYNC IN
3DE/$\overline{RE}$	9	DBE2, DBE10	INIT EN	GND	GND
4A	10	DB3, DB11	RST	AD4, BD4	SLAVE IN
4DE/$\overline{RE}$	11	DBE3, DBE11	GND	GND	GND
5A	19	DB4, DB12	MSG	AD3, BD3	NOT USED
5DE/$\overline{RE}$	20	DBE4, DBE12	TARG EN	GND	GND
6A	21	DB5, DB13	SEL	AD2, BD2	SYNC OUT
6DE/$\overline{RE}$	22	DBE5, DBE13	SEL EN	GND	GND
7A	23	DB6, DB14	C/D	AD1, BD1	MASTER OUT
7DE/$\overline{RE}$	24	DBE6, DBE14	TARG EN	GND	GND
8A	25	DB7, DB15	REQ	AD0, BD0	SELECT OUT
8DE/$\overline{RE}$	26	DBE7, DBE15	TARG EN	GND	GND
9A	27	DBP0, DBP1	I/O	AP, BP	ATTENTION IN
9DE/$\overline{RE}$	28	DBPE0, DBPE1	TARG EN	XMTA, XMTB	V_{CC}

ABBREVIATIONS:

DBn = data bit n, where n = (0,1, . . . ,15)
DBEn = data bit n enable, where n = (0,1, . . . ,15)
DBP0 = parity bit for data bits 0 through 7 or IPI bus A
DBPE0 = parity bit enable for P0
DBP1 = parity bit for data bits 8 through 15 or IPI bus B
DBPE1 = parity bit enable for P1
ADn or BDn = IPI Bus A – Bit n (ADn) or Bus B – Bit n (BDn), where n = (0,1, . . . ,7)
AP or BP = IPI parity bit for bus A or bus B
XMTA or XMTB = transmit enable for IPI bus A or B
BSR = bit significant response
INIT EN = common enable for SCSI initiator mode
TARG EN = common enable for SCSI target mode

NOTE A. Signal inputs are shown as active high. When only active-low inputs are available, logic inversion is accomplished by reversing the B+ and B– connector terminal assignments.

APPLICATION INFORMATION

Function Tables

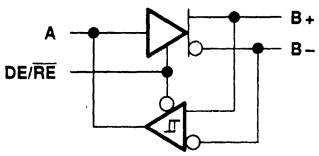
RECEIVER

INPUTS		OUTPUT
B+†	B–†	A
L	H	L
H	L	H

DRIVER

INPUT	OUTPUTS	
A	B+	B–
L	L	H
H	H	L

TRANSCEIVER

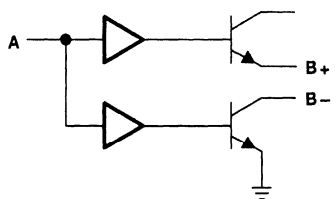


INPUTS				OUTPUTS		
DE/RE	A	B+†	B–†	A	B+	B–
L	–	L	H	L	–	–
L	–	H	L	H	–	–
H	L	–	–	–	L	H
H	H	–	–	–	H	L

DRIVER WITH ENABLE

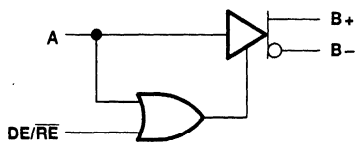
INPUTS		OUTPUTS	
DE/RE	A	B+	B–
L	L	Z	Z
L	H	Z	Z
H	L	L	H
H	H	H	L

WIRED-OR DRIVER



INPUT	OUTPUTS	
A	B+	B–
L	Z	Z
H	H	L

TWO-ENABLE INPUT DRIVER

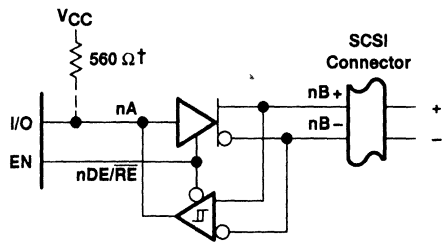


INPUTS		OUTPUTS	
DE/RE	A	B+	B–
L	L	Z	Z
L	H	H	L
H	L	L	H
H	H	H	L

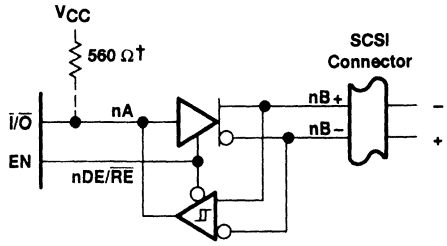
H = high level, L = low level, X = irrelevant, Z = high impedance (off)

† An H in this column represents a voltage of 200 mV or higher than the other bus input. An L represents a voltage of 200 mV or lower than the other bus input. Any voltage less than 200 mV results in an indeterminate receiver output.

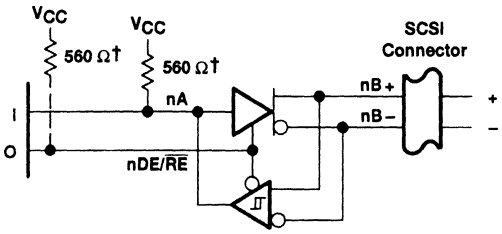
APPLICATION INFORMATION



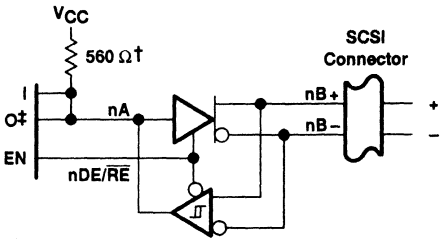
(a) ACTIVE-HIGH BIDIRECTIONAL I/O WITH SEPARATE ENABLE



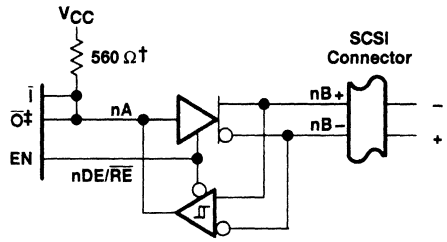
(b) ACTIVE-LOW BIDIRECTIONAL I/O WITH SEPARATE ENABLE



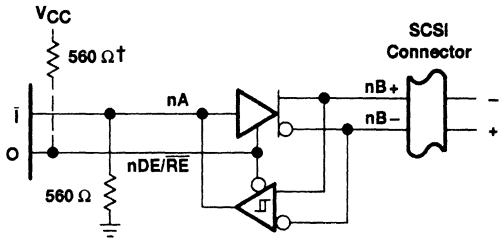
(c) WIRED-OR DRIVER AND ACTIVE-HIGH INPUT



(d) SEPARATE ACTIVE-HIGH INPUT, OUTPUT, AND ENABLE



(e) SEPARATE ACTIVE-LOW INPUT AND OUTPUT AND ACTIVE-HIGH ENABLE



(f) WIRED-OR DRIVER AND ACTIVE-LOW INPUT

† When 0 is open drain
‡ Must be open-drain or 3-state output
NOTE A. The BSR, $\overline{CRE}$, A, and DE/$\overline{RE}$ inputs have internal pullups. CDE0, CDE1, and CDE2 have internal pulldowns.

Figure 18. Typical SCSI Transceiver Connections

APPLICATION INFORMATION

channel logic configurations with control input logic

The following logic diagrams show the positive-logic representation for all combinations of control inputs. The control inputs are from MSB to LSB; the BSR, CDE0, CDE1, CDE2, and $\overline{CRE}$ bit values are shown below the diagrams. Channel 1 is at the top of the logic diagrams; channel 9 is at the bottom of the logic diagrams.

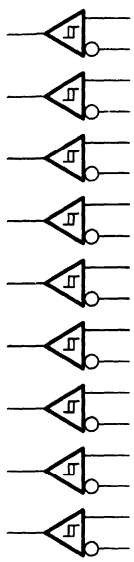


Figure 19. 00000

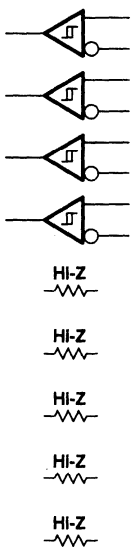


Figure 20. 00001

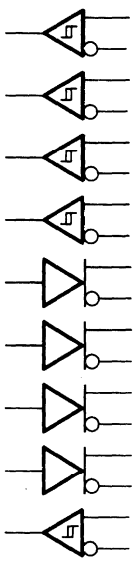


Figure 21. 00010

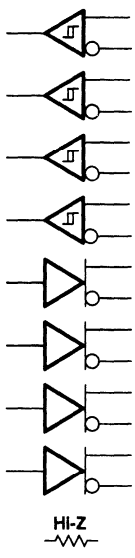


Figure 22. 00011

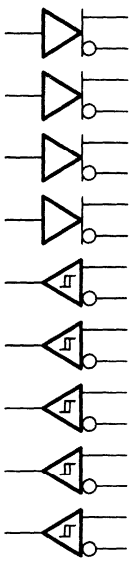


Figure 23. 00100

APPLICATION INFORMATION

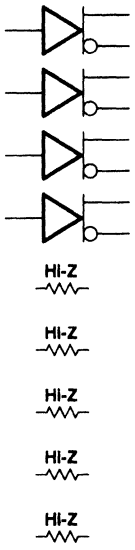


Figure 24. 00101

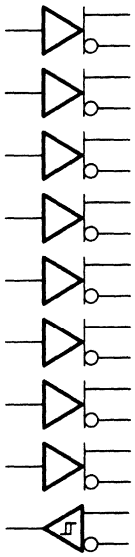


Figure 25. 00110

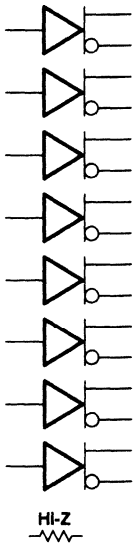


Figure 26. 00111

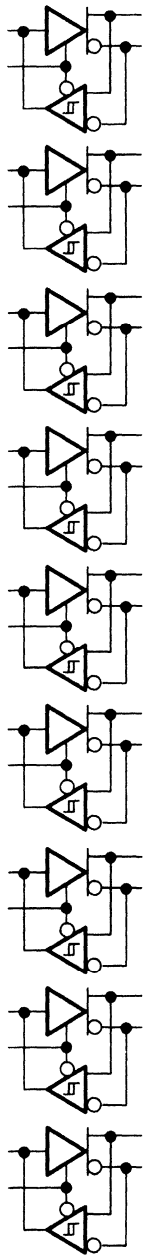


Figure 27. 01000

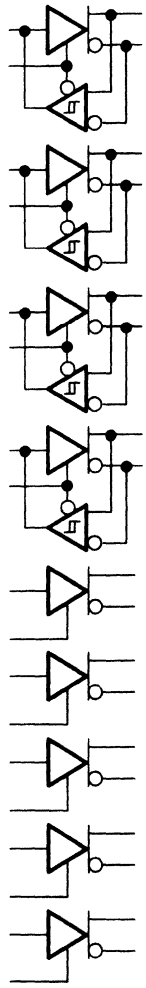


Figure 28. 01001

APPLICATION INFORMATION

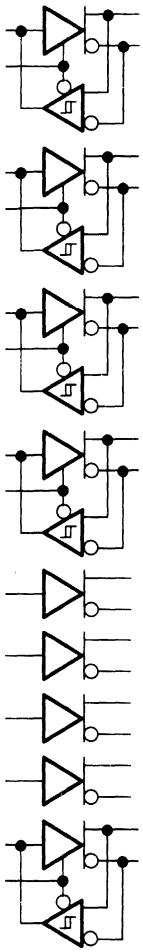


Figure 29. 01010

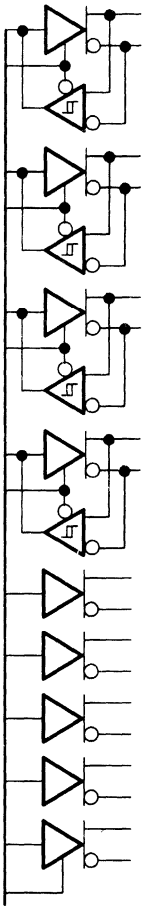


Figure 30. 01011

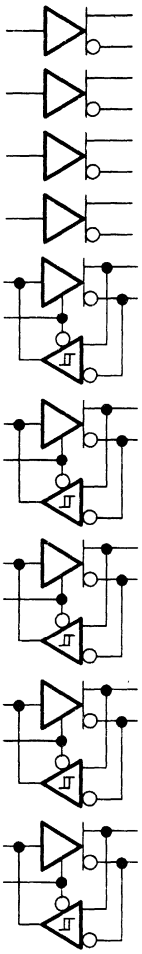


Figure 31. 01100

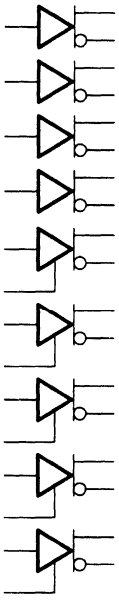


Figure 32. 01101

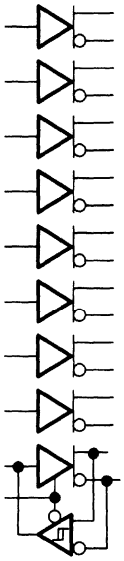


Figure 33. 01110

APPLICATION INFORMATION

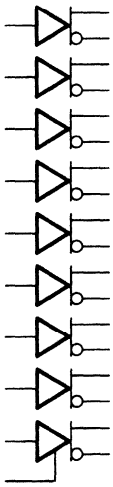


Figure 34. 01111

Figure 35. 10000 and 10001

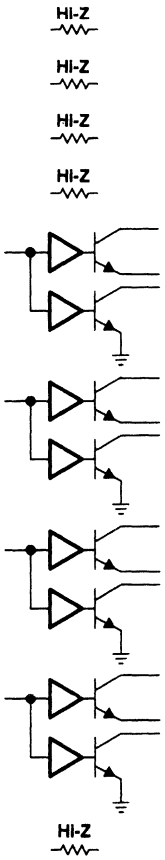


Figure 36. 10010 and 10011

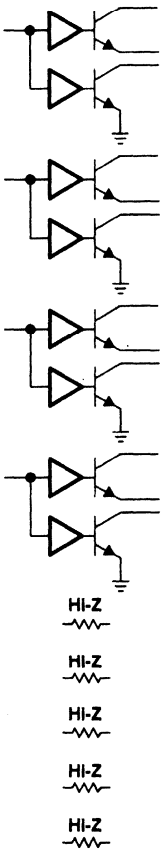


Figure 37. 10100 and 10101

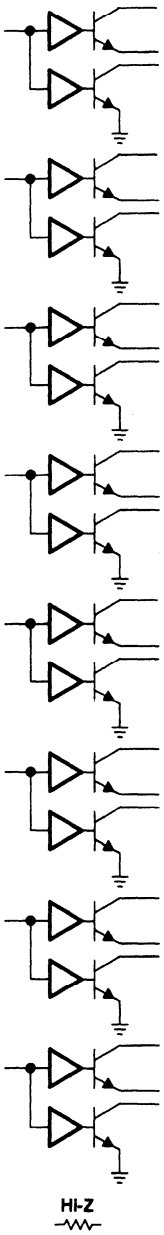


Figure 38. 10110 and 10111

APPLICATION INFORMATION

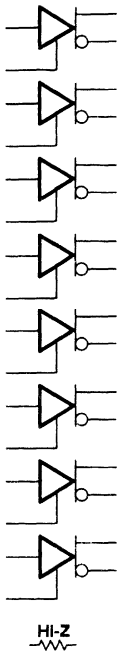


Figure 39. 11000 and 11001

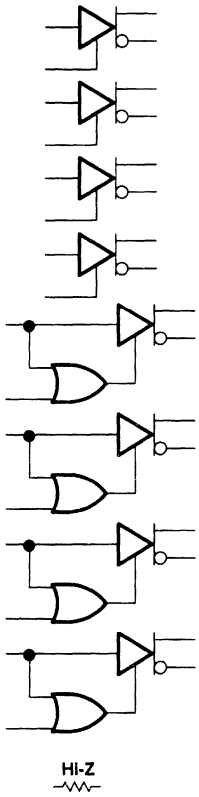


Figure 40. 11010 and 11011

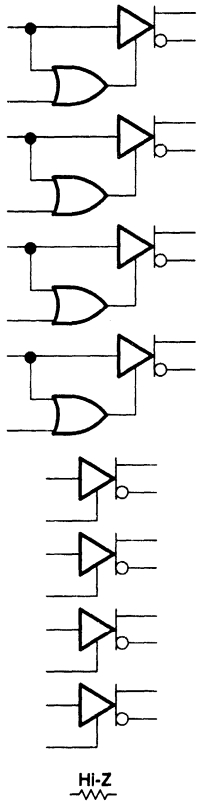


Figure 41. 11100 and 11101

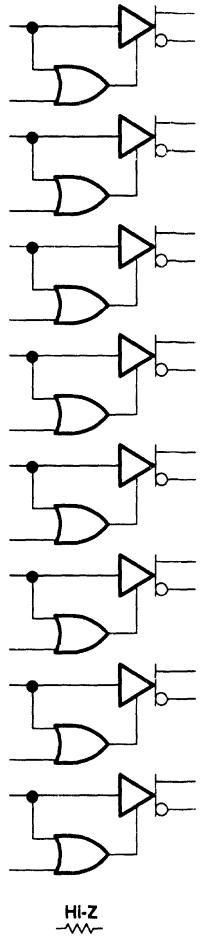


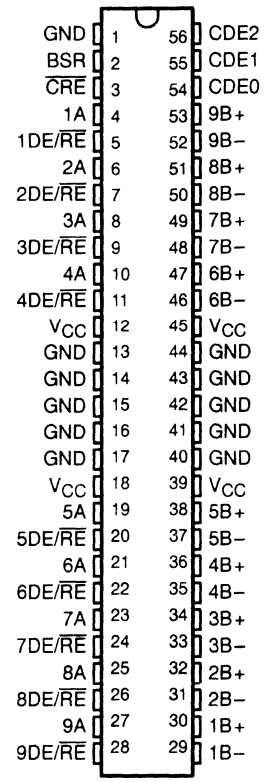
Figure 42. 11110 and 11111

SN75LBC976
9-CHANNEL DIFFERENTIAL TRANSCEIVER

SLLS133D – AUGUST 1992 – REVISED MAY 1995

- **Nine Differential Channels for the Data and Control Paths of the Differential Small Computer Systems Interface (SCSI) and Intelligent Peripheral Interface (IPI-2)**
- **Meets or Exceeds the Requirements of ANSI Standard RS-485 and ISO 8482:1987(E)**
- **Packaged in Shrink Small-Outline Package With 25-mil Terminal Pitch**
- **Designed to Operate at 10 Million Transfers Per Second**
- **Low Disabled Supply Current 1.4 mA Typical**
- **Thermal-Shutdown Protection**
- **Power-Up/Power-Down Glitch Protection**
- **Positive and Negative Output-Current Limiting**
- **Open-Circuit Fail-Safe Receiver Design**

DL PACKAGE
(TOP VIEW)



Pins 13 through 17 and 40 through 44 are connected together to the package lead frame and signal ground.

description

The SN75LBC976 is a nine-channel differential transceiver based on the 75LBC176 LinASIC™ cell. Use of TI's LinBiCMOS™† process technology allows the power reduction necessary to integrate nine differential transceivers. On-chip enabling logic makes this device applicable for the data path (eight data bits plus parity) and the control path (nine bits) for both the Small Computer Systems Interface (SCSI) and the Intelligent Peripheral Interface (IPI-2) standard data interfaces.

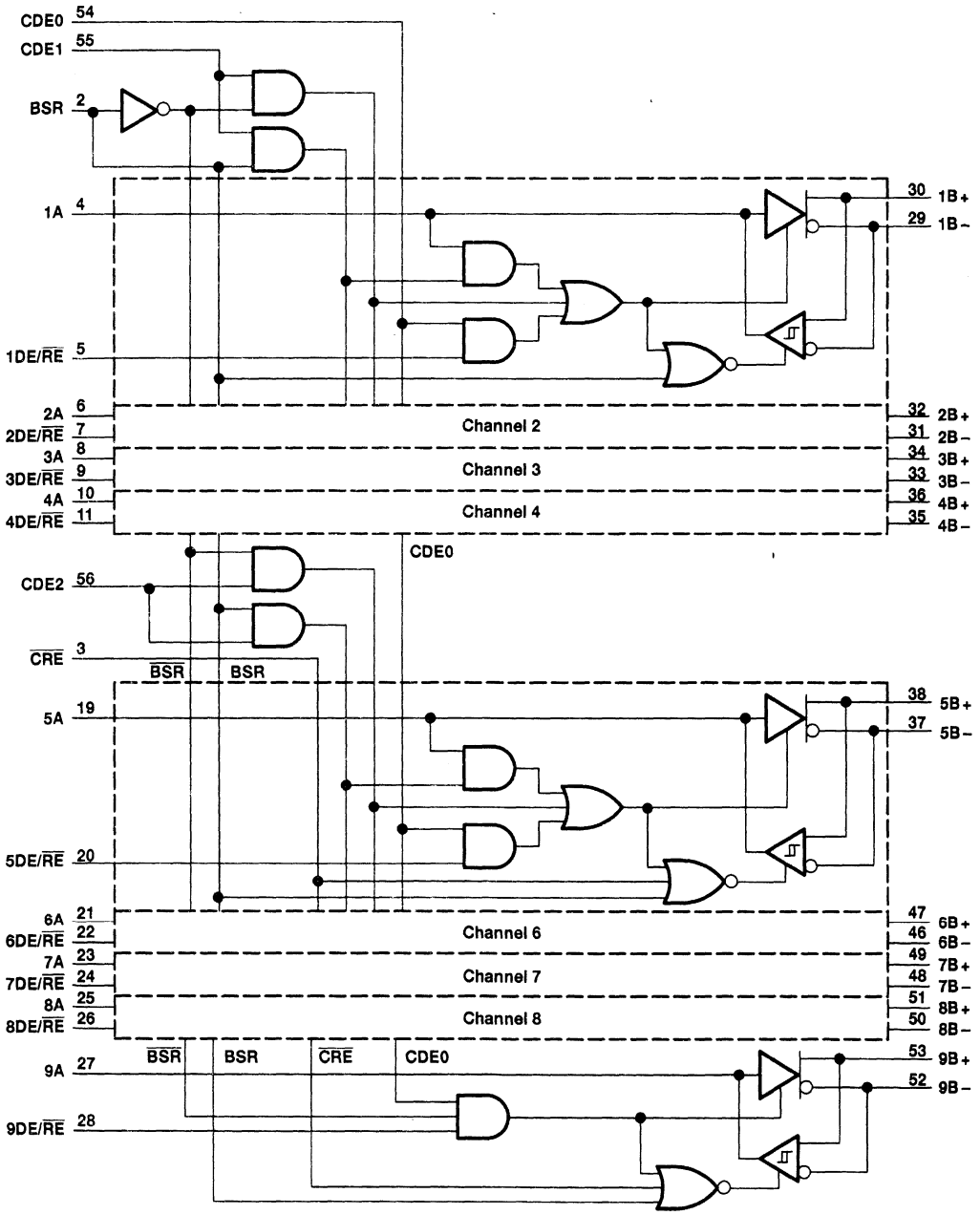
The SN75LBC976 is packaged in a shrink small-outline package (DL) with improved thermal characteristics using heat-sink terminals. This package is ideal for low-profile, space-restricted applications such as hard disk drives.

The switching speed and testing capabilities of the SN75LBC976 are sufficient to transfer data over the data bus at 10 million transfers per second. Each of the nine channels conforms to the requirements of the ANSI RS-485 and ISO 8482:1987(E) standards referenced by ANSI X3.129-1986 (IPI), ANSI X3.131-1993 (SCSI-2), and the proposed SCSI-3 standards.

The SN75LBC976 is characterized for operation from 0°C to 70°C.

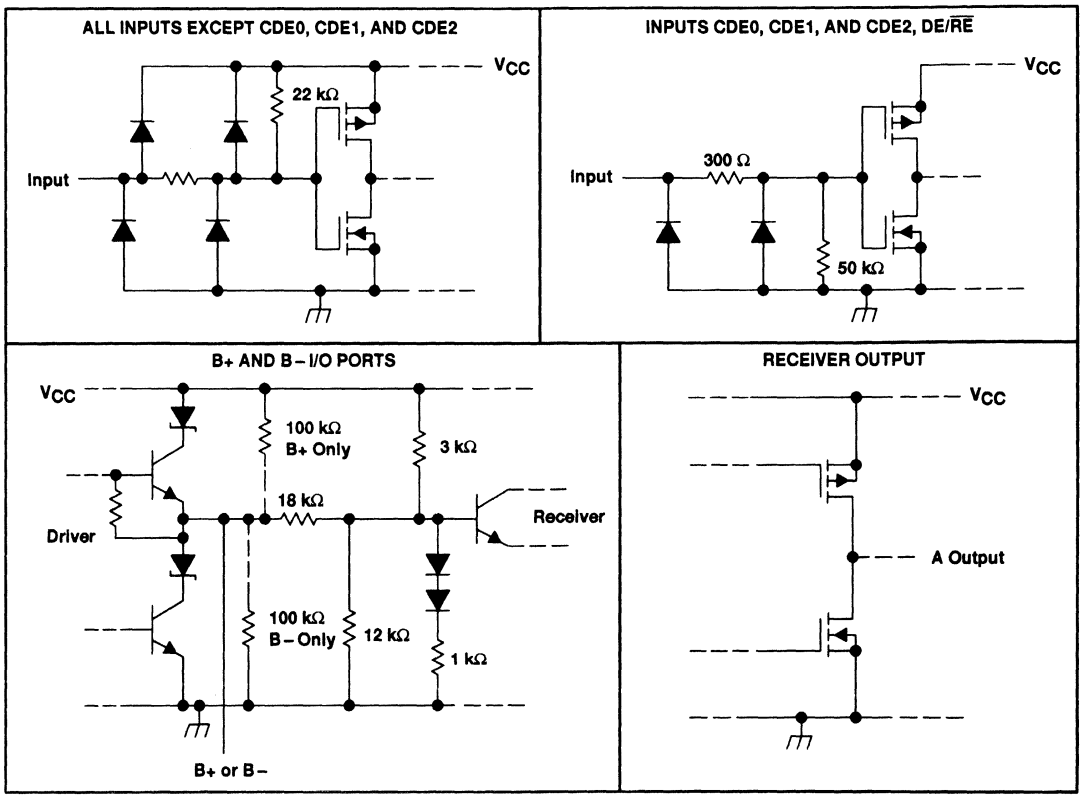
† Patent pending
LinASIC and LinBiCMOS are trademarks of Texas Instruments Incorporated.

logic diagram (positive logic)†



† For additional logic diagrams, see Application Information, Table 1 and Figures 7 through 44.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	−0.3 V to 7 V
Bus voltage range	−10 V to 15 V
Data I/O and control (A-side) voltage range	−0.3 V to 7 V
Continuous power dissipation	internally limited
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common-mode), V_O, V_I, or V_{IC}	B+ or B–			12	V
				–7	
High-level input voltage, V_{IH}	All except B+ and B–	2			V
Low-level input voltage, V_{IL}	All except B+ and B–			0.8	V
High-level output current, I_{OH}	B+ or B–			–60	mA
	A			–8	mA
Low-level output current, I_{OL}	B+ or B–			60	mA
	A			8	mA
Operating free-air temperature, T_A		0		70	°C

device electrical characteristics over recommended ranges of operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_{IH}	High-level input current	BSR, A, DE/$\overline{RE}$, and $\overline{CRE}$	See Figure 1	V_{IH} = 2 V			–200	µA
		CDE0, CDE1, and CDE2					100	µA
I_{IL}	Low-level input current	BSR, A, DE/$\overline{RE}$, and $\overline{CRE}$		V_{IL} = 0.8 V			–200	µA
		CDE0, CDE1, and CDE2					100	µA
I_{CC}	Supply current	All drivers and receivers disabled	BSR and CDE0 at 5 V, Other inputs at 0 V			1.4	3	mA
		All receivers enabled	No load, V_{ID} = 5 V, All other inputs at 0 V			29	45	mA
		All drivers enabled	BSR at 0 V, No load, All other inputs at 5 V			4.8	10	mA
C_O	Bus port output capacitance		B+ or B–			16		pF
C_{pd}	Power dissipation capacitance‡		One driver			460		pF
			One receiver			50		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ C_{pd} determines the no-load dynamic current consumption; $I_S = C_{pd} \cdot V_{CC} \cdot f + I_{CC}$.

driver electrical characteristics over recommended ranges of operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OD} \rvert$	Differential output voltage	V_{test} = –7 V to 12 V, See Figure 2	1	2		V
I_{OS}	Output short-circuit current	See Figure 3			±250	mA
I_{OZ}	High-impedance-state output current	See receiver input current				

receiver electrical characteristics over recommended ranges of operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{ID} = 200 mV, See Figure 1	I_{OH} = −8 mA,	2.5			V
V_{OL}	Low-level output voltage		V_{ID} = −200 mV, See Figure 1	I_{OL} = 8 mA,			0.8	V
V_{IT+}	Positive-going input threshold voltage		I_{OH} = −8 mA,	See Figure 1			0.2	V
V_{IT-}	Negative-going input threshold voltage		I_{OL} = 8 mA,	See Figure 1	−0.2			V
V_{hys}	Receiver input hysteresis voltage ($V_{IT+} - V_{IT-}$)					45		mV
I_I	Receiver input current	B+ and B−	V_I = 12 V, Other input at 0 V,	V_{CC} = 5 V, See Figure 1		0.7	1	mA
			V_I = 12 V, Other input at 0 V,	V_{CC} = 0, See Figure 1		0.8	1	mA
			V_I = −7 V, Other input at 0 V,	V_{CC} = 5 V, See Figure 1		−0.5	−0.8	mA
			V_I = −7 V, Other input at 0 V,	V_{CC} = 0, See Figure 1		−0.4	−0.8	mA
I_{OZ}	High-impedance-state output current		See Figure 1	V_O = GND			−200	µA
				V_O = V_{CC}			50	

driver switching characteristics over recommended operating conditions (unless otherwise noted) (see Figure 4)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$t_{d(OD)}$	Differential delay time, high- to low-level output ($t_{d(ODH)}$) or low- to high-level output ($t_{d(ODL)}$)			7.6		19.6	ns
		V_{CC} = 5 V,	T_A = 25°C	9.1		17.1	
		V_{CC} = 5 V,	T_A = 70°C	11.5		19.5	
$t_{sk(lim)}$	Skew limit, the maximum difference in propagation delay times between any two drivers on any two devices					12	ns
		V_{CC} = 5 V,	See Note 2			8	
$t_{sk(p)}$	Pulse skew ($\lvert t_{d(ODL)} - t_{d(ODH)} \rvert$)				0	6	ns
t_t	Transition time (t_r or t_f)				10		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 2: This specification applies to any 5°C band within the operating temperature range.

receiver switching characteristics over recommended operating conditions (see Figure 5) (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{pd}	Propagation delay time, high- to low-level output (t_{PLH}) or low- to high-level output (t_{PHL})			21.5		33	ns
		V_{CC} = 5 V,	T_A = 25°C	22.6		31.6	
		V_{CC} = 5 V,	T_A = 70°C	23.4		32.4	
$t_{sk(lim)}$	Skew limit, the maximum difference in propagation delay times between any two drivers on any two devices					12	ns
		V_{CC} = 5 V,	See Note 2			9	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)				2	6	ns
t_t	Transition time (t_r or t_f)				3		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: This specification applies to any 5°C band within the operating temperature range.

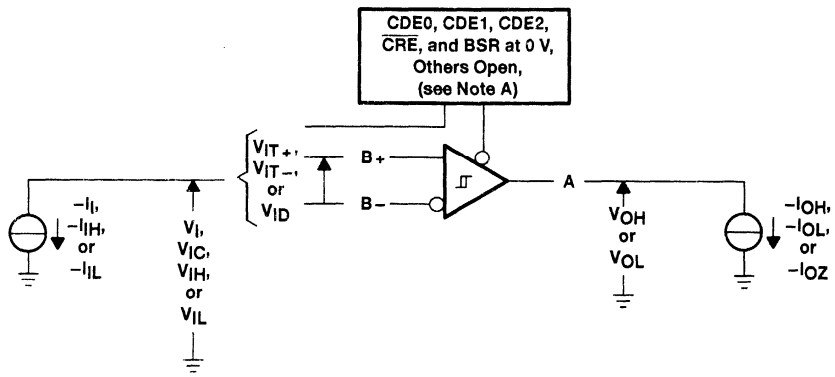
transceiver switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{en(RXL)}$	Enable time, transmit-to-receive to low-level output	See Figure 6		150	ns
$t_{en(RXH)}$	Enable time, transmit-to-receive to high-level output			150	ns
$t_{en(TXL)}$	Enable time, receive-to-transmit to low-level output			80	ns
$t_{en(TXH)}$	Enable time, receive-to-transmit to high-level output			80	ns
t_{su}	Setup time, CDE0, CDE1, CDE2, BSR, or $\overline{CRE}$ to active input(s) or output(s)		150		ns

thermal characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	Board mounted, No air flow		50		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance			12		°C/W

PARAMETER MEASUREMENT INFORMATION



NOTE A: For the I_{OZ} measurement, BSR is at 5 V and CDE0, CDE1, and CDE2 are at 0 V.

Figure 1. Receiver Test Circuit and Input Conditions

PARAMETER MEASUREMENT INFORMATION

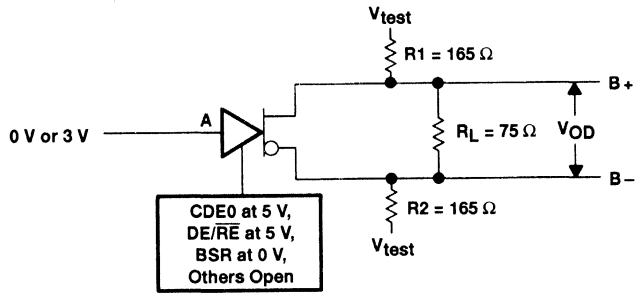
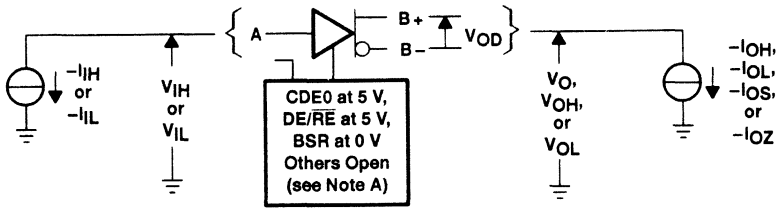


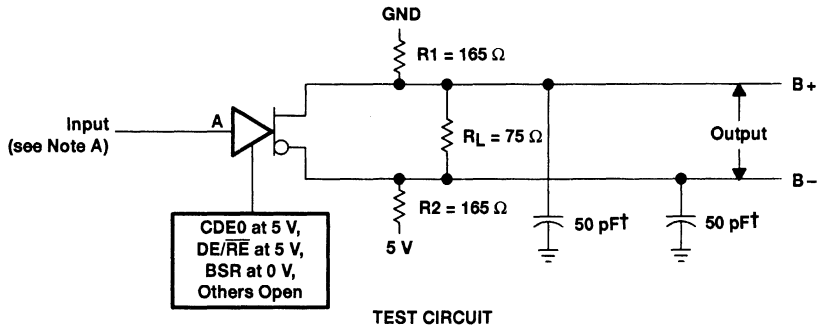
Figure 2. Driver V_{OD} Test Circuit



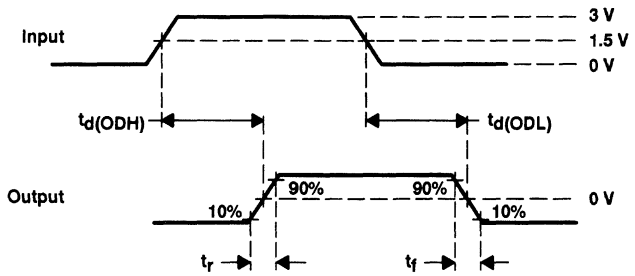
NOTE A: For the I_{OZ} test, the BSR input is at 5 V and all others are at 0 V.

Figure 3. Driver Test Circuit and Input Conditions

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



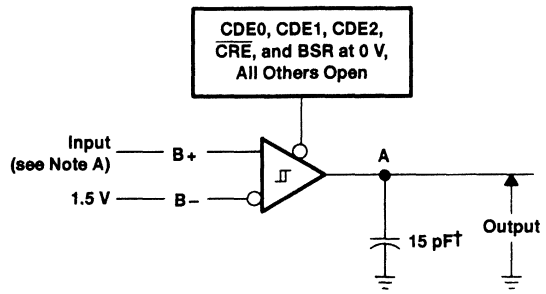
VOLTAGE WAVEFORMS

† Includes probe and jig capacitance.

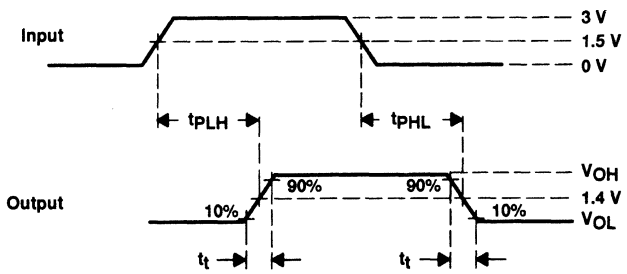
NOTE A: The input is provided by a pulse generator with an output of 0 to 3 V, PRR of 1 MHz, 50% duty cycle, t_r and t_f < 6 ns, and Z_O = 50 Ω.

Figure 4. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



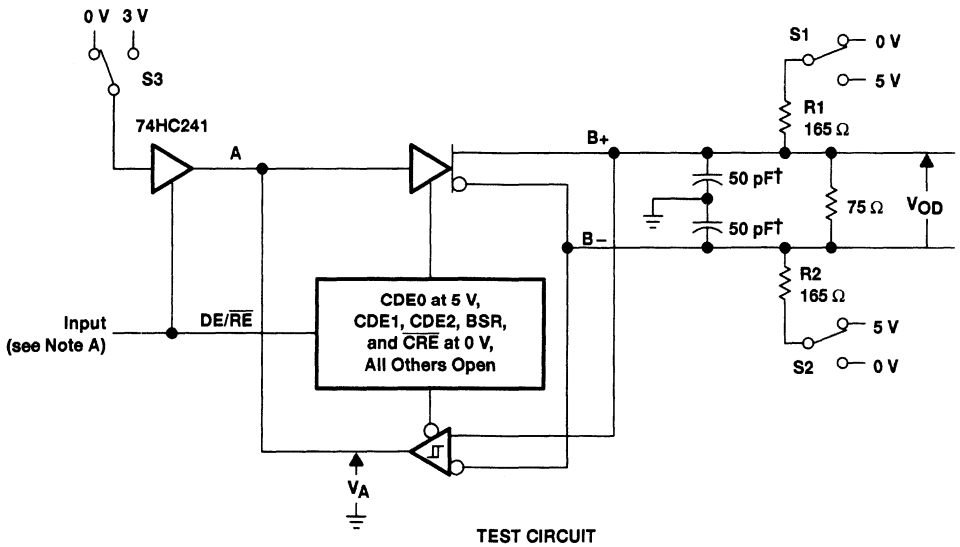
VOLTAGE WAVEFORMS

† Includes probe and jig capacitance.

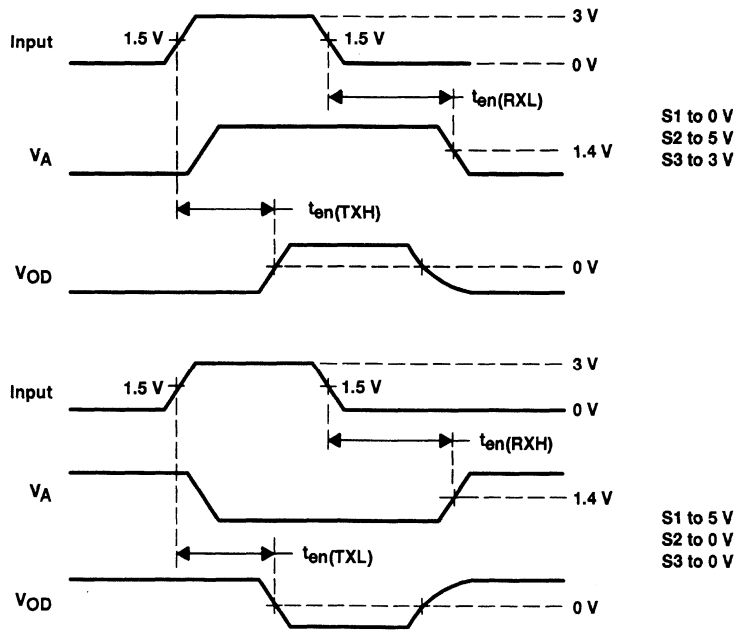
NOTE A: The input is provided by a pulse generator with an output of 0 to 3 V, PRR of 1 MHz, 50% duty cycle, t_r and $t_f < 6$ ns, and $Z_O = 50\ \Omega$.

Figure 5. Receiver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

† Includes probe and jig capacitance.

NOTE A: The input is provided by a pulse generator with an output of 0 to 3 V, PRR of 1 MHz, 50% duty cycle, t_r and t_f < 6 ns, and Z_O = 50 Ω.

Figure 6. Enable Time Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

AVERAGE SUPPLY CURRENT
vs
FREQUENCY

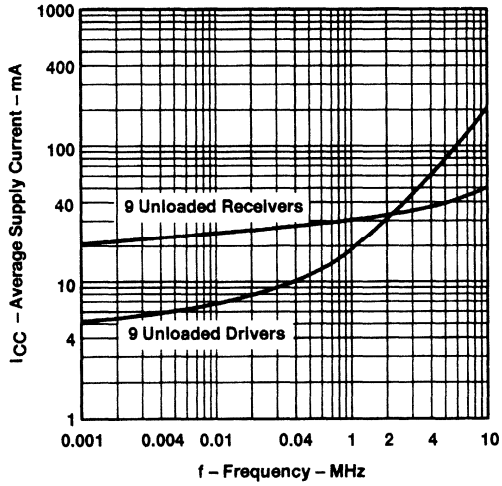


Figure 7

INPUT CURRENT
vs
INPUT VOLTAGE

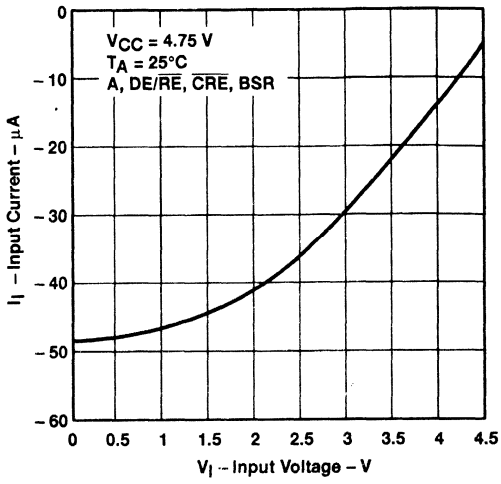


Figure 8

INPUT CURRENT
vs
INPUT VOLTAGE

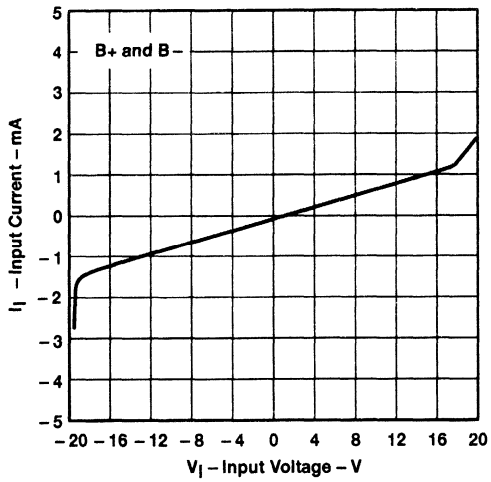


Figure 9

TYPICAL CHARACTERISTICS

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

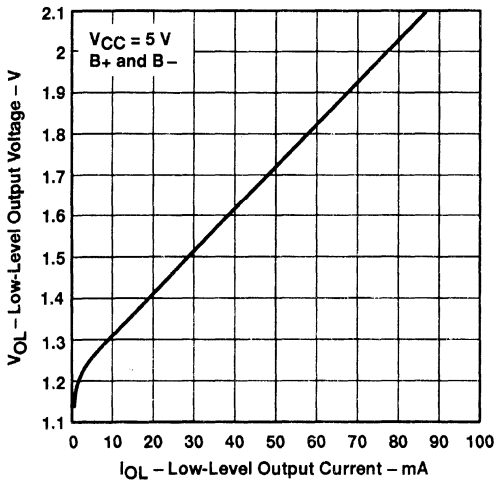


Figure 10

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

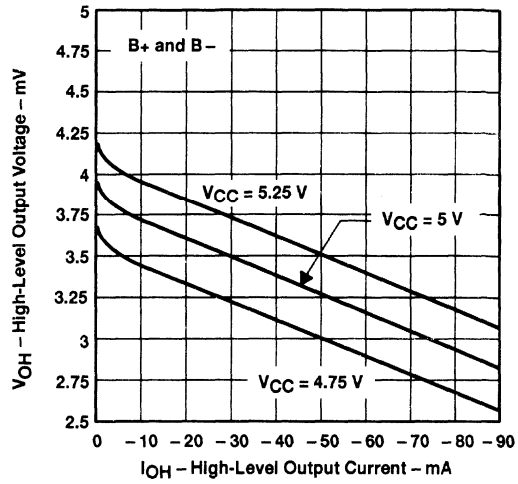


Figure 11

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

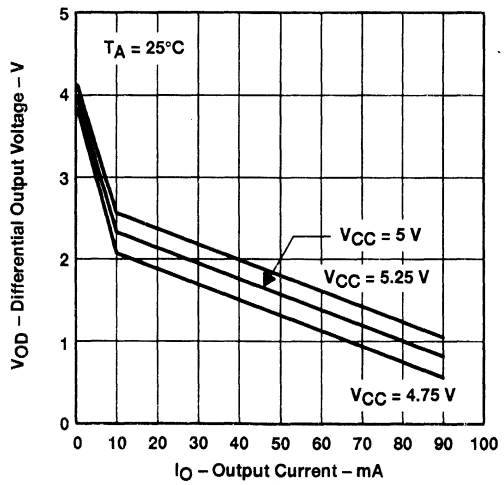


Figure 12

TYPICAL CHARACTERISTICS

DRIVER
LOW-LEVEL OUTPUT CURRENT
vs
SUPPLY VOLTAGE

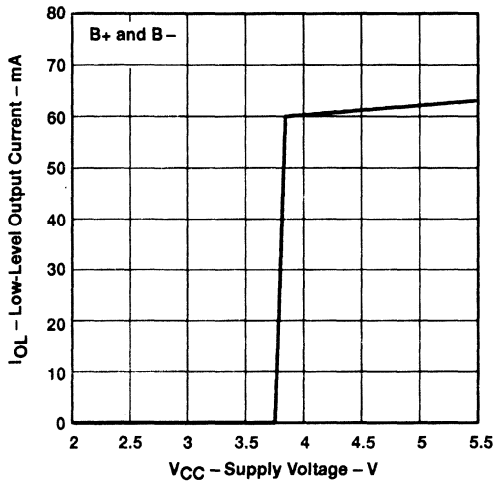


Figure 13

DRIVER
HIGH-LEVEL OUTPUT CURRENT
vs
SUPPLY VOLTAGE

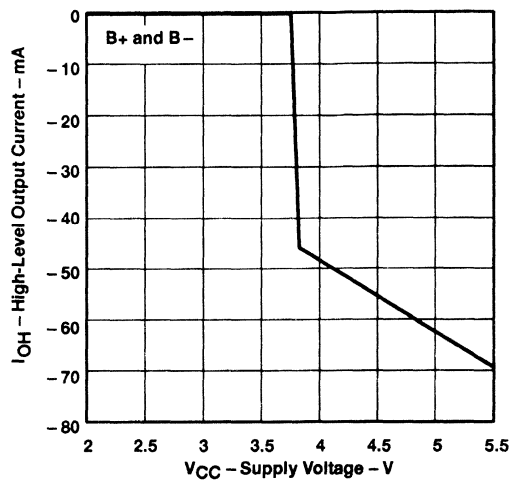


Figure 14

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

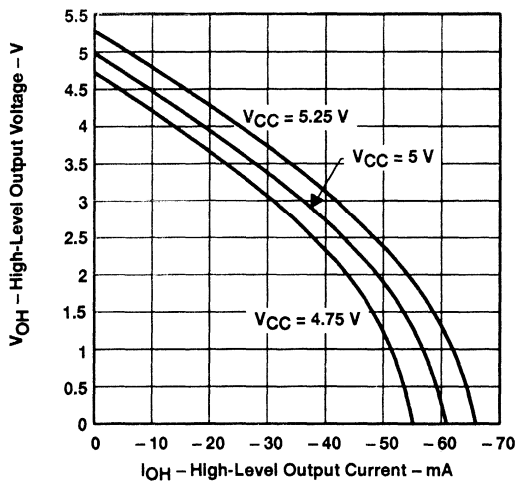


Figure 15

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

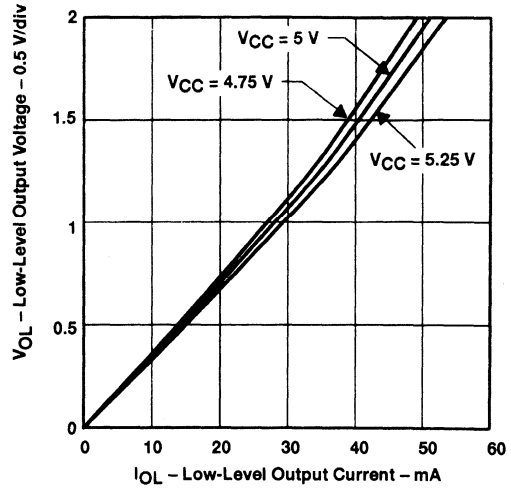


Figure 16

TYPICAL CHARACTERISTICS

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

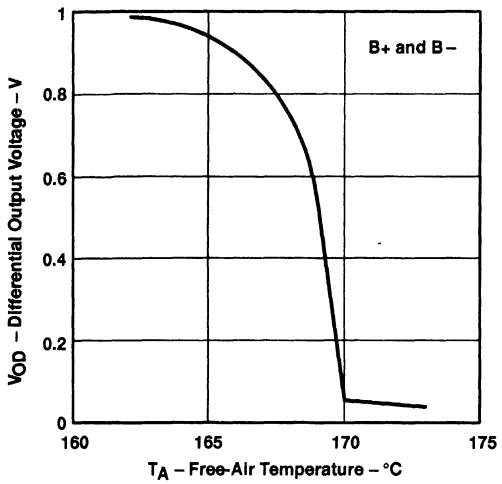


Figure 17

RECEIVER
PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

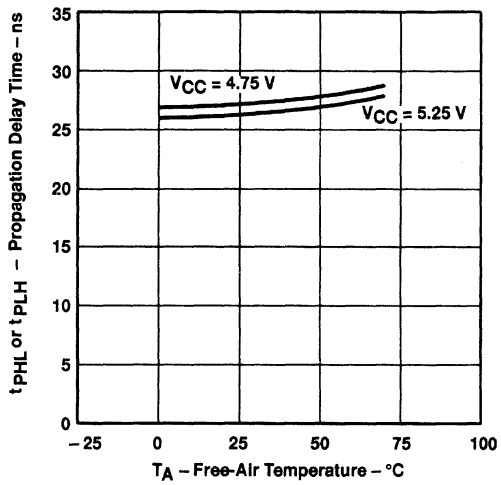


Figure 18

DRIVER
PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

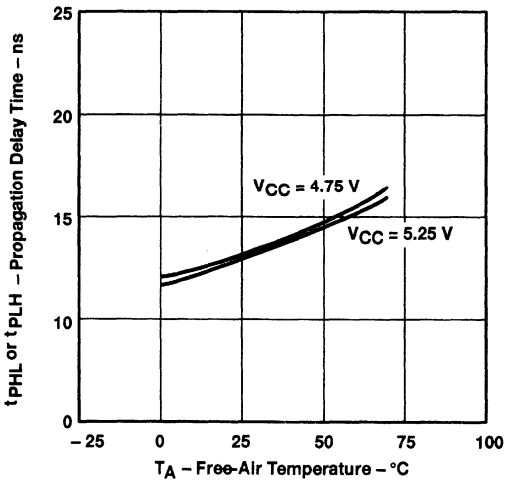


Figure 19

APPLICATION INFORMATION

Table 1. Typical Signal and Terminal Assignments

SIGNAL	TERMINAL	SCSI DATA	SCSI CONTROL	IPI DATA	IPI CONTROL
CDE0	54	DIFFSENSE	DIFFSENSE	V_{CC}	V_{CC}
CDE1	55	GND	GND	XMTA, XMTB	GND
CDE2	56	GND	GND	XMTA, XMTB	SLAVE/MASTER
BSR	2	GND	GND	GND, BSR	GND
$\overline{CRE}$	3	GND	GND	GND	V_{CC}
1A	4	DB0, DB8	ATN	AD7, BD7	NOT USED
1DE/$\overline{RE}$	5	DBE0, DBE8	INIT EN	GND	GND
2A	6	DB1, DB9	BSY	AD6, BD6	NOT USED
2DE/$\overline{RE}$	7	DBE1, DBE9	BSY EN	GND	GND
3A	8	DB2, DB10	ACK	AD5, BD5	SYNC IN
3DE/$\overline{RE}$	9	DBE2, DBE10	INIT EN	GND	GND
4A	10	DB3, DB11	RST	AD4, BD4	SLAVE IN
4DE/$\overline{RE}$	11	DBE3, DBE11	GND	GND	GND
5A	19	DB4, DB12	MSG	AD3, BD3	NOT USED
5DE/$\overline{RE}$	20	DBE4, DBE12	TARG EN	GND	GND
6A	21	DB5, DB13	SEL	AD2, BD2	SYNC OUT
6DE/$\overline{RE}$	22	DBE5, DBE13	SEL EN	GND	GND
7A	23	DB6, DB14	C/D	AD1, BD1	MASTER OUT
7DE/$\overline{RE}$	24	DBE6, DBE14	TARG EN	GND	GND
8A	25	DB7, DB15	REQ	AD0, BD0	SELECT OUT
8DE/$\overline{RE}$	26	DBE7, DBE15	TARG EN	GND	GND
9A	27	DBP0, DBP1	I/O	AP, BP	ATTENTION IN
9DE/$\overline{RE}$	28	DBPE0, DBPE1	TARG EN	XMTA, XMTB	V_{CC}

ABBREVIATIONS:

DBn, data bit n, where n = (0,1, . . . ,15)
DBEn, data bit n enable, where n = (0,1, . . . ,15)
DBP0, parity bit for data bits 0 through 7 or IPI bus A
DBPE0, parity bit enable for P0
DBP1, parity bit for data bits 8 through 15 or IPI bus B
DBPE1, parity bit enable for P1
ADn or BDn, IPI Bus A – Bit n (ADn) or Bus B – Bit n (BDn), where n = (0,1, . . . ,7)
AP or BP, IPI parity bit for bus A or bus B
XMTA or XMTB, transmit enable for IPI bus A or B
BSR, bit significant response
INIT EN, common enable for SCSI initiator mode
TARG EN, common enable for SCSI target mode

NOTE: Signal inputs are shown as active high. If only active-low inputs are available, logic inversion is accomplished by reversing the B+ and B– connecter terminal assignments.

APPLICATION INFORMATION

Function Tables

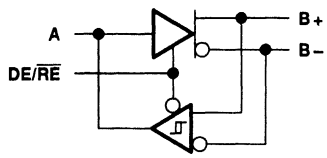
RECEIVER

INPUTS		OUTPUT
B+†	B–†	A
L	H	L
H	L	H

DRIVER

INPUT	OUTPUTS	
A	B+	B–
L	L	H
H	H	L

TRANSCEIVER

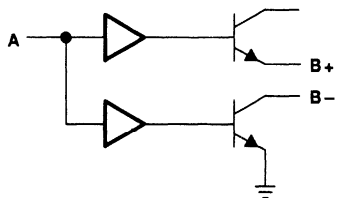


INPUTS				OUTPUTS		
DE/RE	A	B+†	B–†	A	B+	B–
L	–	L	H	L	–	–
L	–	H	L	H	–	–
H	L	–	–	–	L	H
H	H	–	–	–	H	L

DRIVER WITH ENABLE

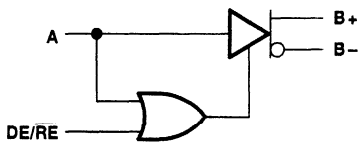
INPUTS		OUTPUTS	
DE/RE	A	B+	B–
L	L	Z	Z
L	H	Z	Z
H	L	L	H
H	H	H	L

WIRED-OR DRIVER



INPUT	OUTPUTS	
A	B+	B–
L	Z	Z
H	H	L

TWO-ENABLE INPUT DRIVER

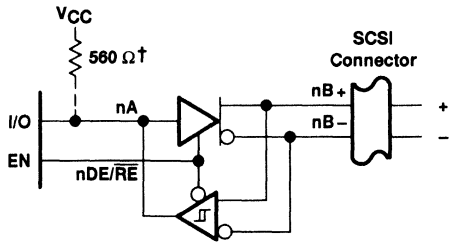


INPUTS		OUTPUTS	
DE/RE	A	B+	B–
L	L	Z	Z
L	H	H	L
H	L	L	H
H	H	H	L

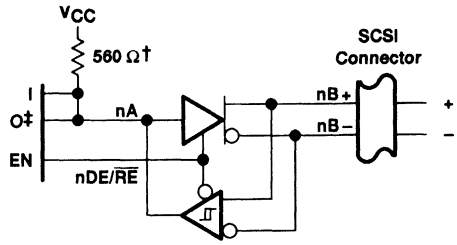
H = high level, L = low level, X = irrelevant, Z = high impedance (off)

† An H in this column represents a voltage 200 mV higher than the other bus input. An L represents a voltage 200 mV lower than the other bus input. Any voltage less than 200 mV results in an indeterminate receiver output.

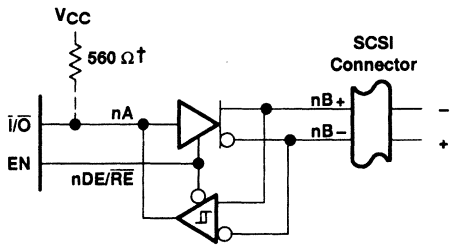
APPLICATION INFORMATION



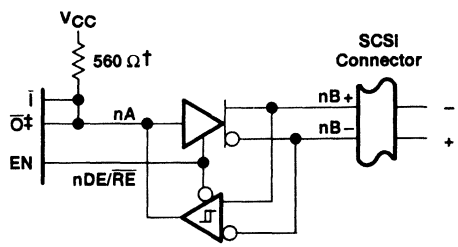
(a) ACTIVE-HIGH BIDIRECTIONAL I/O WITH SEPARATE ENABLE



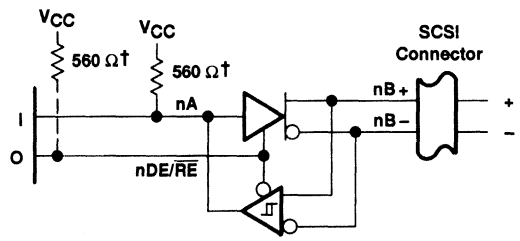
(d) SEPARATE ACTIVE-HIGH INPUT, OUTPUT, AND ENABLE



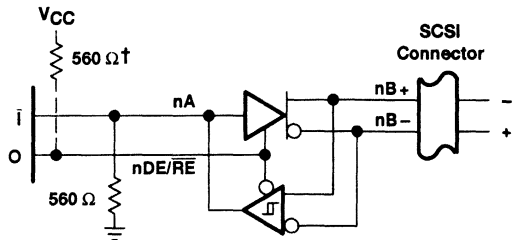
(b) ACTIVE-LOW BIDIRECTIONAL I/O WITH SEPARATE ENABLE



(e) SEPARATE ACTIVE-LOW INPUT AND OUTPUT AND ACTIVE-HIGH ENABLE



(c) WIRED-OR DRIVER AND ACTIVE-HIGH INPUT



(f) WIRED-OR DRIVER AND ACTIVE-LOW INPUT

† If 0, is open drain
‡ Must be open-drain or 3-state output
NOTE: The BSR, $\overline{CRE}$, A, and DE/$\overline{RE}$ inputs have internal pullups. CDE0, CDE1, and CDE2 have internal pulldowns.

Figure 20. Typical SCSI Transceiver Connections

APPLICATION INFORMATION

channel logic configurations with control input logic

The following logic diagrams show the positive-logic representation for all combinations of control inputs. The control inputs are from MSB to LSB; BSR, CDE0, CDE1, CDE2, and $\overline{CRE}$, and are shown below the diagrams. Channel 1 is at the top and channel 9 is at the bottom of the logic diagrams.

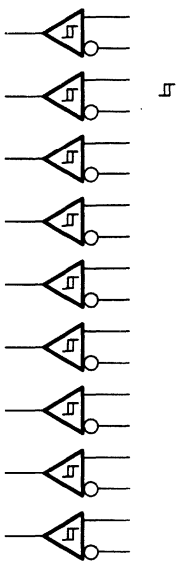


Figure 21. 00000

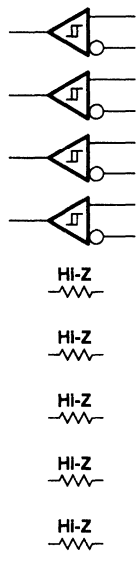


Figure 22. 00001

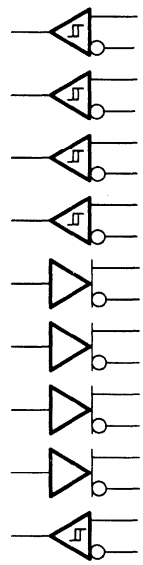


Figure 23. 00010

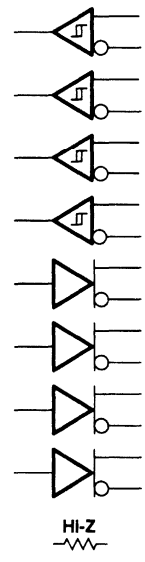


Figure 24. 00011

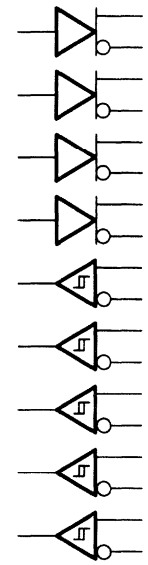


Figure 25. 00100

APPLICATION INFORMATION

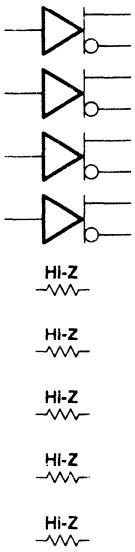


Figure 26. 00101

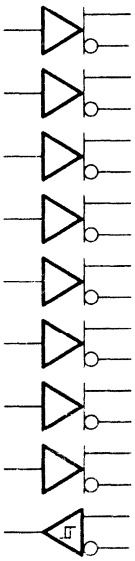


Figure 27. 00110

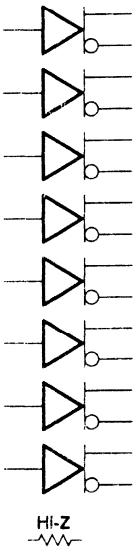


Figure 28. 00111

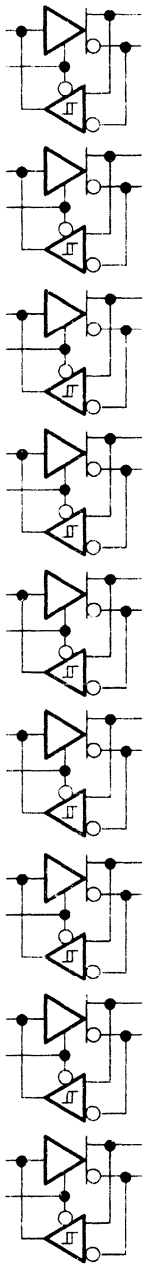


Figure 29. 01000

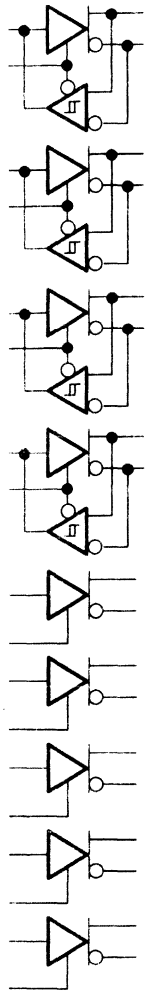


Figure 30. 01001

APPLICATION INFORMATION

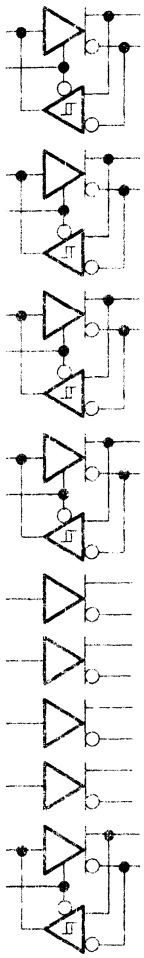


Figure 31. 01010

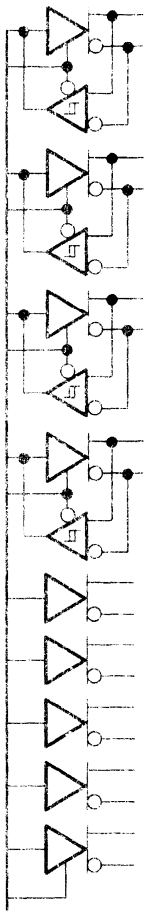


Figure 32. 01011

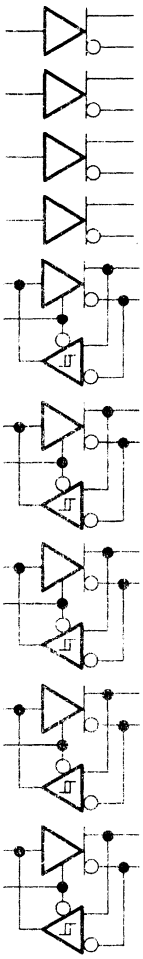


Figure 33. 01100

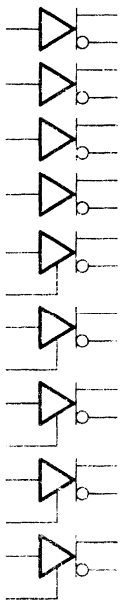


Figure 34. 01101

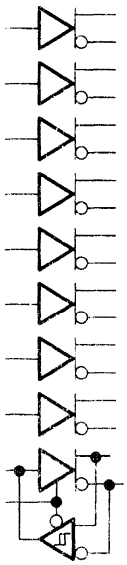


Figure 35. 01110

APPLICATION INFORMATION

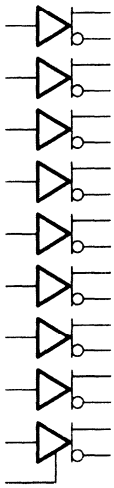


Figure 36. 01111

Figure 37. 10000 and 10001

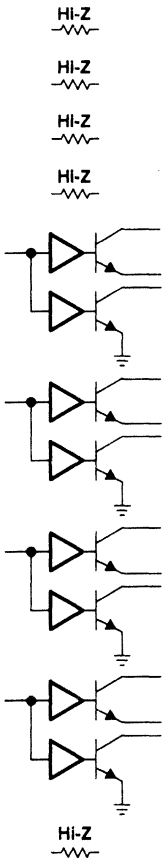


Figure 38. 10010 and 10011

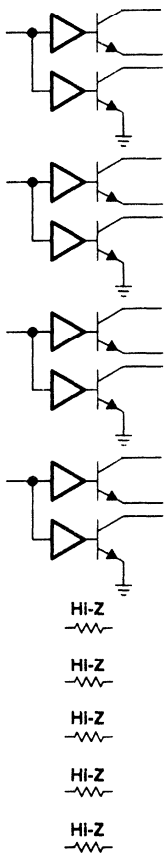


Figure 39. 10100 and 10101

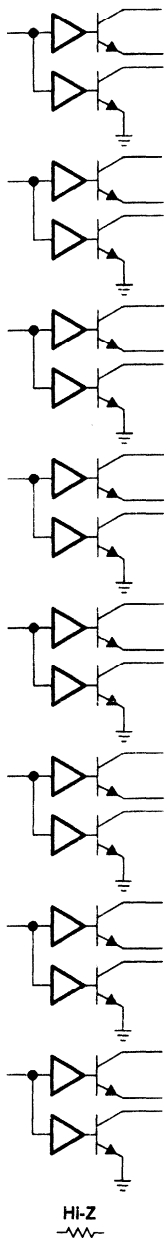


Figure 40. 10110 and 10111

APPLICATION INFORMATION

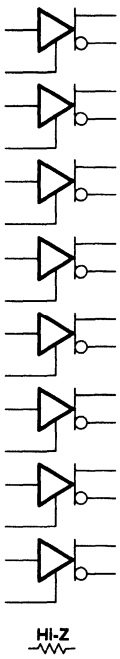


Figure 41. 11000 and 11001

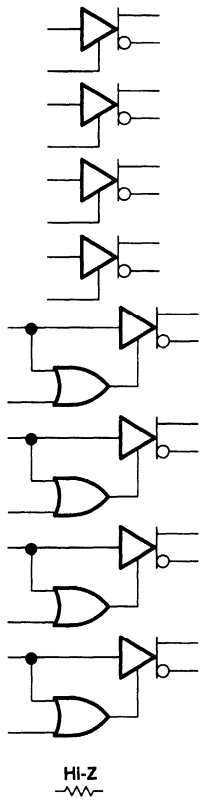


Figure 42. 11010 and 11011

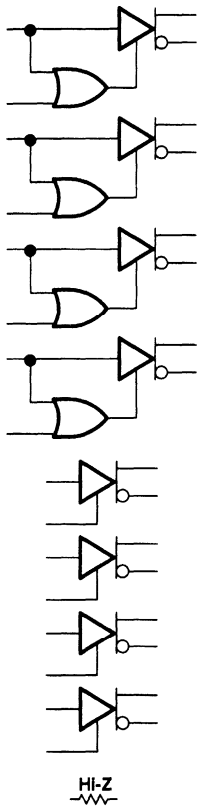


Figure 43. 11100 and 11101

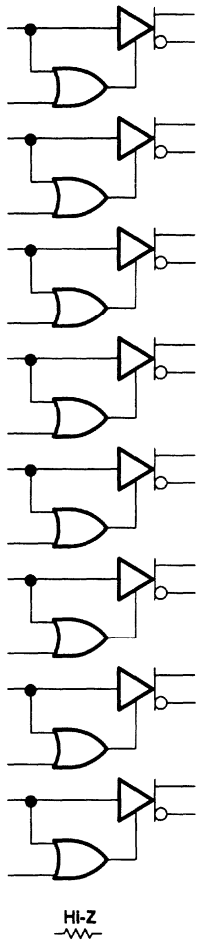
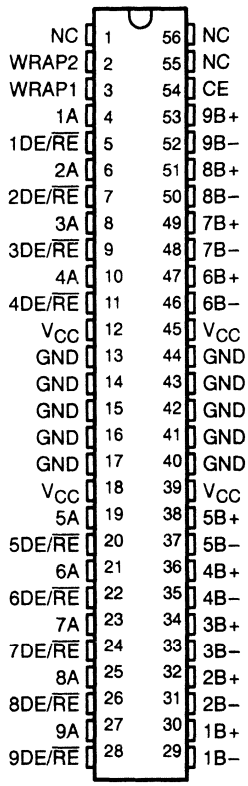


Figure 44. 11110 and 11111

SLLS134D – APRIL 1992 – REVISED MAY 1995

- **Nine Differential Channels for the Data and Control Paths of the Differential Small Computer Systems Interface (SCSI)**
- **Meets or Exceeds the Requirements of ANSI Standard RS-485 and ISO 8482:1987(E)**
- **Packaged in Shrink Small-Outline Package With 25-mil Terminal Pitch**
- **Designed to Operate at 10 Million Transfers Per Second**
- **Low Disabled Supply Current 1.4 mA Typ**
- **Thermal Shutdown Protection**
- **Power-Up/Power-Down Glitch Protection**
- **Positive and Negative Output-Current Limiting**
- **Open-Circuit Fail-Safe Receiver Design**

DL PACKAGE
(TOP VIEW)



Pins 13 through 17 and 40 through 44 are connected together to the package lead frame and signal ground.

description

The SN75LBC978 is a nine-channel differential transceiver based on the 75LBC176 LinASIC™ cell. Use of TI's LinBiCMOS™† process technology allows the power reduction necessary to integrate nine differential balanced transceivers†. On-chip enabling logic makes this device applicable for the data path (eight data bits plus parity) and the control path (nine bits) for the Small Computer Systems Interface (SCSI) standard. The WRAP function allows in-circuit testing and wired-OR channels for the BSY, RST, and SEL signals of the SCSI bus.

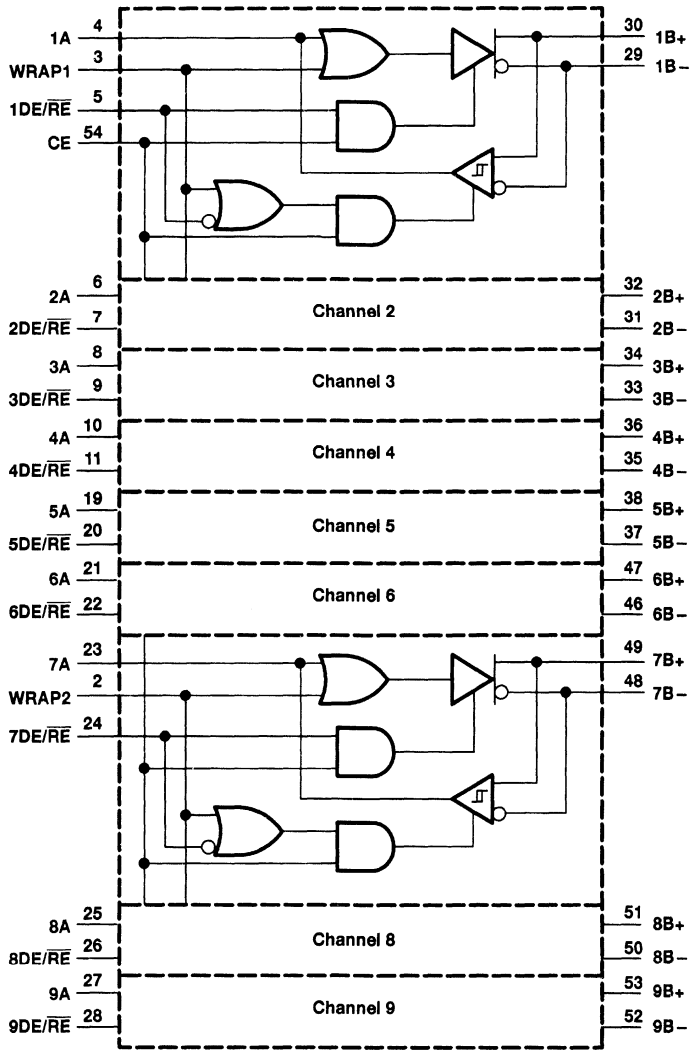
The SN75LBC978 is packaged in a shrink small-outline package (DL) with improved thermal characteristics using heat-sink terminals. This package is ideal for low-profile, space-restricted applications such as hard disk drives.

The switching speed of the SN75LBC978 is sufficient to transfer data over the data bus at 10 million transfers per second. Each of the nine identical channels conforms to the requirements of the ANSI RS-485 and ISO 8482:1987(E) standards referenced by ANSI X3.131-1993 (SCSI-2) and the proposed SCSI-3 standards.

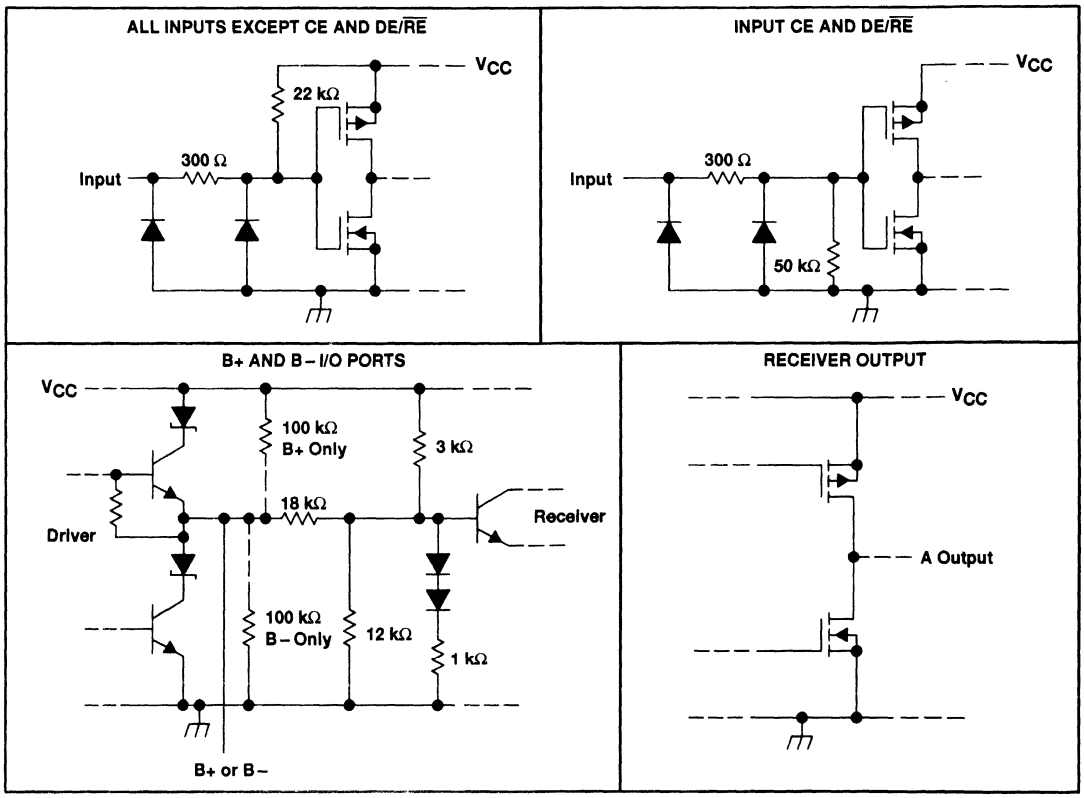
The SN75LBC978 is characterized for operation from 0°C to 70°C.

† Patent Pending
LinASIC and LinBiCMOS are trademarks of Texas Instruments Incorporated.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	−0.3 V to 7 V
Bus voltage range	−10 V to 15 V
Data I/O and control (A-side) voltage range	−0.3 V to 7 V
Continuous power dissipation	internally limited
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are dc and with respect to GND.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common-mode), V_O, V_I, or V_{IC}	B+ or B–			12	V
				–7	
High-level input voltage, V_{IH}	All except B+ and B–	2			V
Low-level input voltage, V_{IL}	All except B+ and B–			0.8	V
High-level output current, I_{OH}	B+ or B–			–60	mA
	A			–8	mA
Low-level output current, I_{OL}	B+ or B–			60	mA
	A			8	mA
Operating free-air temperature, T_A		0		70	°C

device electrical characteristics over recommended ranges of operating conditions

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_{IH}	High-level input current	A, WRAP, DE/$\overline{RE}$	See Figure 1	V_{IH} = 2 V			–200	µA
		CE					100	µA
I_{IL}	Low-level input current	A, WRAP, DE/$\overline{RE}$		V_{IL} = 0.8 V			–200	µA
		CE					100	µA
I_{CC}	Supply current	All drivers and receivers disabled	CE at 0 V			1.4	3	mA
		All receivers enabled	No load, CE at 5 V,	V_{ID} = 5 V, WRAP and DE/$\overline{RE}$ at 0 V		29	45	mA
		All drivers enabled	No load, WRAP at 0 V	CE and DE/$\overline{RE}$ at 5 V,		7	10	mA
C_O	Bus port output capacitance		B+ or B–			19		pF
C_{pd}	Power dissipation capacitance		One driver			460		pF
			One receiver			40		pF

driver electrical characteristics over recommended ranges of operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OD} \rvert$	Differential output voltage	V_{test} = –7 V to 12 V, See Figure 2	1	2		V
I_{OS}	Output short-circuit current	See Figure 3			±250	mA
I_{OZ}	High-impedance-state output current	See receiver input current				

receiver electrical characteristics over recommended ranges of operating conditions (unless otherwise noted) (see Figure 3)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{ID} = 200 mV,	I_{OH} = −8 mA	2.5			V
V_{OL}	Low-level output voltage		V_{ID} = −200 mV,	I_{OL} = 8 mA			0.8	V
V_{IT+}	Differential-input high-level threshold voltage		I_{OH} = −8 mA				0.2	V
V_{IT-}	Differential-input low-level threshold voltage		I_{OL} = 8 mA		−0.2			V
V_{hys}	Receiver input hysteresis voltage ($V_{IT+} - V_{IT-}$)					45		mV
I_I	Receiver input current	B+ and B−	V_I = 12 V, Other input at 0 V	V_{CC} = 5 V,		0.7	1	mA
			V_I = 12 V, Other input at 0 V	V_{CC} = 0 V,		0.8	1	mA
			V_I = −7 V, Other input at 0 V	V_{CC} = 5 V,		−0.5	−0.8	mA
			V_I = −7 V, Other input at 0 V	V_{CC} = 0 V,		−0.4	−0.8	mA
I_{OZ}	High-impedance-state output current		V_O = GND				−200	µA
			V_O = V_{CC}				50	

driver switching characteristics over recommended ranges of operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$t_{d(OD)}$	Differential delay time, high- to low-level output ($t_{d(ODH)}$) or low- to high-level output ($t_{d(ODL)}$)	See Figure 4		11.8		26.4	ns
		V_{CC} = 5 V, See Figure 4	T_A = 25°C,	14	18	22	
		V_{CC} = 5 V, See Figure 4	T_A = 70°C,	18	22	26	
$t_{sk(lim)}$	Skew limit, the maximum difference in propagation delay times between any two drivers on any two devices					15	ns
		V_{CC} = 5 V,	See Note 2			8	
$t_{sk(p)}$	Pulse skew ($\lvert t_{d(ODL)} - t_{d(ODH)} \rvert$)	See Figure 4			0	6	ns
t_t	Transition time (t_r or t_f)				10		ns

receiver switching characteristics over recommended ranges of operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{pd}	Propagation delay time, high- to low-level output (t_{PHL}) or low- to high-level output (t_{PLH})	See Figure 5		19.5		30.7	ns
		V_{CC} = 5 V, See Figure 5	T_A = 25°C,	20.2	24.7	29.2	
		V_{CC} = 5 V, See Figure 5	T_A = 70°C,	21.1	25.6	30.1	
$t_{sk(lim)}$	Skew limit, the maximum difference in propagation delay times between any two drivers on any two devices					12	ns
		V_{CC} = 5 V,	See Note 2			9	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)	See Figure 5			2	6	ns
t_t	Transition time (t_r or t_f)				3		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ C_{pd} determines the no-load dynamic current consumption; $I_S = C_{pd} \cdot V_{CC} \cdot f + I_{CC}$.

NOTE 2: This specification applies to any 5°C band within the operating temperature range.

transceiver switching characteristics over recommended ranges of operating conditions

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{en(TXL)}$	Enable time, transmit-to-receive to low-level output	See Figure 6		80	ns
$t_{en(TXH)}$	Enable time, transmit-to-receive to high-level output			80	ns
$t_{en(RXL)}$	Enable time, receive-to-transmit to low-level output			150	ns
$t_{en(RXH)}$	Enable time, receive-to-transmit to high-level output			150	ns
t_{su}	Setup time, WRAP1 or WRAP2 before active input(s) or output(s)		150		ns

thermal characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	Board mounted, No air flow		50		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance			12		°C/W

PARAMETER MEASUREMENT INFORMATION

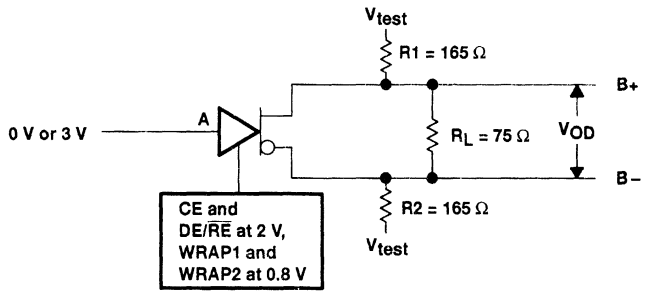
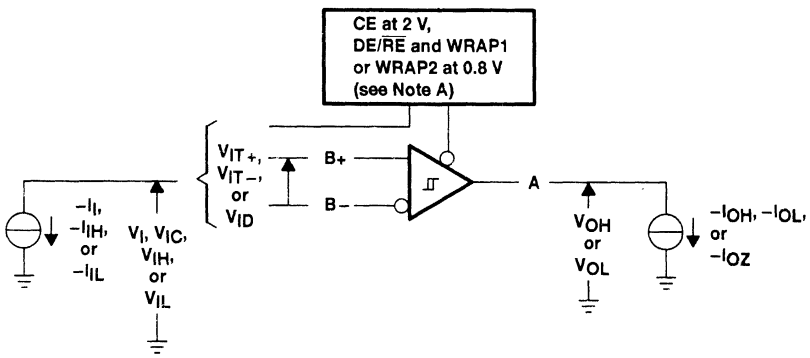


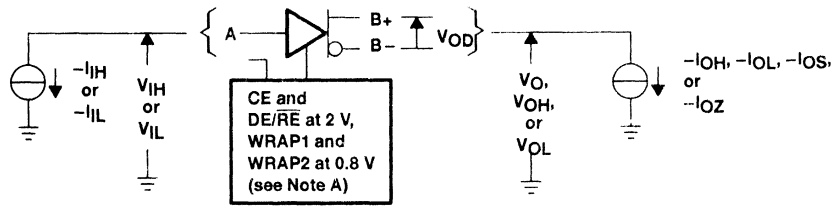
Figure 1. Driver V_{OD} Test Circuit



NOTE A: For the I_{OZ} measurement, CE is at 0.8 V.

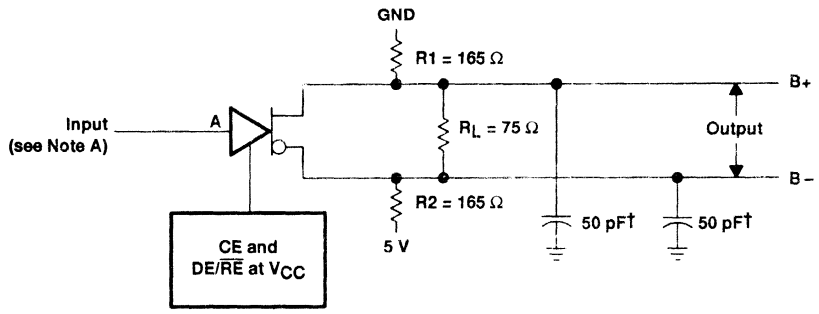
Figure 2. Receiver Test Circuit and Input Conditions

PARAMETER MEASUREMENT INFORMATION

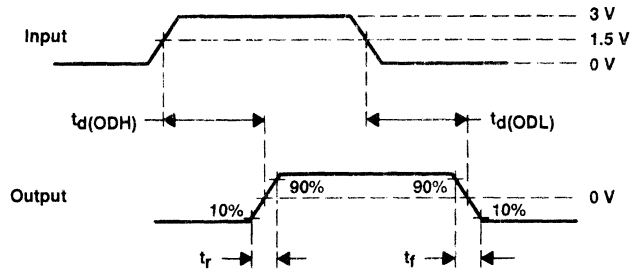


NOTE A: For the I_{OZ} test, the CE input is at 0.8 V.

Figure 3. Driver Test and Input Conditions



TEST CIRCUIT



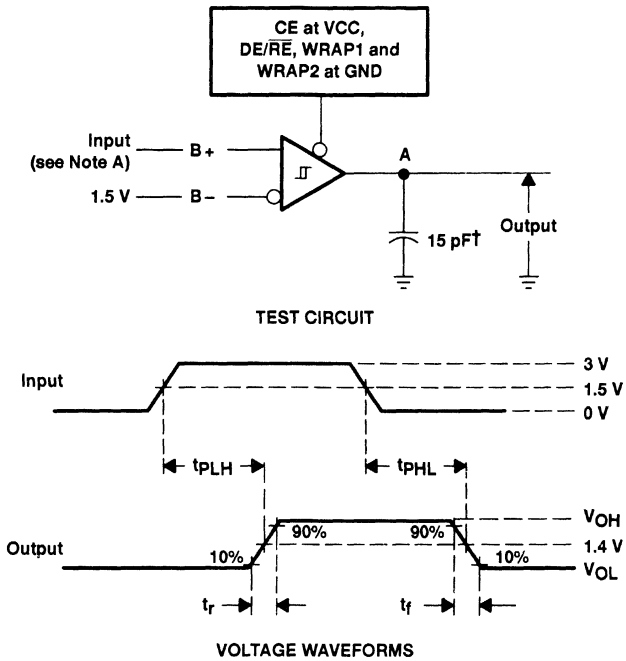
VOLTAGE WAVEFORMS

† Includes probe and jig capacitance.

NOTE A: The input is provided by a pulse generator with an output of 0 to 3 V, PRR of 1 MHz, 50% duty cycle, t_r and t_f < 6 ns, and Z_O = 50 Ω.

Figure 4. Driver Propagation Delay Time Test Circuit and Waveforms

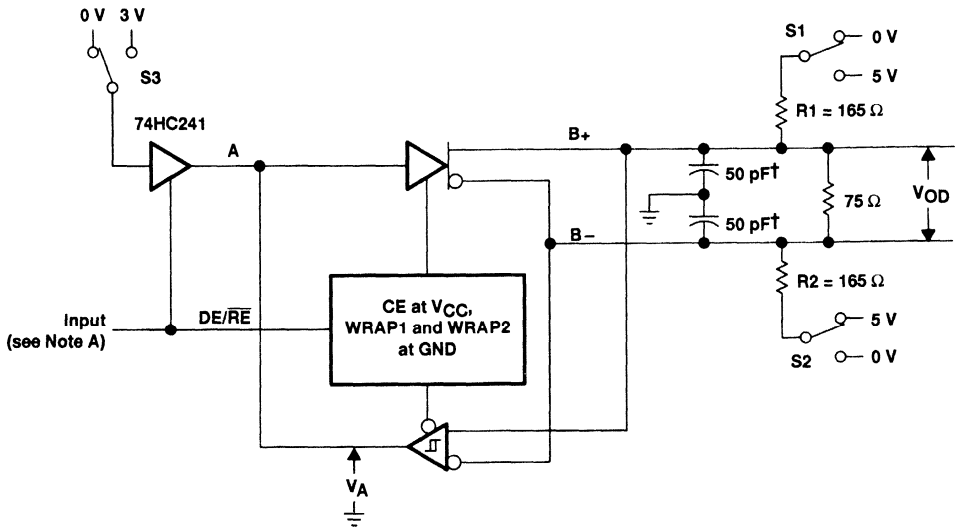
PARAMETER MEASUREMENT INFORMATION



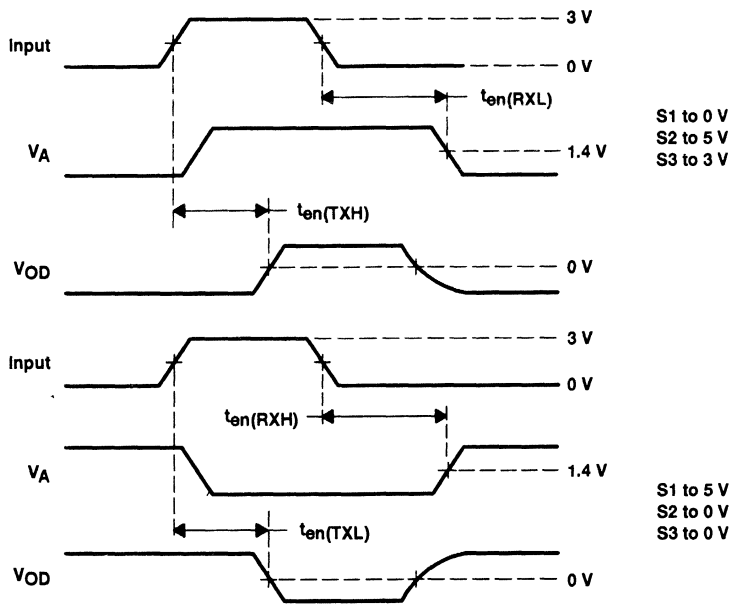
† Includes probe and jig capacitance.
NOTE A: The input is provided by a pulse generator with an output of 0 to 3 V, PRR of 1 MHz, 50% duty cycle, t_r and t_f < 6 ns, and Z_O = 50 Ω.

Figure 5. Receiver Propagation Delay Time Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

† Includes probe and jig capacitance.

NOTE A: The input is provided by a pulse generator with an output of 0 to 3 V, PRR of 1 MHz, 50% duty cycle, t_r and t_f < 6 ns, and Z_O = 50 Ω.

Figure 6. Enable Time Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

AVERAGE SUPPLY CURRENT
vs
FREQUENCY

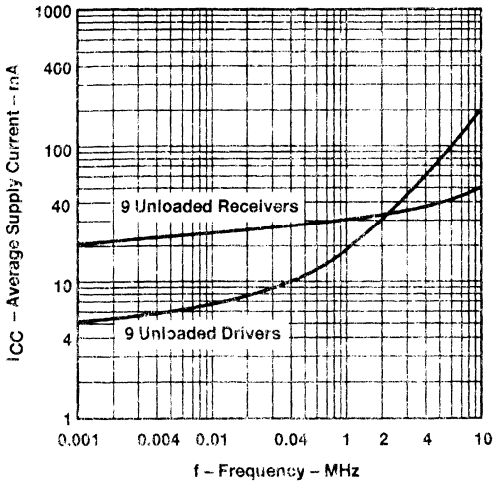


Figure 7

INPUT CURRENT
vs
INPUT VOLTAGE

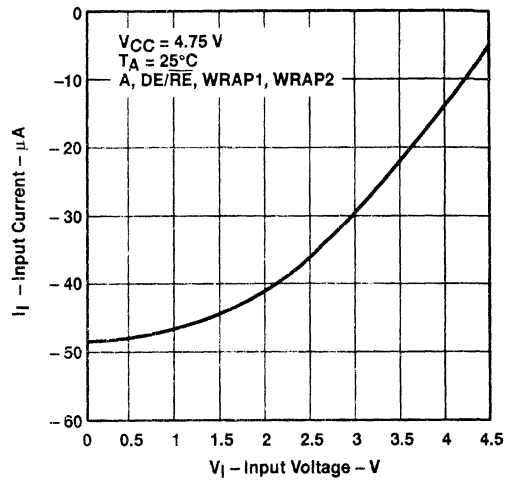


Figure 8

INPUT CURRENT
vs
INPUT VOLTAGE

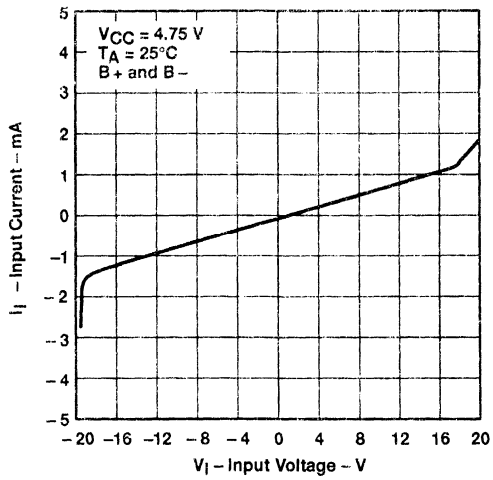


Figure 9

TYPICAL CHARACTERISTICS

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

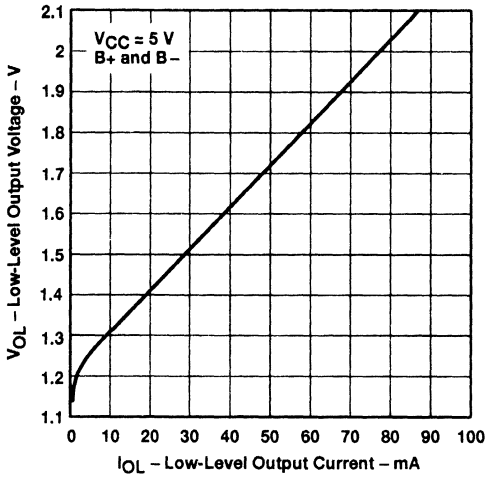


Figure 10

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

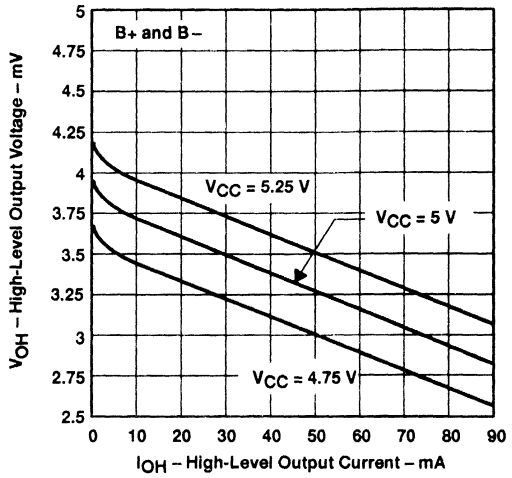


Figure 11

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

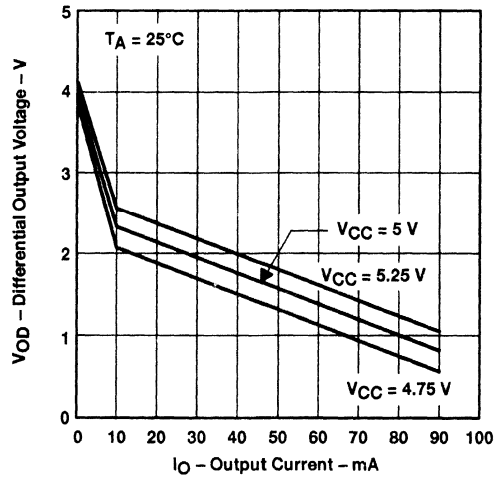


Figure 12

TYPICAL CHARACTERISTICS

DRIVER
LOW-LEVEL OUTPUT CURRENT
vs
SUPPLY VOLTAGE

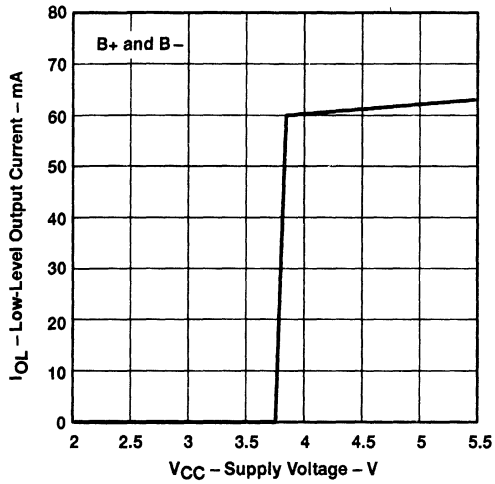


Figure 13

DRIVER
HIGH-LEVEL OUTPUT CURRENT
vs
SUPPLY VOLTAGE

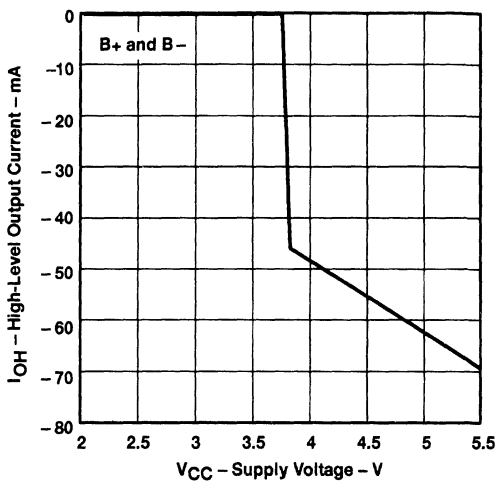


Figure 14

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

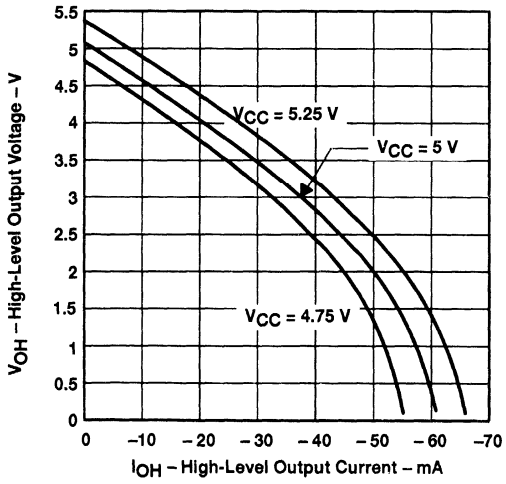


Figure 15

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

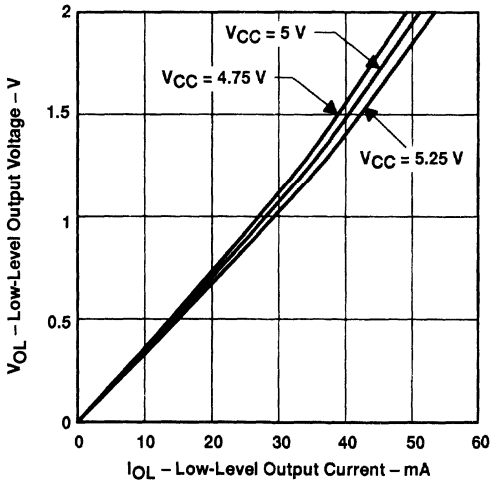


Figure 16

TYPICAL CHARACTERISTICS

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

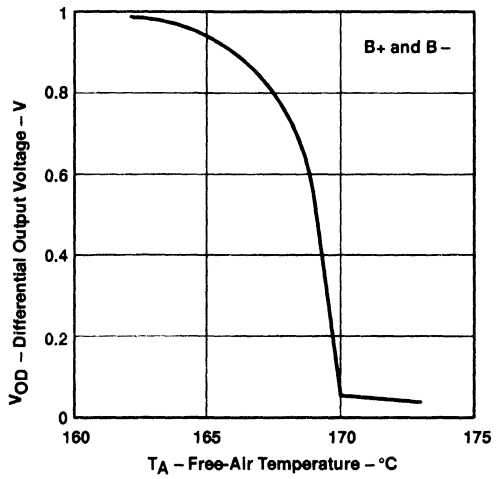


Figure 17

RECEIVER
PROPAGATION DELAY
vs
FREE-AIR TEMPERATURE

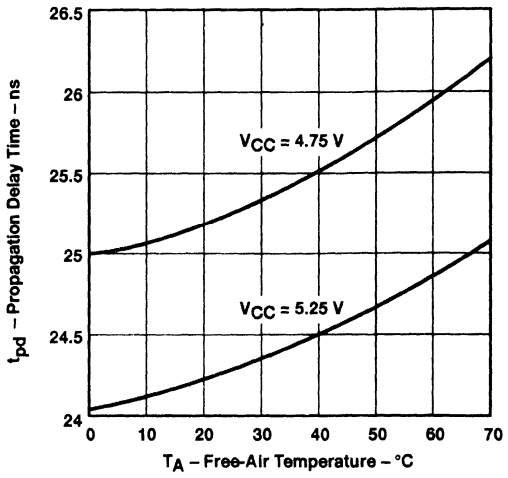


Figure 18

DRIVER
PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

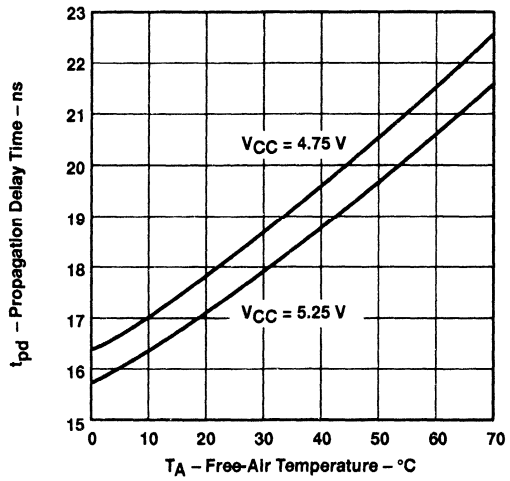


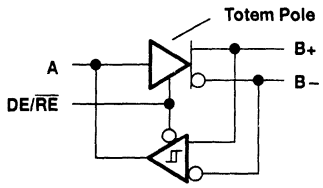
Figure 19

APPLICATION INFORMATION

Function Tables for Possible Channel Configurations

Table 1

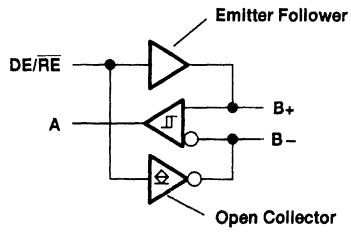
CE is high, WRAP1 or WRAP2 is low



INPUTS				OUTPUTS		
DE/$\overline{RE}$	A	B+†	B–†	A	B+	B–
L	X	L	H	L	Z	Z
L	X	H	L	H	Z	Z
H	L	X	X	Z	L	H
H	H	X	X	Z	H	L

Table 2

CE is high, WRAP1 or WRAP2 is high



INPUTS			OUTPUTS		
DE/$\overline{RE}$	B+	B–	A	B+	B–
L	L	H	L	Z	Z
L	H	L	H	Z	Z
H	X	X	H	H	L
H	X	X	H	H	L

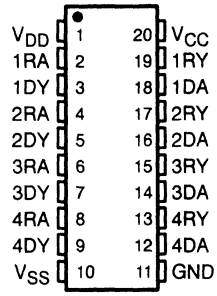
H = high level L = low level X = irrelevant Z = high impedance

† An H in this column represents a voltage 200 mV higher than the other bus input. An L represents a voltage 200 mV lower than the other bus input. Any voltage less than 200 mV results in an indeterminate receiver output.

SLLS151B – DECEMBER 1988 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of ANSI EIA/TIA-232-E and ITU Recommendation V.28**
- **Very Low Power Consumption 5 mW Typ**
- **Wide Driver Supply Voltage . . . ±4.5 V to ±15 V**
- **Driver Output Slew Rate Limited to 30 V/μs Max**
- **Receiver Input Hysteresis . . . 1000 mV Typ**
- **Push-Pull Receiver Outputs**
- **On-Chip Receiver 1-μs Noise Filter**
- **Functionally Interchangeable With Motorola MC145404**

DW OR N PACKAGE
(TOP VIEW)



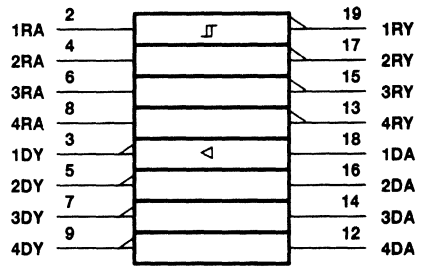
description

The SN65C1154 and SN75C1154 are low-power BiMOS devices containing four independent drivers and receivers that are used to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). This device has been designed to conform to ANSI EIA/TIA-232-E. The drivers and receivers of the SN65C1154 and SN75C1154 are similar to those of the SN75C188 quadruple driver and SN75C189A quadruple receiver, respectively. The drivers have a controlled output slew rate that is limited to a maximum of 30 V/μs and the receivers have filters that reject input noise pulses of shorter than 1 μs. Both these features eliminate the need for external components.

The SN65C1154 and SN75C1154 have been designed using low-power techniques in a BiMOS technology. In most applications, the receivers contained in these devices interface to single inputs of peripheral devices such as ACEs, UARTs, or microprocessors. By using sampling, such peripheral devices are usually insensitive to the transition times of the input signals. If this is not the case or for other uses, it is recommended that the SN65C1154 and SN75C1154 receiver outputs be buffered by single Schmitt input gates or single gates of the HCMOS, ALS, or 74F logic families.

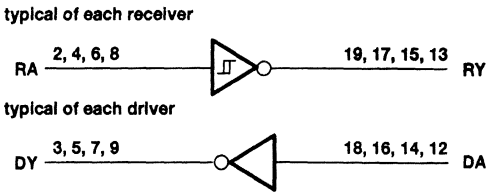
The SN65C1154 is characterized for operation from −40°C to 85°C. The SN75C1154 is characterized for operation from 0°C to 70°C.

logic symbol†

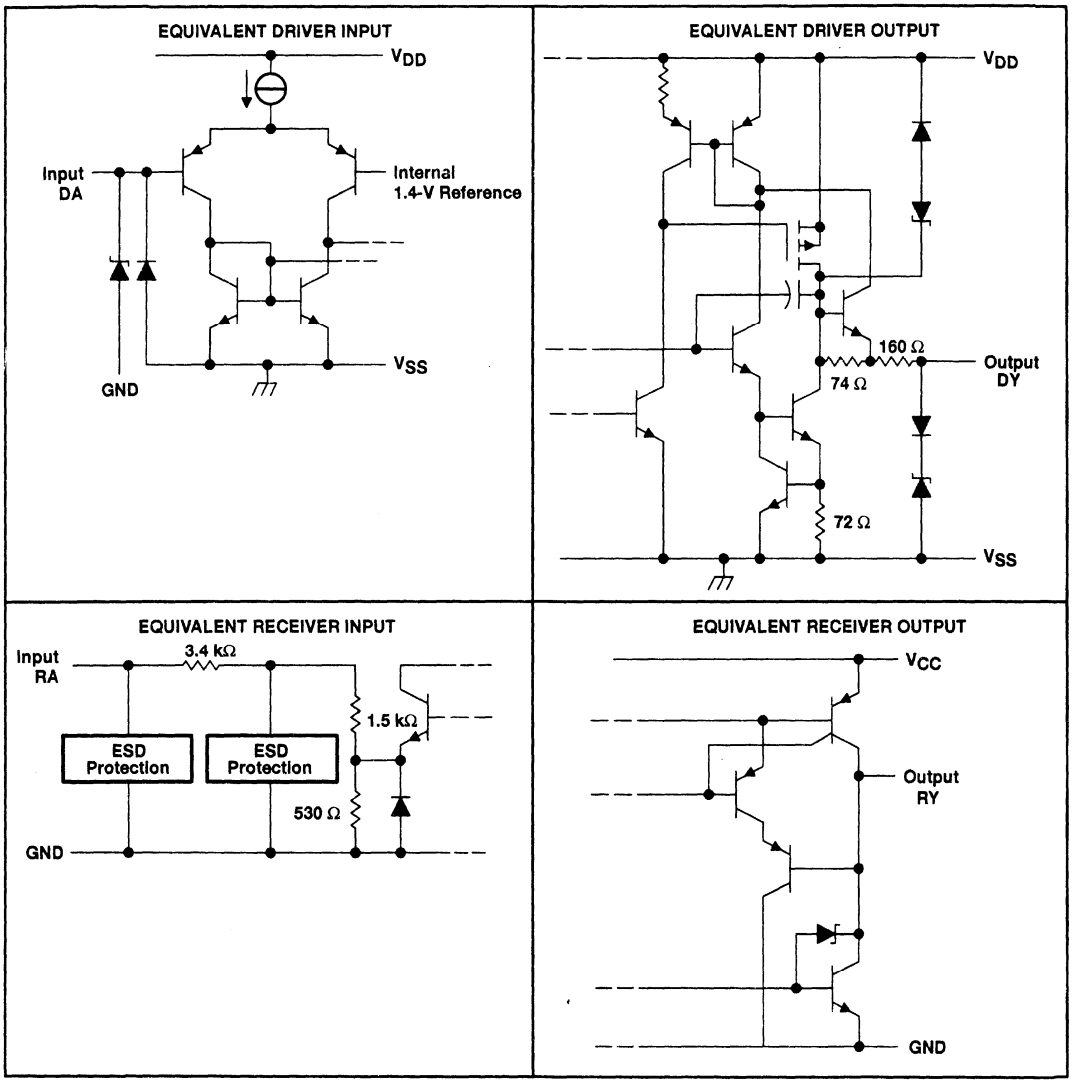


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 15 V
Supply voltage, V_{SS} ..... −15 V
Supply voltage, V_{CC} ..... 7 V
Input voltage range, V_I: Driver ..... V_{SS} to V_{DD}
Receiver ..... −30 V to 30 V
Output voltage range, V_O: Driver ..... (V_{SS} −6 V) to (V_{DD} + 6 V)
Receiver ..... −0.3 V to (V_{CC} + 0.3 V)
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65C1154 ..... −40°C to 85°C
SN75C1154 ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to the network GND terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW	585 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.5	12	15	V
Supply voltage, V_{SS}		−4.5	−12	−15	V
Supply voltage, V_{CC}		4.5	5	6	V
Input voltage, V_I	Driver	V_{SS}+2		V_{DD}	V
	Receiver			±25	
High-level input voltage, V_{IH}	Driver	2			V
Low-level input voltage, V_{IL}				0.8	
High-level output current, I_{OH}	Receiver			−1	mA
High-level output current, I_{OL}				3.2	mA
Operating free-air temperature, T_A	SN65C1154	−40		85	°C
	SN75C1154	0		70	

DRIVER SECTION

electrical characteristics over operating free-air temperature range, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ±10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{IL} = 0.8 V, See Figure 1	R_L = 3 kΩ,	V_{DD} = 5 V, V_{SS} = −5 V	4	4.5		V
				V_{DD} = 12 V, V_{SS} = −12 V	10	10.8		
V_{OL}	Low-level output voltage (see Note 2)	V_{IH} = 2 V, See Figure 1	R_L = 3 kΩ,	V_{DD} = 5 V, V_{SS} = −5 V		−4.4	−4	V
				V_{DD} = 12 V, V_{SS} = −12 V		−10.7	−10	
I_{IH}	High-level input current	V_I = 5 V,	See Figure 2				1	µA
I_{IL}	Low-level input current	V_I = 0,	See Figure 2				−1	µA
$I_{OS(H)}$	High-level short circuit output current‡	V_I = 0.8 V,	V_O = 0 or V_{SS},	See Figure 1	−7.5	−12	−19.5	mA
$I_{OS(L)}$	Low-level short circuit output current‡	V_I = 2 V,	V_O = 0 or V_{DD},	See Figure 1	7.5	12	19.5	mA
I_{DD}	Supply current from V_{DD}	No load, All inputs at 2 V or 0.8 V		V_{DD} = 5 V, V_{SS} = −5 V		115	250	µA
				V_{DD} = 12 V, V_{SS} = −12 V		115	250	
I_{SS}	Supply current from V_{SS}	No load, All inputs at 2 V or 0.8 V		V_{DD} = 5 V, V_{SS} = −5 V		−115	−250	µA
				V_{DD} = 12 V, V_{SS} = −12 V		−115	−250	
r_o	Output resistance	V_{DD} = V_{SS} = V_{CC} = 0,	V_O = −2 V to 2 V,	See Note 3	300	400		Ω

† All typical values are at T_A = 25°C.
‡ Not more than one output should be shorted at one time.
NOTES: 2. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only.
3. Test conditions are those specified by EIA/TIA-232-E.

switching characteristics, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ±10%, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output§	R_L = 3 to 7 kΩ, C_L = 15 pF, See Figure 3		1.2	3	µs
t_{PHL}	Propagation delay time, high- to low-level output§			2.5	3.5	µs
t_{TLH}	Transition time, low- to high-level output¶		0.53	2	3.2	µs
t_{THL}	Transition time, high- to low-level output¶		0.53	2	3.2	µs
t_{TLH}	Transition time, low- to high-level output#	R_L = 3 to 7 kΩ, C_L = 2500 pF, See Figure 3		1	2	µs
t_{THL}	Transition time, high- to low-level output#	R_L = 3 to 7 kΩ, C_L = 2500 pF, See Figure 3		1	2	µs
SR	Output slew rate	R_L = 3 to 7 kΩ, C_L = 15 pF, See Figure 3	4	10	30	V/µs

§ t_{PHL} and t_{PLH} include the additional time due to on-chip slew rate control and are measured at the 50% points.
¶ Measured between 10% and 90% points of output waveform.
# Measured between 3 V and −3 V points of output waveform (EIA/TIA-232-E conditions) with all unused inputs tied either high or low.

RECEIVER SECTION

electrical characteristics over operating free-air temperature range, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ± 10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	See Figure 5			1.7	2.1	2.55	V
V_{IT-}	Negative-going input threshold voltage	See Figure 5			0.65	1	1.25	V
V_{hys}	Input hysteresis voltage (V_{IT+} − V_{IT-})				600	1000		mV
V_{OH}	High-level output voltage	V_I = 0.75 V, I_{OH} = −20 μA, See Figure 5 and Note 4			3.5			V
		V_I = 0.75 V, See Figure 5	I_{OH} = −1 mA	V_{CC} = 4.5 V	2.8	4.4		
				V_{CC} = 5 V	3.8	4.9		
				V_{CC} = 5.5 V	4.3	5.4		
V_{OL}	Low-level output voltage	V_I = 3 V, I_{OL} = 3.2 mA, See Figure 5				0.17	0.4	V
I_{IH}	High-level input current	V_I = 25 V			3.6	4.6	8.3	mA
		V_I = 3 V			0.43	0.55	1	
I_{IL}	Low-level input current	V_I = −25 V			−3.6	−5	−8.3	
		V_I = −3 V			−0.43	−0.55	−1	
$I_{OS(H)}$	Short-circuit output at high level	V_I = 0.75 V, V_O = 0, See Figure 4				−8	−15	mA
$I_{OS(L)}$	Short-circuit output at low level	V_I = V_{CC}, V_O = V_{CC}, See Figure 4				13	25	mA
I_{CC}	Supply current from V_{CC}	No load, All inputs at 0 or 5 V		V_{DD} = 5 V, V_{SS} = −5 V		400	600	μA
				V_{DD} = 12 V, V_{SS} = −12 V		400	600	

† All typical values are at T_A = 25°C.

NOTE 4: If the inputs are left unconnected, the receiver interprets this as an input low and the receiver outputs will remain in the high state.

switching characteristics, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ± 10%, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 50 pF, R_L = 5 kΩ, See Figure 6		3	4	μs
t_{PHL}	Propagation delay time, high- to low-level output			3	4	μs
t_{TLH}	Transition time, low- to high-level output			300	450	ns
t_{THL}	Transition time, high- to low-level output			100	300	ns
$t_{w(N)}$	Duration of longest pulse rejected as noise‡	C_L = 50 pF, R_L = 5 kΩ	1		4	μs

‡ The receiver ignores any positive- or negative-going pulse that is less than the minimum value of $t_{w(N)}$ and accepts any positive- or negative-going pulse greater than the maximum of $t_{w(N)}$.

PARAMETER MEASUREMENT INFORMATION

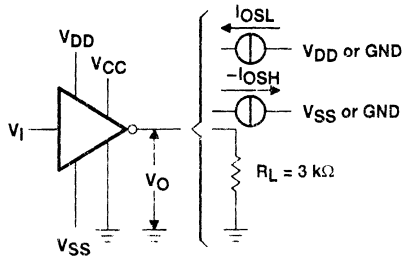


Figure 1. Driver Test Circuit
V_{OH}, V_{OL}, I_{OSL}, I_{OSH}

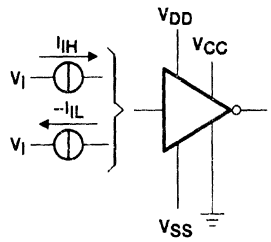
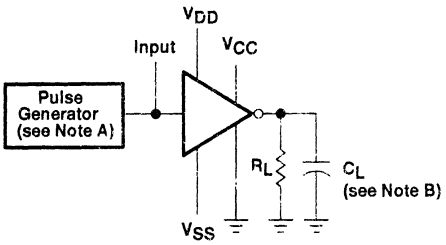
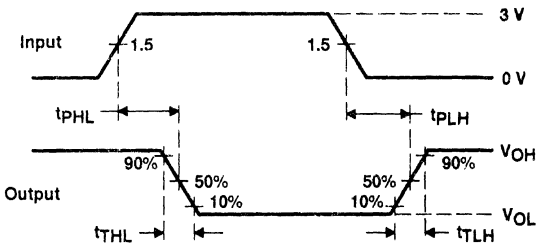


Figure 2. Driver Test Circuit, I_{IL}, I_{IH}



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: t_W = 25 µs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f < 50$ ns.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

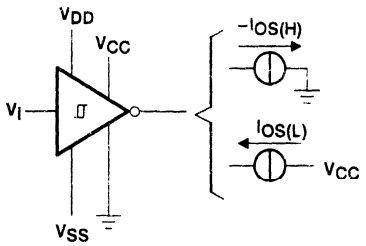


Figure 4. Receiver Test Circuit, I_{OSH}, I_{OSL}

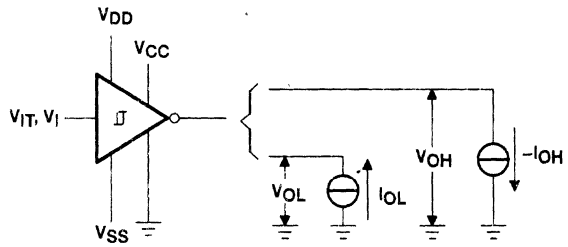
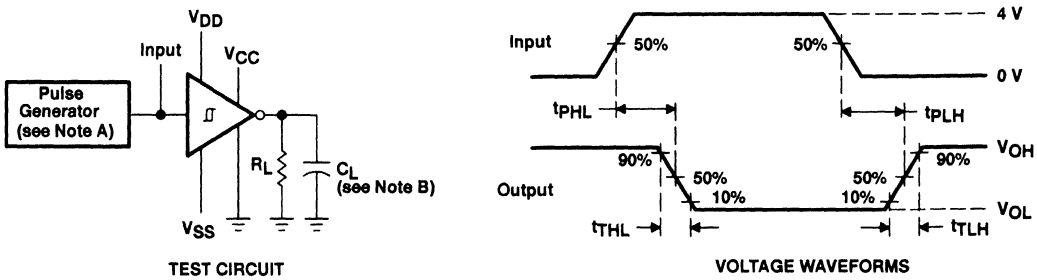


Figure 5. Receiver Test Circuit, V_{IT}, V_{OL}, V_{OH}

PARAMETER MEASUREMENT INFORMATION



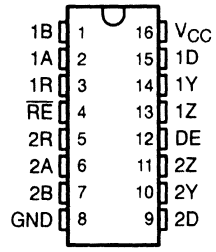
NOTES: A. The pulse generator has the following characteristics: t_w = 25 μs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f < 50$ ns.
B. C_L includes probe and jig capacitance.

Figure 6. Receiver Test Circuit and Voltage Waveforms

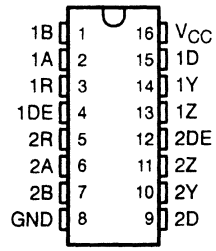
SLLS159B – MARCH 1993 – REVISED JUNE 1995

- **Meet or Exceed Standards EIA/TIA-422-B and ITU Recommendation V.11**
- **BiCMOS Process Technology**
- **Low Supply Current Requirements 9 mA Max**
- **Low Pulse Skew**
- **Receiver Input Impedance . . . 17 kΩ Typ**
- **Receiver Input Sensitivity . . . ±200 mV**
- **Receiver Common-Mode Input Voltage Range of −7 V to 7 V**
- **Operate From Single 5-V Power Supply**
- **Glitch-Free Power-Up/Power-Down Protection**
- **Receiver 3-State Outputs Active-Low Enable for SN75C1167 Only**
- **Improved Replacements for the MC34050 and MC34051**

SN65C1167, SN75C1167 . . . N OR NS† PACKAGE
(TOP VIEW)



SN65C1168, SN75C1168 . . . N OR NS† PACKAGE
(TOP VIEW)



† The NS package is only available left-ended taped and reeled (order device SNx5C116xNSLE).

description

The SN65C1167, SN75C1167, SN65C1168 and SN75C1168 dual drivers and receivers are monolithic integrated circuits designed for balanced transmission lines and meet EIA Standards EIA/TIA-422-B, ITU recommendation V.11.

The SN65C1167 and SN75C1167 combine dual 3-state differential line drivers and 3-state differential line receivers, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as direction control. The SN65C1168 and SN75C1168 drivers have individual active-high enables.

The SN65C1167 and SN65C1168 are characterized from −40°C to 85°C. The SN75C1167 and SN75C1168 are characterized for operation from 0°C to 70°C.

Function Tables

EACH DRIVER

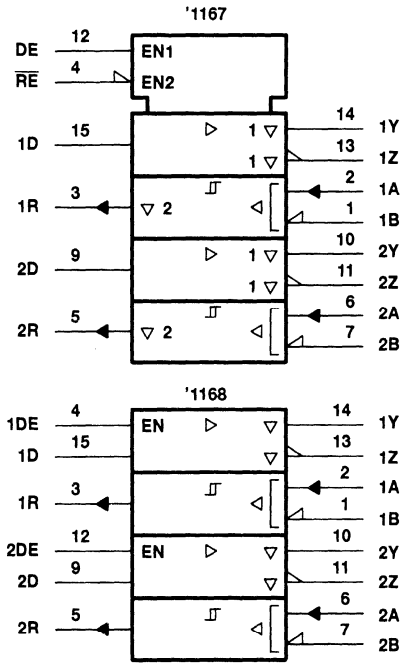
INPUT	ENABLE	OUTPUTS	
D	DE	Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

'1167, EACH RECEIVER

DIFFERENTIAL INPUTS	ENABLE	OUTPUT
A – B	$\overline{RE}$	R
$V_{ID} \geq 0.2$ V	L	H
$-0.2\text{ V} < V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

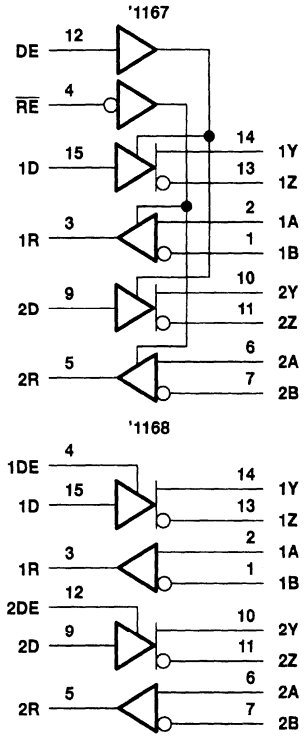
H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

logic symbols†

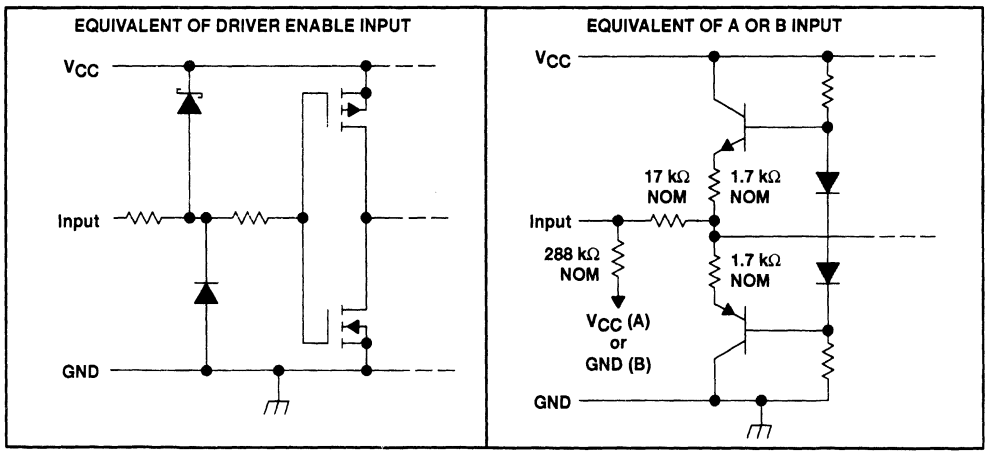


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

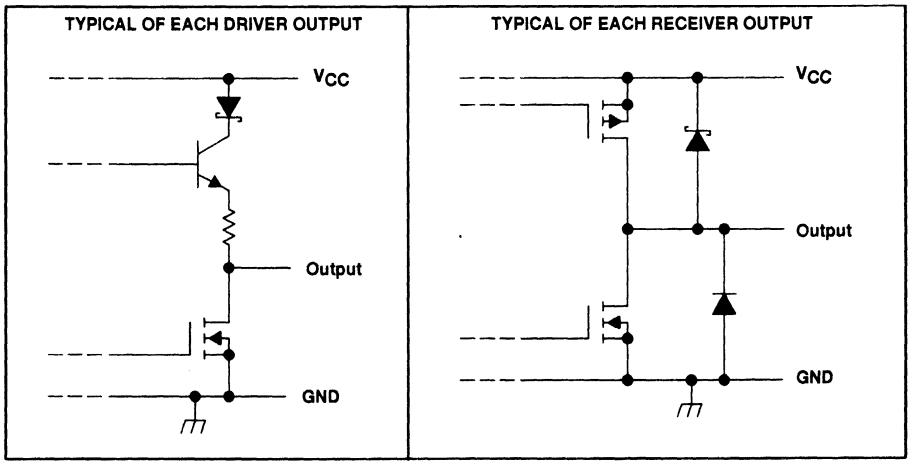
logic diagrams (positive logic)



schematics of inputs



schematics of outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Input voltage range, V_I ..... −0.5 V to V_{CC} + 0.5 V
Input voltage range, V_I (A or B, Receiver) ..... −11 V to 14 V
Differential input voltage range, V_{ID}, Receiver (see Note 2) ..... −14 V to 14 V
Output voltage range, V_O, Driver ..... −5 V to 7 V
Clamp current range, I_{IK} or I_{OK}, Driver ..... ±20 mA
Output current range, I_O, Driver ..... ±150 mA
Supply current, I_{CC} ..... 200 mA
GND current ..... −200 mA
Output current range, I_O, Receiver ..... ±25 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN75C1167, SN75C1168 ..... 0°C to 70°C
SN65C1167, SN65C1168 ..... −40°C to 85°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values except differential input voltage are with respect to the network GND.
2. Differential input voltage is measured at the noninverting terminal with respect to the inverting terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
N	1250 mW	10 mW/°C	800 mW	650 mW
NS	625 mW	5 mW/°C	400 mW	325 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
Common-mode input voltage, V_{IC} (see Note 3)	Receiver			±7	V
Differential input voltage, V_{ID}	Receiver			±7	V
High-level input voltage, V_{IH}	Except A, B	2			V
Low-level input voltage, V_{IL}	Except A, B			0.8	V
High-level output current, I_{OH}	Receiver			−6	mA
	Driver			−20	
Low-level output current, I_{OL}	Receiver			6	mA
	Driver			20	
Operating free-air temperature, T_A	SN65C1167, SN65C1168	−40		85	°C
	SN75C1167, SN75C1168	0		70	

NOTE 3: Refer to EIA standard RS-422-A for exact conditions

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA					−1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V,	V_{IL} = 0.8 V,	I_{OH} = −20 mA	2.4	3.4		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V,	V_{IL} = 0.8 V,	I_{OL} = 20 mA		0.2	0.4	V
$\lvert V_{OD1}\rvert$	Differential output voltage	I_O = 0 mA			2		6	V
$\lvert V_{OD2}\rvert$	Differential output voltage	R_L = 100 Ω, See Figure 1 and Note 3			2	3.1		V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage						±0.4	V
V_{OC}	Common-mode output voltage						±3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage						±0.4	V
$I_{O(OFF)}$	Output current with power off (see Note 3)	V_{CC} = 0 V	V_O = 6 V				100	µA
			V_O = −0.25 V				−100	µA
I_{OZ}	High-impedance-state output current	V_O = 2.5 V					20	µA
		V_O = 5 V					−20	
I_{IH}	High-level input current	V_I = V_{CC} or V_{IH}					1	µA
I_{IL}	Low-level input current	V_I = GND or V_{IL}					−1	µA
I_{OS}	Short-circuit output current	V_O = V_{CC} or GND,		See Note 4	−30		−150	mA
I_{CC}	Supply current (total package)	No load, Enabled	V_I = V_{CC} or GND			4	6	mA
			V_I = 2.4 or 0.5 V,	See Note 5		5	9	
C_i	Input capacitance					6		pF

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

NOTES: 3. Refer to EIA standard RS-422-A for exact conditions.
4. Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
5. This parameter is measured per input, while the other inputs are at V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	R_1 = R_2 = 50 Ω, C_1 = C_2 = C_3 = 40 pF, See Figure 2	R_3 = 500 Ω, S1 is open,		7	12	ns
t_{PLH}	Propagation delay time, low- to high-level output				7	12	ns
$t_{sk(p)}$	Pulse skew				0.5	4	ns
t_r	Rise time	R_1 = R_2 = 50 Ω, C_1 = C_2 = C_3 = 40 pF, See Figure 3	R_3 = 500 Ω, S1 is open,		5	10	ns
t_f	Fall time				5	10	ns
t_{PZH}	Output enable time to high level	R_1 = R_2 = 50 Ω, C_1 = C_2 = C_3 = 40 pF, See Figure 4	R_3 = 500 Ω, S1 is closed,		10	19	ns
t_{PZL}	Output enable time to low level				10	19	ns
t_{PHZ}	Output disable time from low level	R_1 = R_2 = 50 Ω, C_1 = C_2 = C_3 = 40 pF, See Figure 4	R_3 = 500 Ω, S1 is closed,		7	16	ns
t_{PLZ}	Output disable time from high level				7	16	ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage, differential input						0.2	V
V_{IT-}	Negative-going input threshold voltage, differential input				−0.2‡			V
V_{hys}	Input hysteresis ($V_{IT+} - V_{IT-}$)					60		mV
V_{IK}	Input clamp voltage, $\overline{RE}$	'1167	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage		V_{ID} = 200 mV,	I_{OH} = −6 mA	3.8	4.2		V
V_{OL}	Low-level output voltage		V_{ID} = −200 mV,	I_{OL} = 6 mA		0.1	0.3	V
I_{OZ}	High-impedance-state output current	'1167	V_O = V_{CC} or GND			±0.5	±5	µA
I_I	Line input current		Other input at 0 V	V_I = 10 V			1.5	mA
				V_I = −10 V			−2.5	
I_I	Enable input current, $\overline{RE}$	'1167	V_I = V_{CC} or GND				±1	µA
r_i	Input resistance		V_{IC} = −7 V to 7 V,	Other input at 0 V	4	17		kΩ
I_{CC}	Supply current (total package)		No load, Enabled	V_I = V_{CC} or GND		4	6	mA
				V_{IH} = 2.4 V or 0.5 V, See Note 5		5	9	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 5	9	17	27	ns
t_{PHL}	Propagation delay time, high- to low-level output		9	17	27	ns
t_{TLH}	Transition time, low- to high-level output	V_{IC} = 0 V, See Figure 5		4	9	ns
t_{THL}	Transition time, high- to low-level output			4	9	ns
t_{PZH}	Output enable time to high level	R_L = 1 kΩ, See Figure 6		13	22	ns
t_{PZL}	Output enable time to low level			13	22	ns
t_{PHZ}	Output disable time from high level			13	22	ns
t_{PLZ}	Output disable time from low level			13	22	ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
NOTE 5: Measured per input while the other inputs are at V_{CC} or GND.

PARAMETER MEASUREMENT INFORMATION

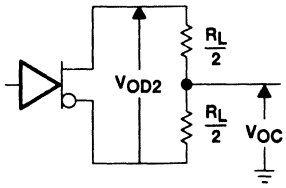


Figure 1. Driver Test Circuit, V_{OD} and V_{OC}

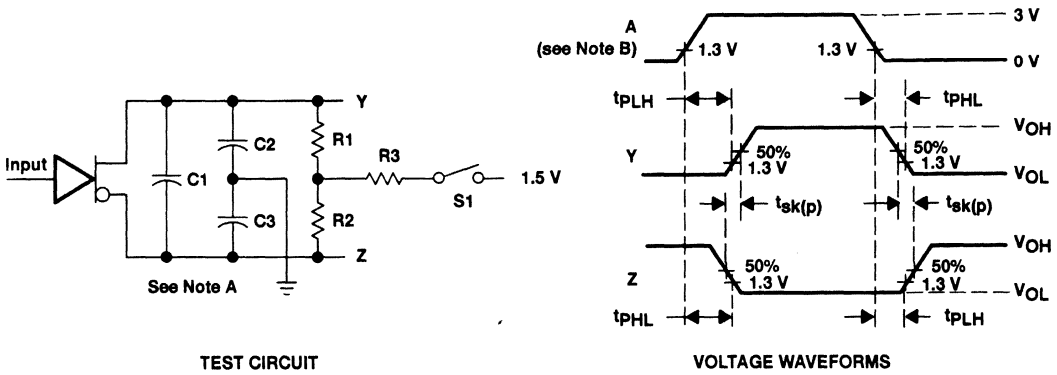


Figure 2. Driver Test Circuit and Voltage Waveforms

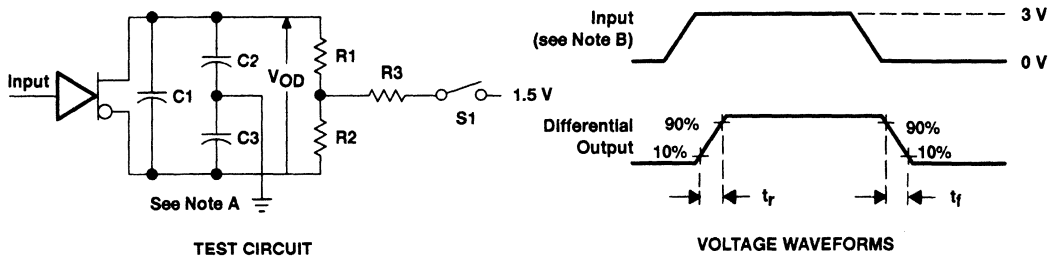
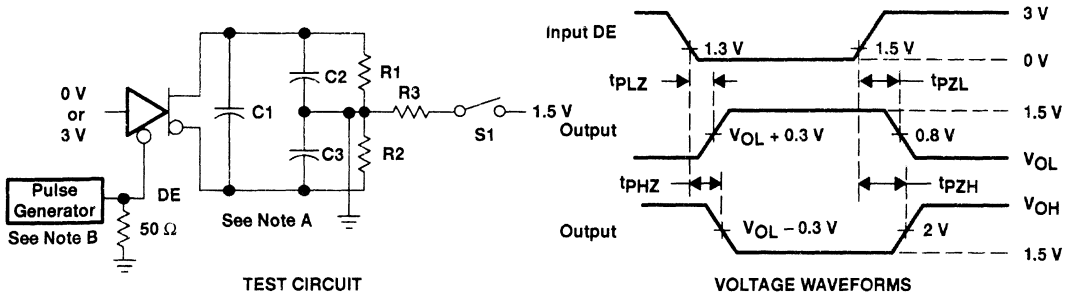


Figure 3. Driver Test Circuit and Voltage Waveforms

NOTES: A. C1, C2, and C3 includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6$ ns.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C1, C2, and C3 include probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6$ ns.

Figure 4. Driver Test Circuit and Voltage Waveforms

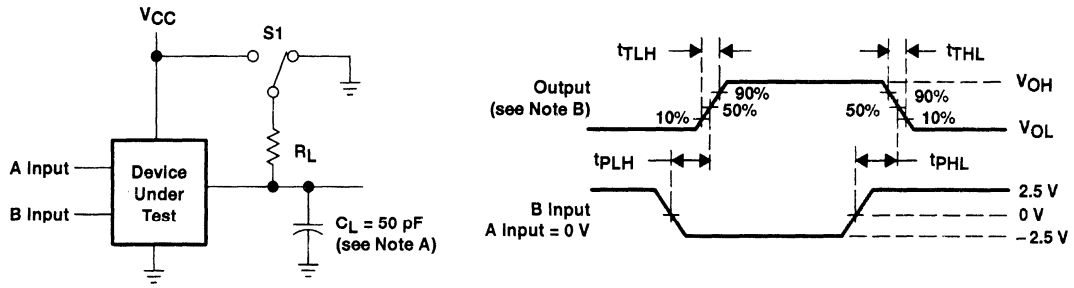


Figure 5. Receiver Test Circuit and Voltage Waveforms

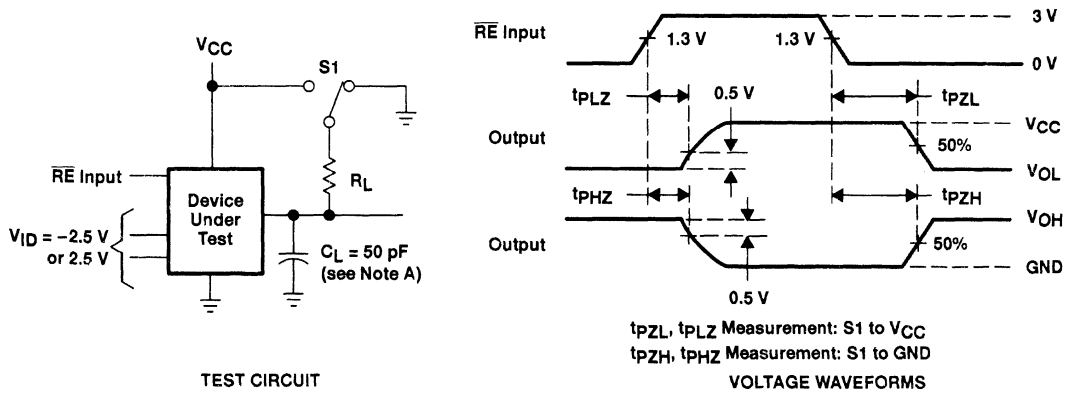


Figure 6. Receiver Test Circuit and Voltage Waveforms

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6$ ns.

SLLS059B – FEBRUARY 1990 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendations V.10 and V.11**
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noise Environments**
- **Driver Positive- and Negative-Current Limiting**
- **Thermal Shutdown Protection**
- **Driver 3-State Outputs**
- **Receiver Common-Mode Input Voltage Range of –12 V to 12 V**
- **Receiver Input Sensitivity . . . ±200 mV**
- **Receiver Hysteresis . . . 50 mV Typ**
- **Receiver Input Impedance . . . 12 kΩ Min**
- **Receiver 3-State Outputs (SN751177 Only)**
- **Operates From Single 5-V Supply**

description

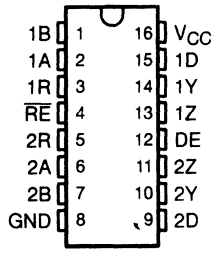
The SN751177 and SN751178 dual differential drivers and receivers are monolithic integrated circuits that are designed for balanced multipoint bus transmission at rates up to 10 Mbits per second. They are designed to improve the performance of full-duplex data communications over long bus lines and meet ANSI Standards EIA/TIA-422-B, RS-485 and ITU Recommendations V.10 and V.11.

The SN751177 and SN751178 driver outputs provide limiting for both positive and negative currents and thermal-shutdown protection from line fault conditions on the transmission bus line.

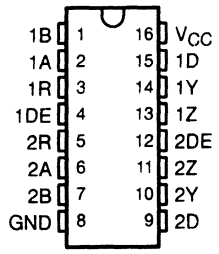
The receiver features high input impedance of at least 12 kΩ, an input sensitivity of ±200 mV over a common-mode input voltage range of –12 V to 12 V and typical input hysteresis of 50 mV. Fail-safe design ensures that if the receiver inputs are open, the receiver outputs will always be high.

The SN751177 and SN751178 are characterized for operation from –20°C to 85°C.

SN751177 . . . N PACKAGE
(TOP VIEW)



SN751178 . . . N OR NS† PACKAGE
(TOP VIEW)



† The NS package is only available left-end taped and reeled (order device SN751177NSLE).

Function Tables

SN751177, SN751178
EACH DRIVER

INPUT	ENABLE	OUTPUTS	
D	DE	Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

SN751177
EACH RECEIVER

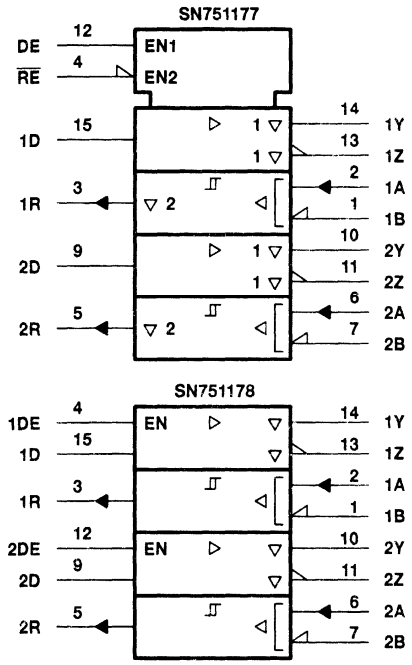
DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

SN751178
EACH RECEIVER

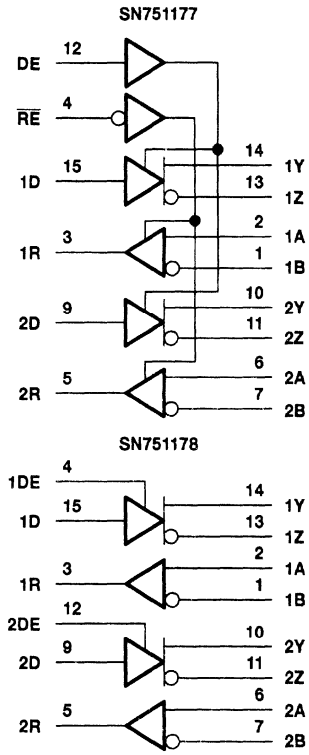
DIFFERENTIAL INPUTS A – B	OUTPUT R
$V_{ID} \geq 0.2$ V	H
-0.2 V $< V_{ID} < 0.2$ V	?
$V_{ID} \geq -0.2$ V	L

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

logic symbols†

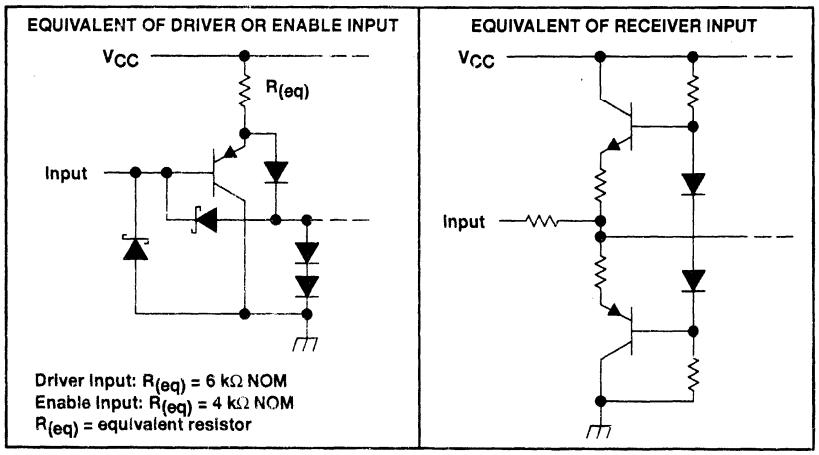


logic diagrams (positive logic)



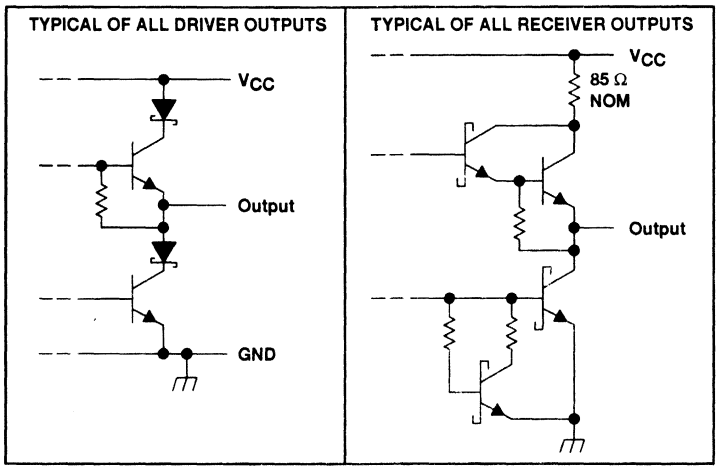
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematics of inputs



All resistors values are nominal.

schematics of outputs



All resistors values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I (DE, $\overline{RE}$, and D inputs)	7 V
Receiver input voltage range, V_I (A or B inputs)	−25 V to 25 V
Receiver differential input voltage range, V_{ID} (see Note 2)	−25 V to 25 V
Driver output voltage range, V_O	−10 V to 15 V
Receiver low-level output current, I_{OL}	50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3)	1150 mW
Operating free-air temperature range, T_A	−20°C to 85°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.
2. Differential input voltage is measured at the noninverting terminal with respect to the inverting terminal.
3. For operation above 25°C free-air temperature, derate to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	DE, $\overline{RE}$, and D inputs	2			V
Low-level input voltage, V_{IL}				0.8	V
Common-mode output voltage, V_{OC}	Driver	−7†		12	V
High-level output current, I_{OH}				−60	mA
Low-level output current, I_{OL}				60	mA
Common-mode input voltage, V_{IC}	Receiver			±12	V
Differential input voltage, V_{ID}				±12	V
High-level output current, I_{OH}				−400	μA
Low-level output current, I_{OL}				16	mA
Operating free-air temperature, T_A		−20		85	°C

† The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.

DRIVER SECTIONS

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −33 mA			3.7		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = 33 mA			1.1		V
$\lvert V_{OD1}\rvert$	Differential output voltage	I_O = 0		1.5		6	V
$\lvert V_{OD2}\rvert$	Differential output voltage	R_L = 100 Ω, See Figure 1		2			V
				1/2 V_{OD1}			
		R_L = 54 Ω, See Figure 1		1.5		5	
V_{OD3}	Differential output voltage	See Note 4		1.5		5	V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage (see Note 5)	R_L = 54 Ω or 100 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage			−1‡		3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage (see Note 5)					±0.2	V
I_O	Output current with power off	V_{CC} = 0, V_O = −7 V to 12 V				±100	μA
I_{OZ}	High-impedance-state output current	V_O = −7 V to 12 V				±100	μA
I_{IH}	High-level input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level input current	V_{IL} = 0.4 V				−100	μA
I_{OS}	Short-circuit output current (see Note 6)	V_O = −7 V				−250	mA
		V_O = V_{CC}				250	
		V_O = 12 V				250	
I_{CC}	Supply current	No load	Outputs enabled		80	110	mA
			Outputs disabled		50	80	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

‡ The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.

NOTES: 4. See ANSI Standard RS-485 Figure 3.5, Test Termination Measurement 2

5. $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

6. Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics at V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω,	See Figure 3		20	25	ns
$t_{t(OD)}$	Differential output transition time				27	35	ns
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 27 Ω,	See Figure 4		20	25	ns
t_{PHL}	Propagation delay time, high- to low-level output				20	25	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 5		80	120	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 6		40	60	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 5		90	120	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 6		30	45	ns

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	EIA/TIA-422-B	RS-485
$\lvert V_{OD1} \rvert$	V_O	V_O
$\lvert V_{OD2} \rvert$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\lvert V_{OD3} \rvert$		V_t (test termination measurement 2)
$\Delta \lvert V_{OD} \rvert$	$\lvert\lvert V_t \rvert - \lvert \overline{V}_t \rvert\rvert$	$\lvert\lvert V_t \rvert - \lvert \overline{V}_t \rvert\rvert$
V_{OC}	$\lvert V_{OS} \rvert$	$\lvert V_{OS} \rvert$
$\Delta \lvert V_{OC} \rvert$	$\lvert V_{OS} - \overline{V}_{OS} \rvert$	$\lvert V_{OS} - \overline{V}_{OS} \rvert$
I_{OS}	$\lvert I_{sa} \rvert, \lvert I_{sb} \rvert$	
I_O	$\lvert I_{xa} \rvert, \lvert I_{xb} \rvert$	I_{ia}, I_{ib}

RECEIVER SECTIONS

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{IT-}	Negative-going input threshold voltage		V_O = 0.5 V,	I_O = 16 mA	−0.2‡			V
V_{hys}	Input hysteresis voltage ($V_{IT+} - V_{IT-}$)					50		mV
V_{IK}	Enable clamp voltage	SN751177	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage		V_{ID} = 200 mV,	I_{OH} = −400 μA	2.7			V
V_{OL}	Low-level output voltage		V_{ID} = −200 mV	I_{OL} = 8 mA			0.45	V
				I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	SN751177	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current (see Note 7)		Other input at 0 V	V_I = 12 V			1	mA
				V_I = −7 V			−0.8	
I_{IH}	High-level enable input current	SN751177	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable input current	SN751177	V_{IL} = 0.4 V				−100	μA
I_{OS}	Short-circuit output current (see Note 6)				−15		−85	μA
I_{CC}	Supply current		No load,	Outputs enabled		80	110	mA
r_i	Input resistance				12			kΩ

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

‡ The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.

NOTES: 6. Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

7. Refer to ANSI Standards EIA/TIA-422-B, EIA/TIA-423-A, RS-485-A for exact conditions

switching characteristics at V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output		V_{ID} = –1.5 V to 1.5 V, See Figure 7		20	35	ns
t_{PHL}	Propagation delay time, high- to low-level output				22	35	ns
t_{PZH}	Output enable time to high level	SN751177	See Figure 8		17	25	ns
t_{PZL}	Output enable time to low level				20	27	ns
t_{PHZ}	Output disable time from high level				25	40	ns
t_{PLZ}	Output disable time from low level				30	40	ns

PARAMETER MEASUREMENT INFORMATION

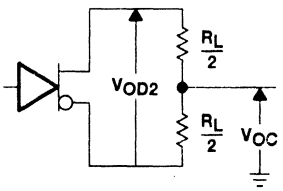


Figure 1. Driver Test Circuit, V_{OD} and V_{OC}

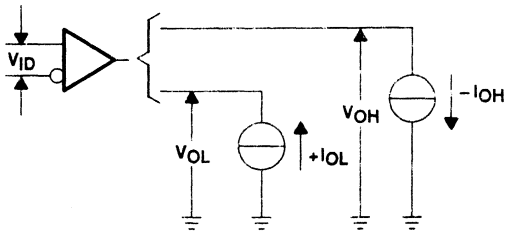
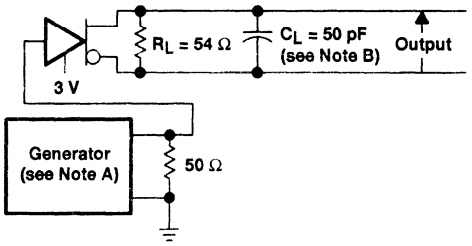
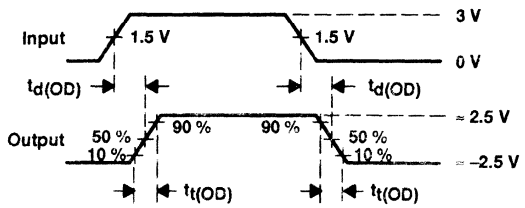


Figure 2. Receiver Test Circuit, V_{OH} and V_{OL}



TEST CIRCUIT

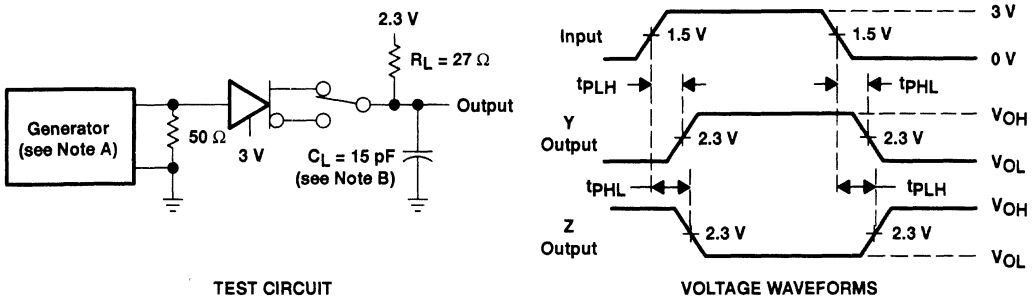


VOLTAGE WAVEFORMS

Figure 3. Driver Differential Output Delay and Transition Time Test Circuit and Voltage Waveforms

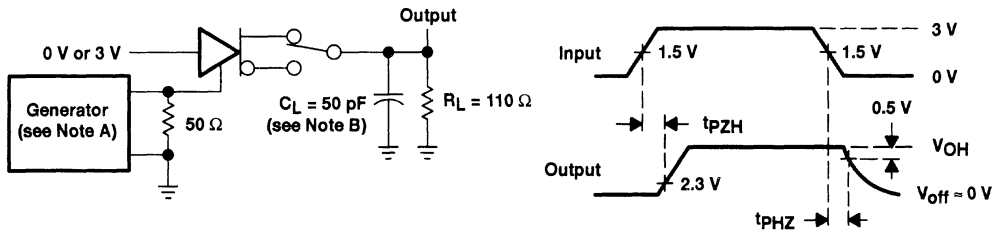
NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



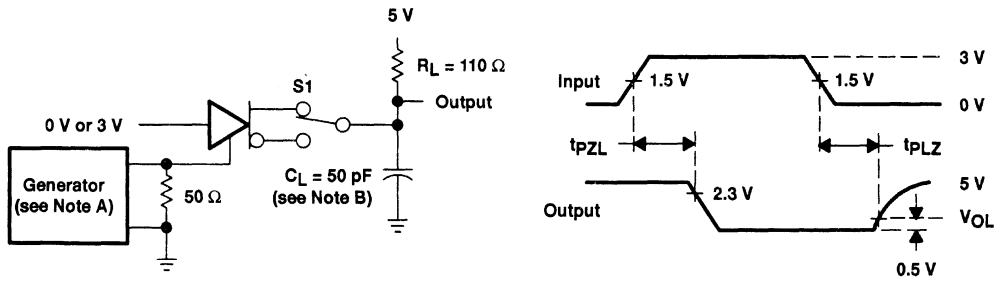
TEST CIRCUIT VOLTAGE WAVEFORMS

Figure 4. Driver Propagation Delay Time Test Circuit and Voltage Waveforms



TEST CIRCUIT VOLTAGE WAVEFORMS

Figure 5. Driver Enable and Disable Time Test Circuit and Voltage Waveforms



TEST CIRCUIT VOLTAGE WAVEFORMS

Figure 6. Driver Enable and Disable Time Test Circuit and Voltage Waveforms

NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

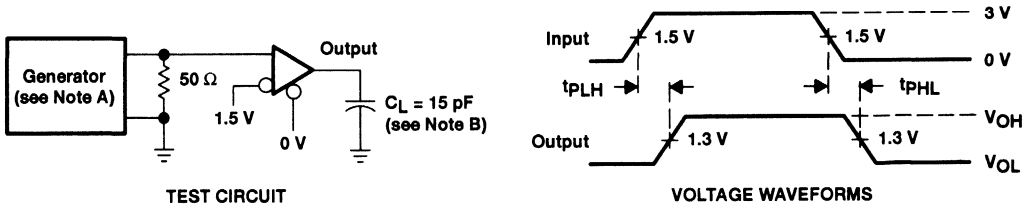


Figure 7. Receiver Propagation Delay Time Test Circuit and Voltage Waveforms

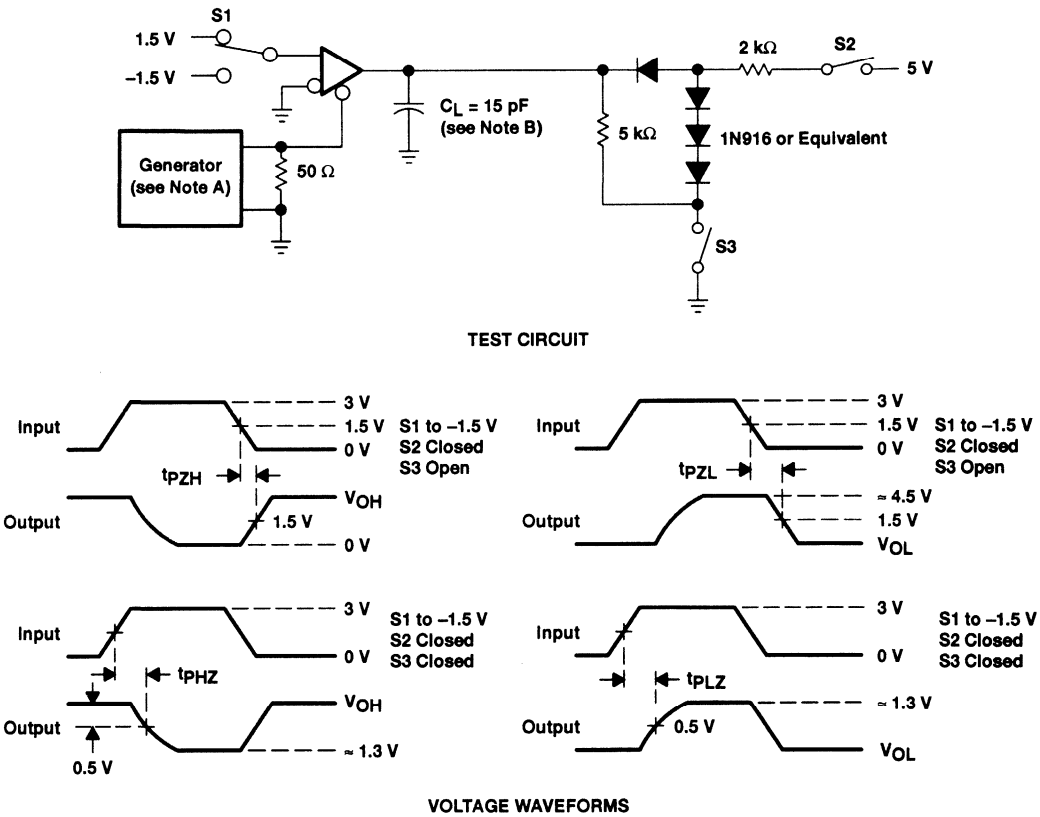


Figure 8. Receiver Output Enable and Disable Time Test Circuit and Voltage Waveforms

NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, Z_O = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns.
B. C_L includes probe and jig capacitance.

SN75ALS1177, SN75ALS1178
DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

SLLS154A– MARCH 1993 – REVISED MAY 1995

- **Meets or Exceeds Standards EIA/TIA-422-B, RS-485, CCITT Recommendation V.11**
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments**
- **Low Supply Current Requirement 50 mA Max**
- **Driver Positive- and Negative-Current Limiting**
- **Driver Common-Mode Output Voltage Range of –7 V to 12 V**
- **Thermal Shutdown Protection**
- **Driver 3-State Outputs Active-High Enable**
- **Receiver Common-Mode Input Voltage Range of –12 V to 12 V**
- **Receiver Input Sensitivity . . . ±200 mV**
- **Receiver Hysteresis . . . 50 mV Typ**
- **Receiver High Input Impedance 12 kΩ Min**
- **Receiver 3-State Outputs Active-Low Enable for SN75ALS1177 Only**
- **Operates From Single 5-V Supply**

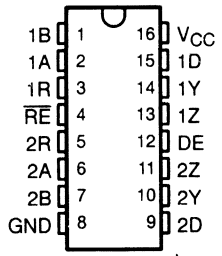
description

The SN75ALS1177 and SN75ALS1178 dual differential drivers and receivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet standards EIA/TIA-422-B, RS-485, and CCITT Recommendation V.11.

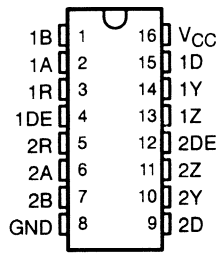
The SN75ALS1177 combines dual 3-state differential line drivers and dual 3-state differential input line receivers, both of which operate from a single 5-V power supply. The drivers and receivers have active-high and active-low enables, respectively, which can be externally connected together to function as direction control. The SN75ALS1178 drivers each have an individual active-high enable. Fail-safe design ensures that when the receiver inputs are open, the receiver outputs are always high.

The SN75ALS1177 and SN75ALS1178 are characterized for operation from 0°C to 70°C.

SN75ALS1177 . . . N OR NS† PACKAGE
(TOP VIEW)



SN75ALS1178 . . . N OR NS† PACKAGE
(TOP VIEW)



† The NS package is only available in left-end taped and reeled (SN75ALS1177NSLE and SN75ALS1178SNLE).

Function Tables

SN75ALS1177, SN75ALS1178
EACH DRIVER

INPUT	ENABLE	OUTPUTS	
D	DE	Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

SN75ALS1177, EACH RECEIVER

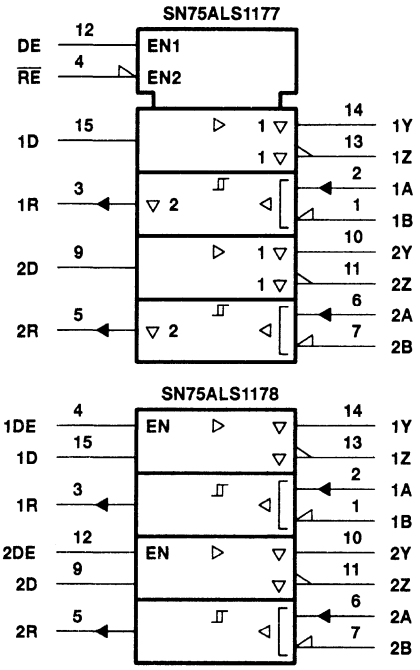
DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

SN75ALS1178, EACH RECEIVER

DIFFERENTIAL INPUTS A – B	OUTPUT R
$V_{ID} \geq 0.2$ V	H
-0.2 V $< V_{ID} < 0.2$ V	?
$V_{ID} \leq -0.2$ V	L
Open	H

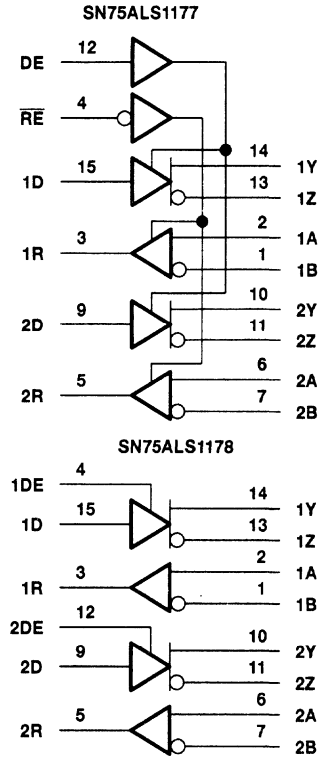
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

logic symbols†

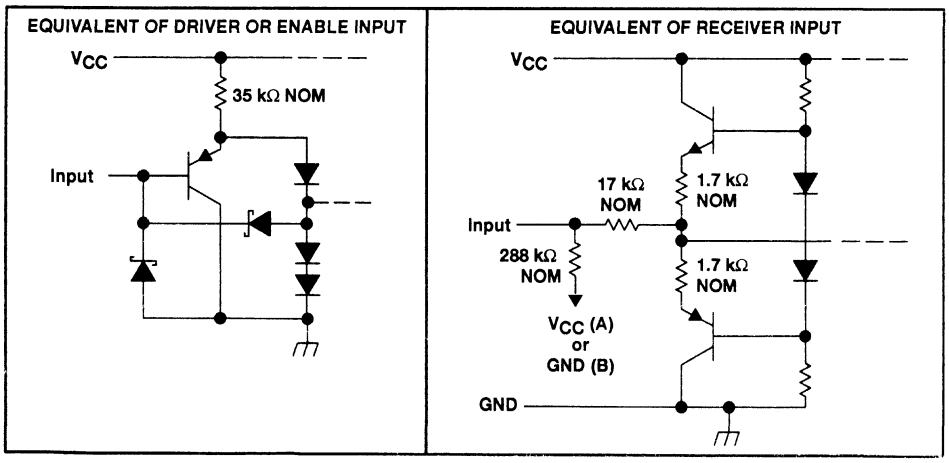


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

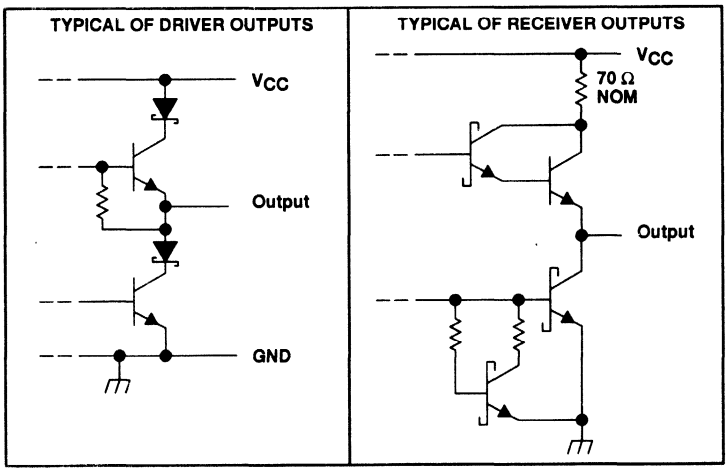


equivalent schematics



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

schematics of outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I (DE, $\overline{RE}$, and D inputs) ..... 7 V
Output voltage range, V_O (Driver) ..... −9 V to 14 V
Input voltage range, Receiver ..... −14 V to 14 V
Receiver differential-input voltage range (see Note 2) ..... −14 V to 14 V
Receiver low-level output current ..... 50 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.
2. Differential input voltage is measured at the noninverting terminal with respect to the inverting terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
N	1150 mW	9.2 mW/°C	736 mW
NS	625 mW	4.0 mW/°C	445 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Differential input voltage, V_{ID}	Receiver			±12	V
Common-mode output voltage, V_{OC}	Driver	−7†		12	V
Common-mode input voltage, V_{IC}	Receiver			±12	V
High-level input voltage, V_{IH}	DE, $\overline{RE}$, D	2			V
Low-level input voltage, V_{IL}	DE, $\overline{RE}$, D			0.8	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

† The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage level only.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, $I_{OH} = -33$ mA			3.3		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 33 mA			1.1		V
$\lvert V_{OD1}\rvert$	Differential output voltage	$I_O = 0$		1.5		6	V
$\lvert V_{OD2}\rvert$	Differential output voltage	V_{CC} = 5 V, R_L = 100 Ω	See Figure 1	1/2 V_{OD1}			V
				2			
		R_L = 54 Ω		1.5		5	
$\lvert V_{OD3}\rvert$	Differential output voltage	See Note 3		1.5		5	V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage (see Note 4)	R_L = 54 Ω or 100 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage			−1‡		3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage (see Note 4)					±0.2	V
$I_{O(OFF)}$	Output current with power off	V_{CC} = 0, V_O = −7 V to 12 V				±100	μA
I_{OZ}	High-impedance-state output current	V_O = −7 V to 12 V				±100	μA
I_{IH}	High-level input current	V_{IH} = 2.7 V				100	μA
I_{IL}	Low-level input current	V_{IL} = 0.4 V				−100	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−250	mA
		$V_O = V_{CC}$				250	
		V_O = 12 V				250	
		V_O = 0 V				150	
I_{CC}	Supply current (total package)	No load	Outputs enabled		35	50	mA
			Outputs disabled		20	50	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

‡ The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.

NOTES: 3. See EIA Standard RS-485 Figure 3.5, test termination measurement 2.

4. $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

switching characteristics at V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, high- to low-level output	R_L = 60 Ω, See Figure 3	$C_{L1} = C_{L2}$ = 100 pF,	9	15	22	ns
t_{PHL}	Propagation delay time, low- to high-level output			9	15	22	ns
t_{sk}	Output-to-output skew			0	2	8	ns
t_{PZH}	Output enable time to high level	C_L = 100 pF,	See Figure 4	30	35	50	ns
t_{PZL}	Output enable time to low level	C_L = 100 pF,	See Figure 5	5	15	25	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 4	7	15	30	ns
t_{PLZ}	Output disable time from low level	C_L = 15 pF,	See Figure 5	7	15	30	ns

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{IT-}	Negative-going input threshold voltage		V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Input hysteresis voltage ($V_{IT+} - V_{IT-}$)					50		mV
V_{IK}	Enable input clamp voltage	SN75ALS1177	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage		V_{ID} = 200 mV, See Figure 2	I_{OH} = −400 μA,	2.7			V
V_{OL}	Low-level output voltage		V_{ID} = 200 mV, See Figure 2	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	SN75ALS1177	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current (see Note 5)		Other input at 0 V	V_I = 12 V			1	mA
				V_I = −7 V			−0.8	
I_{IH}	High-level input current, $\overline{RE}$	SN75ALS1177	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level input current, $\overline{RE}$	SN75ALS1177	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance				12			kΩ
I_{OS}	Short-circuit output current		V_O = 0 V,	See Note 6	−15		−85	mA
I_{CC}	Supply current (total package)		No load,	Outputs enabled		35	50	mA

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

‡ The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.

NOTES: 5. Refer to EIA standards RS-422-A, RS-423-A, and RS-485-A for exact conditions.

6. Not more than one output should be shorted at a time.

switching characteristics at V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output		C_L = 15 pF,	See Figure 6	15	25	37	ns
t_{PHL}	Propagation delay time, high- to low-level output				15	25	37	ns
t_{PZH}	Output enable time to high level	SN75ALS1177	C_L = 100 pF,	See Figure 7	10	20	30	ns
t_{PZL}	Output enable time to low level	SN75ALS1177	C_L = 100 pF,	See Figure 7	10	20	30	ns
t_{PHZ}	Output disable time from high level	SN75ALS1177	C_L = 15 pF,	See Figure 7	5	12	16	ns
t_{PLZ}	Output disable time from low level	SN75ALS1177	C_L = 15 pF,	See Figure 7	5	12	16	ns

PARAMETER MEASUREMENT INFORMATION

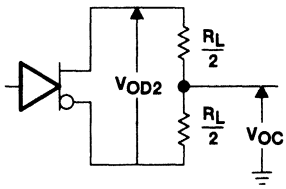


Figure 1. Driver Test Circuit, V_{OD} and V_{OC}

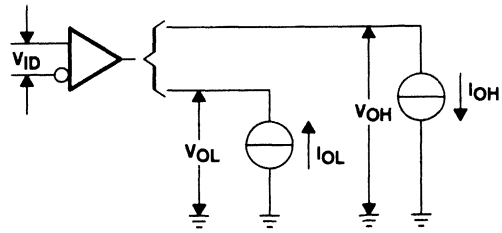
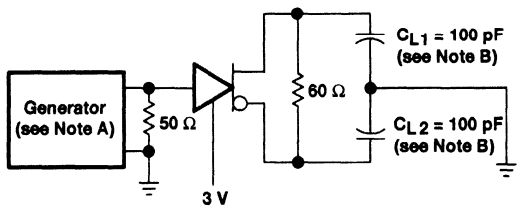
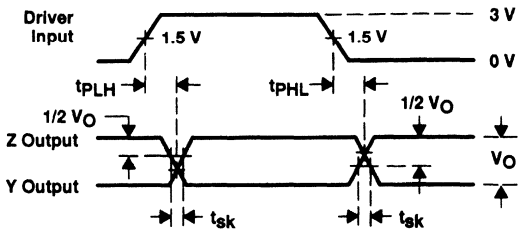


Figure 2. Receiver Test Circuit, V_{OH} and V_{OL}



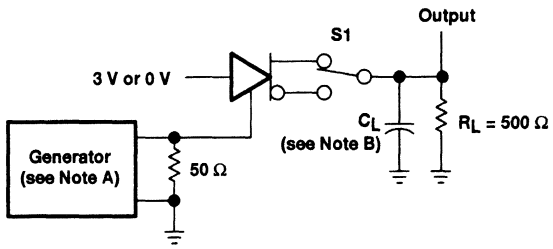
DRIVER TEST CIRCUIT



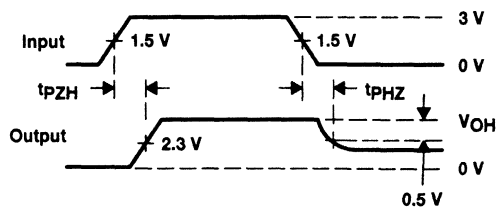
DRIVER VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Propagation Delay Times



DRIVER TEST CIRCUIT

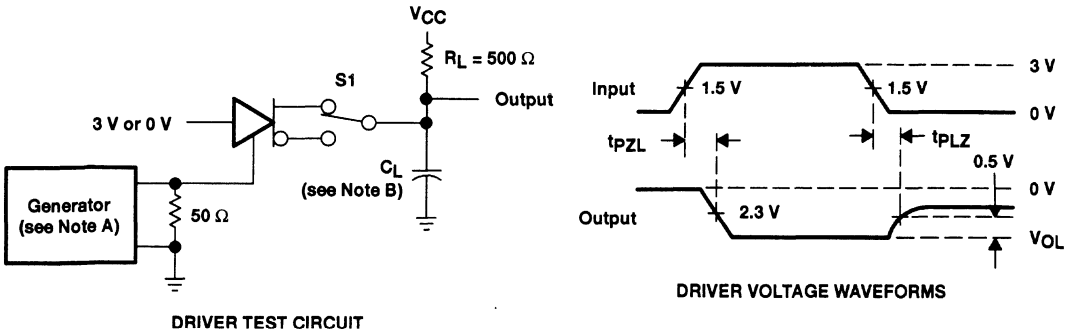


DRIVER VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.
B. C_L includes probe and jig capacitance.

Figure 4. Driver Enable and Disable Times

PARAMETER MEASUREMENT INFORMATION

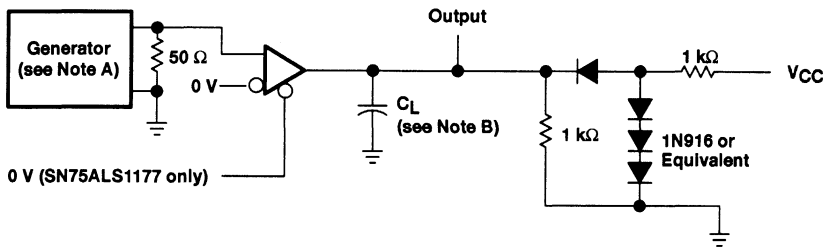


DRIVER TEST CIRCUIT

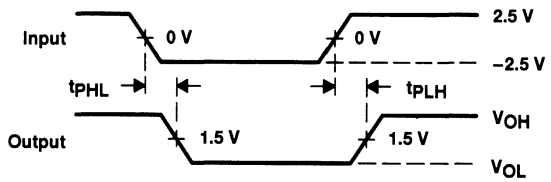
DRIVER VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.
B. C_L includes probe and jig capacitance.

Figure 5. Driver Enable and Disable Times



RECEIVER TEST CIRCUIT

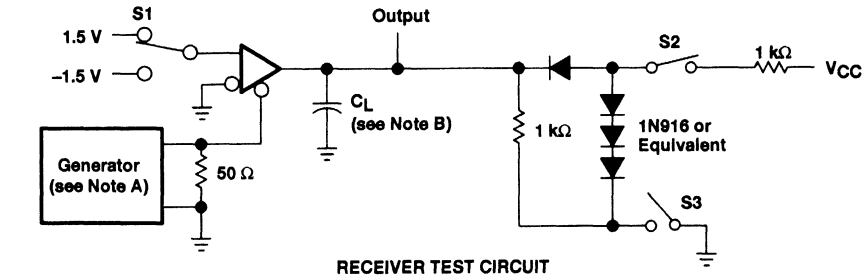


DRIVER VOLTAGE WAVEFORMS

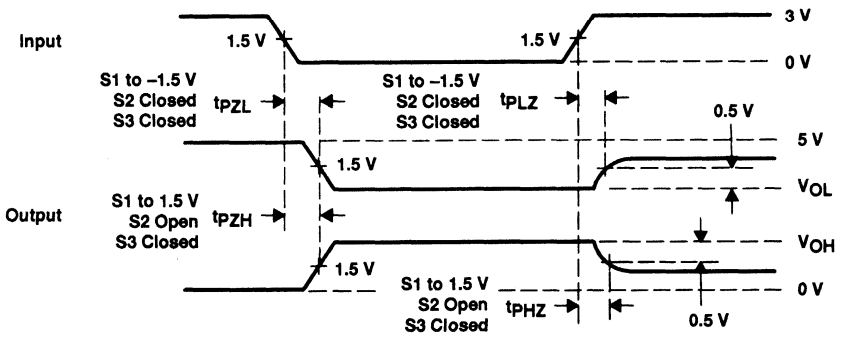
NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.
B. C_L includes probe and jig capacitance.

Figure 6. Receiver Propagation Delay Times

PARAMETER MEASUREMENT INFORMATION



RECEIVER TEST CIRCUIT



RECEIVER VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.
B. C_L includes probe and jig capacitance.

Figure 7. Receiver Output Enable and Disable Times

- **Meet or Exceed the Requirements of ANSI EIA/TIA-232-E and ITU Recommendation V.28**
- **Very Low Power Consumption 5 mW Typ**
- **Wide Driver Supply Voltage Range ±4.5 V to ±15 V**
- **Driver Output Slew Rate Limited to 30 V/μs Max**
- **Receiver Input Hysteresis . . . 1000 mV Typ**
- **Push-Pull Receiver Outputs**
- **On-Chip Receiver 1-μs Noise Filter**
- **Functionally Interchangeable With Motorola MC145406 and Texas Instruments TL145406**

D, DW, OR N PACKAGE
(TOP VIEW)

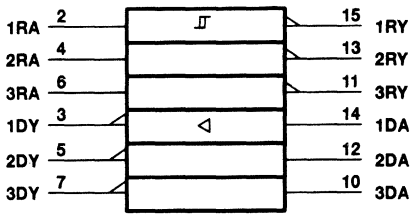
description

The SN65C1406 and SN75C1406 are low-power BiMOS devices containing three independent drivers and receivers that are used to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). This device is designed to conform to ANSI EIA/TIA-232-E. The drivers and receivers of the SN65C1406 and SN75C1406 are similar to those of the SN75C188 quadruple driver and SN75C189A quadruple receiver, respectively. The drivers have a controlled output slew rate that is limited to a maximum of 30 V/μs, and the receivers have filters that reject input noise pulses shorter than 1 μs. Both these features eliminate the need for external components.

The SN65C1406 and SN75C1406 have been designed using low-power techniques in a BiMOS technology. In most applications, the receivers contained in these devices interface to single inputs of peripheral devices such as ACES, UARTs, or microprocessors. By using sampling, such peripheral devices are usually insensitive to the transition times of the input signals. If this is not the case, or for other uses, it is recommended that the SN65C1406 and SN75C1406 receiver outputs be buffered by single Schmitt input gates or single gates of the HCMOS, ALS, or 74F logic families.

The SN65C1406 is characterized for operation from −40°C to 85°C. The SN75C1406 is characterized for operation from 0°C to 70°C.

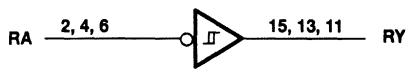
logic symbol†



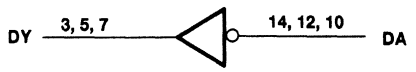
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

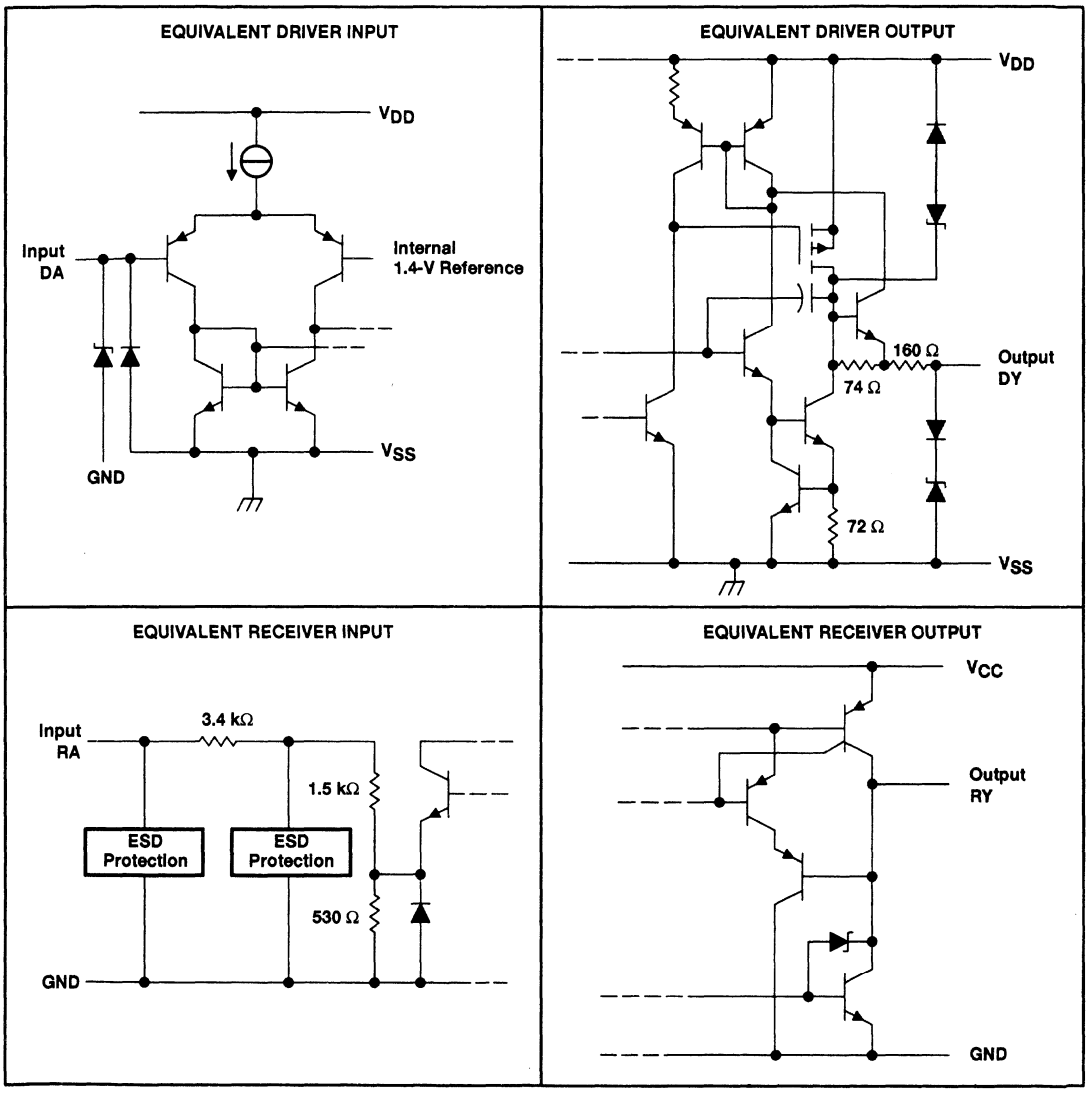
Typical of each receiver



Typical of each driver



schematics of inputs and outputs



All resistor values shown are nominal.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 15 V
Supply voltage, V_{SS} ..... −15 V
Supply voltage, V_{CC} ..... 7 V
Input voltage range, V_I: Driver ..... V_{SS} to V_{DD}
Receiver ..... −30 V to 30 V
Output voltage range, V_O: Driver ..... (V_{SS} − 6 V) to (V_{DD} + 6 V)
Receiver ..... −0.3 V to (V_{CC} + 0.3 V)
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65C1406 ..... −40°C to 85°C
SN75C1406 ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150 °C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
DW	1025 mW	8.2 mW/°C	656 mW	533 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.5	12	15	V
Supply voltage, V_{SS}		−4.5	−12	−15	V
Supply voltage, V_{CC}		4.5	5	6	V
Input voltage, V_I	Driver	V_{SS}+2		V_{DD}	V
	Receiver			±25	
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}				−1	mA
Low-level output current, I_{OL}				3.2	mA
Operating free-air temperature, T_A	SN65C1406	−40		85	°C
	SN75C1406	0		70	

DRIVER SECTION

electrical characteristics over operating free-air temperature range, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ± 10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{IH} = 0.8 V, R_L = 3 kΩ, See Figure 1	V_{DD} = 5 V, V_{SS} = −5 V	4	4.5		V
			V_{DD} = 12 V, V_{SS} = −12 V	10	10.8		
V_{OL}	Low-level output voltage (see Note 2)	V_{IH} = 2 V, R_L = 3 kΩ, See Figure 1	V_{DD} = 5 V, V_{SS} = −5 V		−4.4	−4	V
			V_{DD} = 12 V, V_{SS} = −12 V		−10.7	−10	
I_{IH}	High-level input current	V_I = 5 V, See Figure 2				1	µA
I_{IL}	Low-level input current	V_I = 0, See Figure 2				−1	µA
$I_{OS(H)}$	High-level short circuit output current‡	V_I = 0.8 V, V_O = 0 or V_{SS}, See Figure 1		−7.5	−12	−19.5	mA
$I_{OS(L)}$	Low-level short circuit output current‡	V_I = 2 V, V_O = 0 or V_{DD}, See Figure 1		7.5	12	19.5	mA
I_{DD}	Supply current from V_{DD}	No load, All inputs at 2 V or 0.8 V	V_{DD} = 5 V, V_{SS} = −5 V		115	250	µA
			V_{DD} = 12 V, V_{SS} = −12 V		115	250	
I_{SS}	Supply current from V_{SS}	No load, All inputs at 2 V or 0.8 V	V_{DD} = 5 V, V_{SS} = −5 V		−115	−250	µA
			V_{DD} = 12 V, V_{SS} = −12 V		−115	−250	
r_O	Output resistance	V_{DD} = V_{SS} = V_{CC} = 0, V_O = −2 V to 2 V, See Note 3		300	400		Ω

† All typical values are at T_A = 25°C.
‡ Not more than one output should be shorted at a time.
NOTES: 2. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only.
3. Test conditions are those specified by EIA/TIA-232-E.

switching characteristics at T_A = 25°C, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ± 10%

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output§	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 3		1.2	3	µs
t_{PHL}	Propagation delay time, high- to low-level output§			2.5	3.5	µs
t_{TLH}	Transition time, low- to high-level output¶		0.53	2	3.2	µs
t_{THL}	Transition time, high- to low-level output¶		0.53	2	3.2	µs
t_{TLH}	Transition time, low- to high-level output#	R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF, See Figure 3		1	2	µs
t_{THL}	Transition time, high- to low-level output#	R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF, See Figure 3		1	2	µs
SR	Output slew rate	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Figure 3	4	10	30	V/µs

§ t_{PHL} and t_{PLH} include the additional time due to on-chip slew rate and are measured at the 50% points.
¶ Measured between 10% and 90% points of output waveform
# Measured between 3-V and −3-V points of output waveform (EIA/TIA-232-E conditions) with all unused inputs tied either high or low

RECEIVER SECTION

electrical characteristics over operating free-air temperature range, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ± 10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshhold voltage	See Figure 5		1.7	2	2.55	V
V_{IT-}	Negative-going input threshhold voltage	See Figure 5		0.65	1	1.25	V
V_{hys}	Input hysteresis voltage (V_{IT+}–V_{IT-})			600	1000		mV
V_{OH}	High-level output voltage	V_I = 0.75 V, I_{OH} = −20 μA,	See Figure 5 and Note 4	3.5			V
		V_I = 0.75 V, I_{OH} = −1 mA, See Figure 5	V_{CC} = 4.5 V	2.8	4.4		
			V_{CC} = 5 V	3.8	4.9		
			V_{CC} = 5.5 V	4.3	5.4		
V_{OL}	Low-level output voltage	V_I = 3 V, I_{OL} = 3.2 mA,	See Figure 5		0.17	0.4	V
I_{IH}	High-level input current	V_I = 2.5 V		3.6	4.6	8.3	mA
		V_I = 3 V		0.43	0.55	1	
I_{IL}	Low-level input current	V_I = −2.5 V		−3.6	−5	−8.3	
		V_I = −3 V		−0.43	−0.55	−1	
$I_{OS(H)}$	High-level short-circuit output current	V_I = 0.75 V, V_O = 0,	See Figure 4		−8	−15	mA
$I_{OS(L)}$	Low-level short-circuit output current	V_I = V_{CC}, V_O = V_{CC},	See Figure 4		13	25	mA
I_{CC}	Supply current from V_{CC}	No load, All inputs at 0 or 5 V	V_{DD} = 5 V, V_{SS} = −5 V		320	450	μA
			V_{DD} = 12 V, V_{SS} = −12 V		320	450	

† All typical values are at T_A = 25°C.

NOTE 4: If the inputs are left unconnected, the receiver interprets this as an input low and the receiver outputs will remain in the high state.

switching characteristics at T_A = 25°C, V_{DD} = 12 V, V_{SS} = −12 V, V_{CC} = 5 V ± 10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 50 pF, R_L = 5 kΩ, See Figure 6		3	4	μs
t_{PHL}	Propagation delay time, high- to low-level output			3	4	μs
t_{TLH}	Transition time, low- to high-level output‡			300	450	ns
t_{THL}	Transition time, high- to low-level output‡			100	300	ns
$t_{w(N)}$	Duration of longest pulse rejected as noise§	C_L = 50 pF, R_L = 5 kΩ	1		4	μs

‡ Measured between 10% and 90% points of output waveform

§ The receiver ignores any positive- or negative-going pulse that is less than the minimum value of $t_{w(N)}$ and accepts any positive- or negative-going pulse greater than the maximum of $t_{w(N)}$.

PARAMETER MEASUREMENT INFORMATION

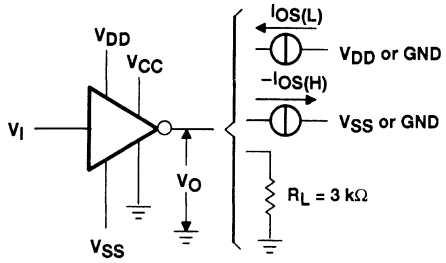


Figure 1. Driver Test Circuit V_{OH}, V_{OL}, $I_{OS(L)}$, $I_{OS(H)}$

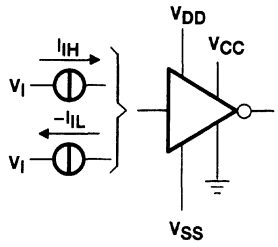
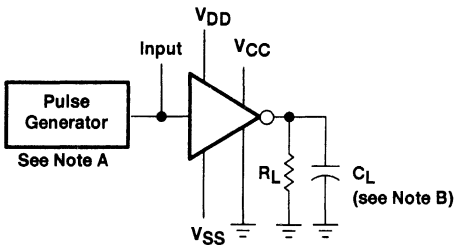
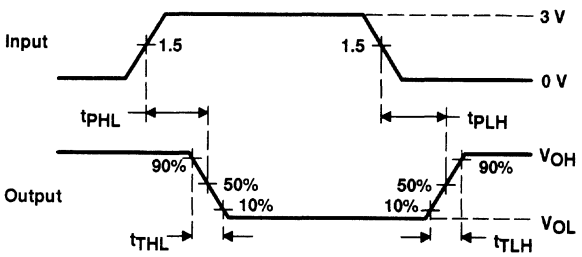


Figure 2. Driver Test Circuit, I_{IL}, I_{IH}



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: t_W = 25 µs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f < 50$ ns.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

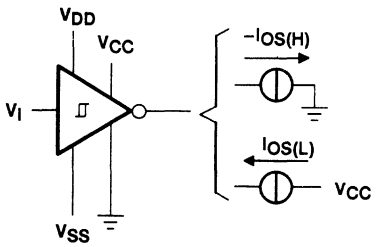


Figure 4. Receiver Test Circuit, $I_{OS(H)}$, $I_{OS(L)}$

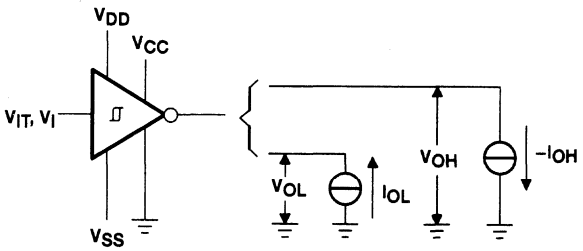


Figure 5. Receiver Test Circuit, V_{IT}, V_{OL}, V_{OH}

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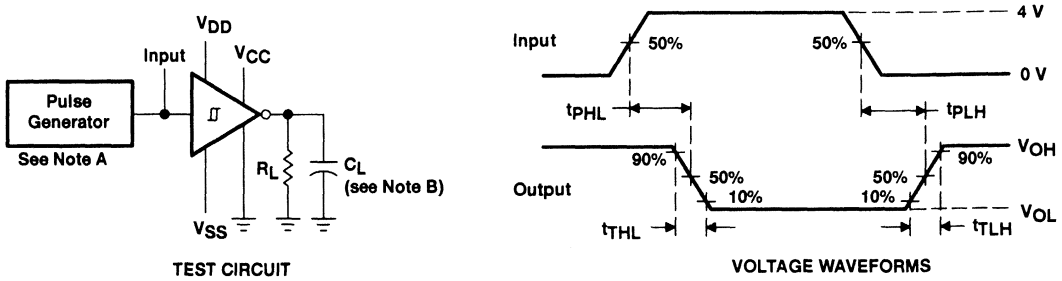
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: t_W = 25 μs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f < 50$ ns.
B. C_L includes probe and jig capacitance.

Figure 6. Receiver Test Circuit and Voltage Waveforms

APPLICATION INFORMATION

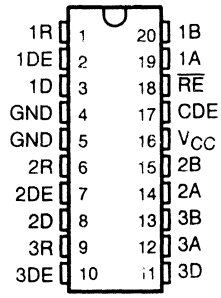
The EIA/TIA-232-E specification is for data interchange between a host computer and a peripheral at signaling rates up to 20 kbps. Many EIA/TIA-232-E devices will operate at higher data rates with lower capacitive loads (short cables). For reliable operation at greater than 20 kbps, the designer needs to have control of both ends of the cable. By mixing different types of EIA/TIA-232-E devices and cable lengths, errors can occur at higher frequencies (above 20 kbps). When operating within the EIA/TIA-232-E requirements of less than 20 kbps and with compliant line circuits, interoperability is assured. For applications operating above 20 kbps, the design engineer should consider devices and system designs that meet the EIA/TIA-423-B requirements.

SN75ALS1711
TRIPLE DIFFERENTIAL BUS TRANSCEIVER

SLLS117B – APRIL 1991 – REVISED MAY 1995

- Three Bidirectional Transceivers
- Driver/Receiver Meets or Exceeds the Requirements of ANSI Standard RS-485 and ANSI Standard X3.131-1986 (SCSI)
- High-Speed Advanced Low-Power Schottky Circuitry
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Wide Positive and Negative Input/Output Bus Voltages Ranges . . . –7 V to 12 V
- Driver Output Capacity . . . ±60 mA
- Driver Positive and Negative Current Limiting
- Thermal Shutdown Protection
- Receiver Input Sensitivity . . . ±200 mV Max
- Receiver Input Impedance . . . 12 kΩ Min
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates From a Single 5-V Supply
- Low Supply-Current Requirements 72 mA Max
- Glitch-Free Power-Up and Power-Down Protection

DW OR N PACKAGE
(TOP VIEW)



Function Tables

EACH DRIVER

INPUT	ENABLES		OUTPUTS	
D	DE	CDE	A	B
H	H	H	H	L
L	H	H	L	H
X	L	X	Z	Z
X	X	L	Z	Z

EACH RECEIVER

DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
V_{ID} = –0.2 V to 0.2 V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

H = high level, L = low-level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

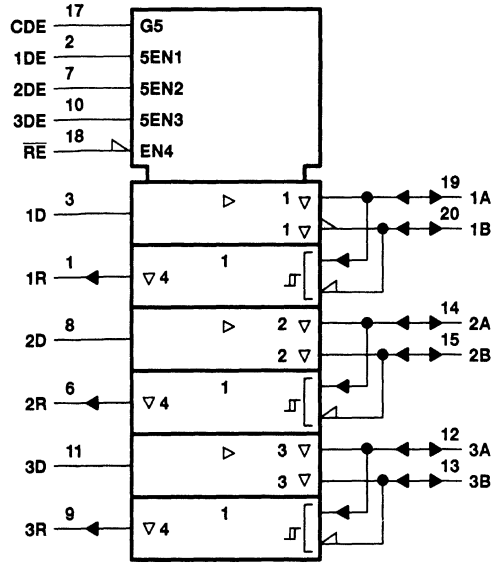
description

The SN75ALS1711 triple differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and meets ANSI Standard RS-485 and ANSI Standard X3.131-1986 (SCSI).

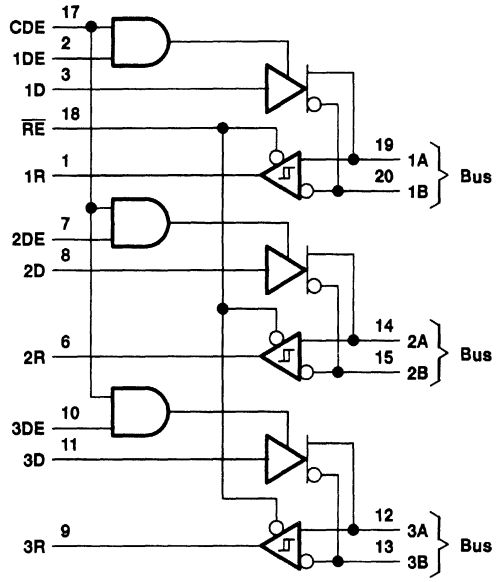
The SN75ALS1711 operates from a single 5-V power supply. The drivers and receivers have individual active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver differential output and the receiver differential input pairs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or V_{CC} is at 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The SN75ALS1711 is characterized for operation from 0°C to 70°C.

logic symbol†

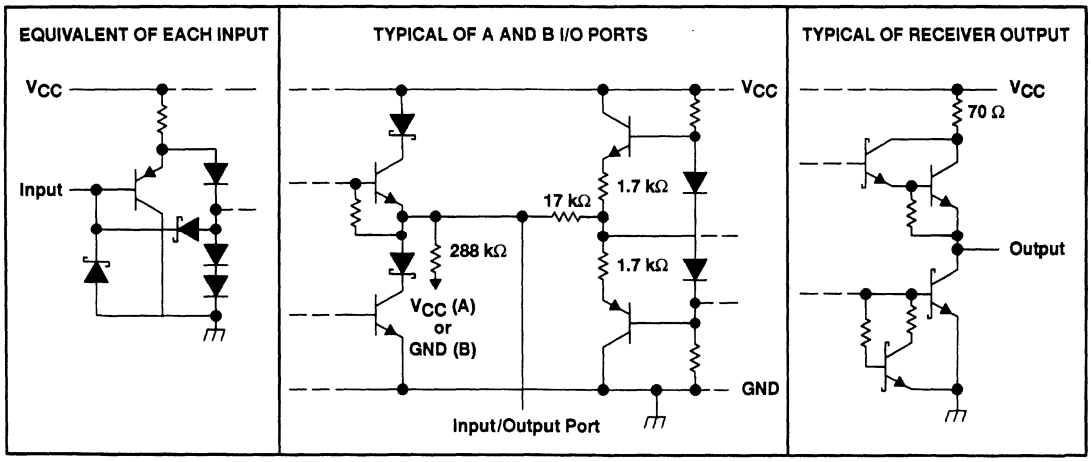


logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs



All values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Enable input voltage range, V_I ..... −0.5 V to V_{CC} + 0.5 V
Input voltage range, V_I: Driver ..... −0.5 V to V_{CC} + 0.5 V
Receiver ..... −9 V to 14 V
Output voltage range, V_O: Driver ..... −9 V to 14 V
Receiver ..... −0.5 V to V_{CC} + 0.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Common-mode input voltage at any bus terminal, V_{IC} (see Note 2)		−7‡		12	V
High-level input voltage, V_{IH}	D, DE, $\overline{RE}$, CDE	2			V
Low-level input voltage, V_{IL}	D, DE, $\overline{RE}$, CDE			0.8	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	µA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_O	Output voltage	$I_O = 0$		0		6	V
V_{OD1}	Differential output voltage	$I_O = 0$		1.5		5	V
V_{OD2}	Differential output voltage	$R_L = 54\ \Omega$, See Figure 1		1.5		5	V
V_{OD3}	Differential output voltage	See Note 3 and Figure 2		1.5		5	V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage‡	$R_L = 54\ \Omega$, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage	$R_L = 54\ \Omega$, See Figure 1				3 −1	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage‡	$R_L = 54\ \Omega$, See Figure 1				±0.2	V
I_{OZ}	High-impedance state output current	Output disabled, $V_{CC} = 5.25$ V	$V_O = 12$ V			1	mA
			$V_O = 7$ V			−0.8	
I_{IH}	High-level input current, DE, EN, CDE	$V_{IH} = 2.4$ V				20	μA
I_{IL}	Low-level input current, DE, EN, CDE	$V_{IL} = 0.4$ V				−200	μA
I_{OS}	Short-circuit output current	$V_O = 12$ V				−250	mA
		$V_O = 7$ V				250	
I_{CC}	Supply current	No load	Outputs enabled		48	72	mA
			Outputs disabled		30	48	

† All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.
‡ $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
NOTE 3: This applies for both power on and off; refer to ANSI Standard RS-485 for exact conditions.

switching characteristics, $V_{CC} = 5$ V ±5%, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Differential propagation delay time, low- to high-level output	$R_L = 54\ \Omega$, $C_L = 100$ pF, See Figure 3		8	13	22	ns
t_{PHL}	Differential propagation delay time, high- to low-level output			8	15	22	
t_{PZH}	Output enable time to high level	$R_L = 110\ \Omega$, See Figure 4	S1 open, S2 closed	30	50	60	ns
t_{PHZ}	Output disable time from high level			4	16	30	
t_{PZL}	Output enable time to low level		S1 closed, S2 open	16	26	45	
t_{PLZ}	Output disable time from low level			4	8	20	

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{IT-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 4 mA	−0.2‡			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)				50		mV
V_{IK}	Input clamp voltage, $\overline{RE}$	I_I = 18 mA				−1.5	V
V_{OH}	High-level output voltage	I_{OH} = −0.4 mA		2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA				0.5	V
I_{OZ}	High-impedance-state output current	V_{CC} = 5.25 V,	V_O = 0.4 V to 2.4 V			±20	µA
I_I	Line input current	Other input at 0, See Note 3	V_I = 12 V			1	mA
			V_I = 7 V			−0.8	
I_{IH}	High-level input current, $\overline{RE}$	V_{IH} = 2.4 V				20	µA
I_{IL}	Low-level input current, $\overline{RE}$	V_{IL} = 0.4 V				−200	µA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current§	V_O = 0		−15		−130	mA
I_{CC}	Supply current	No load	Outputs enabled		48	72	mA
			Outputs disabled		30	48	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
§ Not more than one output should be shorted at one time.
NOTE 3: This applies for both power on and off; refer to ANSI Standard RS-485 for exact conditions.

switching characteristics, V_{CC} = 5 V ± 5%, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See Figures 5 and 6		13	20	37	ns
t_{PHL}	Propagation delay time, high- to low-level output			13	20	37	
t_{PZH}	Output enable time to high level	See Figures 5 and 7	S1 to 1.5 V, S2 open, S3 closed	3	9	20	ns
t_{PHZ}	Output disable time from high level			8	15	22	
t_{PZL}	Output enable time to low level		S1 to −1.5 V, S2 closed, S3 open	5	10	20	
t_{PZL}	Output enable time to low level			5	9	16	

PARAMETER MEASUREMENT INFORMATION

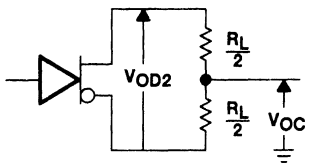


Figure 1. Driver V_{OD} and V_{OC}

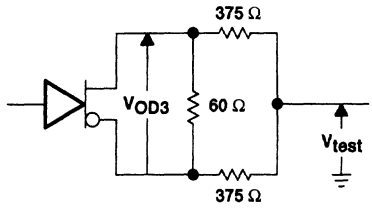
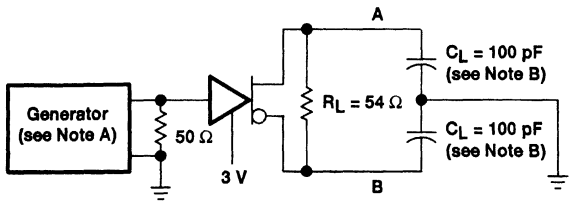


Figure 2. Driver V_{OD3}



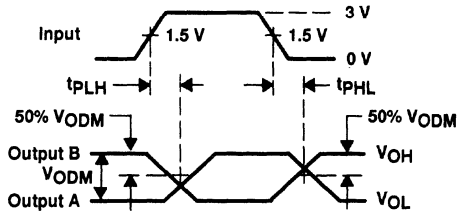
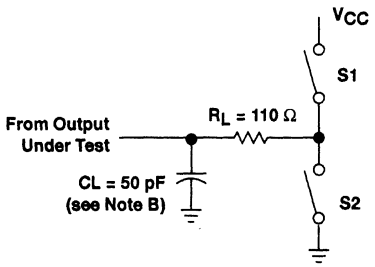


Figure 3. Driver Propagation Delay Times



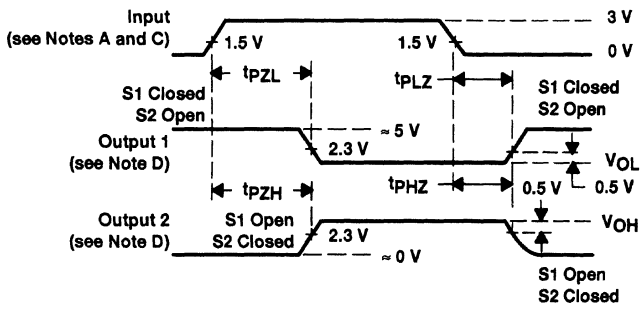


Figure 4. Driver Enable/Disable Times

NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 10 ns, t_f ≤ 10 ns.
B. C_L includes probe and jig capacitance.
C. Each enable is tested separately.
D. Output 1 and output 2 are outputs with internal conditions such that the output is low or high except when disabled by the output control.

PARAMETER MEASUREMENT INFORMATION

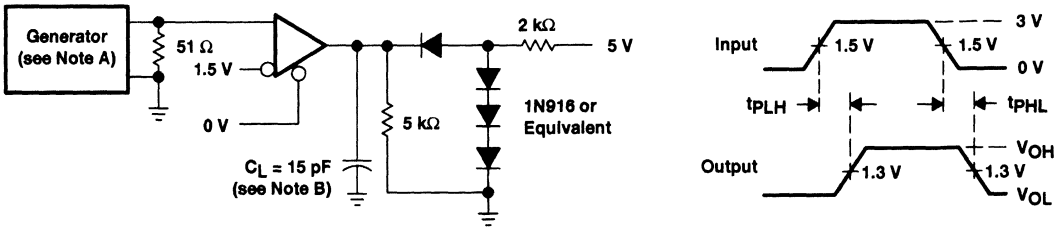


Figure 5. Receiver Propagation Delay Times

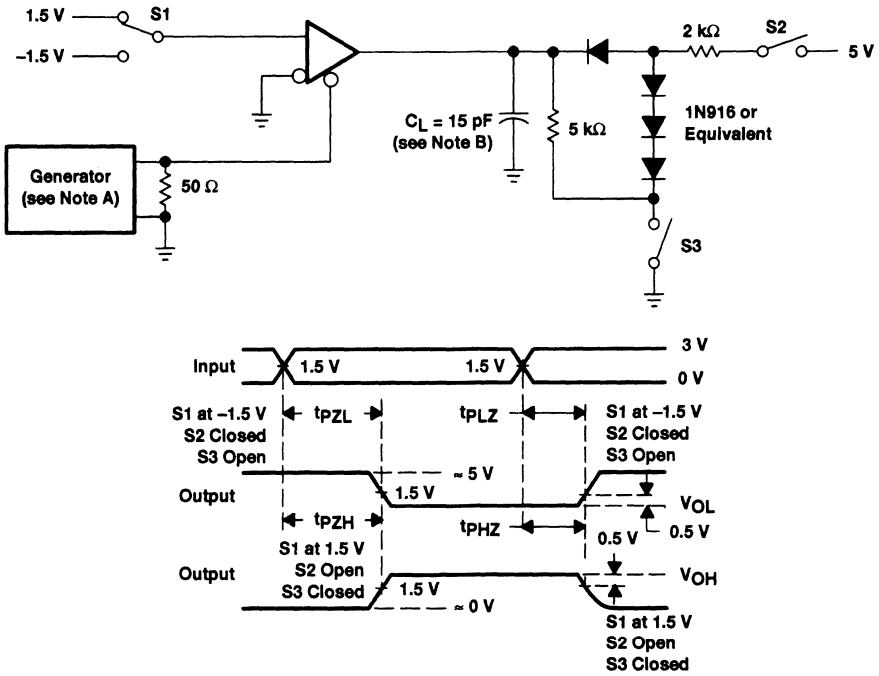


Figure 6. Receiver Enable/Disable Times

NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 10 ns, t_f ≤ 10 ns.
B. C_L includes probe and jig capacitance.

- **Meets or Exceeds the Requirements of IBM™ 360/370 Input/Output Interface Specification for 4.5 Mb/s Operation**
- **Single 5-V Supply**
- **Uncommited Emmitter-Follower Output Structure for Party-Line Operation**
- **Driver Output Short-Circuit Protection**
- **Driver Input/Receiver Output Compatible With TTL**
- **Receiver Input Resistance . . . 7.4 kΩ to 20 kΩ**
- **Ratio Specification for Propagation Delay Time, Low-to-High/High-to-Low**

description

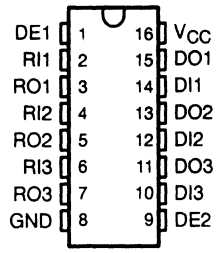
The SN751730 triple line driver/receiver is specifically designed to meet the input/output interface specifications for IBM System 360/370. It is also compatible with standard TTL logic and supply voltage levels.

The low-impedance emitter-follower driver outputs of the SN751730 drive terminated lines such as coaxial cable or twisted pair. Having the outputs uncommitted allows wired-OR logic to be performed in party-line applications. Output short-circuit protection is provided by an internal clamping network that turns on when the output voltage drops below approximately 2.5 V.

An open line affects the receiver input as does a low-level input voltage.

All the driver inputs and receiver outputs are in conventional TTL configuration and the gating can be used during power-up and power-down sequences to ensure that no noise is introduced to the line by pulling either DE1 or DE2 to a low level.

D OR N PACKAGE
(TOP VIEW)



Function Tables

EACH DRIVER

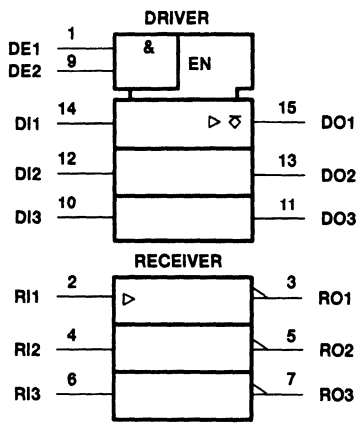
INPUTS			OUTPUT
DI	DE1	DE2	DO
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

EACH RECEIVER

INPUT RI	OUTPUT RO
L	H
H	L
Open	H

H = high level, L = low level, X = irrelevant

logic symbols†



† These symbols are in accordance with ANSI/IEE Std 91-1984 and IEC Publication 617-12.

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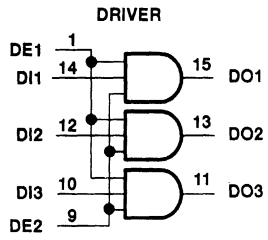
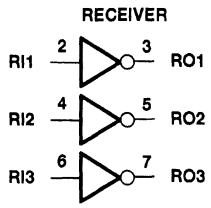
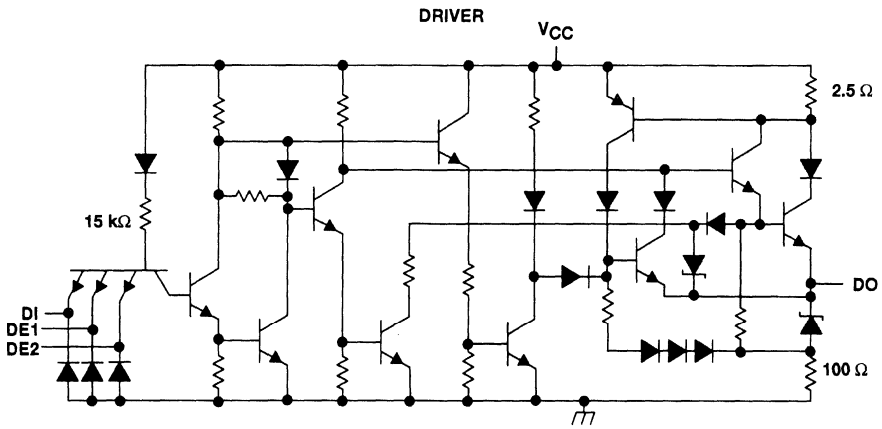
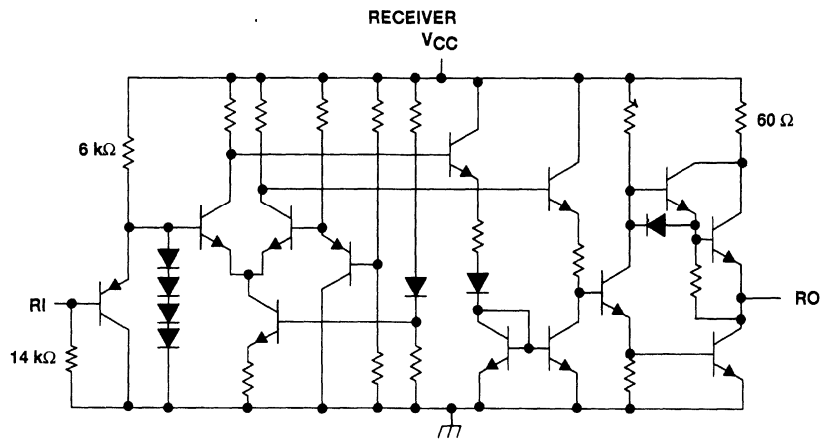
logic diagrams (positive logic)





equivalent schematics of driver and receiver†





† All resistor values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage range, V_I: Driver ..... −0.5 V to 7 V
Receiver ..... −0.5 V to 7 V
Output voltage range, V_O: Driver ..... −0.5 V to 7 V
Enable input voltage range ..... −0.5 V to 7 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mV	7.6 mW/°C	608 mW
N	1150 mV	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	Driver, Enable	2			V
	Receiver	1.55			
Low-level input voltage, V_{IL}	Driver, Enable			0.8	V
	Receiver			1.15	
Operating free-air temperature, T_A		0		70	°C

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
V_{IK}	Input clamp voltage		V_{CC} = 4.75 V,	I_{IL} = −18 mA		−1.5	V
V_{OH}	High-level output voltage		V_{CC} = 4.75 V, I_{OH} = −59.3 mA	V_{IH} = 2 V, T_A = 25°C	3.11		V
			V_{CC} = 5.25 V, I_{OH} = −78.1 mA	V_{IH} = 2 V,		4.10	
			V_{CC} = 4.75 V, R_L = 51.4 Ω	V_{IH} = 2 V,	3.05		
			V_{CC} = 5.25 V, R_L = 56.9 Ω	V_{IH} = 2 V,		4.20	
V_{ODH}	Differential high-level output voltage		R_L = 46.3 Ω or 56.9 Ω			0.50	V
V_{OL}	Low-level output voltage		V_{CC} = 5.25 V, V_{IL} = 0.8 V, V_{IH} = 4.5 V	I_{OL} = −0.24 mA		0.15	V
				R_L = 56.9 Ω		0.15	
I_{IH}	High-level input current	DI	V_{CC} = 5.25 V,	V_{IH} = 2.7 V		20	μA
		DE				60	
I_{IL}	Low-level input current	DI	V_{CC} = 5.25 V,	V_{IH} = 0.4 V		−400	μA
		DE				−1200	
I_{OH}	High-level output current		V_{CC} = 4.75 V, V_{OH} = 5 V	V_{IL} = 0		100	μA
				V_{IH} = 4.5 V		100	
I_{OS}	Short-circuit output current†		V_{CC} = 5.25 V	V_{IH} = 4.5 V		−30	mA
I_{CCH}	Supply current (total package)		V_{CC} = 5.25 V, No load	$V_{I(D)}$ = 4.5 V, $V_{I(R)}$ = 0		47	mA
I_{CCL}				$V_{I(D)}$ = 0, $V_{I(R)}$ = 4.5 V		80	

† No more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V ±5%, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 47.5 Ω,	See Figure 1	6.5	12	18.5	ns
t_{PHL}	Propagation delay time, high- to low-level output			6.5	12	18.5	ns
Δt_{pd}	Differential propagation delay time‡					10	ns
t_r	Output rise time	V_{CC} = 5 V, R_L = 47.5 Ω, See Figure 1	V_O = 0.15 V to 3.05 V, C_L = 10.2 pF,	5	10		ns
t_f	Output fall time			5	13		ns
SR	Slew rate	V_O = 1 V to 3 V average, R_L = 47.5 Ω, See Figure 1	C_L = 10.2 pF,			0.65	V/ns

‡ $\Delta t_{pd} = |t_{PLH} - t_{PHL}|$

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, I_{OH} = −400 μA	V_I = 1.15 V,	2.7		V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IH} = 1.55 V	I_{OL} = 8 mA		0.5	V
			I_{OL} = 4 mA		0.4	
r_I	Input resistance	V_{CC} = 0,	V_I = 0.15 V to 3.9 V	7.4	20	kΩ
I_{IH}	High-level input current	V_{CC} = 4.75 V,	V_{IH} = 3.11 V		0.42	mA
I_{IL}	Low-level input current	V_{CC} = 5.25 V,	V_{IL} = 0.15 V	−0.24	0.04	mA
I_{OS}†	Short-circuit output current	V_{CC} = 5.25 V,	V_{IL} = 0	−20	−100	mA
I_{CCH}	Supply current (total package)	V_{CC} = 5.25 V, No load	$V_{I(D)}$ = 4.5 V, $V_{I(R)}$ = 0		47	mA
I_{CCL}			$V_{I(D)}$ = 0, $V_{I(R)}$ = 4.5 V		80	

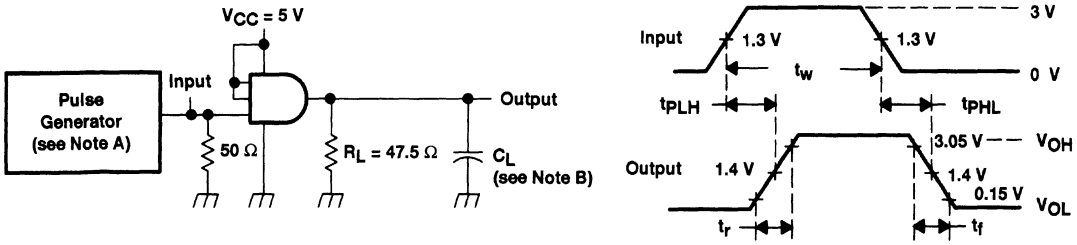
† Only one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V ±5%, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 2 kΩ, C_L = 15 pF, See Figure 2	7.5	12	19.5	ns
t_{PHL}	Propagation delay time, high- to low-level output		7.5	12	19.5	ns
Δt_{pd}‡	Differential propagation delay time				10	ns

‡ $\Delta t_{pd} = |t_{PLH} - t_{PHL}|$

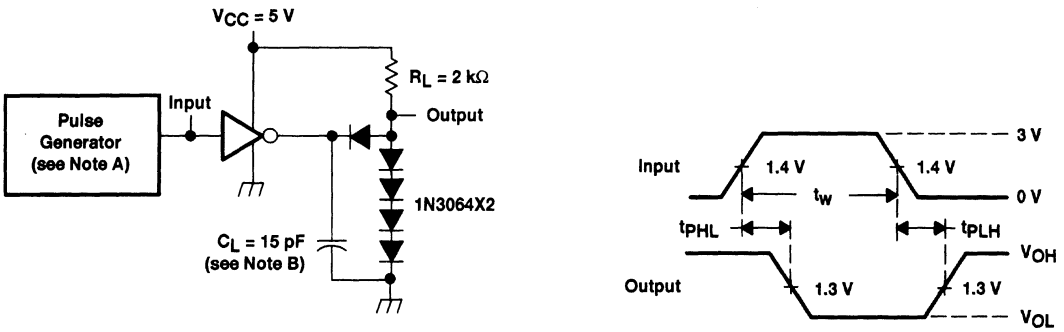
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT **VOLTAGE WAVEFORMS**

NOTES: A. The pulse generator has the following characteristics: $Z_O \approx 50\ \Omega$, $t_W \leq 500$ ns, PRR ≤ 1 MHz, $t_f \leq 6$ ns, $t_r \leq 15$ ns.
B. C_L includes probe and jig capacitance.

Figure 1. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT **VOLTAGE WAVEFORMS**

NOTES: A. The pulse generator has the following characteristics: $Z_O \approx 50\ \Omega$, $t_W \leq 500$ ns, PRR ≤ 1 MHz, $t_f \leq 10$ ns, $t_r \leq 10$ ns.
B. C_L includes probe and jig capacitance.

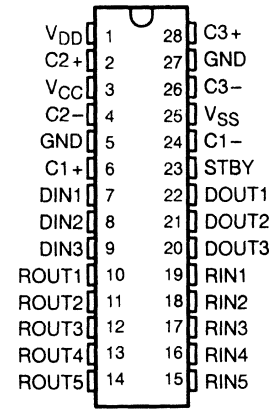
Figure 2. Receiver Test Circuit and Voltge Waveforms

SN75LV4735
3.3-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER

SLLS135E – FEBRUARY 1992 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of ANSI EIA/TIA-232-E and ITU V.28**
- **Operates With Single 3.3-V Power Supply**
- **LinBiCMOS™ Process Technology**
- **Three Drivers and Five Receivers**
- **±30-V Input Levels (Receiver)**
- **ESD Protection on RS-232 Lines Exceeds 6 kV Per MIL-STD-883C, Method 3015**
- **Applications**
  - **EIA/TIA-232 Interface**
  - **Battery-Powered Systems**
  - **Notebook PC**
  - **Computers**
  - **Terminals**
  - **Modems**
- **Voltage Converter Operates With Low Capacitance . . . 0.47 μF Min**
- **Functionally Compatible With the SN75LV4737A**

DB PACKAGE
(TOP VIEW)



† The DB package is only available in left-end taped and reeled (SN75LV4735DBLE).

description

The SN75LV4735† is a low-power 3.3-V multichannel RS-232 line driver/receiver. It includes three independent RS-232 drivers and five independent RS-232 receivers. It is designed to operate off a single 3.3-V supply and has an internal switched-capacitor voltage converter to generate the RS-232 output levels. The SN75LV4735 provides a single chip, single 3.3-V supply interface between the asynchronous communications element (ACE or UART) and the serial-port connector of the data terminal equipment (DTE). This device has been designed to conform to standard ANSI EIA/TIA-232-E.

The switched-capacitor voltage converter of the SN75LV4735 uses five small external capacitors to generate the positive and negative voltages required by EIA/TIA-232-E line drivers from a single 3.3-V input. The drivers feature output slew-rate limiting to eliminate the need for external filter capacitors. The receivers can accept ±30 V without damage.

The device also features a reduced power or standby mode that cuts the quiescent power to the integrated circuits when not transmitting data between the CPU and peripheral equipment. The STBY input is driven high for standby (reduced power) mode and driven low for normal operating mode. When in the standby mode, all driver outputs (DOUT1–3) and receiver outputs (ROUT1–5) are in the high-impedance state. If the standby feature is not used in an application, STBY should be tied to GND.

The SN75LV4735 has been designed using LinBiCMOS™ technology and cells contained in the Texas Instruments LinASIC™ library. The SN75LV4735 is characterized for operation from 0°C to 70°C.

† Patent-pending design

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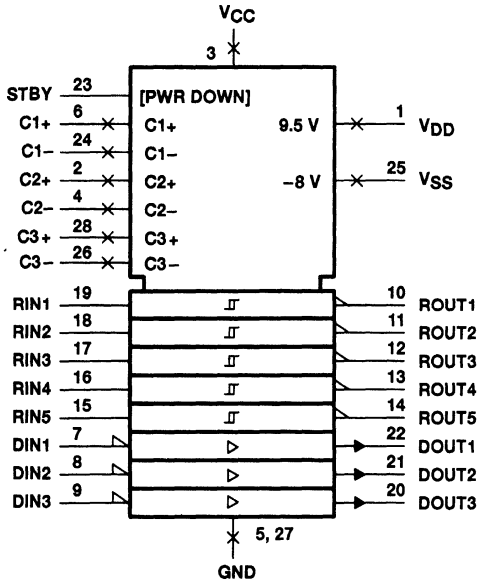
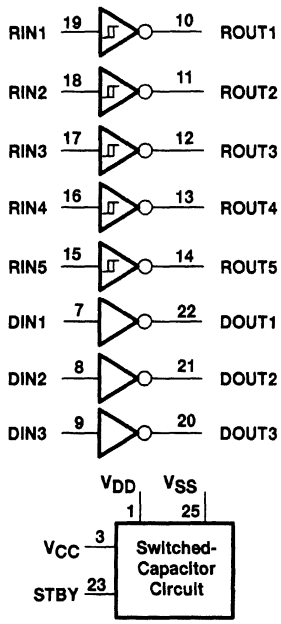
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Function Tables

EACH DRIVER

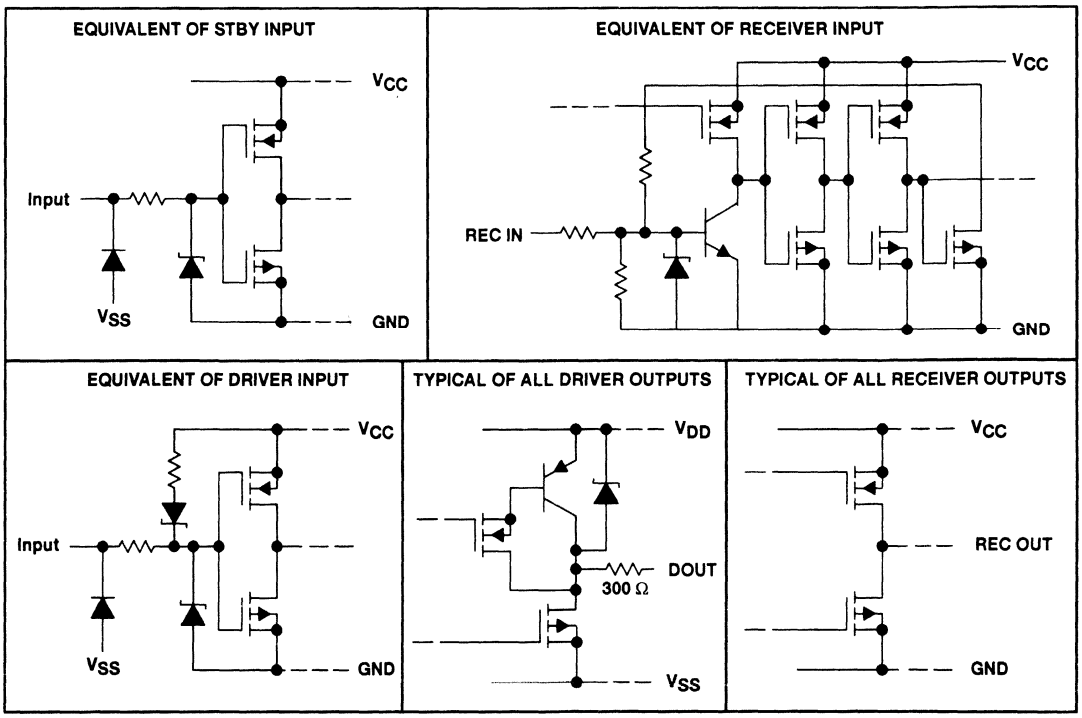
INPUTS		OUTPUT
DIN	STBY	
X	H	Z
L	L	H
H	L	L
Open	L	L

EACH RECEIVER

INPUTS		OUTPUT
RIN	STBY	
X	H	Z
L	L	H
H	L	L
Open	L	H

H = high level, L = low level, X = irrelevant, Z = high impedance (off)

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} ..... 4 V
Positive output supply voltage, V_{DD} (see Note 1) ..... 15 V
Negative output supply voltage, V_{SS} ..... −15 V
Input voltage range, V_I: DIN1–DIN3, STBY ..... −0.3 V to 7 V
RIN1–RIN5 ..... −30 V to 30 V
Output voltage range, V_O: DOUT1–DOUT3 ..... V_{SS} − 0.3 V to V_{DD} + 0.3 V
ROUT1–ROUT5 ..... −0.3 V to 7 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to network GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DB	668 mW	5.3 mW/°C	430 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
Positive output supply voltage, V_{DD}		8	10		V
Negative output supply voltage, V_{SS}		−7	−8		V
Input voltage, V_I (see Note 2)	RIN(1–5)			±30	V
High-level input voltage, V_{IH}	DIN(1–3), STBY	2			V
Low-level input voltage, V_{IL}	DIN(1–3), STBY			0.8	V
External capacitor		0.47	1		µF
Operating free-air temperature, T_A		0		70	°C

NOTE 2: The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only. For example, if −10 V is a maximum, the typical value is a more negative voltage.

supply currents

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current from V_{CC} (normal operating mode)	No load, STBY at 0 V, All other inputs open		8.5	20	mA
$I_{CC(SB)}$	Supply current (standby mode)	No load, STBY at V_{CC}, All other inputs open			10	µA

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DRIVER SECTION

electrical characteristics over operating free-air temperature range, V_{CC} = 3.3 V ±0.3 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		R_L = 3 kΩ	5.5	7		V
V_{OL}	Low-level output voltage (see Note 2)		R_L = 3 kΩ		−5.5	−5	V
I_{IH}	High-level input current		V_I at V_{CC}			1	µA
I_{IL}	Low-level input current	STBY	V_I at GND			−1	µA
		Other inputs	V_I at GND			−10	µA
$I_{OS(H)}$	High-level short-circuit output current (see Note 3)		V_{CC} = 3.6 V, V_O = 0		−10	−20	mA
$I_{OS(L)}$	Low-level short-circuit output current (see Note 3)		V_{CC} = 3.6 V, V_O = 0		10	20	mA
r_O	Output resistance		V_{CC} = V_{DD} = V_{SS} = 0, V_O = −2 V to 2 V, See Note 4	300			Ω

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

NOTES: 2. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only.
3. Not more than one output should be shorted at one time.
4. Test conditions are those specified by EIA/TIA-232-E.

switching characteristics, V_{CC} = 3.3 V ±0.3 V, T_A = 0°C to 70°C

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 3 kΩ to GND, C_L = 50 pF, See Figure 2	200	400	600	ns
t_{PHL}	Propagation delay time, high- to low-level output		100	200	350	ns
t_{PZL}	Output enable time to low level (see Note 5)	R_L = 3 kΩ to GND, C_L = 50 pF, See Figure 3		3	7	ms
t_{PZH}	Output enable time to high level (see Note 5)			1	5	ms
t_{PHZ}	Output disable time from high level (see Note 5)			1	3	µs
t_{PLZ}	Output disable time from low level (see Note 5)			0.5	3	µs
SR	Output slew rate (see Note 6)	R_L = 3 kΩ to 7 kΩ, C_L = 50 pF, See Figure 2	3		30	V/µs
SR(tr)	Transition-region slew rate	R_L = 3 kΩ to GND, C_L = 2500 pF, See Figure 4		3		V/µs

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

NOTES: 5. Output enable occurs when STBY is driven low. Output disable occurs when STBY is driven high.
6. Measured between 3-V and −3-V points of output waveform (EIA/TIA-232-E conditions); all unused inputs are tied either high or low.

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage			2.2	2.6	V
V_{IT-}	Negative-going input threshold voltage		0.6	1		V
V_{hys}	Input hysteresis voltage ($V_{IT+} - V_{IT-}$)		0.5	1.2	1.8	V
V_{OH}	High-level output voltage	I_{OH} = −2 mA, See Note 7	2.4	2.6		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA		0.2	0.4	V
r_I	Input resistance	V_I = ±3 V to ±25 V	3	5	7	kΩ

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

NOTE 7: If the inputs are left unconnected, the receiver interprets this as an input low, and the receiver outputs remain in the high state.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 3 kΩ to GND, See Figure 5	45	80	130	ns
t_{PHL}	Propagation delay time, high- to low-level output		70	100	170	ns
t_{PZL}	Output enable time to low level (see Note 5)	R_L = 3 kΩ to GND, See Figure 6		160	250	ns
t_{PZH}	Output enable time to high level (see Note 5)			4	10	µs
t_{PHZ}	Output disable time from high level (see Note 5)			300	500	ns
t_{PLZ}	Output disable time from low level (see Note 5)			140	200	ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

NOTE 5: Output enable occurs when STBY is driven low. Output disable occurs when STBY input is driven high.

APPLICATION INFORMATION

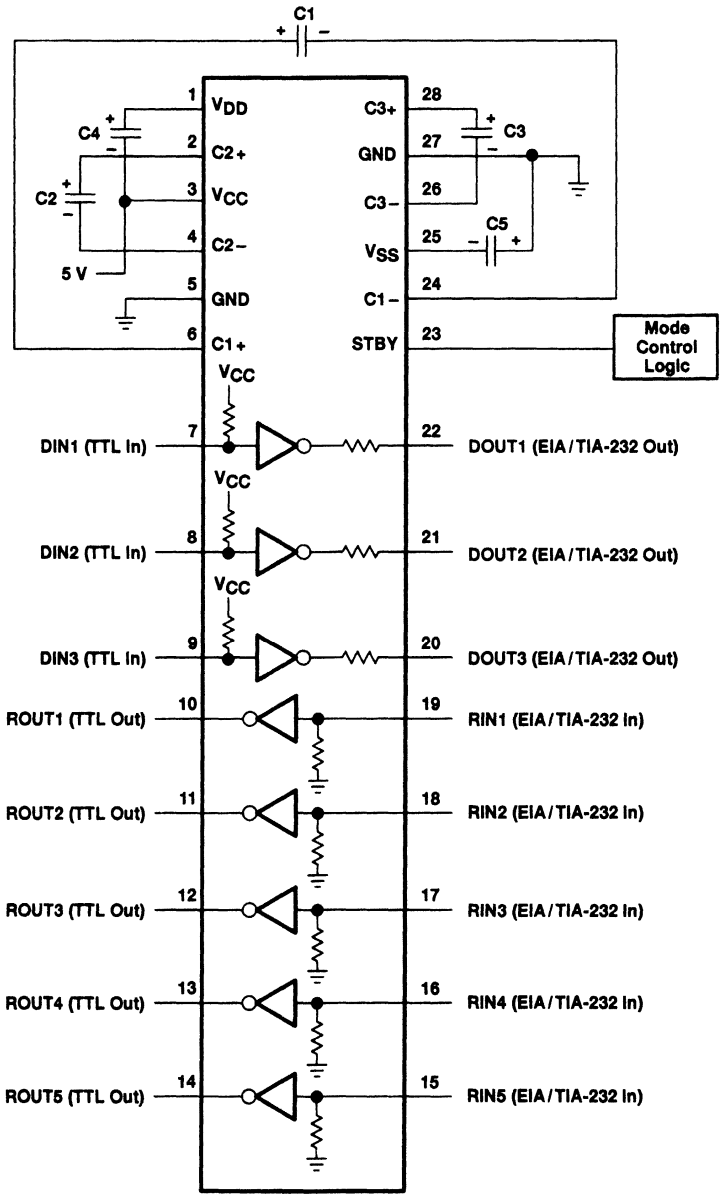
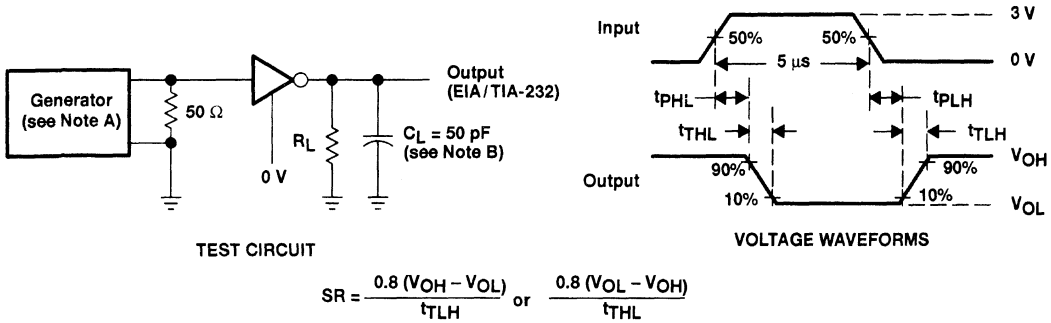


Figure 1. Typical Operating Circuit

PARAMETER MEASUREMENT INFORMATION



$$SR = \frac{0.8\,(V_{OH} - V_{OL})}{t_{TLH}} \text{ or } \frac{0.8\,(V_{OL} - V_{OH})}{t_{THL}}$$

Figure 2. Driver Test Circuit and Voltage Waveforms, Slew Rate at 5-μs Input

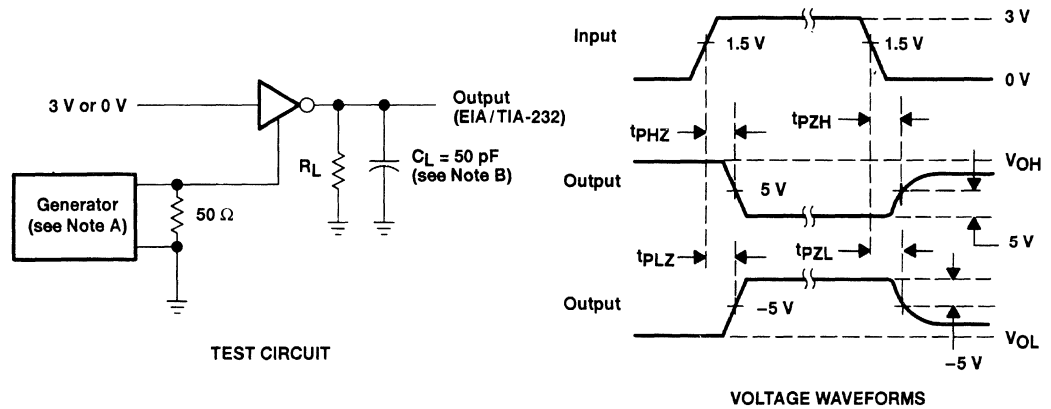
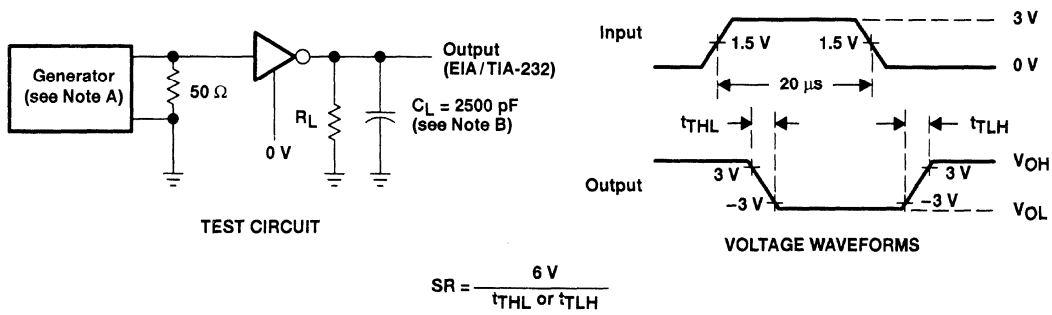


Figure 3. Driver Test Circuit and Voltage Waveforms



$$SR = \frac{6\text{ V}}{t_{THL} \text{ or } t_{TLH}}$$

Figure 4. Driver Test Circuit and Voltage Waveforms, Slew Rate at 20-μs Input

NOTES: A. The pulse generator has the following characteristics: 50% duty cycle, $t_r \leq 10$ ns, $t_f = 10$ ns.
B. C_L includes probe and jig capacitance

PARAMETER MEASUREMENT INFORMATION

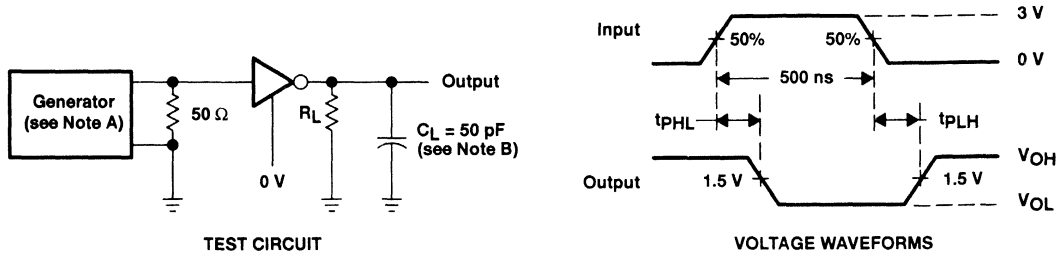


Figure 5. Receiver Test Circuit and Voltage Waveforms

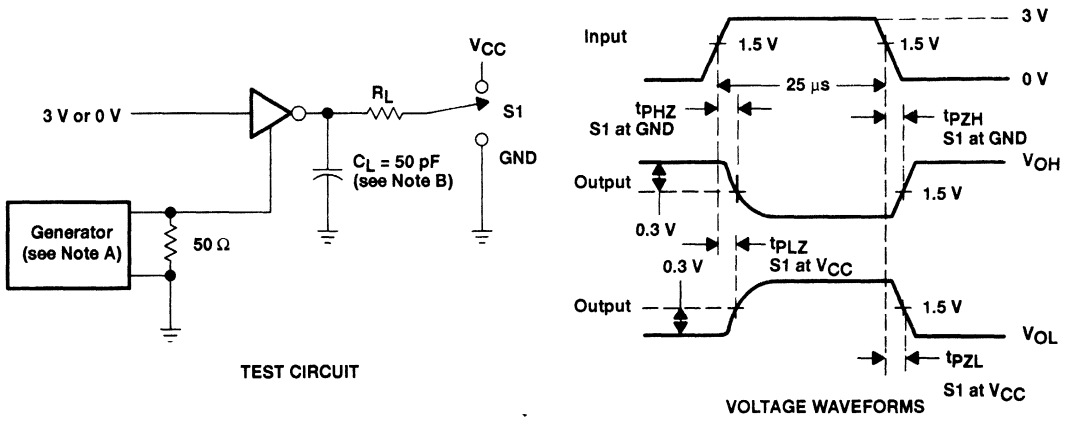


Figure 6. Receiver Test Circuit and Voltage Waveforms Enable and Disable Times

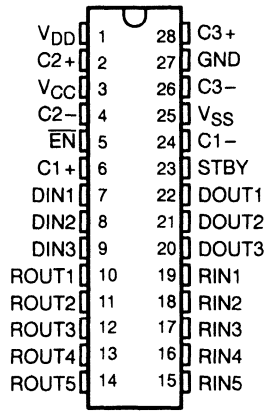
NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r \leq 10$ ns, $t_f = 10$ ns.
B. C_L includes probe and jig capacitance.

SN75LV4737A
3.3-V/5-V MULTICHANNEL RS232 LINE DRIVER/RECEIVER

SLLS178A – APRIL 1994 – REVISED NOVEMBER 1994

- **Single-Chip and Single-Supply Interface for IBM PC/AT Serial Port**
- **Meets or Exceeds the Requirements of EIA/TIA-232-E and ITU v.11 Standards**
- **Operates With 3.3-V or 5-V Supplies**
- **One Receiver Remains Active During Standby (Wake-Up Mode)**
- **Designed to Operate at 128 kbits Over a 3-m Cable**
- **Low Standby Current . . . 5 μA Max**
- **ESD Protection on RS-232 Pins Meets or Exceeds 4 kV (HBM) and 1.5 kV (HBM) on All Pins Per MIL-STD-883C, Method 3015**
- **External Capacitors . . . 0.1 μF**
  (V_{CC} = 3.3 V Five External Capacitors)
  (V_{CC} = 5 V Four External Capacitors)
- **Packaged in Shrink Small-Outline Package With 25-Mil Terminal Pitch and Maximum 2-mm Height (SSOP)**
- **Accepts 5-V Logic Input With 3.3-V Supply**
- **Pin Compatible With the SN75LV4735**
- **Applications**
  EIA/TIA-232 Interface
  Battery-Powered Systems, PDAs
  Notebook, Laptop, and Palmtop PCs
  External Modems and Hand-Held Terminals

DB PACKAGE†
(TOP VIEW)



† The DB package is only available in left-ended tape and reel (order part number SN75LV4737ADBLE).

description

The SN75LV4737A‡ consists of three line drivers, five line receivers, and a charge-pump circuit. It provides the electrical interface between an asynchronous communication controller and the serial-port connector and meets the requirements of EIA/TIA-232-E. This combination of drivers and receivers matches those needed for the typical serial port used in an IBM PC/AT or compatibles. The charge pump and five small external capacitors allow operation from a single 3.3-V supply and four capacitors for operation from a 5-V supply.

The device has flexible control options for power management when the serial port is inactive. A common disable for all of the drivers and receivers is provided with the active-high STBY input. The active-low $\overline{EN}$ input is an enable for one receiver to implement a wake-up feature for the serial port. All the logic inputs can accept signals from controllers operating from a 5-V supply even though the SN75LV4737A is operating from 3.3 V.

The SN75LV4737A is characterized for operation over the temperature range of 0°C to 70°C.

‡ Patent-pending design

Function Tables

EACH DRIVER

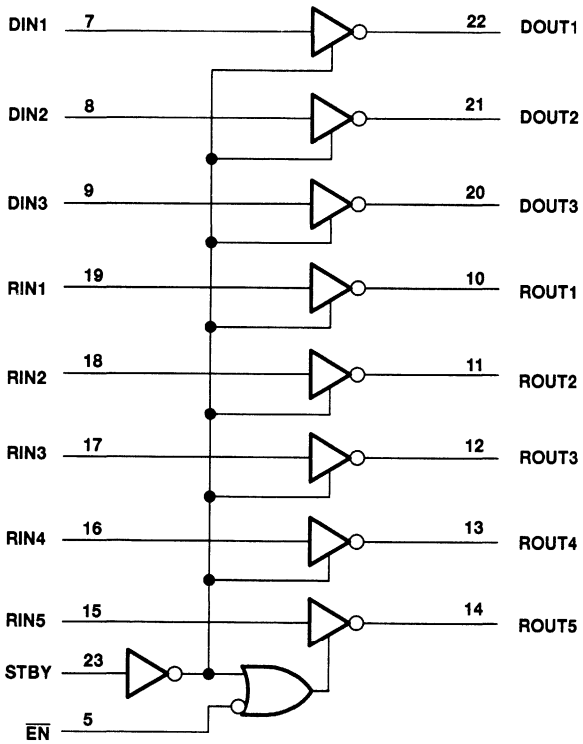
INPUTS		OUTPUTS
DIN	STBY	DOUT
X	H	Z
L	L	H
H	L	L
Open	L	L

EACH RECEIVER

INPUTS				OUTPUTS	
STBY	$\overline{EN}$	RIN5	RIN1–RIN4	ROUT5	ROUT1–ROUT4
H	H	X	X	Z	Z
H	L	H	X	L	Z
H	L	L	X	H	Z
L	X	L	L	H	H
L	X	H	H	L	L

H = high level, Low = low level, X = irrelevant, Z = high impedance (off)

logic diagram (positive logic)



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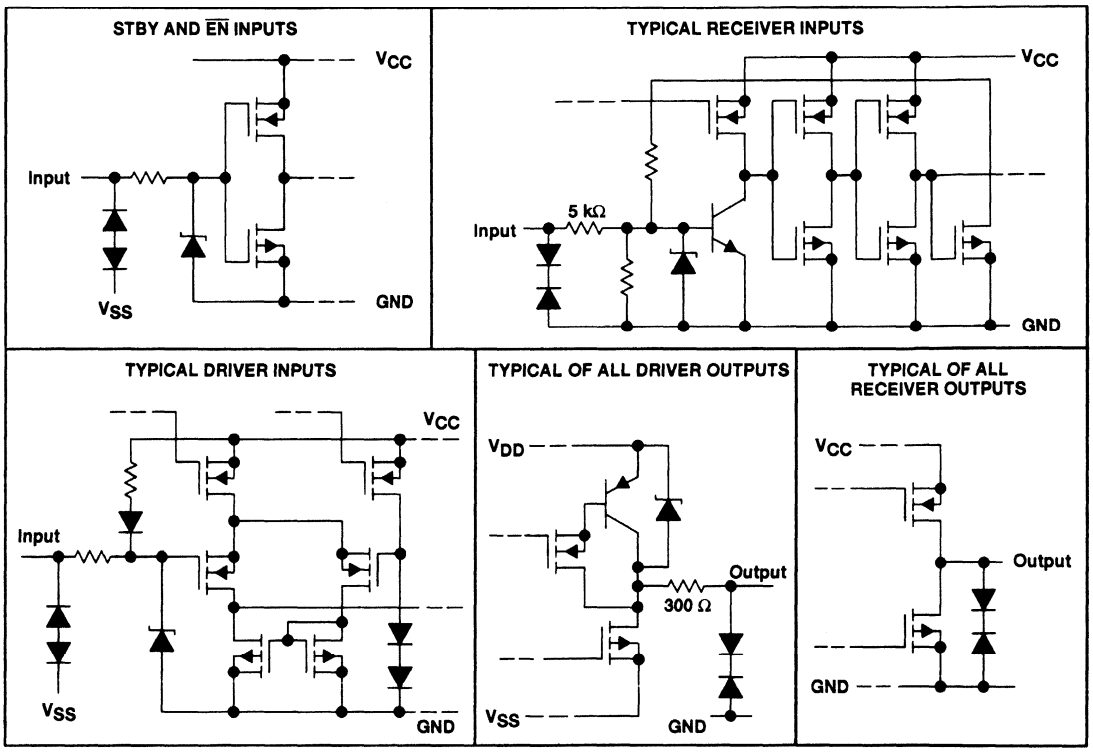
schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	7 V
Positive output supply voltage, V_{DD} (see Note 1)	15 V
Negative output supply voltage, V_{SS}	−15 V
Input voltage range, V_I: Driver	−3 V to 7 V
Receiver	−30 V to 30 V
Output voltage range, V_O: Driver	V_{SS} − 0.3 V to V_{DD} + 0.3 V
Receiver	−0.3 V to 7 V
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to network GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DB	668 mW	5.3 mW/°C	430 mW

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage	V_{CC} = 3.3 V		3	3.3	3.6	V
	V_{CC} = 5 V		4.5	5	5.5	V
Driver high-level input voltage, V_{IH}	V_{CC} = 3.3 V	DIN, $\overline{EN}$, STBY	2			V
	V_{CC} = 5 V	DIN	2			
		$\overline{EN}$, STBY	2.5			
Driver low-level input voltage, V_{IL}	DIN, $\overline{EN}$, STBY				0.8	V
Receiver input voltage, V_I					±30	V
External capacitor	3.3-V operation (C1, C2, C3, C4, C5), 5-V operation (C1, C3, C4, C5), See Note 2 and Figures 6 and 7		0.1			μF
Operating free-air temperature, T_A			0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figures 6 and 7)

PARAMETER		TEST CONDITIONS		V_{CC} = 3.3 V			V_{CC} = 5 V			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{DD}	Positive supply voltage	No load		8	10		7	8.7		V
V_{SS}	Negative supply voltage	No load			−9.5	−7		−8	−6	V
I_I	Input current ($\overline{EN}$, STBY)	See Notes 3 and 4				±2			±2	μA
I_{CC}	Supply current	No load, Inputs open	STBY at GND, $\overline{EN}$ at V_{CC} or GND	8.4	10	18	10	12	20.7	mA
	Supply current (standby mode) (see Note 3)		$\overline{EN}$, STBY at V_{CC}			5			5	μA
	Supply current (wake-up mode) (see Note 4)		$\overline{EN}$ at GND, STBY at V_{CC}			10			10	μA

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V and T_A = 25°C.

NOTES: 2. C2 is only needed for 3.3-V operation.
3. When STBY mode is not used, STBY input must be taken low.
4. When wake-up mode is not used, $\overline{EN}$ input must be taken high.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	R_L = 3 kΩ		5.5	7		V
V_{OL}	Low-level output voltage	R_L = 3 kΩ			−6	−5	V
I_{IH}	High-level input current	$V_I = V_{CC}$				1	μA
I_{IL}	Low-level input current	V_I at GND				−10	μA
I_{OS}	Short-circuit output current (see Note 5)	V_{CC} = 3.6 V,	V_O = 0 V		±15	±40	mA
		V_{CC} = 5.5 V,	V_O = 0 V				
r_o	Output resistance	$V_{CC} = V_{DD} = V_{SS}$ = 0 V,	V_O = ±2 V	300	500		Ω

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 50 pF, R_L = 3 kΩ to 7 kΩ, See Figure 1	V_{CC} = 3.3 V	100	500	850	ns
			V_{CC} = 5 V	100	500	850	ns
t_{PHL}	Propagation delay time, high- to low-level output		V_{CC} = 3.3 V	100	500	850	ns
			V_{CC} = 5 V	100	500	850	ns
t_{PZH}	Output enable time to high level	C_L = 50 pF, See Figure 2	R_L = 3 kΩ to 7 kΩ,		1	5	ms
t_{PZL}	Output enable time to low level				3	7	ms
t_{PHZ}	Output disable time from high level	C_L = 50 pF, R_L = 3 kΩ to 7 kΩ, See Figure 2	V_{CC} = 3.3 V		0.9	3	μs
			V_{CC} = 5 V		0.6	3	
t_{PLZ}	Output disable time from low level		V_{CC} = 3.3 V		0.5	3	
			V_{CC} = 5 V		0.3	3	
SR	Slew rate	C_L = 50 pF, See Figure 1	R_L = 3 kΩ to 7 kΩ,	4		30	V/μs
SR(tr)	Slew rate, transition region	C_L = 2500 pF, See Figure 3	R_L = 3 kΩ to 7 kΩ,	3		30	V/μs

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V and T_A = 25°C.

NOTE 5: Short-circuit durations should be controlled to prohibit exceeding the device absolute power dissipation ratings and not more than one output should be shorted at a time.

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

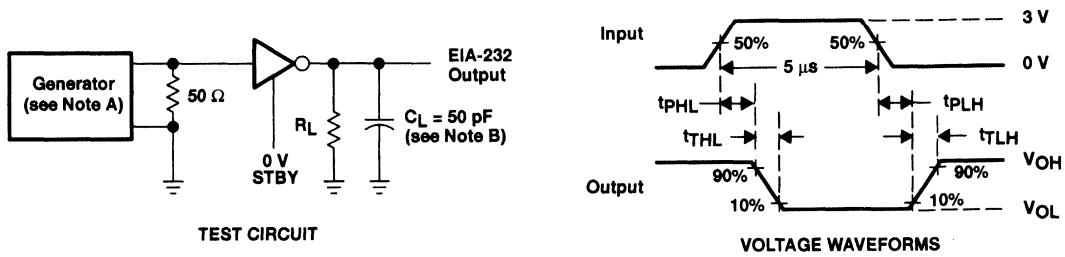
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA	3.3 V	2.4	3		V
			5 V	3.5	5		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.2	0.4	V
V_{IT+}	Positive-going input threshold voltage				2.2	2.6	V
V_{IT-}	Negative-going input threshold voltage			0.6	1		V
V_{hys}	Input hysteresis ($V_{IT+} - V_{IT-}$)			0.5	1.2	1.8	V
r_i	Input resistance	V_I = ±3 V to ±25 V		3	5	7	kΩ

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V and T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF, R_L = 3 kΩ to GND

PARAMETER		TEST CONDITIONS	V_{CC} = 3.3 V			V_{CC} = 5 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 4	10	70	200	10	70	200	ns
t_{PHL}	Propagation delay time, high- to low-level output		10	60	200	10	55	200	ns
t_{PLH}	Propagation delay time, low- to high-level output (wake-up mode)			40	200		40	200	µs
t_{PHL}	Propagation delay time, high- to low-level output (wake-up mode)			90	500		70	500	ns
t_{PZH}	Output enable time to high level	See Figure 5		3	10		1.2	10	µs
t_{PZL}	Output enable time to low level			100	250		60	250	ns
t_{PHZ}	Output disable time from high level		100	200	600	100	150	600	ns
t_{PLZ}	Output disable time from low level			130	250		60	250	ns

PARAMETER MEASUREMENT INFORMATION



$$SR = \frac{0.8\ V(V_{OH} - V_{OL})}{t_{TLH}} \text{ or } \frac{0.8\ V(V_{OL} - V_{OH})}{t_{THL}}$$

Figure 1. Driver Propagation Delay Times and Slew Rate (5-μs Input)

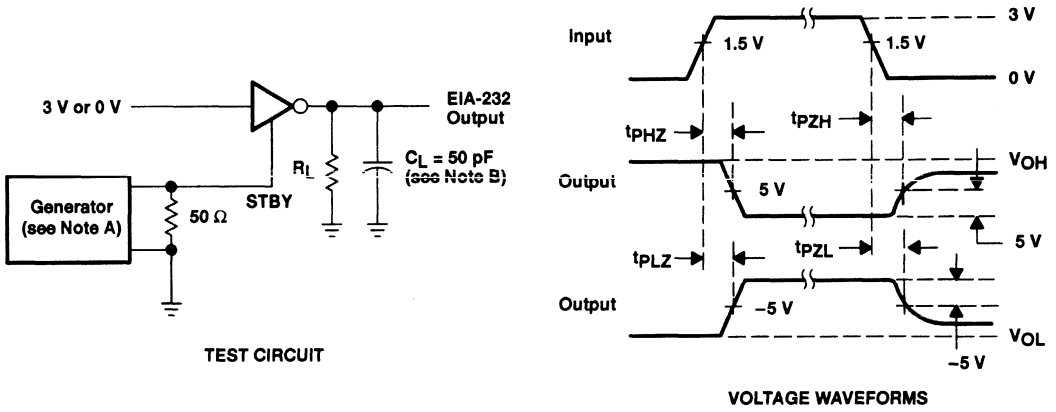
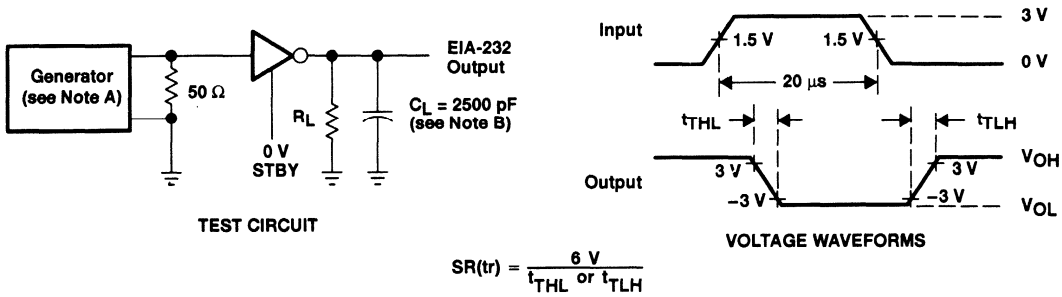


Figure 2. Driver Enable and Disable Test Times



$$SR(tr) = \frac{6\ V}{t_{THL} \text{ or } t_{TLH}}$$

Figure 3. Driver Transition Times and Slew Rate (20-μs Input)

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION

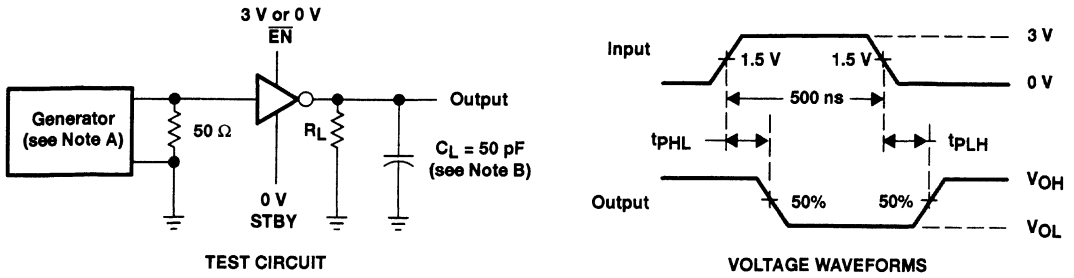


Figure 4. Receiver Propagation Delay Times

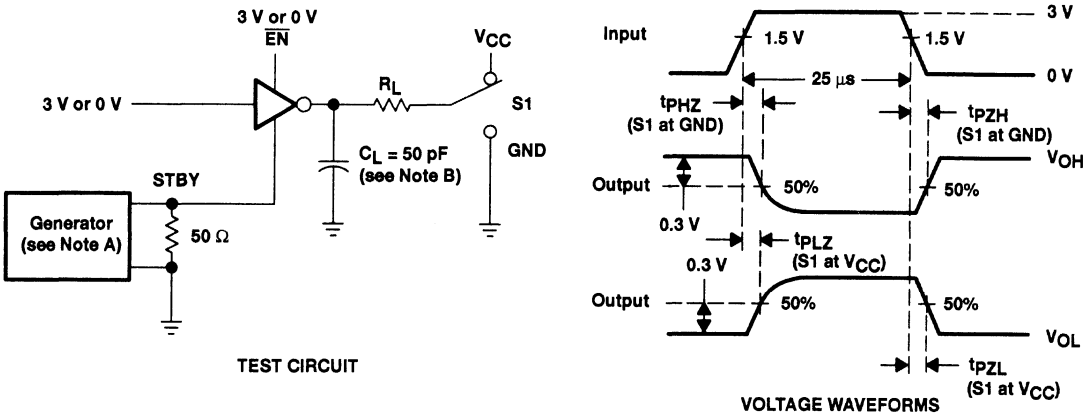


Figure 5. Receiver Enable and Disable Times

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, Z_O = 50 Ω, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.
B. C_L includes probe and jig capacitance.

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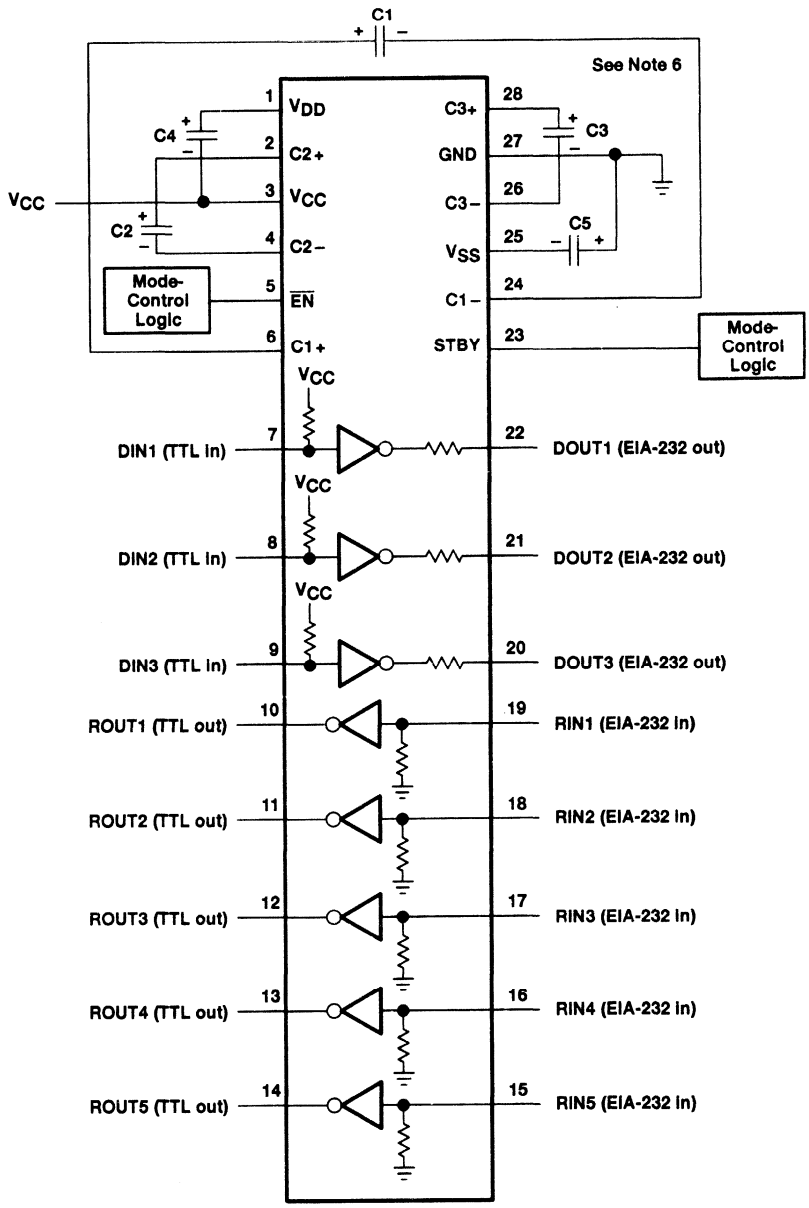
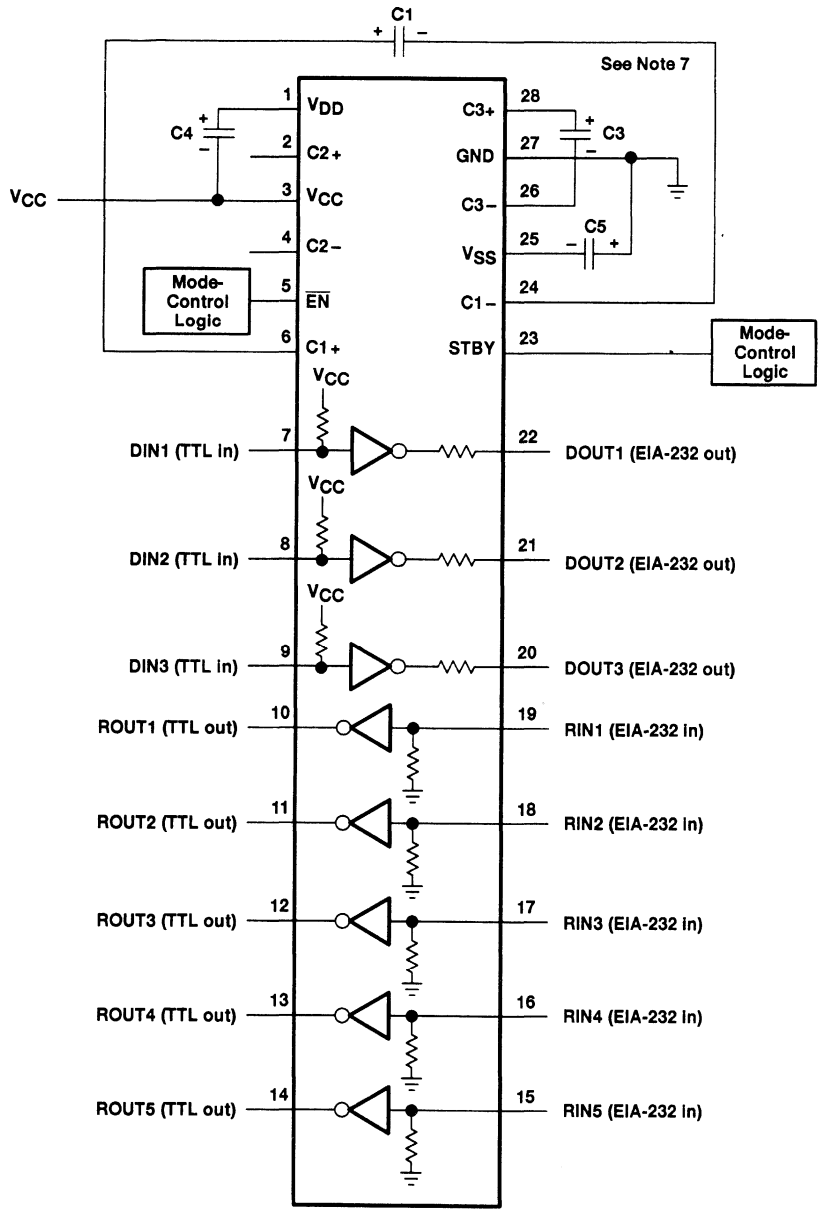
APPLICATION INFORMATION



NOTE 6: C1 = C2 = C3 = C4 = C5 = 0.1 μF

Figure 6. Typical 3.3-V Operating Circuit

APPLICATION INFORMATION



NOTE 7: C2 is not used.
C1 = C3 = C4 = C5 = 0.1 μF

Figure 7. Typical 5-V Operating Circuit

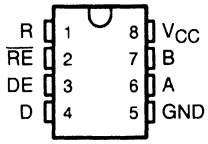
- **Bidirectional Transceiver**
- **Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendation V.11**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Low Skew . . . 6 ns Max**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Low Supply-Current Requirements 30 mA Max**
- **Wide Positive and Negative Input/Output Bus Voltage Ranges**
- **Driver Output Capacity . . . ±60 mA**
- **Thermal Shutdown Protection**
- **Driver Positive and Negative Current Limiting**
- **Receiver Input Impedances . . . 12 kΩ Min**
- **Receiver Input Sensitivity . . . ±200 mV Max**
- **Receiver Input Hysteresis . . . 120 mV Typ**
- **Fail Safe . . . High Receiver Output With Inputs Open**
- **Operates From a Single 5-V Supply**
- **Glitch-Free Power-Up and Power-Down Protection**
- **Interchangeable With National DS3695 and DS3695A**

description

The TL3695 differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus-transmission lines. It is designed for balanced transmission lines and meets ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendation V.11.

The TL3695 combines a 3-state differential line driver and a differential input line receiver both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a directional control. The driver differential outputs and the receiver differential inputs are connected

D OR P PACKAGE
(TOP VIEW)



Function Tables

DRIVER

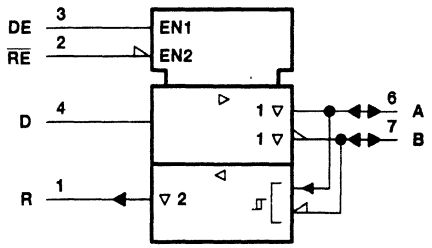
INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Inputs Open	L	H

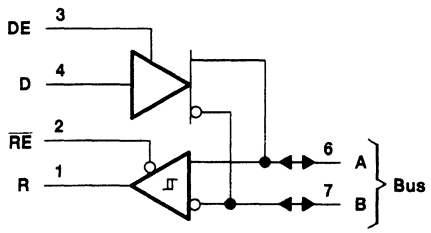
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

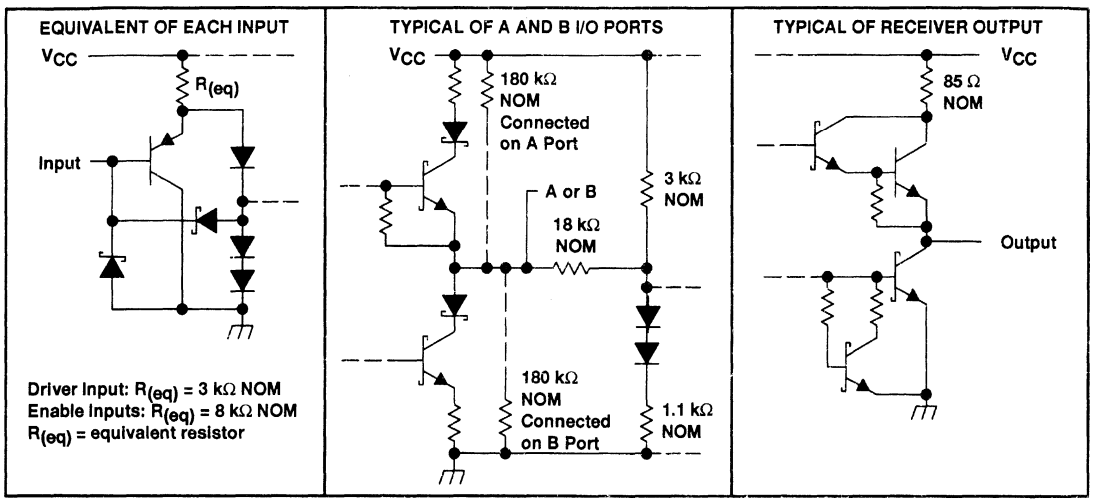


description (continued)

internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus when the driver is disabled or V_{CC} = 0. This port features wide positive and negative common-mode voltage ranges making the device suitable for party line applications.

The TL3695 is characterized for operation from 0°C to 70°C.

schematic of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Voltage range at any bus terminal ..... −10 V to 15 V
Enable input voltage, V_I ..... 5.5 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12	V
				−7	
High-level Input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level Input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 2)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	µA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\lvert V_{OD1}\rvert$	Differential output voltage	I_O = 0		1.5		5	V
$\lvert V_{OD2}\rvert$	Differential output voltage	R_L = 100 Ω, See Figure 1		1/2 V_{OD1} or 2§			V
		R_L = 54 Ω, See Figure 1		1.5	2.5	5	V
V_{OD3}	Differential output voltage	V_{test} = −7 V to 12 V, See Figure 2		1.5		5	V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage¶	R_L = 54 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage					3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage¶					±0.2	V
I_O	Output current	Output disabled, See Note 3	V_O = 12 V			1	mA
			V_O = −7 V			−0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	µA
I_{IL}	Low-level input current	V_I = 0.4 V				−200	µA
I_{OS}	Short-circuit output current	V_O = −6 V				−250	mA
		V_O = 0				−150	
		V_O = V_{CC}				250	
		V_O = 8 V				250	
I_{CC}	Supply current	No load	Outputs enabled		23	50	mA
			Outputs disabled		19	35	

† The power-off measurement in ANSI Standard EIA/TIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
‡ All typical values are at V_{CC} = 5 V and T_A = 25°C.
§ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V whichever is greater.
¶ $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

NOTE 3: This applies for both power on and off; refer to ANSI Standard RS-485 for exact conditions. The EIA/TIA-422-B limit does not apply for a combined driver and receiver terminal.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	$C_{L1} = C_{L2} = 100$ pF,	$R_L = 60\ \Omega$,	See Figure 3		8	22	ns
	Skew ($\lvert t_{d(ODH)} - t_{d(ODL)} \rvert$)					1	8	ns
$t_{t(OD)}$	Differential output transition time					8	18	ns
t_{PZH}	Output enable time to high level	$C_L = 100$ pF,	$R_L = 500\ \Omega$,	See Figure 4			50	ns
t_{PZL}	Output enable time to low level	$C_L = 100$ pF,	$R_L = 500\ \Omega$,	See Figure 5			50	ns
t_{PHZ}	Output disable time from high level	$C_L = 15$ pF,	$R_L = 500\ \Omega$,	See Figure 4		8	30	ns
t_{PLZ}	Output disable time from low level	$C_L = 15$ pF,	$R_L = 500\ \Omega$,	See Figure 5		8	30	ns

† All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.

SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	EIA/TIA-422-B	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\lvert V_{OD1} \rvert$	V_o	V_o
$\lvert V_{OD2} \rvert$	V_t ($R_L = 100\ \Omega$)	V_t ($R_L = 54\ \Omega$)
$\lvert V_{OD3} \rvert$		V_t (test termination measurement 2)
V_{test}		V_{tst}
$\Delta \lvert V_{OD} \rvert$	$\lvert \lvert V_t \rvert - \lvert \overline{V}_t \rvert \rvert$	$\lvert \lvert V_t \rvert - \lvert \overline{V}_t \rvert \rvert$
V_{OC}	$\lvert V_{os} \rvert$	$\lvert V_{os} \rvert$
$\Delta \lvert V_{OC} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$
I_{OS}	$\lvert I_{sa} \rvert, \lvert I_{sb} \rvert$	
I_O	$\lvert I_{xa} \rvert, \lvert I_{xb} \rvert$	I_{ia}, I_{ib}

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{IT-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2‡			V
V_{hys}	Hysteresis voltage (V_{IT+}−V_{IT-})	V_{OC} = 0			70		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV or inputs open, I_{OH} = −400 µA, See Figure 6		2.4			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 6	I_{OL} = 16 mA			0.5	V
			I_{OL} = 8 mA			0.45	
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	µA
I_I	Line input current	Other input = 0, See Note 4	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	µA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	µA
r_I	Input resistance			12			kΩ
I_{OS}	Short-circuit output current	V_O = 0		−15		−85	mA
I_{CC}	Supply current	No load	Outputs enabled		23	50	mA
			Outputs disabled		19	35	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 4: This applies for both power on and power off. Refer to ANSI Standard RS-485 for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 15 pF

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_{ID} = −1.5 V to 1.5 V, See Figure 7		14	37	ns
t_{PHL}	Propagation delay time, high- to low-level output			14	37	ns
t_{PZH}	Output enable time to high level	See Figure 8		7	20	ns
t_{PZL}	Output enable time to low level			7	20	ns
t_{PHZ}	Output disable time from high level	See Figure 8		7	16	ns
t_{PLZ}	Output disable time from low level			8	16	ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

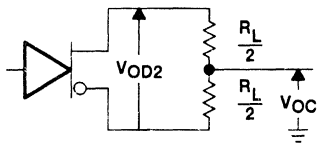


Figure 1. Driver V_{OD} and V_{OC}

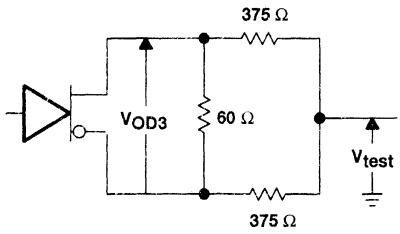
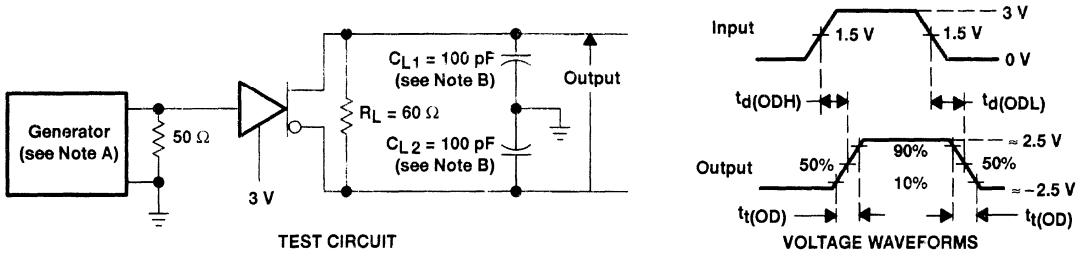
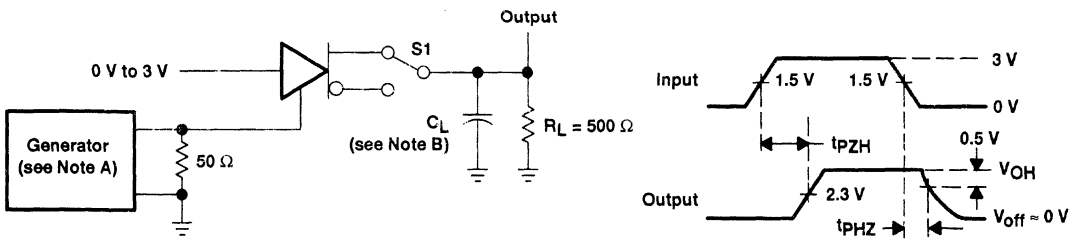


Figure 2. Driver V_{OD3}



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

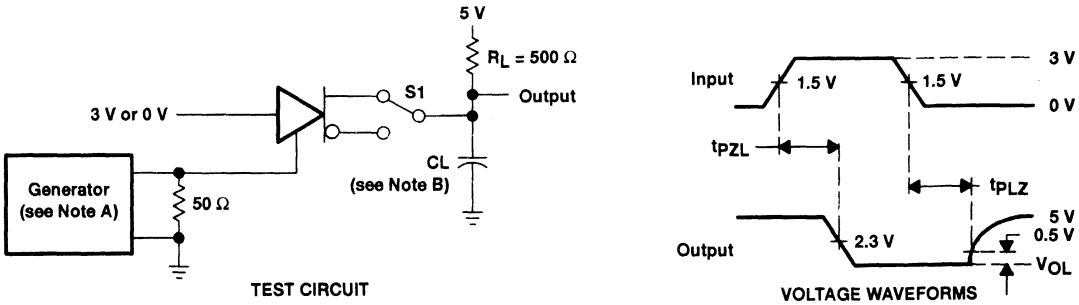
Figure 3. Driver Differential-Output Test Circuit and Voltage Waveforms



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 4. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: C. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns, Z_O = 50 Ω..
D. C_L includes probe and jig capacitance.

Figure 5. Driver Test Circuit and Voltage Waveforms

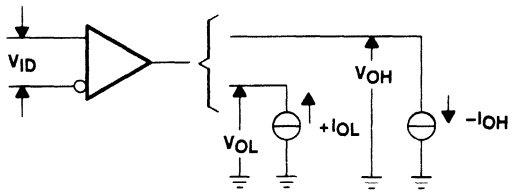
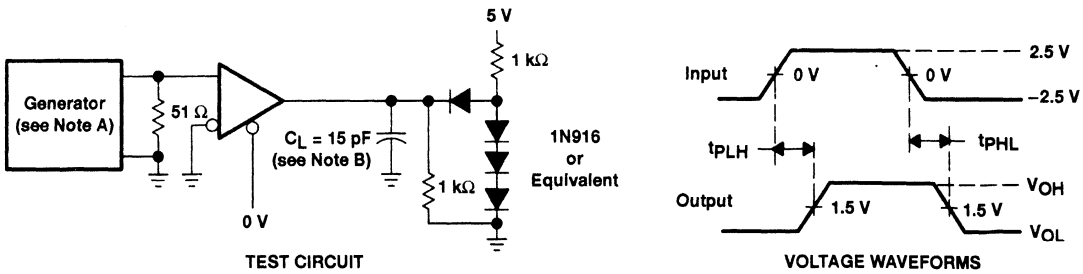


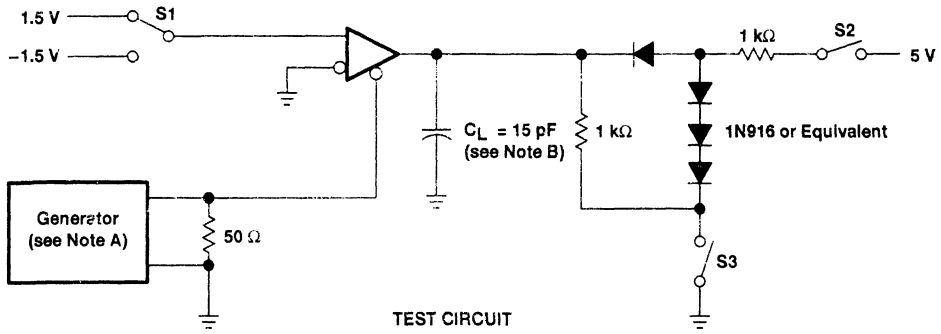
Figure 6. Receiver V_{OH} and V_{OL}



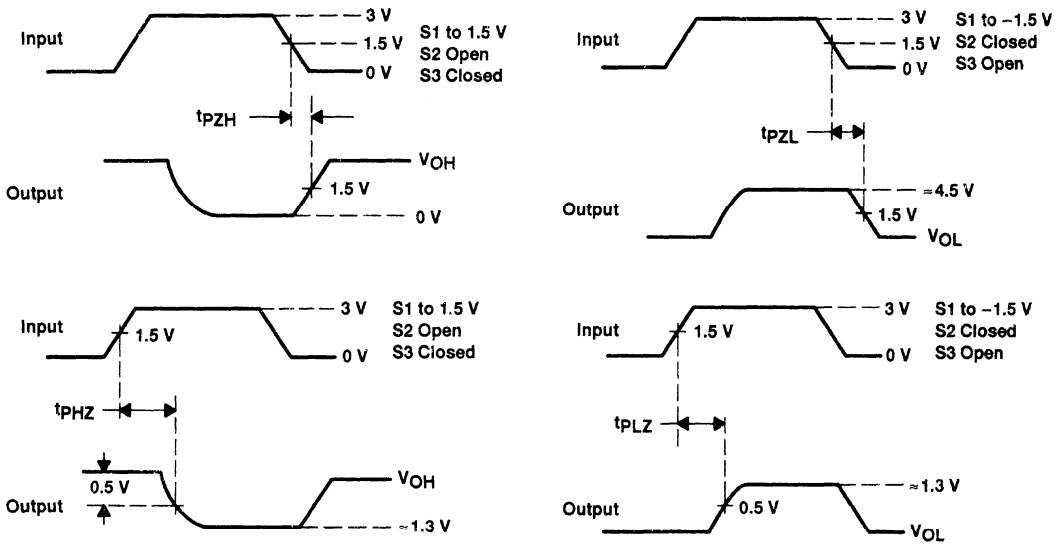
NOTES: E. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns, Z_O = 50 Ω.
F. C_L includes probe and jig capacitance.

Figure 7. Receiver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 8. Receiver Test Circuit and Voltage Waveforms

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

DRIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

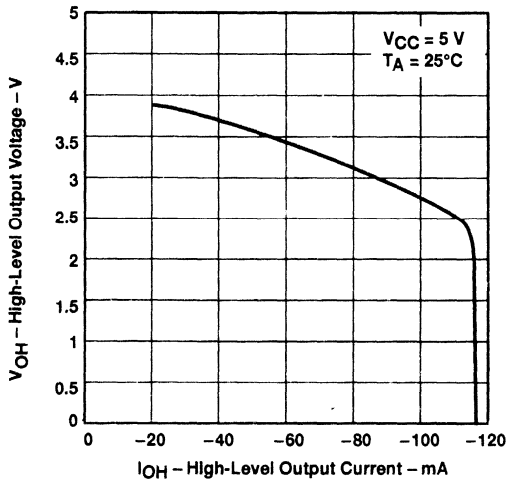


Figure 9

DRIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

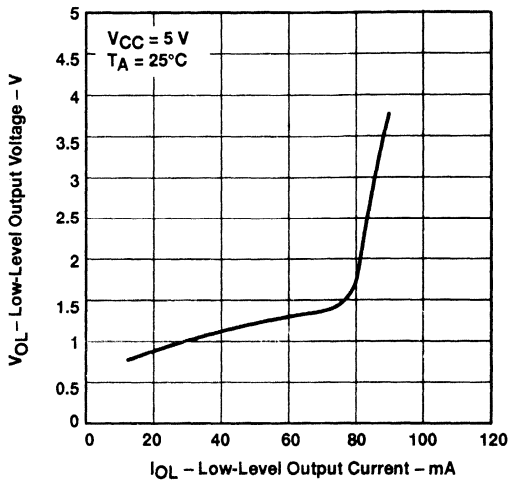


Figure 10

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

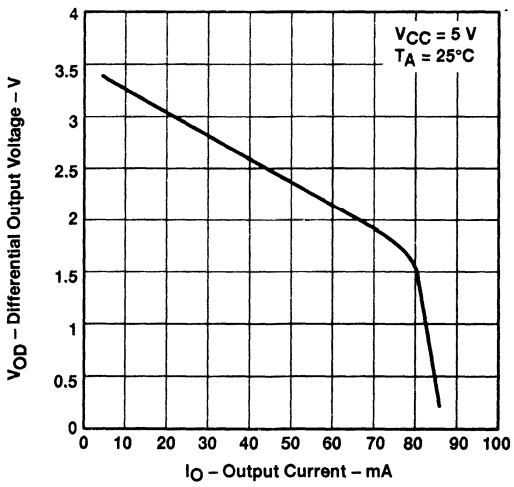


Figure 11

TYPICAL CHARACTERISTICS

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

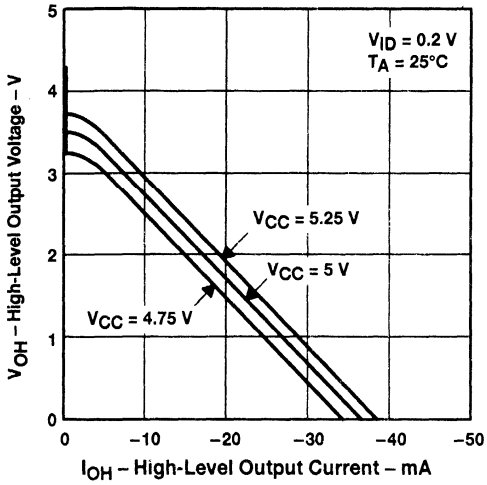


Figure 12

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

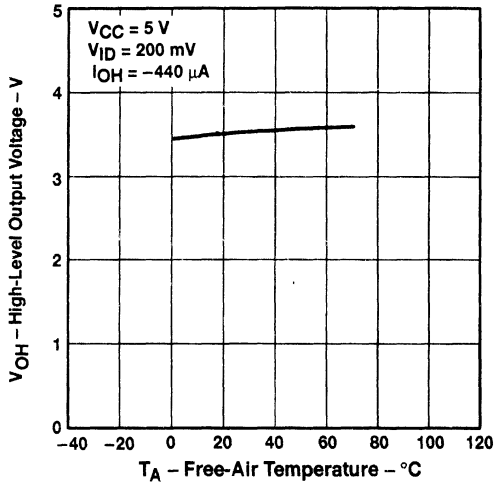


Figure 13

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

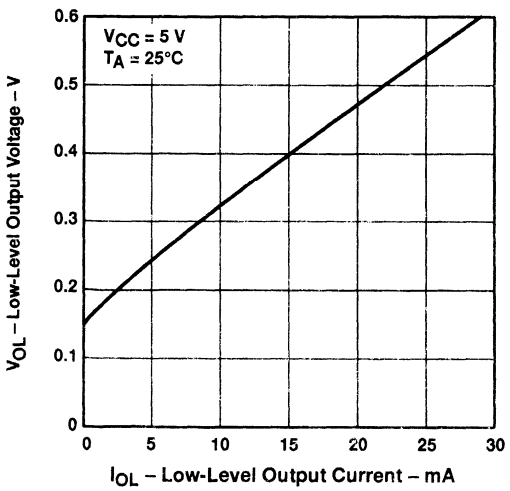


Figure 14

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

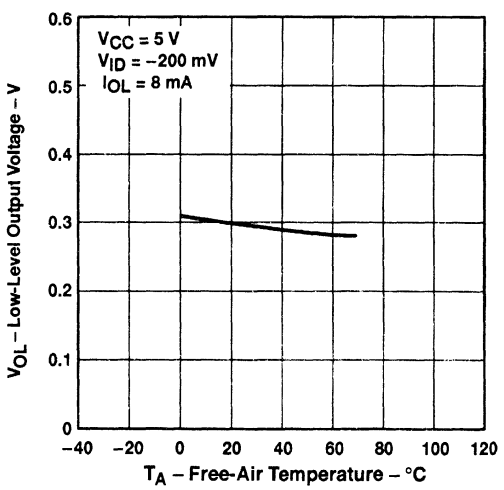


Figure 15

TYPICAL CHARACTERISTICS

RECEIVER
OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

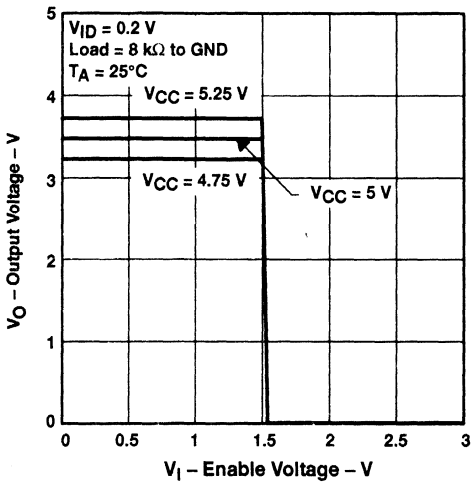


Figure 16

RECEIVER
OUTPUT VOLTAGE
vs
ENABLE VOLTAGE

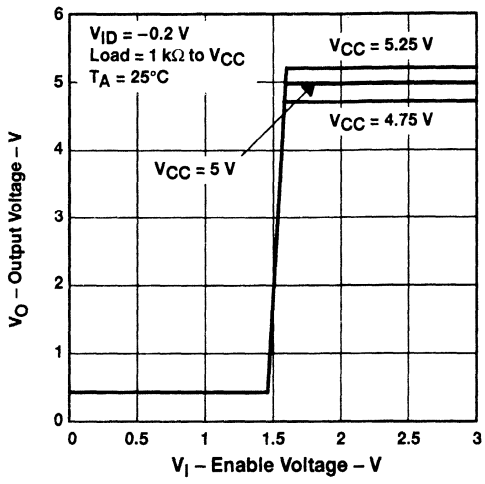
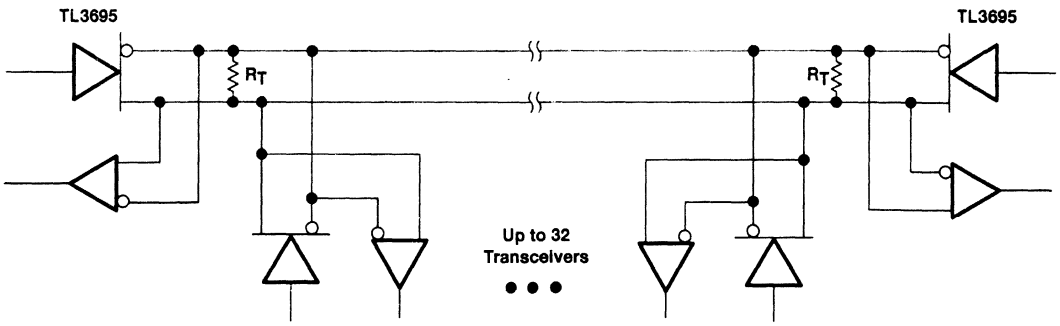


Figure 17

APPLICATION INFORMATION



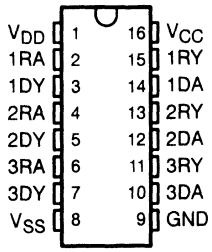
NOTE A: The line should be terminated at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

Figure 18. Typical Application Circuit

SLLS185A – DECEMBER 1994 – REVISED MARCH 1995

- **Three Drivers and Three Receivers That Meet or Exceed the Requirements of ANSI EIA/TIA-232-E and ITU V.28**
- **Designed to Support Data Rates Up to 120 kbits/s Over 3-m Cable**
- **ESD Protection Exceeds 5 kV on All Pins**
- **Flow-Through Design**
- **Wide-Driver Supply Voltage . . . ±4.5 V to ±15 V**
- **Functionally Interchangeable With Motorola MC145406 and Texas Instruments SN75C1406**

DW OR N PACKAGE
(TOP VIEW)



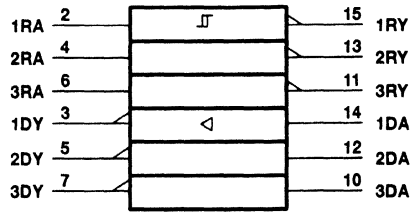
description

The TL145406 is a bipolar device containing three independent drivers and receivers that are used to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). The drivers and receivers of the TL145406 are similar to those of the SN75188 quadruple driver and SN75189A quadruple receiver, respectively. The pinout matches the flow-through design of the SN75C1406 to reduce the board space required and allow easy interconnection. The bipolar circuits and processing of the TL145406 provide a rugged low-cost solution for this function at the expense of quiescent power and external passive components relative to the SN75C1406.

The TL145406 complies with the requirements of the EIA/TIA 232-E and ITU (formerly CCITT) V.28 standards. These standards are for data interchange between a host computer and peripheral at signalling rates up to 20 kbits/s. The switching speeds of the TL145406 are fast enough to support rates up to 120 kbits/s with lower capacitive loads (shorter cables). Interoperability at the higher signalling rates cannot be assured unless the designer has design control of the cable and the interface circuits at both ends. For interoperability at signalling rates to 120 kbits/s, use of EIA/TIA-423-B (ITU V.10) and EIA/TIA-422-B (ITU V.11) standards are recommended.

The TL145406 is characterized for operation from 0°C to 70°C.

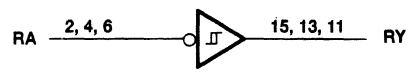
logic symbol†



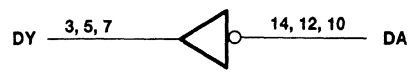
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

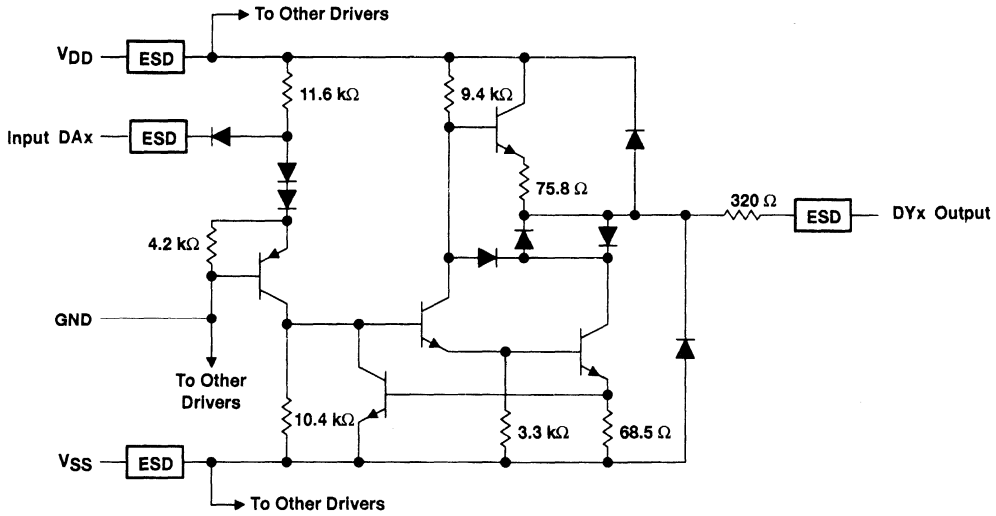
Typical of each receiver



Typical of each driver

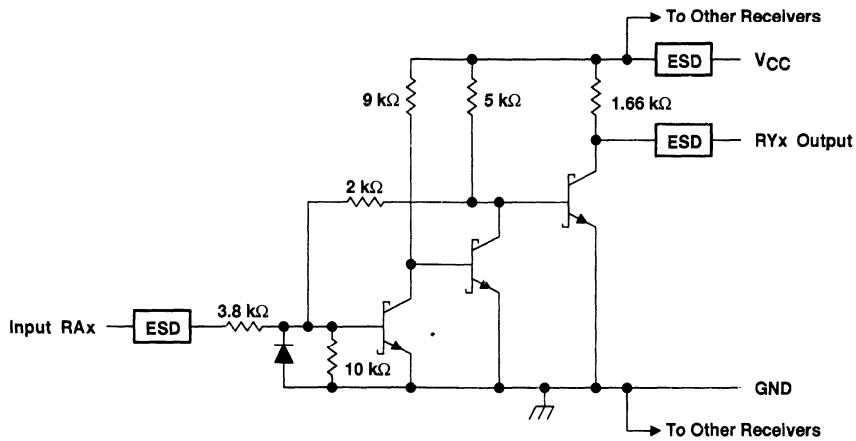


schematic (each driver)



Resistor values shown are nominal.

schematic (each receiver)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) ..... 10 V
Supply voltage, V_{DD} (see Note 1) ..... 15 V
Supply voltage, V_{SS} (see Note 1) ..... −15 V
Input voltage range: Driver ..... −15 V to 7 V
Receiver ..... −30 V to 30 V
Driver output voltage range ..... −15 V to 15 V
Receiver low-level output current ..... 20 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE‡

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A \le 70°C$ POWER RATING
DW	1256 mW	9.7 mW/°C	819 mW
N	1943 mW	14.9 mW/°C	1272 mW

‡ Dissipation ratings are the inverse of the traditional junction-to-case thermal resistance ($R_{\theta JA}$).

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		7.5	9	15	V
Supply voltage, V_{SS}		−7.5	−9	−15	V
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level input voltage, V_{IH} (driver only)		1.9			V
Low-level input voltage, V_{IL} (driver only)				0.8	V
High-level output current, I_{OH}	Driver			−6	mA
	Receiver			−0.5	
Low-level output current, I_{OL}	Driver			6	mA
	Receiver			16	
Operating free-air temperature, T_A		0		70	°C

supply currents

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
I_{DD}	Supply current from V_{DD}	All inputs at 1.9 V,	No load	V_{DD} = 9 V,	V_{SS} = −9 V			15	mA
				V_{DD} = 12 V,	V_{SS} = −12 V			19	
				V_{DD} = 15 V,	V_{SS} = −15 V			25	
		All inputs at 0.8 V,	No load	V_{DD} = 9 V,	V_{SS} = −9 V			4.5	mA
				V_{DD} = 12 V,	V_{SS} = −12 V			5.5	
				V_{DD} = 15 V,	V_{SS} = −15 V			9	
I_{SS}	Supply current from V_{SS}	All inputs at 1.9 V,	No load	V_{DD} = 9 V,	V_{SS} = −9 V			−15	mA
				V_{DD} = 12 V,	V_{SS} = −12 V			−19	
				V_{DD} = 15 V,	V_{SS} = −15 V			−25	
		All inputs at 0.8 V,	No load	V_{DD} = 9 V,	V_{SS} = −9 V			−3.2	mA
				V_{DD} = 12 V,	V_{SS} = −12 V			−3.2	
				V_{DD} = 15 V,	V_{SS} = −15 V			−3.2	
I_{CC}	Supply current from V_{CC}	V_{CC} = 5 V,	All inputs at 5 V,	No load			13.2	20	mA

DRIVER SECTION

electrical characteristics over recommended operating free-air temperture range, V_{DD} = 9V, V_{SS} = −9 V, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_{IL} = 0.8 V,	R_L = 3 kΩ,	See Figure 1	6	7.5		V
V_{OL}	Low-level output voltage (see Note 2)	V_{IH} = 1.9 V,	R_L = 3 kΩ,	See Figure 1		−7.5	−6	V
I_{IH}	High-level input current	V_I = 5 V,	See Figure 2				10	μA
I_{IL}	Low-level input current	V_I = 0,	See Figure 2				−1.6	mA
$I_{OS(H)}$	High-level short-circuit output current (see Note 3)	V_{IL} = 0.8 V,	V_O = 0 or V_{SS},	See Figure 1	−4.5	−10	−19.5	mA
$I_{OS(L)}$	Low-level short-circuit output current	V_{IH} = 2 V,	V_O = 0 or V_{DD},	See Figure 1	4.5	10	19.5	mA
r_O	Output resistance (see Note 4)	V_{CC} = V_{DD} = V_{SS} = 0,		V_O = −2 V to 2 V	300			Ω

NOTES: 2. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only (e.g., if −10 V is maximum, the typical value is a more negative voltage).
3. Output short-circuit conditions must maintain the total power dissipation below absolute maximum ratings.
4. Test conditions are those specified by EIA/TIA-232-E and as listed above.

switching characteristics, V_{CC} = 5 V, V_{DD} = 12 V, V_{SS} = −12 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 3 kΩ to 7 kΩ,	C_L = 15 pF, See Figure 3		315	500	ns
t_{PHL}	Propagation delay time, high- to low-level output				75	175	ns
t_{TLH}	Transition time, low- to high-level output	R_L = 3 kΩ to 7 kΩ,	C_L = 15 pF, See Figure 3		60	100	ns
		R_L = 3 kΩ to 7 kΩ,	C_L = 2500 pF, See Figure 3 and Note 5		1.7	2.5	μs
t_{THL}	Transition time, high- to low-level output	R_L = 3 kΩ to 7 kΩ,	C_L = 15 pF, See Figure 3		40	75	ns
		R_L = 3 kΩ to 7 kΩ,	C_L = 2500 pF, See Figure 3 and Note 6		1.5	2.5	μs

NOTES: 5. Measured between −3 V and 3 V points of the output waveform (EIA/TIA-232-E conditions). All unused inputs are tied.
6. Measured between 3 V and −3 V points of the output waveform (EIA/TIA-232-E conditions). All unused inputs are tied.

RECEIVER SECTION

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going threshold voltage	See Figure 5	T_A = 25°C	1.75	1.9	2.3	V
			T_A = 0°C to 70 °C	1.55		2.3	
V_{IT-}	Negative-going threshold voltage			0.75	0.97	1.25	
V_{hys}	Input hysteresis ($V_{IT+} - V_{IT-}$)			0.5			
V_{OH}	High-level output voltage	I_{OH} = −0.5 mA	V_{IH} = 0.75 V	2.6	4	5	V
			Inputs open	2.6			
V_{OL}	Low-level output voltage	I_{OL} = 10 mA,	V_I = 3 V		0.2	0.45	V
I_{IH}	High-level input current	V_I = 25 V,	See Figure 5	3.6		8.3	mA
		V_I = 3 V,	See Figure 5	0.43			
I_{IL}	Low-level input current	V_I = −25 V,	See Figure 5	−3.6		−8.3	mA
		V_I = −3 V,	See Figure 5	−0.43			
I_{OS}	Short-circuit output current				−3.4	−12	mA

† All typical values are at T_A = 25°C, V_{CC} = 5, V_{DD} = 9 V, and V_{SS} = −9 V.

switching characteristics, V_{CC} = 5 V, V_{DD} = 12 V, V_{SS} = −12 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 50 pF, R_L = 5 kΩ, See Figure 6		107	425	ns
t_{PHL}	Propagation delay time, high- to low-level output			42	150	ns
t_{TLH}	Transition time, low- to high-level output			175	400	ns
t_{THL}	Transition time, high- to low-level output			16	60	ns

PARAMETER MEASUREMENT INFORMATION

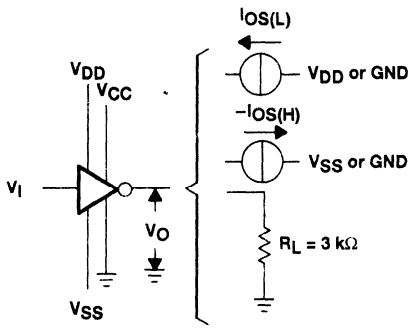


Figure 1. Driver Test Circuit for V_{OH}, V_{OL}, $I_{OS(H)}$, and $I_{OS(L)}$

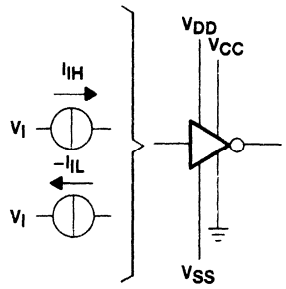
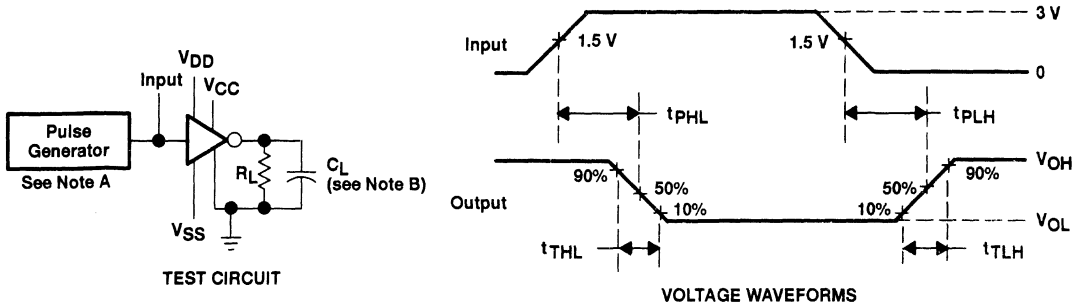


Figure 2. Driver Test Circuit for I_{IH} and I_{IL}

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: t_w = 25 µs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

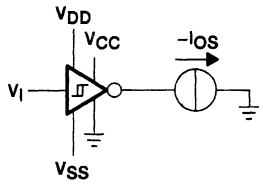


Figure 4. Receiver Test Circuit for I_{OS}

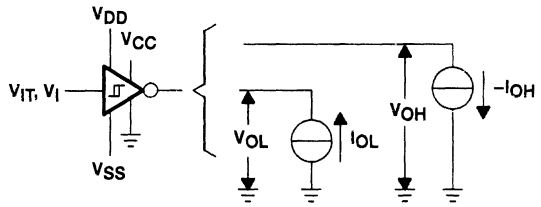
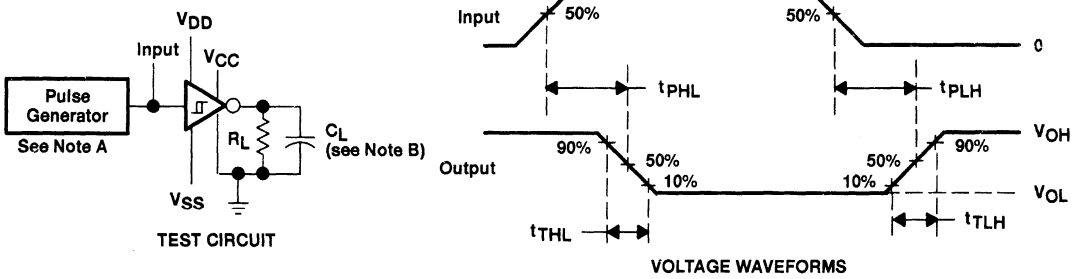


Figure 5. Receiver Test Circuit for V_{IT}, V_{OH}, and V_{OL}



NOTES: A. The pulse generator has the following characteristics: t_w = 25 µs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.
B. C_L includes probe and jig capacitance.

Figure 6. Receiver Propagation and Transition Times

TYPICAL CHARACTERISTICS

DRIVER
VOLTAGE TRANSFER CHARACTERISTICS

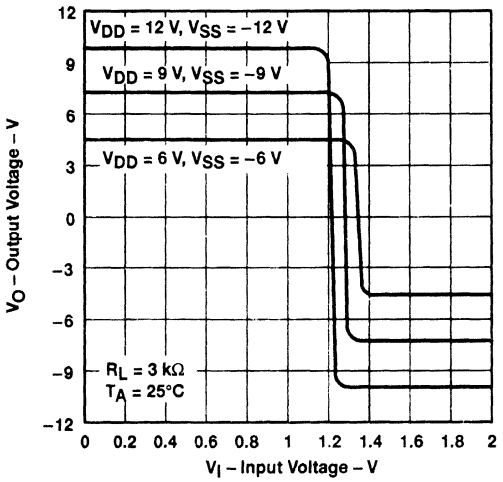


Figure 7

DRIVER
OUTPUT CURRENT
vs
OUTPUT VOLTAGE

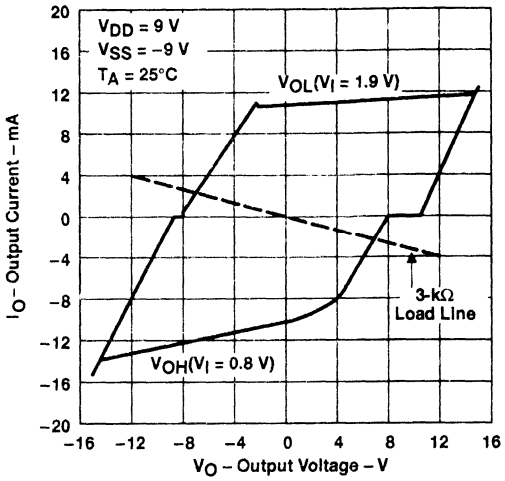


Figure 8

DRIVER
SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

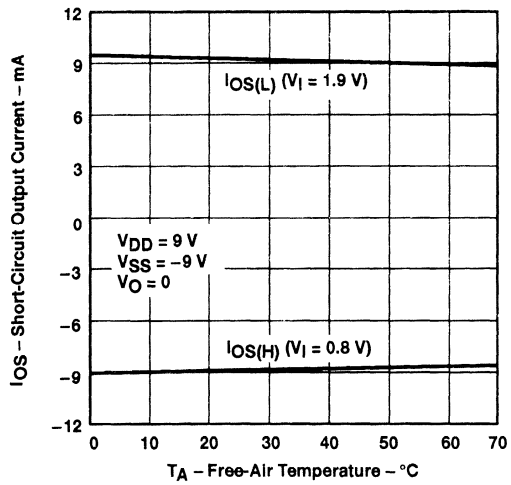


Figure 9

DRIVER
SLEW RATE
vs
LOAD CAPACITANCE

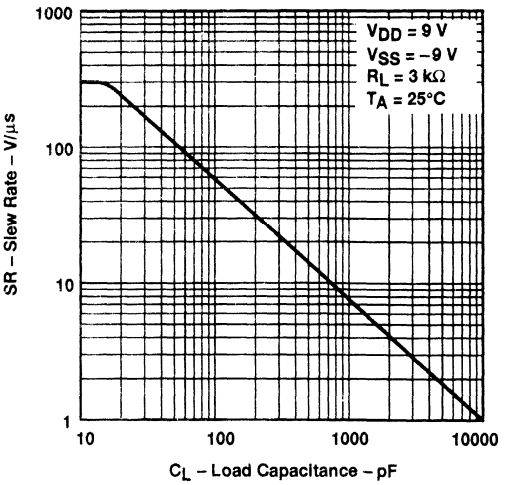


Figure 10

TYPICAL CHARACTERISTICS

RECEIVER
INPUT THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

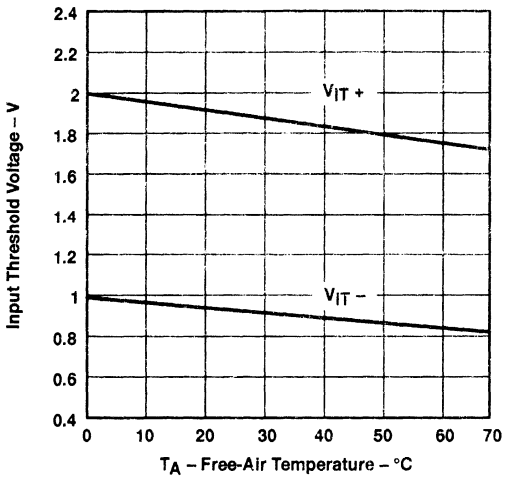


Figure 11

RECEIVER
INPUT THRESHOLD VOLTAGE
vs
SUPPLY VOLTAGE

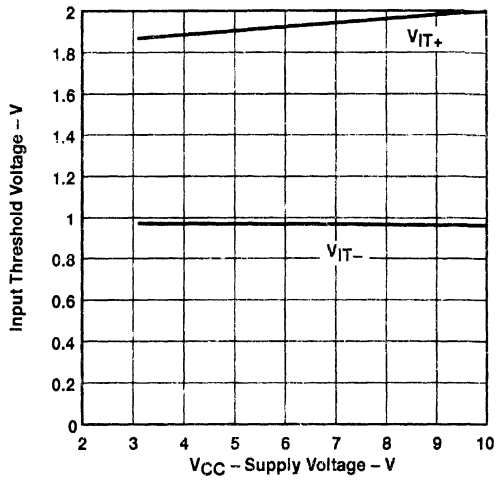
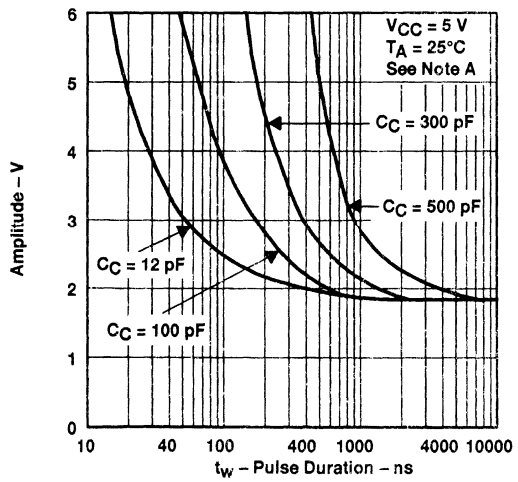


Figure 12

RECEIVER
NOISE REJECTION



NOTE A: This figure shows the maximum amplitude of a positive-going pulse that, starting from 0, does not cause a change of the output level.

Figure 13

RECEIVER
MAXIMUM SUPPLY VOLTAGE
vs
FREE-AIR TEMPERATURE

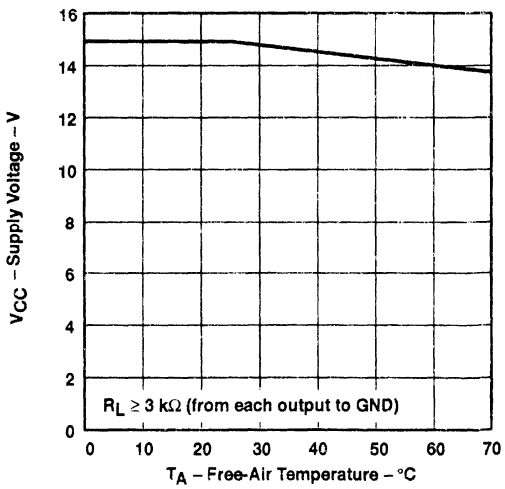


Figure 14

APPLICATION INFORMATION

Diodes placed in series with the V_{DD} and V_{SS} leads protect the TL145406 during the fault condition in which the device outputs are shorted to ±15 V and the power supplies are at low. Diodes also provide low-impedance paths to ground (see Figure 15).

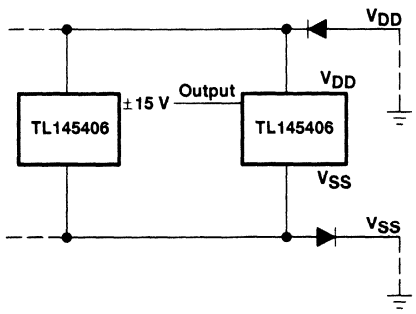
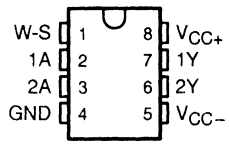


Figure 15. Power-Supply Protection to Meet Power-Off Fault Conditions of ANSI EIA/TIA-232-E

SLLS110B – OCTOBER 1980 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-423-B and -232-E and ITU Recommendations V.10 and V.28**
- **Output Slew Rate Control**
- **Output Short-Circuit-Current Limiting**
- **Wide Supply Voltage Range**
- **8-Pin Package**
- **Designed to Be Interchangeable With National DS9636A**

D OR P PACKAGE
(TOP VIEW)

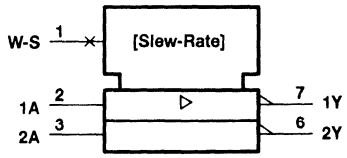


description

The uA9636AC is a dual, single-ended line driver designed to meet ANSI Standards EIA/TIA-423-B and EIA/TIA-232-E and ITU Recommendations V.10 and V.28. The slew rates of both amplifiers are controlled by a single external resistor, $R_{(WS)}$, connected between the wave-shape-control (W-S) terminal and GND. Output current limiting is provided. Inputs are compatible with TTL and CMOS and are diode protected against negative transients. This device operates from ±12 V and is supplied in an 8-pin package.

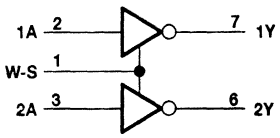
The uA9636AC is characterized for operation from 0°C to 70°C.

logic symbol†



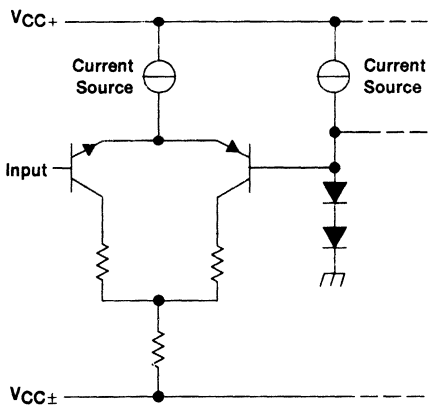
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram

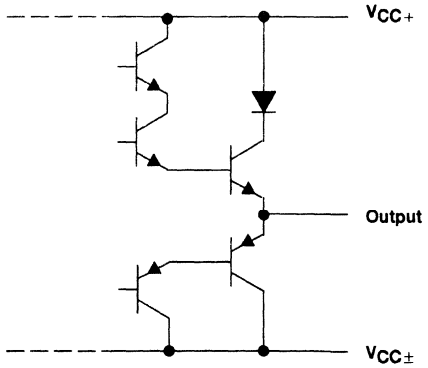


schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Positive supply voltage range, V_{CC+} (see Note 1) ..... V_{CC-} to 15 V
Negative supply voltage range, V_{CC-} ..... 0.5 V to −15 V
Output voltage, V_O ..... ±15 V
Output current, I_O ..... ±150 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Positive supply voltage, V_{CC+}	10.8	12	13.2	V
Negative supply voltage, V_{CC-}	−10.8	−12	−13.2	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Wave-shaping resistor, $R_{(WS)}$	10		1000	kΩ
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of free-air temperature, supply voltage, and wave-shaping resistance (unless otherwise noted)

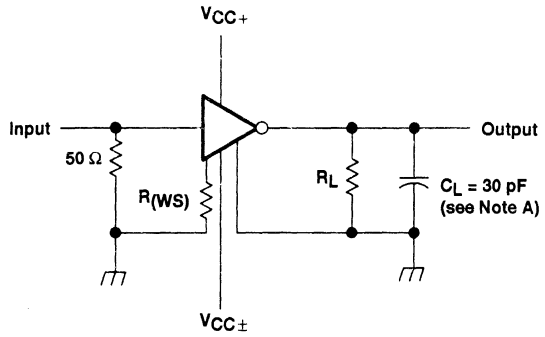
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −15 mA			−1.1	−1.5	V
V_{OH}	High-level output voltage	V_I = 0.8 V	R_L = ∞	5	5.6	6	V
			R_L = 3 kΩ to GND	5	5.6	6	
			R_L = 450 Ω to GND	4	5.4	6	
V_{OL}	Low-level output voltage	V_I = 2 V	R_L = ∞	−6‡	−5.7	−5	V
			R_L = 3 kΩ to GND	−6‡	−5.6	−5	
			R_L = 450 Ω to GND	−6‡	−5.4	−4	
I_{IH}	High-level input current	V_I = 2.4 V				10	μA
		V_I = 5.5 V				100	
I_{IL}	Low-level input current	V_I = 0.4 V			−20	−80	μA
I_O	Output current (power off)	$V_{CC\pm}$ = 0,	V_O = ± 6 V			±100	μA
I_{OS}	Short-circuit output current§	V_I = 2 V		15	25	150	mA
		V_I = 0		−15	−40	−150	
r_O	Output resistance	R_L = 450 Ω			25	50	Ω
I_{CC+}	Positive supply current	V_{CC} = ±12 V, $R_{(WS)}$ = 100 kΩ,	V_I = 0, Output open		13	18	mA
I_{CC-}	Negative supply current	V_{CC} = ±12 V, $R_{(WS)}$ = 100 kΩ,	V_I = 0, Output open		−13	−18	mA

† All typical values are at V_{CC} = ±12 V, T_A = 25°C.
‡ The algebraic convention, in which the less-positive (more-negative) limit is designated as minimum, is used in this data sheet for logic voltage levels, e.g., when −5 V is the maximum, the minimum is a more-negative voltage.
§ Not more than one output should be shorted to ground at a time.

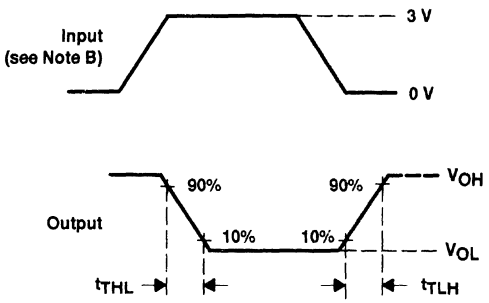
switching characteristics, $V_{CC\pm}$ = ±12 V, T_A = 25°C (see Figure 1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{TLH}	Transition time, low- to high-level output	R_L = 450 kΩ, C_L = 30 pF	$R_{(WS)}$ = 10 kΩ	0.8	1.1	1.4	μs
			$R_{(WS)}$ = 100 kΩ	8	11	14	
			$R_{(WS)}$ = 500 kΩ	40	55	70	
			$R_{(WS)}$ = 1 MΩ	80	110	140	
t_{THL}	Transition time, high- to low-level output	R_L = 450 kΩ, C_L = 30 pF	$R_{(WS)}$ = 10 kΩ	0.8	1.1	1.4	μs
			$R_{(WS)}$ = 100 kΩ	8	11	14	
			$R_{(WS)}$ = 500 kΩ	40	55	70	
			$R_{(WS)}$ = 1 MΩ	80	110	140	

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$, PRR ≤ 1 kHz, duty cycle = 50%.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

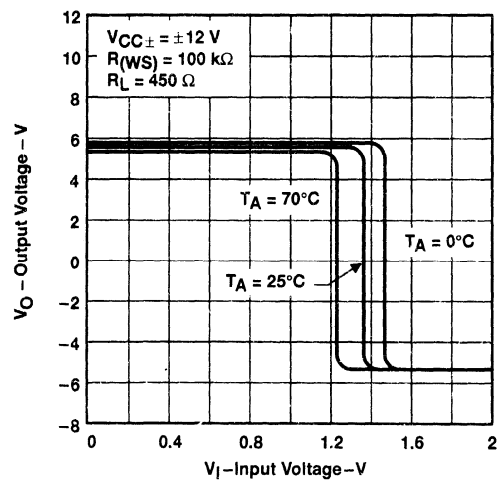


Figure 2

INPUT CURRENT
vs
INPUT VOLTAGE

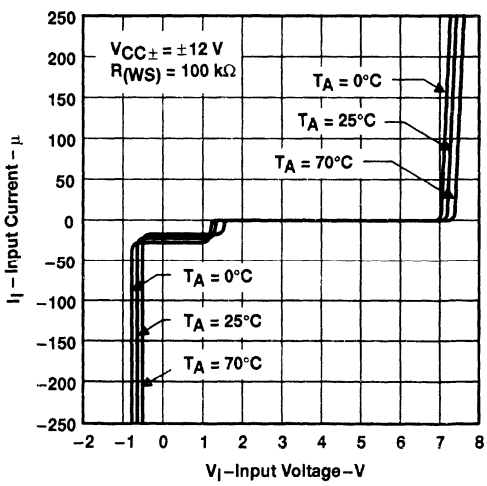


Figure 3

TYPICAL CHARACTERISTICS

OUTPUT CURRENT
vs
OUTPUT VOLTAGE
(POWER ON)

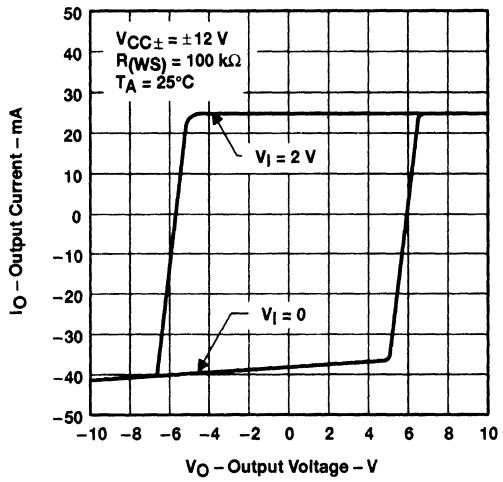


Figure 4

OUTPUT CURRENT
vs
OUTPUT VOLTAGE
(POWER OFF)

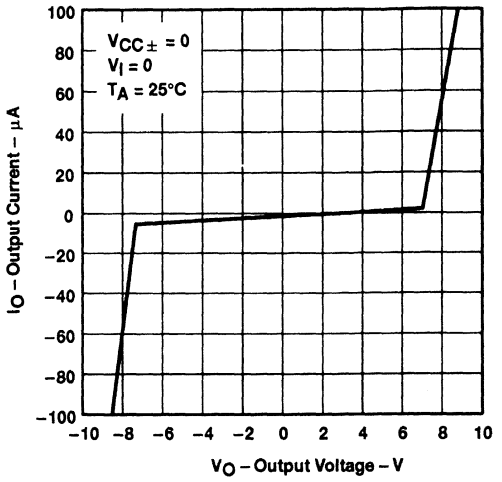


Figure 5

TRANSITION TIME
vs
WAVE-SHAPING RESISTANCE

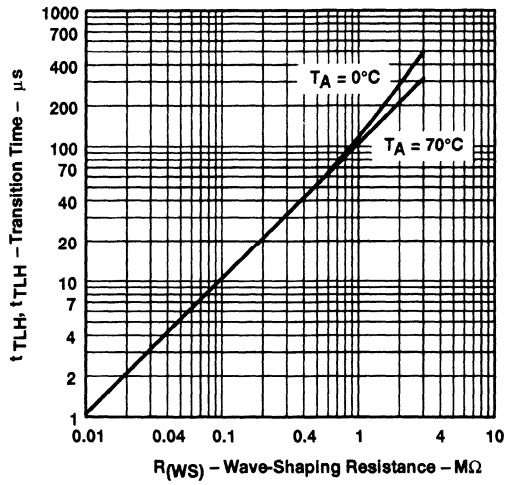


Figure 6

APPLICATION INFORMATION

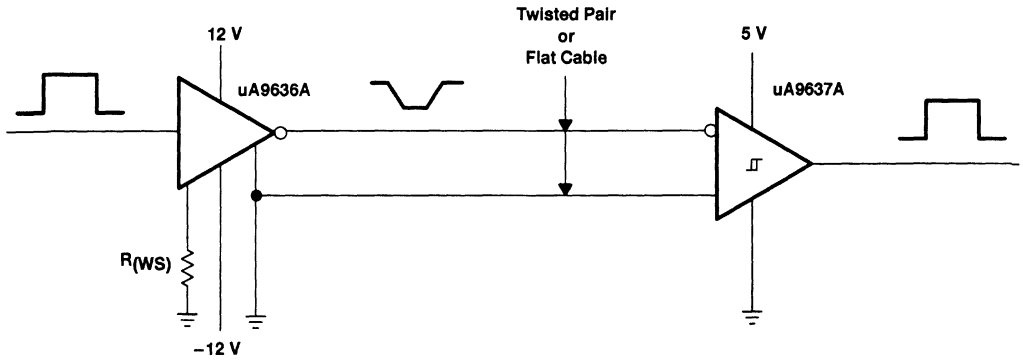


Figure 7. EIA/TIA-423-B System Application

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

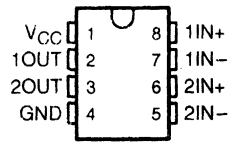
- **Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-422-B and EIA/TIA-423-B and ITU Recommendations V.10 and V.11**
- **Operates From Single 5-V Power Supply**
- **Wide Common-Mode Voltage Range**
- **High Input Impedance**
- **TTL-Compatible Outputs**
- **High-Speed Schottky Circuitry**
- **8-Pin Dual-In-Line and Small-Outline Packages**
- **Designed to Be Interchangeable With National DS9637A**

description

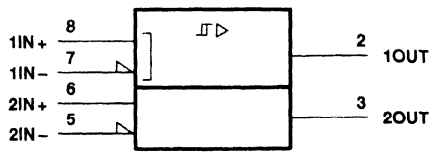
The uA9637AC is a dual differential line receiver designed to meet ANSI Standards EIA/TIA-422-B and EIA/TIA-423-B and ITU Recommendations V.10 and V.11. The line receiver utilizes Schottky circuitry and have TTL-compatible outputs. The inputs are compatible with either a single-ended or a differential-line system. This device operates from a single 5-V power supply and is supplied in an 8-pin dual-in-line package or small-outline package.

The uA9637AC is characterized for operation from 0°C to 70°C.

uA9637C . . . D OR P PACKAGE
(TOP VIEW)

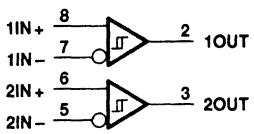


logic symbol†



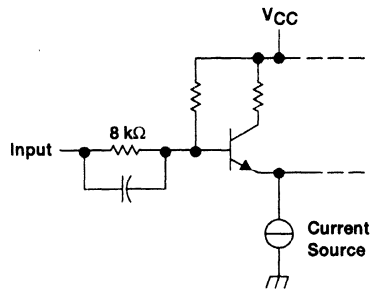
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram

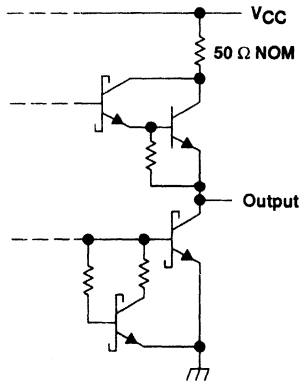


schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Input voltage, V_I ..... ±15 V
Differential input voltage, V_{ID} (see Note 2) ..... ±15 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to 5.5 V
Low-level output current, I_{OL} ..... 50 mA
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	—
P	1000 mW	8.0 mW/°C	640 mW	—

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage, common-mode input voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	See Note 3				0.2	V
						0.4	
V_{IT-}	Negative-going input threshold voltage	See Note 3		−0.2			V
				−0.4§			
V_{hys}	Hysteresis voltage ($V_{IT+}-V_{IT-}$)				70		mV
V_{OH}	High-level output voltage	V_{ID} = 0.2 V,	I_O = −1 mA	2.5	3.5		V
V_{OL}	Low-level output voltage	V_{ID} = −0.2 V,	I_O = 20 mA		0.35	0.5	V
I_I	Input current	V_{CC} = 0 to 5.5 V, See Note 4	V_I = 10 V		1.1	3.25	mA
			V_I = −10 V		−1.6	−3.25	
I_{OS}	Short-circuit output current¶	V_O = 0,	V_{ID} = 0.2 V	−40	−75	−100	mA
I_{CC}	Supply current	V_{ID} = −0.5 V,	No load		35	50	mA

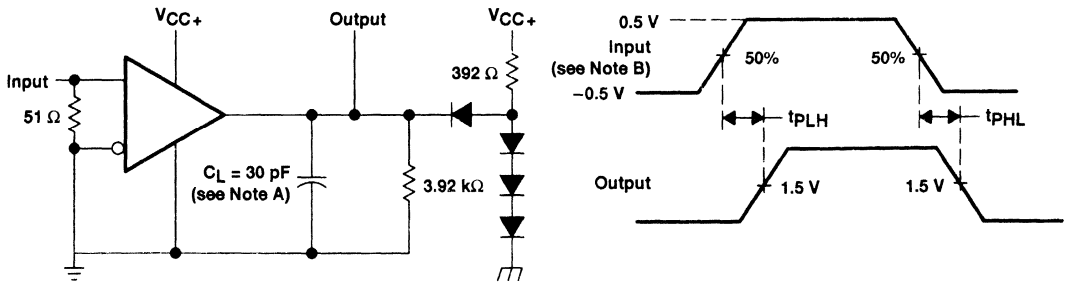
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.
¶ Only one output should be shorted at a time, and duration of the short circuit should not exceed one second.

NOTES: 3. The expanded threshold parameter is tested with a 500-Ω resistor in series with each input.
4. The input not under test is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 30 pF, See Figure 1		15	25	ns
t_{PHL}	Propagation delay time, high- to low-level output			13	25	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

VOLTAGE WAVEFORM

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 5 MHz, duty cycle = 50%.

Figure 1. Test Circuit and Voltage Waveform

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

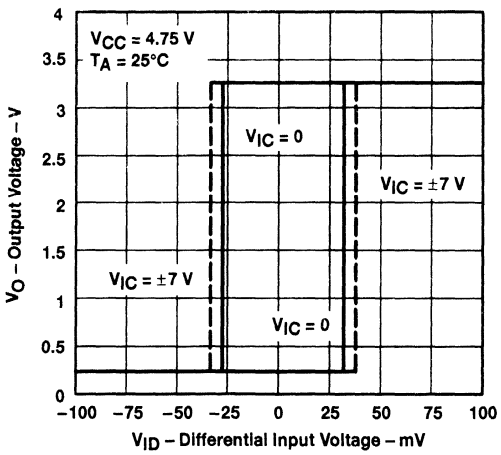


Figure 2

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

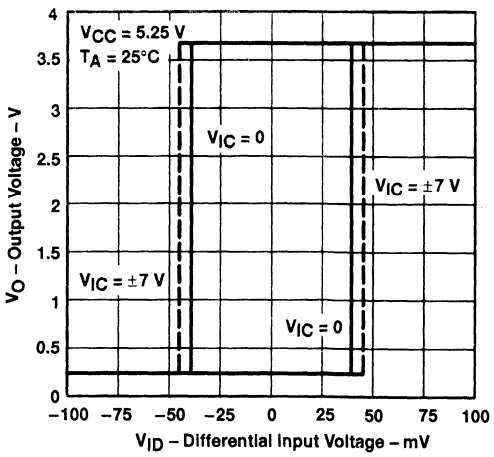


Figure 3

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

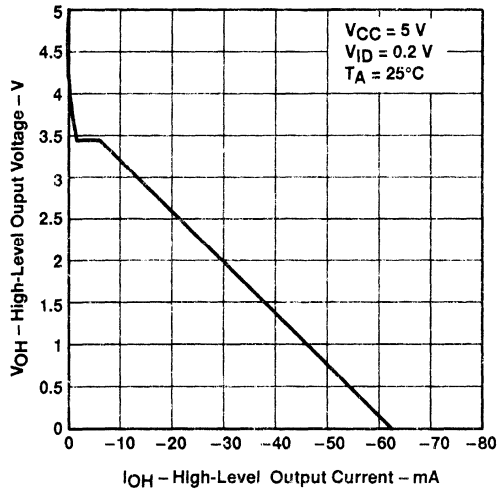


Figure 4

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

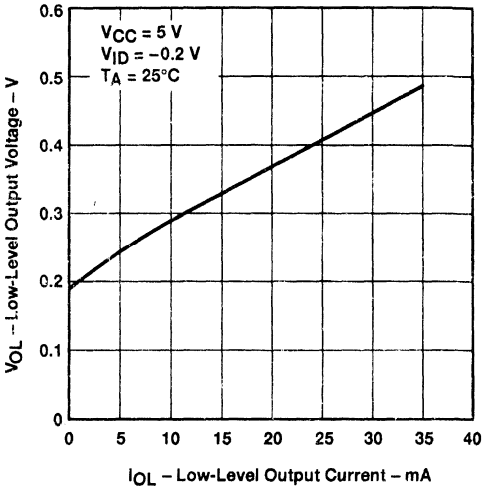


Figure 5

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

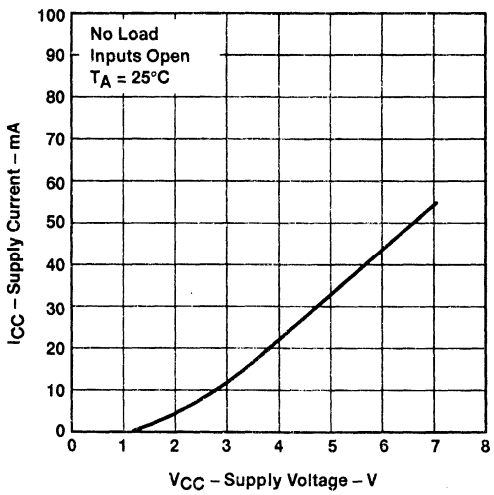


Figure 6

APPLICATION INFORMATION

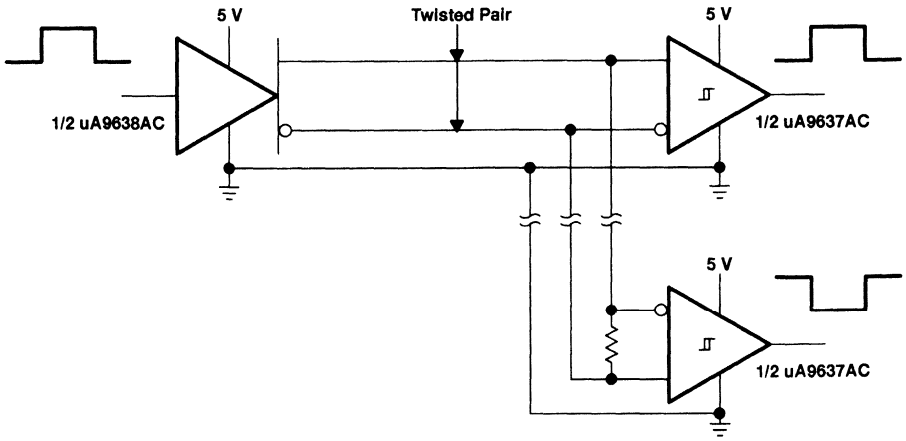
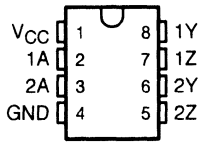


Figure 7. EIA/TIA-422-B System Applications

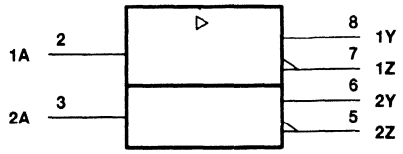
SLLS112C – OCTOBER 1980 – REVISED APRIL 1994

- **Meets or Exceeds ANSI Standard EIA/TIA-422-B**
- **Operates From a Single 5-V Power Supply**
- **Drives Loads as Low as 50 Ω up to 15 Mbps**
- **TTL- and CMOS-Input Compatibility**
- **Output Short-Circuit Protection**
- **Interchangeable With National Semiconductor™ DS9638**

D OR P PACKAGE
(TOP VIEW)



logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

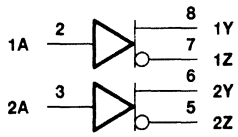
description

The uA9638C is a dual high-speed differential line driver designed to meet ANSI Standard EIA/TIA-422-B. The inputs are TTL and CMOS compatible and have input clamp diodes. Schottky-diode-clamped transistors are used to minimize propagation delay time. This device operates from a single 5-V power supply and is supplied in an 8-pin package.

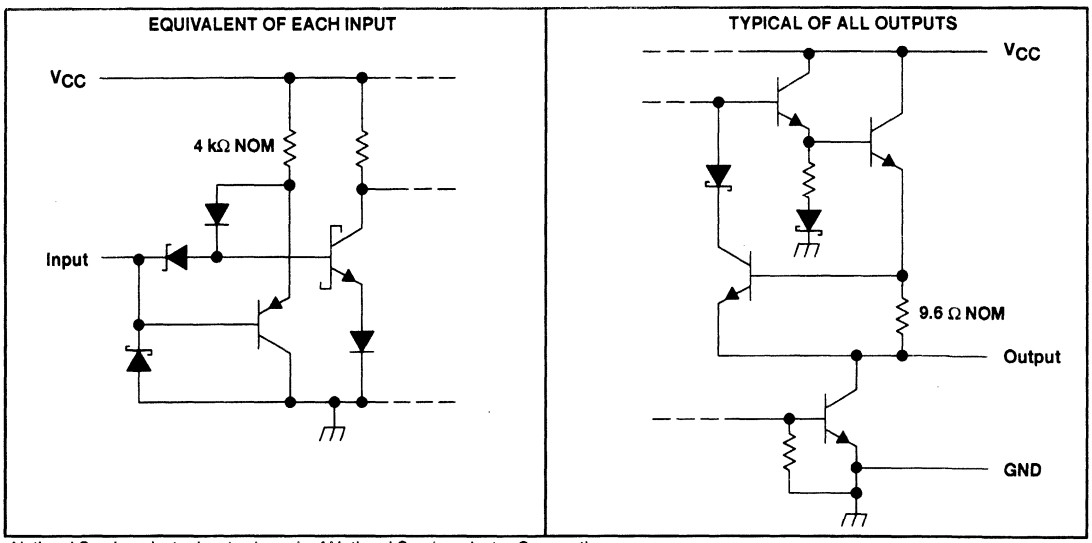
The uA9638 provides the current needed to drive low-impedance loads at high speeds. Typically used with twisted-pair cabling and differential receiver(s), base-band data transmission can be accomplished up to and exceeding 15 Mbps in properly designed systems. The uA9637A dual line receiver is commonly used as the receiver. For even faster switching speeds in the same pin configuration, see the SN75ALS191.

The uA9638C is characterized for operation from 0°C to 70°C.

logic diagram



schematics of inputs and outputs



National Semiconductor is a trademark of National Semiconductor Corporation.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Input voltage range, V_I ..... −0.5 V to 7 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values except differential output voltages are with respect to network GND.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−50	mA
Low-level output current, I_{OL}			50	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V, I_I = −18 mA				−1	−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OH} = −10 mA		2.5	3.5		V
			I_{OH} = −40 mA		2			
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V, I_{OL} = 40 mA	V_{IL} = 0.8 V,				0.5	V
$\|V_{OD1}\|$	Magnitude of differential output voltage	V_{CC} = 5.25 V, I_O = 0					$2V_{OD2}$	V
$\|V_{OD2}\|$	Magnitude of differential output voltage	V_{CC} = 4.75 V to 5.25 V, See Figure 1	R_L = 100 Ω,		2			V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage‡						±0.4	V
V_{OC}	Common-mode output voltage§						3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage‡						±0.4	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V			0.1	100	µA
			V_O = −0.25 V			−0.1	−100	
			V_O = −0.25 V to 6 V				±100	
I_I	Input current	V_{CC} = 5.25 V, V_I = 5.5 V					50	µA
I_{IH}	High-level input current	V_{CC} = 5.25 V, V_I = 2.7 V					25	µA
I_{IL}	Low-level input current	V_{CC} = 5.25 V, V_I = 0.5 V					−200	µA
I_{OS}	Short-circuit output current¶	V_{CC} = 5.25 V, V_O = 0			−50		−150	mA
I_{CC}	Supply current (both drivers)	V_{CC} = 5.25 V, No load,		All inputs at 0 V		45	65	mA

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level or vice versa.
§ In Standard EIA-422-A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
¶ Only one output at a time should be shorted, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	C_L = 15 pF,	R_L = 100 Ω,	See Figure 2		10	20	ns
$t_{t(OD)}$	Differential output transition time					10	20	ns
$t_{sk(o)}$	Output skew	See Figure 2				1		ns

PARAMETER MEASUREMENT INFORMATION

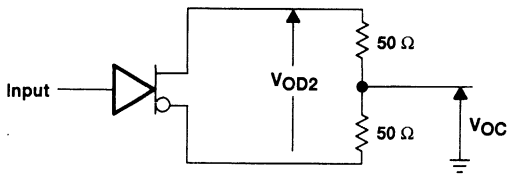
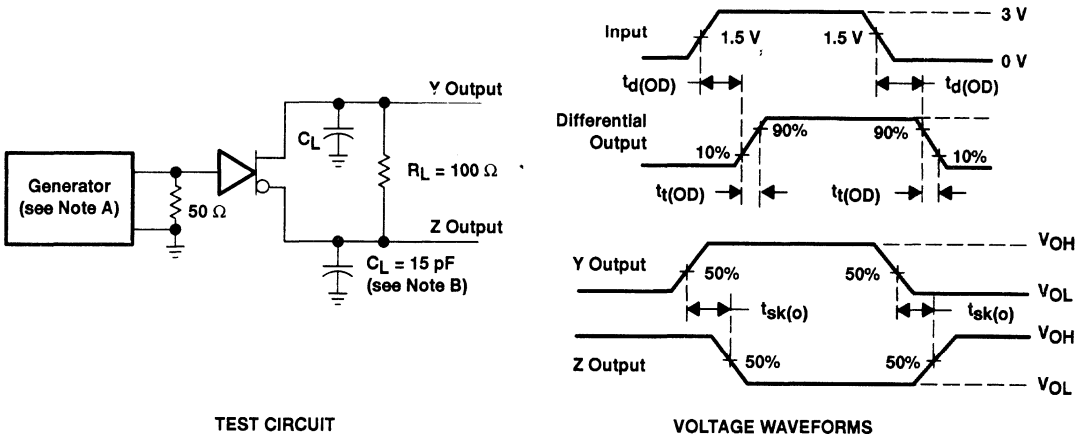


Figure 1. Differential and Common-Mode Output Voltages



TEST CIRCUIT **VOLTAGE WAVEFORMS**

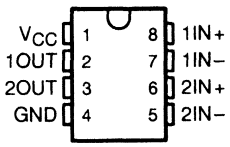
NOTES: A. The input pulse generator has the following characteristics: Z_O = 50 Ω, PRR ≤ 500 kHz, t_W = 100 ns, t_r = ≤ 5 ns.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms

SLLS113B – OCTOBER 1986 – REVISED MAY 1995

- **Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-422-B and EIA/TIA-423-B and ITU Recommendations V.10 and V.11**
- **Operates From Single 5-V Power Supply**
- **Wide Common-Mode Voltage Range**
- **High Input Impedance**
- **TTL-Compatible Outputs**
- **High-Speed Schottky Circuitry**
- **8-Pin Dual-In-Line and Small-Outline Packages**
- **Designed to Be Interchangeable With National DS9639AC**

D OR P PACKAGE
(TOP VIEW)

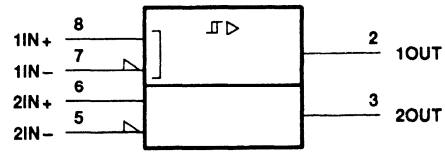


description

The uA9639C is a dual differential line receiver designed to meet ANSI Standards EIA/TIA-422-B and EIA/TIA-423-B and ITU Recommendations V.10 and V.11. It utilizes Schottky circuitry and has TTL-compatible outputs. The inputs are compatible with either a single-ended or a differential-line system. This device operates from a single 5-V power supply and is supplied in an 8-pin, dual-in-line package and small-outline package.

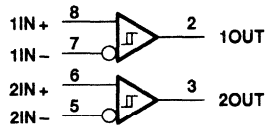
The uA9639C is characterized for operation from 0°C to 70°C.

logic symbol†

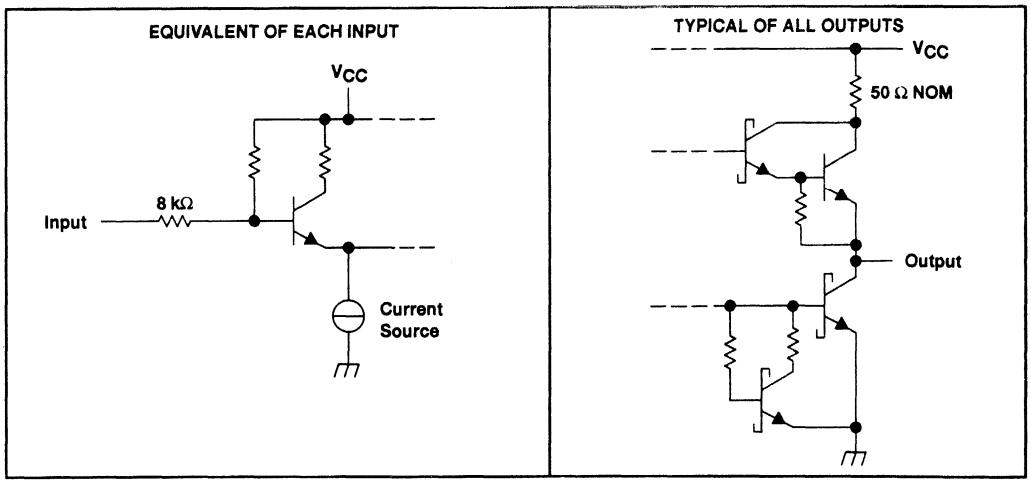


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Input voltage, V_I ..... ±15 V
Differential input voltage, V_{ID} (see Note 2) ..... ±15 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to 5.5 V
Low-level output current, I_{OL} ..... 50 mA
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage, common-mode input voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	See Note 3				0.2	V
						0.4	
V_{IT-}	Negative-going input threshold voltage	See Note 3		−0.2			V
				−0.4§			
V_{hys}	Hysteresis voltage ($V_{IT+}-V_{IT-}$)				70		mV
V_{OH}	High-level output voltage	V_{ID} = 0.2 V,	I_O = −1 mA	2.5	3.5		V
V_{OL}	Low-level output voltage	V_{ID} = −0.2 V,	I_O = 20 mA		0.35	0.5	V
I_I	Input current	V_{CC} = 0 to 5.5 V,	V_I = 10 V		1.1	3.25	mA
		See Note 4	V_I = −10 V		−1.6	−3.25	
I_{OS}	Short-circuit output current¶	V_O = 0,	V_{ID} = 0.2 V	−40	−75	−100	mA
I_{CC}	Supply current	V_{ID} = −0.5 V,	No load		35	50	mA

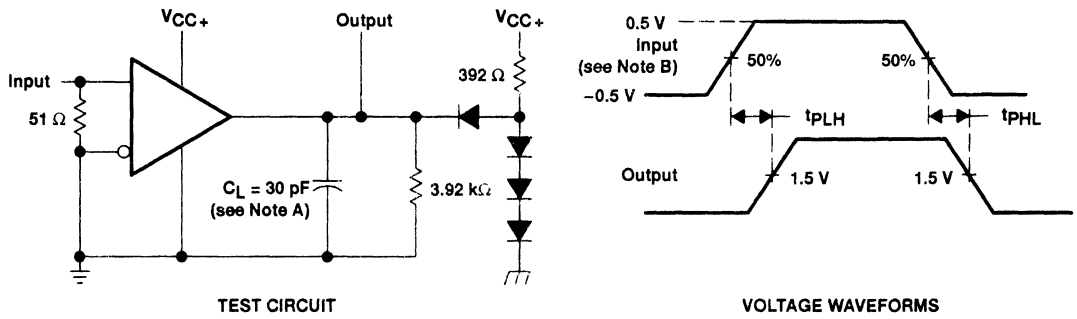
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.
¶ Only one output should be shorted at a time, and duration of the short circuit should not exceed one second.

NOTES: 3. The expanded threshold parameter is tested with a 500-Ω resistor in series with each input.
4. The input not under test is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 0°C to 70°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 50 pF, See Figure 1		85	ns
t_{PHL}	Propagation delay time, high- to low-level output			85	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 5 MHz, duty cycle = 50%.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

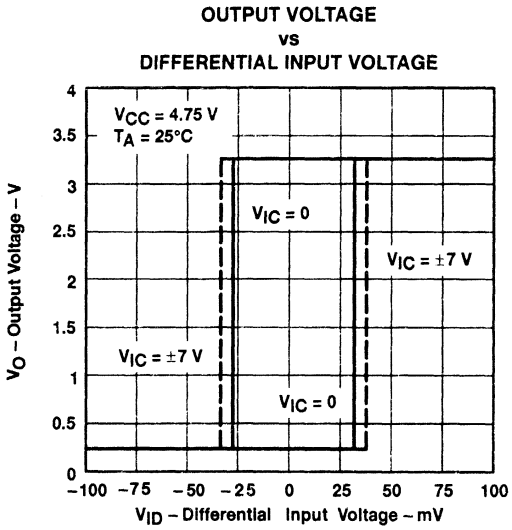


Figure 2

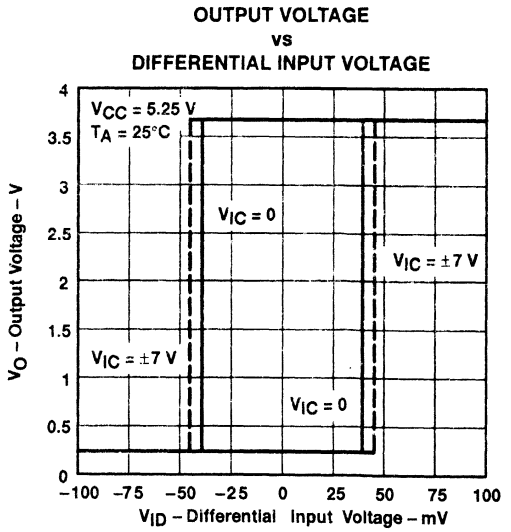


Figure 3

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

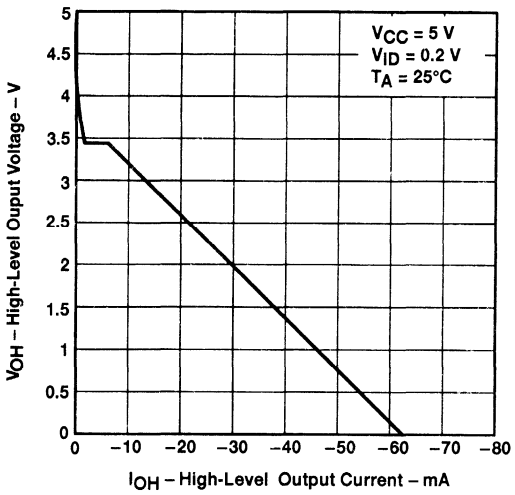


Figure 4

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

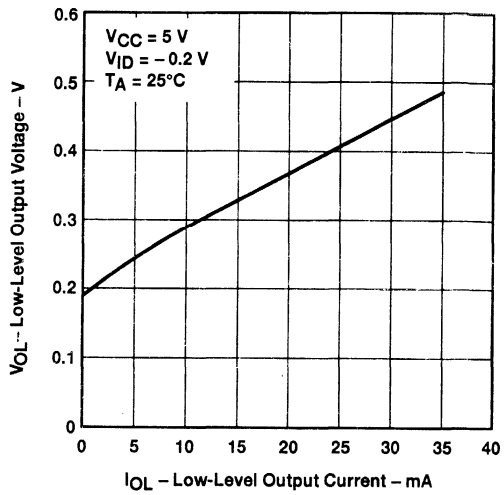


Figure 5

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

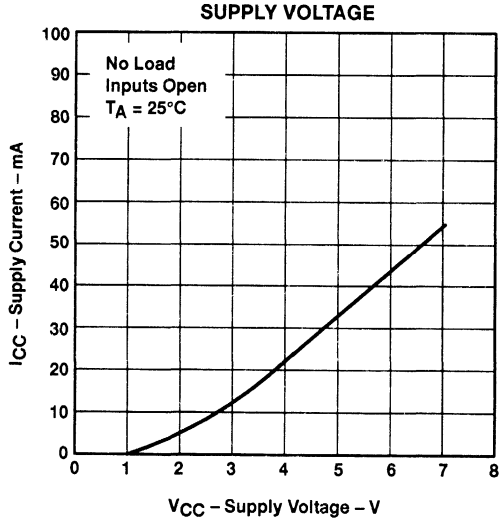


Figure 6

APPLICATION INFORMATION

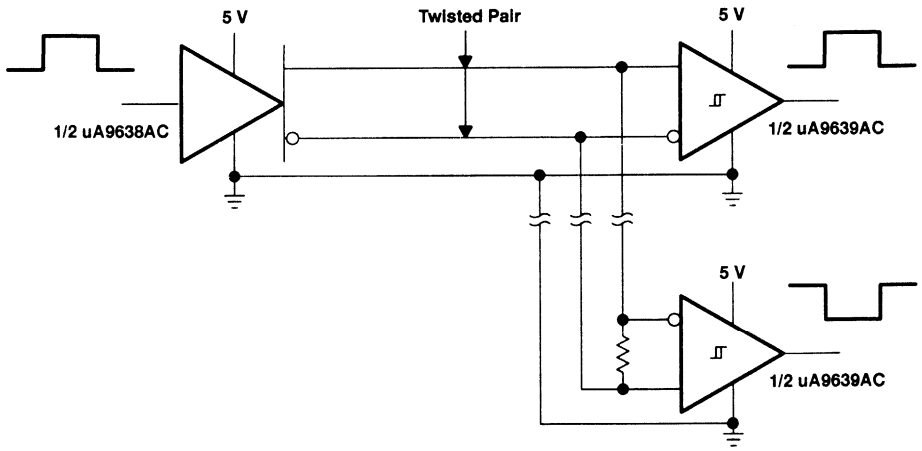
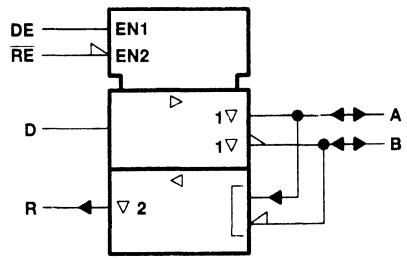


Figure 7. EIA/TIA-422-B System Applications

3 Product Previews

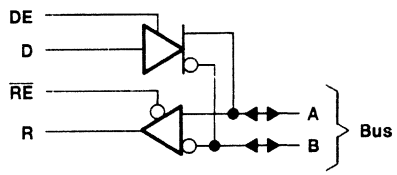
- **Bidirectional Transceiver w/Fail-Safe Receiver**
- **Meets or Exceeds the Requirements of ITU Recommendation V.11**
- **Electrically Compatible With ANSI Standards EIA/TIA-422-B and RS-485**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **3-State Driver and Receiver Outputs**
- **Individual Driver and Receiver Enables**
- **Wide Positive and Negative Input/Output Bus Voltage Ranges**
- **Driver Output Capability . . . ±60 mA Max**
- **Thermal Shutdown Protection**
- **Driver Positive and Negative Current Limiting**
- **Receiver Input Impedance . . . 12 kΩ Min**
- **Receiver Input Sensitivity . . . −300 mV/0 mV**
- **Operates From Single 5-V Supply**
- **Pin Compatible With SN75176A Footprint**

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



description

The SN75276 differential bus transceiver is a monolithic, integrated circuit designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and is electrically compatible with ANSI Standards EIA/TIA-422-B and RS-485, and meets ITU Recommendation V.11.

The fail-safe operation ensures a known level on the circuit output under bus fault conditions. The circuit provides a high-level output under floating-line, idle-line, open-circuit, and short-circuit bus conditions (see Function Tables).

Function Tables

DRIVER

INPUT D	ENABLE DE	OUTPUTS A	OUTPUTS B
H	H	H	L
L	H	L	H
X	L	Z	Z

RECEIVER

DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0$ V	L	H
−0.3 V < V_{ID} < 0 V	L	?
$V_{ID} \leq -0.3$	L	L
X	H	Z
Open	L	H

H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

PRODUCT PREVIEW

description (continued)

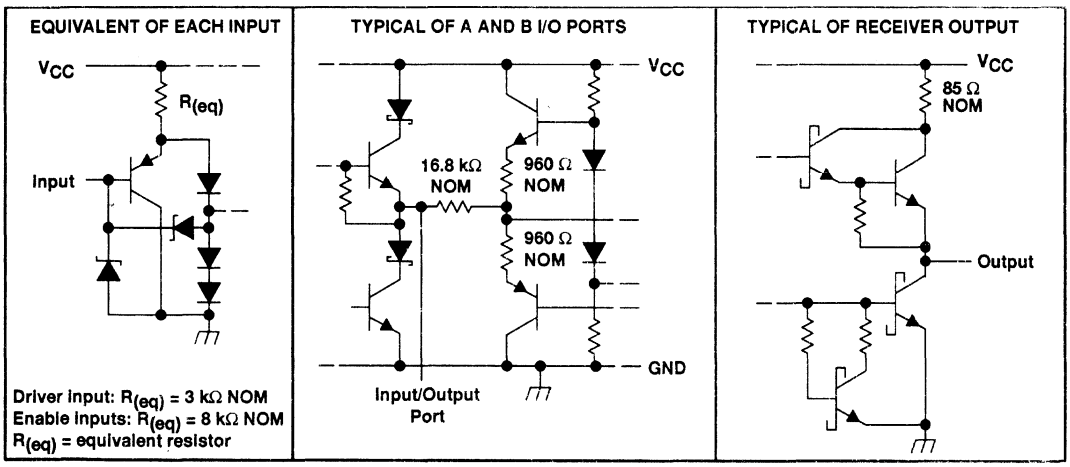
The SN75276 combines a 3-state, differential line driver and a differential input line receiver, both of which operate from a single, 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The driver is designed for up to 60 mA of sink or source current. The driver features positive- and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 kΩ.

The SN75276 can be used in transmission line applications employing the SN75172 and SN75174 quadruple differential line drivers and SN75173 and SN75175 quadruple differential line receivers.

SN75276 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



PRODUCT PREVIEW

SLLS216 – MAY 1995

- **Single-Chip Interface Solution for AppleTalk™ and LocalTalk™**
- **Designed to Operate Up To 1 Mbps In AppleTalk and LocalTalk**
- **Switched-Capacitor Voltage Converter Allows for Single 5-V Operation**
- **9-kV ESD Protection on Bus Terminals**
- **Combines Multiple Components into a Single Chip Solution**
- **LinBiCMOS™ Process Technology**

description

The SN75LBC775 is a low-power LinBiCMOS™ device that incorporates the drivers and receivers for an AppleTalk or a LocalTalk interface and a switched-capacitor voltage converter for a single 5-V supply operation. LocalTalk uses a hybrid of RS-422 with the transceiver connected to the network through a small isolation transformer. The AppleTalk mode provides point-to-point communications and uses the same differential driver and receiver as LocalTalk with the addition of a hybrid RS-423, single-ended handshake driver (HSK) and receiver. In the AppleTalk mode, the port connects directly to the receiver with no isolation transformer.

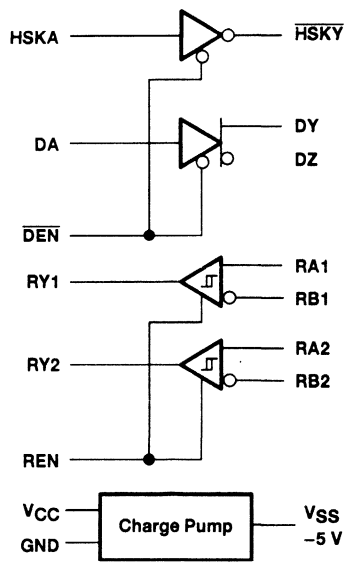
While the device power is turned off (V_{CC} = 0) or disabled in the LocalTalk mode, the outputs are in a high-impedance state. When the driver enable ($\overline{DEN}$) terminal is high, both the differential and serial driver outputs are in a high-impedance state.

The receiver output can be disabled and become a high impedance when the REN terminal is low.

A switched-capacitor voltage converter generates the negative voltage required from a single 5-V supply using two 22-µF capacitors. One capacitor is between the C+ and C– terminals and the second is between V_{SS} and ground.

The SN75LBC755 is characterized for operating over the temperature range of 0°C to 70°C.

functional diagram



PRODUCT PREVIEW

LocalTalk and AppleTalk are trademarks of Apple Computer, Inc.
LinBiCMOS is a trademark of Texas Instruments Incorporated.

DRIVER FUNCTION TABLE

INPUT		ENABLE	OUTPUT		
DA	HSKA	$\overline{DEN}$	A	B	$\overline{HSKY}$
H	X	L	H	L	X
L	X	L	L	H	X
X	H	L	X	X	L
X	L	L	X	X	H
OPEN	OPEN	L	H	L	L
X	X	H	Z	Z	Z
X	X	OPEN	Z	Z	Z

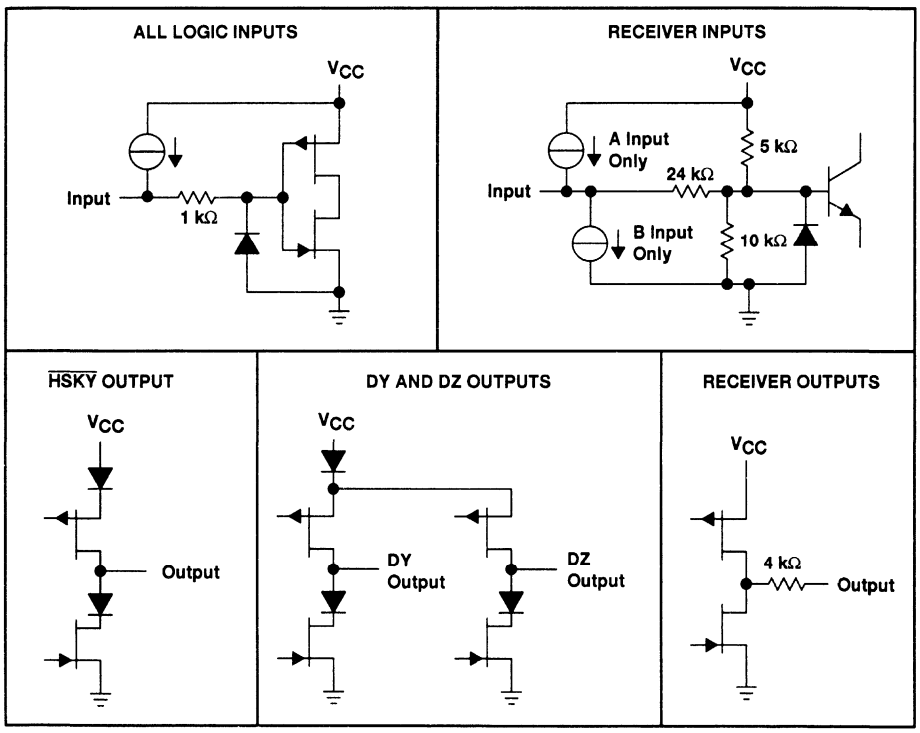
RECEIVER FUNCTION TABLE

INPUT		ENABLE	OUTPUT
RA	RB	$\overline{TEST}$	RY
H	L	H	H
L	H	H	L
OPEN		H	H
SHORT†		H	?
X		L	Z

† $-0.2\ V < V_{ID} < 0.2\ V$

H = high level, L = low level, X = irrelevant, ? = indeterminate, Z = high impedance (off)

schematics of inputs and outputs



PRODUCT PREVIEW

- **Provides Differential SCSI from Single-Ended Controller**
- **Designed to Operate at Fast-SCSI Speeds of 10 Million Data Transfer per Second**
- **Meets or Exceeds the Requirements of ANSI Standard EIA-485 and ISO-8482 Standards**
- **Packaged in Shrink Small-Outline Package with 25 mil Terminal Pitch**
- **Low Disabled Supply Current 22 mA Typ**
- **Thermal Shutdown Protection**
- **Positive- and Negative-Current Limiting**
- **Power-Up/Down Glitch Protection**

description

The SN75LBC970 SCSI differential converter-control is an adaptation of the industry's first nine-channel RS-485 transceiver, the SN75LBC976. When used in conjunction with one or more of its companion data transceiver(s), such as the SN75LBC971, the chip set provides the superior electrical performance of differential SCSI from a single-ended SCSI bus controller. A 16-bit, Fast-SCSI bus can be implemented with just three devices (two for data and one for control) in the space-efficient, 56-pin, shrink small-outline package (SSOP) and a few external components.

In a typical differential SCSI node, the SCSI controller provides the enables for each external RS-485 transceiver. This could require as many as 27 additional terminals for a 16-bit differential bus controller or relegate a 16-bit single-ended controller to only an 8-bit differential bus. Using the standard nine SCSI control signals, the SN75LBC970 control transceiver decodes the state of the bus and enables the SN75LBC971 data transceiver(s) to transmit the single-ended, SCSI input signals differentially to the cable or receive the differential cable signals and drive the single-ended outputs to the controller.

The single-ended, SCSI bus interface consists of CMOS bidirectional inputs and outputs. The drivers are rated at ±16 mA of output current. The receiver inputs are pulled high with approximately 4 mA to eliminate the need for external pullup resistors for the open-drain outputs of most single-ended, SCSI controllers. The single-ended side of the device is not intended to drive the SCSI bus directly.

The differential SCSI bus interface consists of bipolar bidirectional inputs and outputs that meet or exceed the requirements of EIA-485 and ISO 8482-1982/TIA TR30.2 referenced by the American National Standard of Information Systems (ANSI) X3.131-1994 Small Computer System Interface-2 (SCSI-2).

PRODUCT PREVIEW

PRODUCT PREVIEW

description (Continued)

The SN75LBC970 is characterized for operation over the temperature range of 0°C to 70°C.

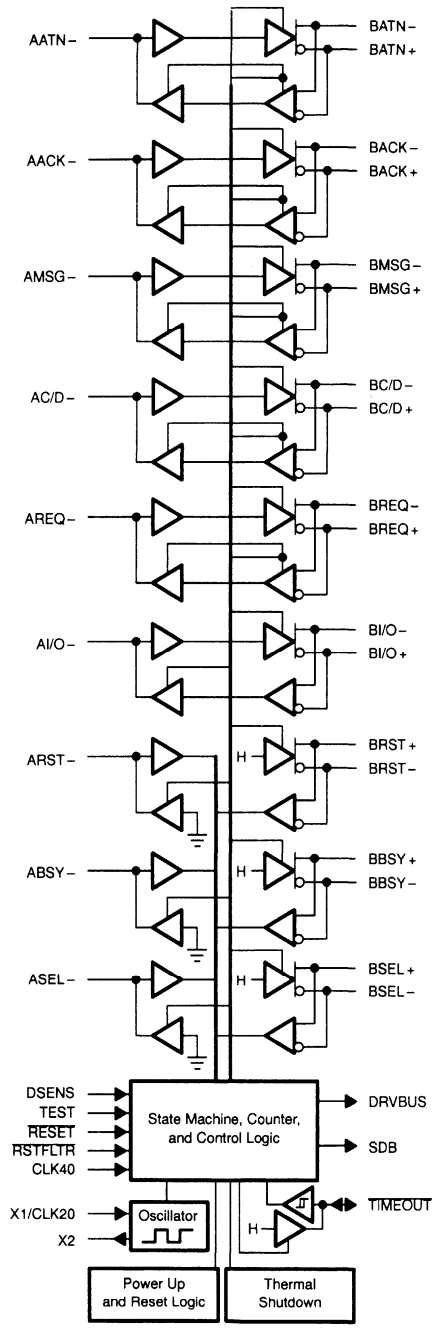
The SN75LBC970 consist of nine RS-485 differential transceivers, nine TTL of CMOS-level compatible transceivers, a state machine and control logic block, a 20-MHz crystal-controlled oscillator, a timer, a power up/down glitch protection circuit, and a thermal-shutdown protection circuit.

The single-ended or controller interface is designated as the A side and the differential port is the B side. Since the device uses the SCSI control signals to decode the state of the bus and data flow direction, the terminal assignments must be matched to the corresponding signal on the SCSI bus. The signal name followed by a a minus sign (–) indicates an active-low signal while a plus sign (+) indicates an active-high signal.

A reset function, which disables all outputs and clears internal latches, can be accomplished from two external inputs and two internally generated signals. $\overline{\text{RESET}}$ (Reset) and DESENS (differential sense) are available to external circuits for a bus reset or to disable all outputs should a single-ended cable be inadvertently connected to a differential connector. The power-up and thermal-shutdown, internally-generated signals have the same effect when the supply voltage is below 3.5 V or the junction temperature exceeds about 175°C.

The remainder of this data sheet contains descriptions of the SN75LBC970 input and output signals followed by the electrical characteristics. The parameter measurement information is followed by the theory of operation, a state flow chart, and a typical circuit in the application information section.

logic diagram (positive logic)



- **Provides Differential SCSI From Single-Ended Controller When Used With the SN75LBC970 Control Transceiver**
- **Designed to Operate at Fast-SCSI Speed of Ten Million Data Transfers per Second**
- **Meets or Exceeds the Requirements of EIA Standard RS-485 and ISO-8482 Standards**
- **Packaged in Shrink Small-Outline Package With 25-Mil Terminal Pitch**
- **Low Disabled-Supply Current 23 mA Typ**
- **Thermal Shutdown Protection**
- **Positive- and Negative-Current Limiting**
- **Power-Up/-Down Glitch Protection**

description

The SN75LBC971 SCSI Differential Converter-Data is an adaptation of the industry's first 9-channel RS-485 transceivers, the SN75LBC976. When used in conjunction with its companion control transceiver, the SN75LBC970, the chip set provides the superior electrical performance of differential SCSI from a single-ended SCSI bus or controller. A 16-bit SCSI bus can be implemented with just three devices (two data and one control) in the space efficient, 56-pin, shrink small-outline package (SSOP) and a few external components. An 8-bit SCSI bus requires only one data and one control transceiver.

In a typical differential SCSI node, the SCSI controller provides an enable for each external RS-485 transceiver channel. This could require as many as 27 extra terminals for a 16-bit differential bus controller or relegate a 16-bit, single-ended controller to only an 8-bit differential bus. Using the standard nine SCSI control signals, the SN75LBC970 control transceiver decodes the state of the bus and enables the SN75LBC971 data transceiver to transmit the single-ended SCSI input signals (A side) differentially to the cable or receive the differential cable signals (B side) and drive the single-ended outputs to the controller.

A reset function, which disables all outputs and clears internal latches, can be accomplished from two external inputs and two internally-generated signals. $\overline{\text{RESET}}$ (reset) and DSENS (differential sense) are available to external circuits for a bus reset or to disable all outputs should a single-ended cable be inadvertently connected to a differential connector. A power-up and thermal-shutdown internally-generated signals have the same effect when the supply voltage is below approximately 3.5-V or the junction temperature exceeds 175°C.

The SCSI, differential, converter-data chip operates in two modes depending on the state of the DRVBUS input. With DRVBUS low, a bidirectional latch circuit sets the direction of data transfer. Each data bit has its own latch, and each bit's direction is independent of all other bits. When both the single-ended and differential sides are not asserted, the latch disables both A and B side output drivers. When the input to either side is asserted, the latch enables the opposite side's driver and sets data flow from the asserted input to the opposite side of the

PRODUCT PREVIEW

description (continued)

device. When the input deasserts, the latch maintains the direction until the receiver on the enabled driver detects a deassertion. The latch then returns to the initial state. No parity checking is done by this device; the parity signal passes through the device like the other data signals do.

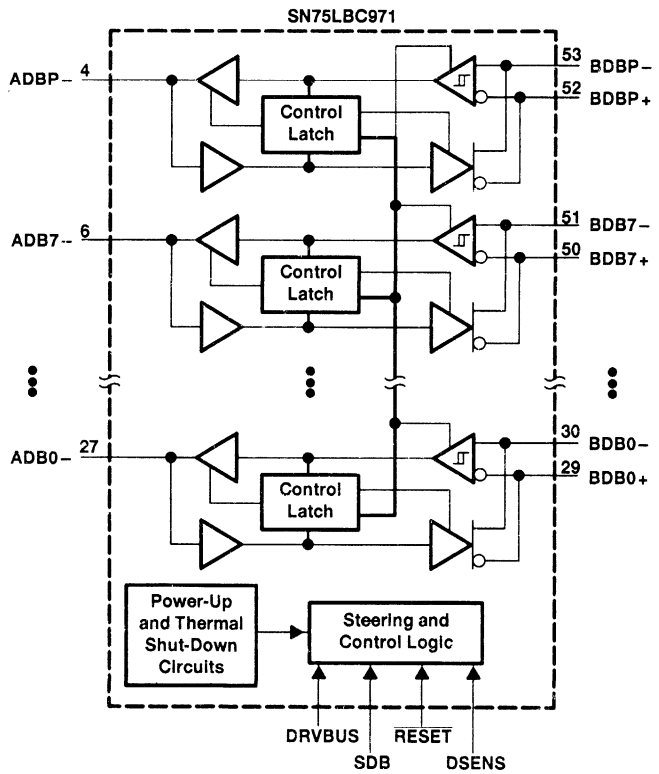
When DRVBUS is high, direction is determined by the SDB signal. However, a change in SDB does not always immediately change the direction. When DRVBUS first asserts, the direction indicated by SDB is latched and takes effect immediately. When SDB changes while DRVBUS is high, the drivers that were on immediately turn off. However, the other driver set does not turn on until the receivers sense a deasserted state on all nine data lines. This is to prevent the active drivers from turning on until all other drivers are off and the terminators pull the lines to a deasserted state.

The single-ended SCSI bus interface consists of CMOS, bidirectional inputs and outputs. The drivers are rated to ±16 mA of output current. The receiver inputs are pulled high with approximately 4-mA to eliminate the need for external pullup resistors for the open-drain outputs of most single-ended SCSI controllers. The single-ended side of the device is not intended to drive the SCSI bus directly.

The differential SCSI bus interface consists of bipolar, bidirectional inputs and outputs that meet or exceed the requirements of EIA-485 and ISO 8482-192/TIA TR30.2 referenced by American National Standard of Information Systems (ANSI) X3.131-1994 Small Computer System Interface-2 (SCSI-2) and the Proposed SCSI-3 Parallel Interface (SPI)-ANSI X3T9.2/91-010.

The SN85LBC971 is characterized for operation over the temperature range of 0°C to 70°C.

functional block diagram



PRODUCT PREVIEW

SGLS091 – JUNE 1995

- **Nine Differential Channels for the Data and Control Paths of the Differential Small Computer Systems Interface (SCSI) and Intelligent Peripheral Interface (IPI-2)**
- **Meets or Exceeds the Requirements of ANSI Standard RS-485 and ISO 8482:1987(E)**
- **Designed to Operate at 10 Million Transfers Per Second**
- **Low Disabled Supply Current 1.4 mA Typical**
- **Thermal Shutdown Protection**
- **Power-Up/Power-Down Glitch Protection**
- **Positive and Negative Output Current Limiting**
- **Open-Circuit Fail-Safe Receiver Design**

description

The SN55LBC976 is a nine-channel differential transceiver based on the SN55LBC176 LinASIC™ cell. Use of TI's LinBiCMOS™† process technology allows the power reduction necessary to integrate nine differential transceivers. On-chip enabling logic makes this device applicable for the data path (eight data bits plus parity) and the control path (nine bits) for both the Small Computer Systems Interface (SCSI) and the Intelligent Peripheral Interface (IPI-2) standard data interfaces.

The switching speed and testing capabilities of the SN55LBC976 are sufficient to transfer data over the data bus at 10 million transfers per second. Each of the nine channels conforms to the requirements of the ANSI RS-485 and ISO 8482:1987(E) standards referenced by ANSI X3.129-1986 (IPI), ANSI X3.131-1993 (SCSI-2), and the proposed SCSI-3 standards.

The SN55LBC976 is characterized for operation from −55°C to 125°C.

PRODUCT PREVIEW

† Patent pending

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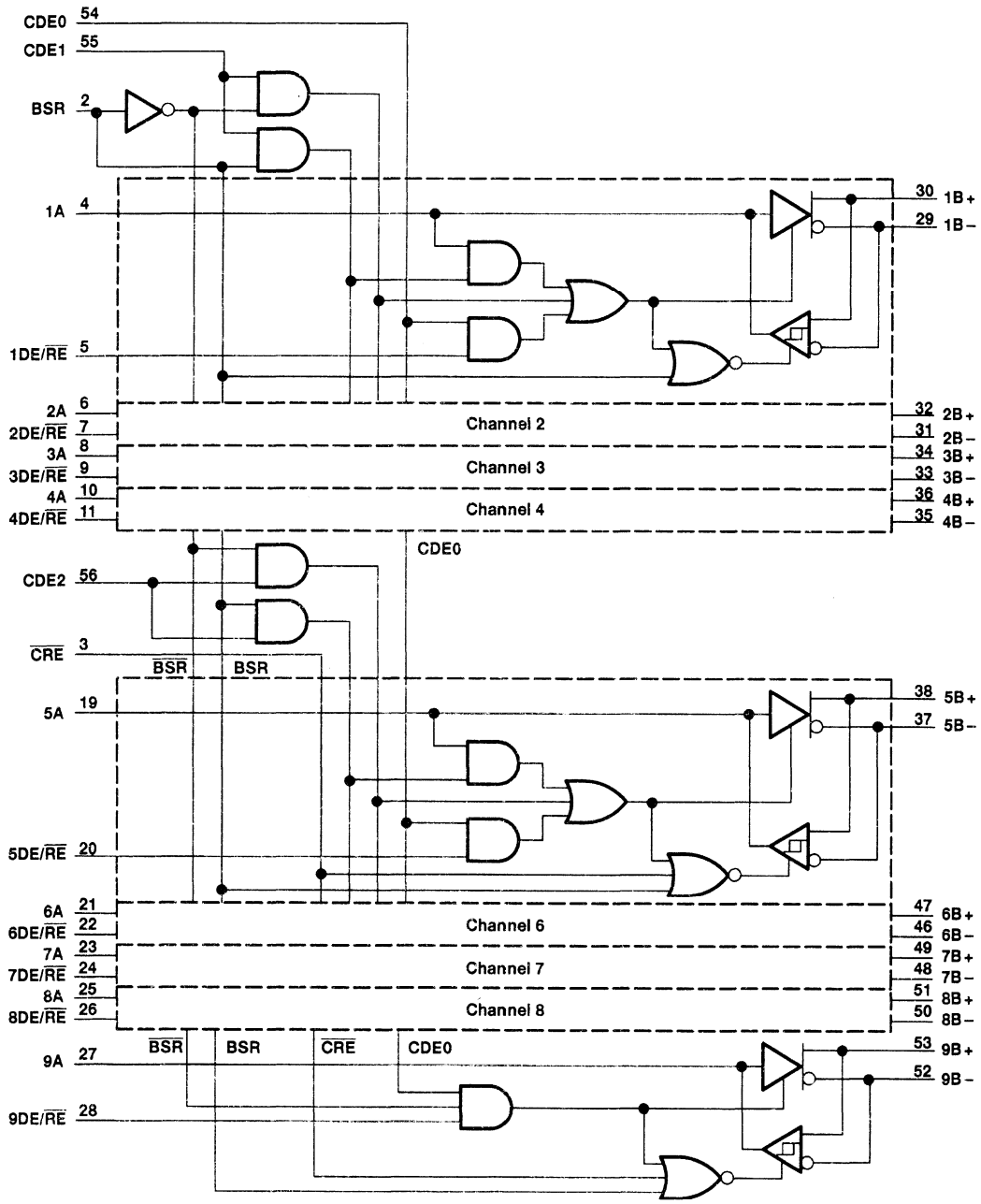
logic diagram (positive logic)†



† For additional logic diagrams, see Application Information, Table 1, and Figures 7 through 44.

PRODUCT PREVIEW

4 Applications

Data Transmission Applications

Contents

Contents (continued)

List of Illustrations

List of Tables

1 Introduction

1.1 Data Transmission

Data transmission as part of TI's linear products portfolio is concerned with the standards involving transmitting data at relatively high speeds down long line lengths, the considerations for which are primarily of an analog more than a digital nature. Likewise the design of data transmission ICs requires experienced analog engineers to implement functions such as slew rate limiting, receiver filtering, and common-mode protection.

In this chapter we concentrate on two very popular transmission standards, RS-232 or as it is now known EIA/TIA-232-E, and the multipoint, half-duplex RS-485 standard. The last section covers the physical layer of the increasingly popular Small Computer Systems Interface (SCSI) Standard.

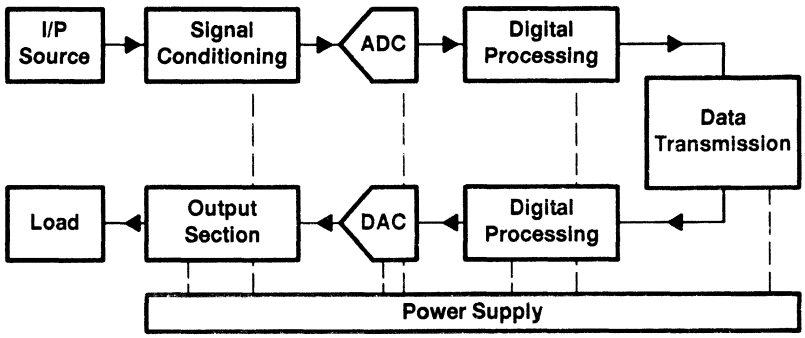


Figure 1–1. Data Transmission

1.1.1 The Need for Transmission Standards

Data transmission standards evolved for two main reasons 1) From the need to transmit data reliably over long distances, and 2) to provide a standard interface to facilitate communication between equipment from different suppliers. Although TTL/logic signal levels and products can be used, they generally lack the power handling capabilities, robustness, and noise margins required for reliable transmission. Indeed for backplane equipment, TTL is no longer specified for the newer high-speed standards (e.g., Futurebus+, which uses BTL transceivers). In general the standards concerned with transmitting data over long distances incorporate wider voltage swings, increased robustness, and higher power outputs than can be delivered using conventional logic products. Similarly, the submicron technologies used in the fabrication of today's logic devices cannot provide the power handling and robustness necessary for successful long distance transmission.

1.1.2 Specialist Technologies

This leads to the need for specialist ICs and technologies to meet the exacting requirements of these transmission standards. The traditional technological answer has been to utilize the inherent robustness afforded by bipolar technologies; however, the additional need for low power consumption and high levels of integration no longer makes this attractive. Semiconductor (SC) manufacturers are now having to develop their technologies to accommodate these requirements. TI has introduced its proprietary LinBiCMOS™ technology combining the robustness of bipolar together with the power consumption and integration afforded by CMOS. Other manufacturers are using pure CMOS and integrating Schottky diodes to the same end. The results of these specialist technologies are very specialized and reliable products that are able to withstand the harsh environment unique to data transmission.

Texas Instruments has been a leading supplier of data transmission products for many years and is continually providing innovation for new fields. Although the following sections are limited to the more

LinBiCMOS is a trademark of Texas Instruments Incorporated.

common interface standards, TI is actively involved in many new emerging standards and markets. For example Futurebus+, a backplane standard with virtually no ceiling on data rate, the high speed serial data link evolving from the P1394 committee and multiplex wiring systems such as ABUS, CAN and VAN. The reader is advised to contact a TI representative for information on these product areas.

With the considerable expertise in design, product definition, and a range of technologies, Texas Instruments is the ideal choice for supplying your data transmission product requirements.

1.1.3 About This Section

This section is split into four distinct sections each of which provides a practical rather than theoretical approach in an attempt to give you an insight into three popular data transmission standards, EIA/TIA-232 (RS-232), RS-485 and the SCSI standard. The section is split as follows:

1. Introduction: This provides an overview of the various factors that affect any data transmission system. Under discussion is the line length versus data rate tradeoff, noise sources, correct line termination and network topology, in addition to explaining the use of eye patterns as a tool to measure transmission quality (see Figure 1–2).

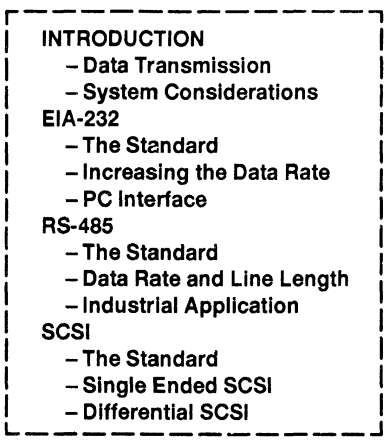


Figure 1–2. Data Transmission Agenda

2. EIA/TIA-232-E (RS-232): This section is a discussion of the standard with particular attention paid to the changes made in the E revision. Also covered is the use of RS-232 at higher data rates up to 116 kbps (kilo bits per second) and an application focus on the popular DB9 PC interface. The generic RS-232 standard is referred to in this book as RS-232, where a parameter is unique to a specific revision the EIA-232 reference is used.

3. EIA RS-485: This section is an overview of the RS-485 specification (see Figure 1–3).

4. EIA/TIA-422-B: This section is an overview of the EIA/TIA-422-B standard (see Figure 1–3).

5. SCSI: In
this section we consider the physical layer of this standard that concern both single-ended and differential transmission. For single ended transmission we look specifically at optimizing the line termination to achieve maximum transmission rate over the 6 meter distance as specified in the standard. The differential SCSI system increases the line length to 25 meters and uses the RS-485 standard to achieve this. We also look at TI's new nine channel RS-485 transceiver that minimizes the problems caused by the 18-line wide bus as defined by the standard (see Figure 1–3).

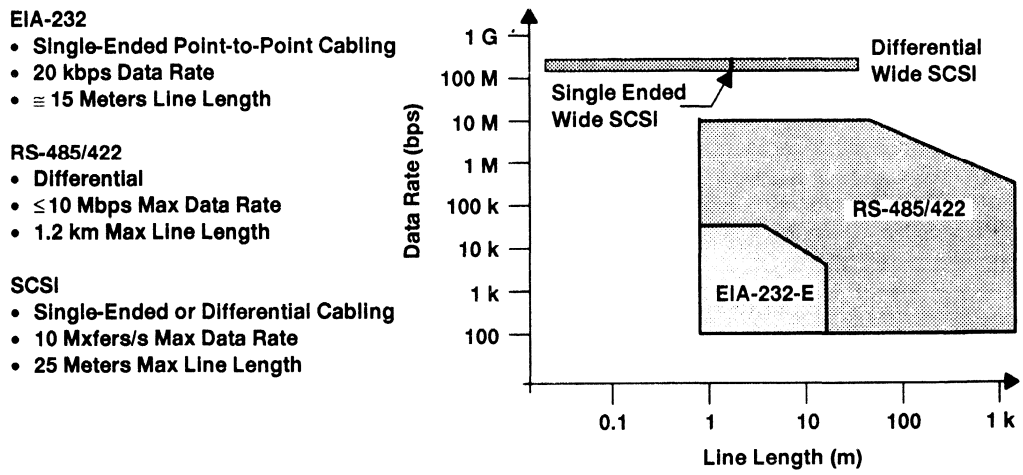


Figure 1–3. Interface Standards

1.2 Overview of the Interface Standards

In Figure 1–3 we can see the relationship of each transmission standard when comparing data rate and line length.

1.2.1 EIA/TIA-232-E

EIA/TIA-232-E (commonly referred to as RS-232) or Recommended Standard 232 is defined in the American National Standard Institution (ANSI) specification as the interface between data terminal equipment and data circuit-terminating equipment employing serial binary data interchange. The standard employs a single-ended serial-transmission scheme and outlines the set of rules for exchanging data between computer equipment, originally this being a computer terminal, which is classified as a type of data terminal equipment (DTE), and a modem, which is a type of data communication equipment (DCE). The standard has evolved over the years with the latest E revision released in July 1991. The standard is now known as EIA/TIA-232-E, with EIA standing for the Electronic Industries Association and TIA for the Telecommunications Industry Association.

As with previous revisions of the standard the maximum data rate is defined as 20 kbits per second (kbps) although there are now a number of software applications that push this data rate up to 116 kbps, well outside the standard. The C revision defined the maximum line length as 15 meters; however, this failed to comprehend the type of cable used and, consequently, the load capacitance on the line driver. Both the D and E revisions addressed this by more correctly defining the line length in terms of load capacitance. The maximum load capacitance is specified as 2500 pF, which translates into using standard cables between 15 and 20 meters long. Line length and data rate are limited as the standard employs single-ended communication that is prone to external factors. For longer line lengths and higher data rates a differential balanced line communication link is essential.

1.2.2 EIA/TIA-422-B and RS-485

RS-485 is primarily an upgrade to the RS-422 standard utilizing similar signal levels but facilitating half duplex, multipoint communication. The standard is less complex than the RS-232 standard as it only specifies the electrical layer of the transmission scheme. Hardware such as the connector is left to the user to define. The standard specifies a balanced transmission line whose maximum line length is undefined but is nominally 1.2 km for 24-AWG cable based on 6-dB signal attenuation. The maximum data rate is also undefined but is specified by the relationship of signal rise time to bit time, which is influenced by the line driver, the line length, and the line loading. In the majority of applications it is the line length that is the limiting factor on data rate due to signal dispersion. This is discussed in later sections.

1.2.3 Small Computer Systems Interface (SCSI)

SCSI is an industry-standard interface, defined by the ANSI, for the interchange of data between a computer and the computer peripherals. Standard SCSI is a byte-wide parallel interface for high-speed data transfer over relatively short distances. The SCSI bus is bidirectional and is terminated at both ends of the cable to reduce reflections. For the single-ended interface, the standard specifies a maximum line length of 6 meters. The maximum data rate is 10 million transfers per second (Mxfers/s). For longer line length applications up to 25 meters, the SCSI standard uses the RS-485 standard as the physical layer. A further development of SCSI is Wide SCSI, which increases the data bus to 16-bits wide. Using the 10 Mxfers/s interface, the bit rate increases to 160 Mbps.

1.2.4 Summary of EIA Interface Standards

Table 1–1. Summary of EIA Interface Standards

PARAMETER		RS-232	RS-423	RS-422	RS-485
Mode Operation		Single-Ended	Single-Ended	Differential	Differential
Number of Drivers and Receivers		1 Driver 1 Receiver	1 Driver 10 Receivers	1 Driver 10 Receivers	32 Drivers 32 Receivers
Maximum Cable Length (m)		15	1200	1200	1200
Maximum Data Rate (bps)		20 k	100 k	10 M	10 M
Maximum Common-Mode Voltage (V)		±3	±3	±7	12 to −7
Minimum Driver Output Levels (V)	Loaded	±5	±3.6	±2	±1.5
	Unloaded	±15	±6	±6	±6
Drive Load (Ω)		3 k to 7 k	450 (Min)	100 (Min)	60 (Min)
Driver Slew Rate		30 V/μs (Max)	NA	NA	NA
Driver-Output Short-Circuit Current Limit (mA)		n/a	150 to GND	150 to GND	150 to GND 250 to −7 or 12 V
Minimum Receiver Input Resistance (kΩ)		3 to 7	4	4	12
Receiver Sensitivity		±3 V	±200 mV	±200 mV	±200 mV

1.3 System Influences

Noise, distortion, and attenuation are always present in data transmission systems and strictly limit performance (see Figure 1–4). We consider each one of these in turn although there is some overlap (i.e., noise can cause distortion).

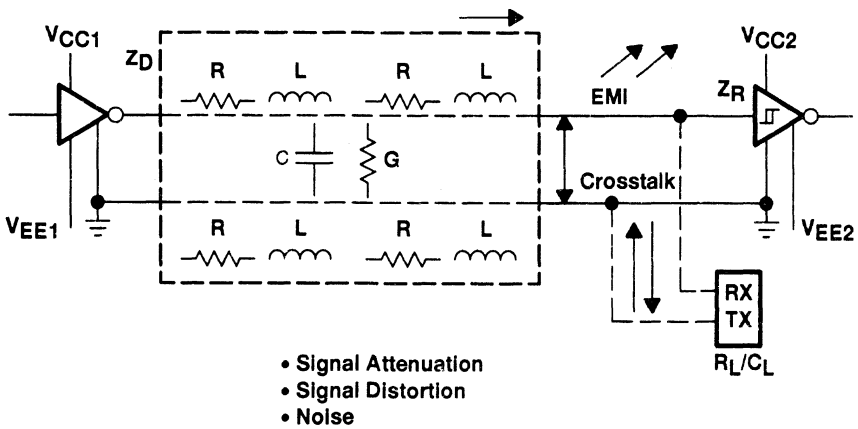


Figure 1–4. System Influences

1.3.1 Signal Attenuation

Any data transmission over wire experiences losses and distortion due to distributed constants present along the cable. The distributed constants are series inductance, shunt capacitance, series resistance and shunt conductance. Attenuation of the signal in a cable is affected by each of these components. The series resistance, R, is frequency dependent and is a result of the dc resistance of the cable and the skin effect. Skin effect is a term that refers to the tendency of electrons to travel to the surface of a conductor at higher frequencies, thereby reducing the overall cross-sectional area and increasing the resistance. The series inductance, L, represents the opposition to change in current levels caused by the collapsing and expanding magnetic fields created due to fluctuating current levels. The shunt capacitance, C, is created by the two conductors in close proximity and separated by a dielectric. As the signal frequency increases the capacitive reactance decreases, consequently reducing the opposition to current flow. The final component, shunt transconductance or G, is a function of the dielectric loss of the insulation around each conductor, which allows some leakage current to pass between conductors. In modern dielectrics this is often assumed to be negligible.

The overall effect of these distributed constants is called the characteristic impedance of the line, Z_O, and is expressed as:

$$Z_O = \sqrt{\frac{R + j2\pi fL}{G + j2\pi fC}}$$

Where:

L is in henries/unit length
R is in ohms/unit length
C is in farads/unit length
G is on mhos/unit length

The current/voltage relationship of an incident wave travelling down a transmission line in the direction of the load is determined by this equation. Equally a reflected wave travelling from the direction of the load is also dependent on this relationship. We revisit this equation when we discuss transmission line termination in section 1.5. The signal velocity along the transmission line and the attenuation depends upon the propagation constant γ of the line. The propagation constant, when separated into its real and imaginary parts, is symbolized by $\alpha + j\beta$ where α is known as the attenuation constant and β as the phase constant. α determines the rate of attenuation and has units of nepers per unit length, and β determines the phase velocity, where:

Phase velocity,

$$Vp = \frac{\omega}{\beta}$$

Where ω is the angular frequency.

Additionally, the propagation constant,

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)\ (G + j\omega C)}$$

In practice the attenuation of a particular cable can be determined from manufacturers' data where a curve of bit rate or frequency is plotted against attenuation, usually quoted per 100 feet or 30 meters. The attenuation constant, β, can be converted to dBs by multiplying it by 8.686.

The maximum attenuation allowable depends on the system configuration but a figure of 6 dBV maximum is a good guide. Actual curves are discussed later in the Section 3.

1.3.2 Signal Distortion

One of the primary causes of signal distortion is the effect known as frequency dispersion. As discussed in subsection 1.3.1, phase velocity and attenuation are both frequency dependent and their effect is to distort

and delay the signal pulse. The high-frequency components contained in the leading and lagging edges of a pulse experience minimum delay but experience maximum attenuation. The pulse top and low-frequency components are subjected to increased delays. The result is that various parts of the pulse arrive at the receiving end at different times and at differing levels causing distortion of the original signal. It follows that the longer the line length is the more the bit rate must be reduced. In many transmission systems it is this factor alone that determines the maximum signalling rate.

Once again cable manufacturers sometimes specify a bit rate versus line length curve but a better way to check signal distortion of your system is by the use of eye patterns or eye diagrams. Indeed, cable manufacturers generate their bit rate/distance curves using eye pattern measurements. Eye patterns allow you to visibly see and measure signal distortion as a function of data rate. See later sections on how to implement eye patterns.

1.3.3 Noise

Noise is generated from a variety of sources and can strongly influence how you implement your data transmission system. All extraneous signals appearing at the receiving end of the transmission circuit that are not due to the input signal are considered as noise. The two most likely sources of noise that affects data transmission systems in the context of this section are common-mode voltages and cross-talk. We discuss both these types of noise and how they relate to the type of transmission system in Section 1.6.

1.4 Eye Patterns

To determine the effects of signal distortion, noise, and signal attenuation, on intersymbol interference (ISI) in a data transmission system, the eye pattern is used. ISI is the effect of neighboring pulses in a pulse train spilling over into adjacent pulses and forces a reduction in the allowable permitted pulse rate for a given line length in order to maintain adequate distinction between adjacent pulses. The eye pattern is displayed on an oscilloscope with the term "eye" coming from the appearance of the trace on the CRT.

1.4.1 Setting Up the Eye Pattern

The eye pattern is obtained by applying a random nonreturn zero (NRZ) code down the transmission line under test. This represents all possible pulse combinations. The signal at the receiving end of the line is connected to the vertical amplifier of an oscilloscope, with the scope triggered using the synchronization clock to the NRZ code generator on a separate trace (see Figure 1–5).

Formation of Eye Pattern

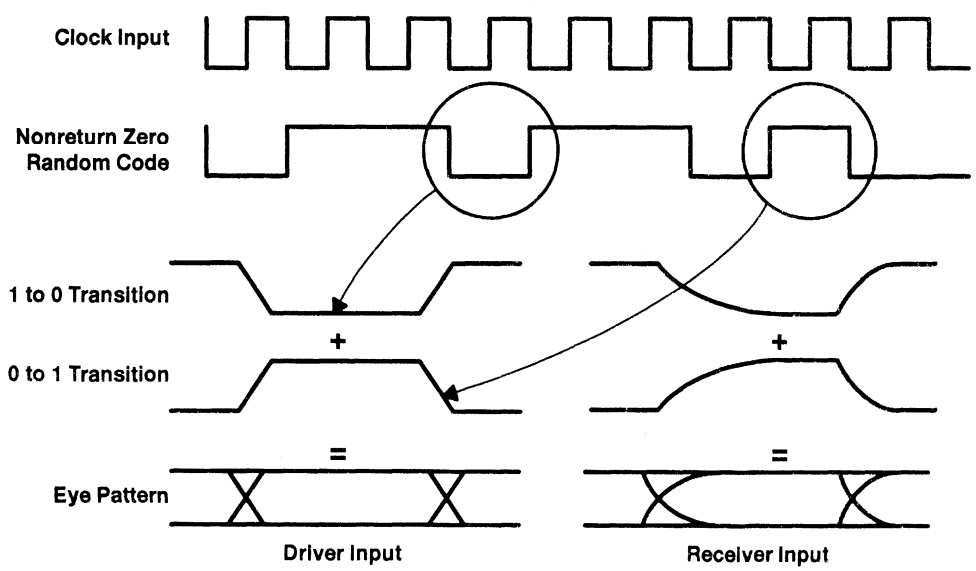


Figure 1–5. Signal Distortion Using Eye Patterns

Over any one unit interval the random code generator should produce a combination of signals. The resulting signals can then be viewed on the oscilloscope over a one unit interval, each unit interval should resemble an eye similar to Figure 1–8. For differential transmission, both signals at the end of the transmission line should be applied to separate amplifiers on the oscilloscope and then summed using the summation facility on the oscilloscope.

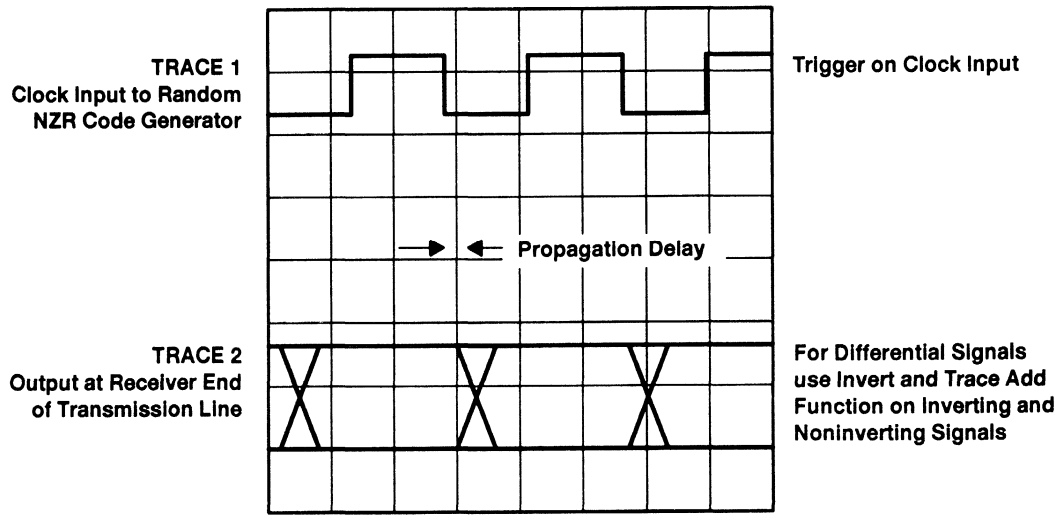


Figure 1–6. Eye Pattern Oscilloscope Trace

Figure 1–7 shows a circuit that generates the NRZ code. In this case we used it to test the RS-485 SN75176-type transceiver.

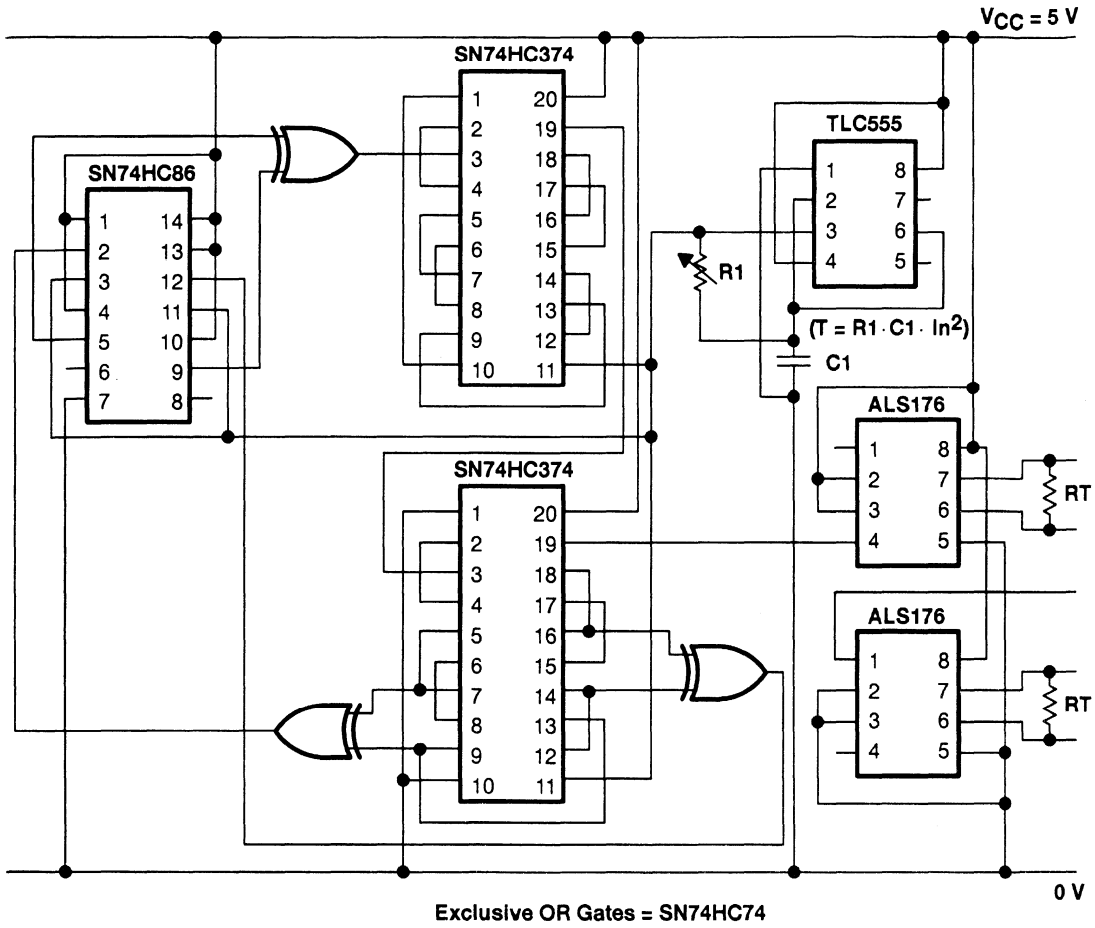
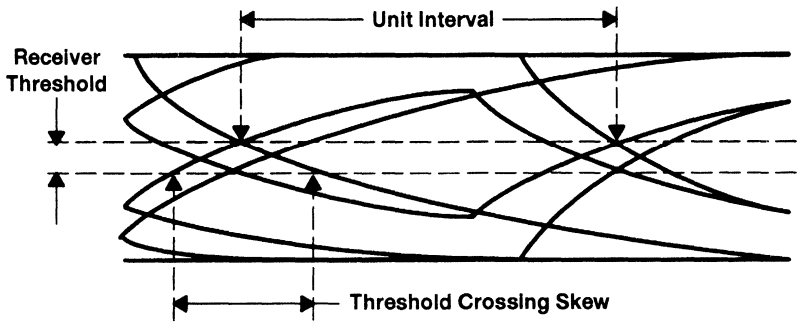


Figure 1–7. NRZ Random Code Generator

1.4.2 Taking Measurements from Eye Patterns

Before considering actual measurements the first key indicator on the performance of the transmission system can be seen by simply looking at the eye pattern. The openness of the eye is an indication of the quality of the transmitted signal and is an indication of the noise and distortion tolerance of the system.

For actual measurements the decision points of the transceiver should be superimposed upon the eye pattern. The vertical distance between the decision points and the signal trace is an approximate indication of the noise margin of the system. The horizontal appearance of the eye can be used to determine the maximum jitter tolerance of the system. A good guide, and one that is used by cable manufacturers to determine data rate versus line length curves, is to design with no more than 5% jitter. Where % jitter is defined as the ratio of threshold crossing skew to unit interval as shown in Figure 1–8. Jitter is caused by a number of factors including signal frequency, noise, and cross-talk. Noise frequency can modulate the transmitted signal, for example 50-Hz hum or from other low-frequency sources. It should also be noted at this point the effect of threshold misalignment that can cause severe problems with the received signal, reducing the detected pulse width considerably.



$$\% \text{ Jitter} = \frac{\text{Threshold Crossing Skew}}{\text{Unit Interval}} \times 100\%$$

NOTE A: Design with no more than 5% jitter

Figure 1–8. Measuring Signal Transmission Quality

1.5 Line Termination

The behavior of the transmitted signal and the integrity of the data at the receiving end depends upon the data rate and line length of the cable. There are two behavioral models of a transmission cable:

- Lumped parameter model (short wire)
- Distributed parameter model (transmission line)

As discussed in subsection 1.3.1 the distributed parameter model represents the connecting circuit in terms of distributed parameters (inductance, capacitance, resistance, conductance), rather than as an equivalent lumped load on the line. The transmission line can be considered in terms of an infinite number of small filter sections and, as a result, the transmission line is said to have a characteristic impedance, Z_O. Z_O is independent of distance along the line and represents the voltage and current relationship for an incident wave at any point as it travels along the line.

1.5.1 Transmission Line Test (Classifying as a Lumped or Distributed Parameter Model)

All cables can be thought of as transmission lines; but the term transmission line is used with differing meanings.

Consider a signal propagating down a simple data link comprising two wires. When the signal starts to change at the transmitter output the effect of this change is eventually seen at the other end of the line. A reflection of the signal occurs, which eventually returns back to the transmitter terminals.

If this happens before the original transmitted signal has risen to its peak value then the line is normally treated as a lumped parameter system rather than as a true transmission line. This is because the line itself does not greatly influence the performance of the system.

A general rule of thumb for determining if a system should be treated as a true transmission line can be formulated. If the transition (rise or fall) time, t_t, of the signal is much less than the round trip propagation delay, $2t_{pd}$, of the signal from transmitter to receiver and back to transmitter, then the cable can be treated as a transmission line and not as a lumped parameter model. A better model is given in Figure 1–9 where a safety margin is built in to the propagation delay/rise time relationship.

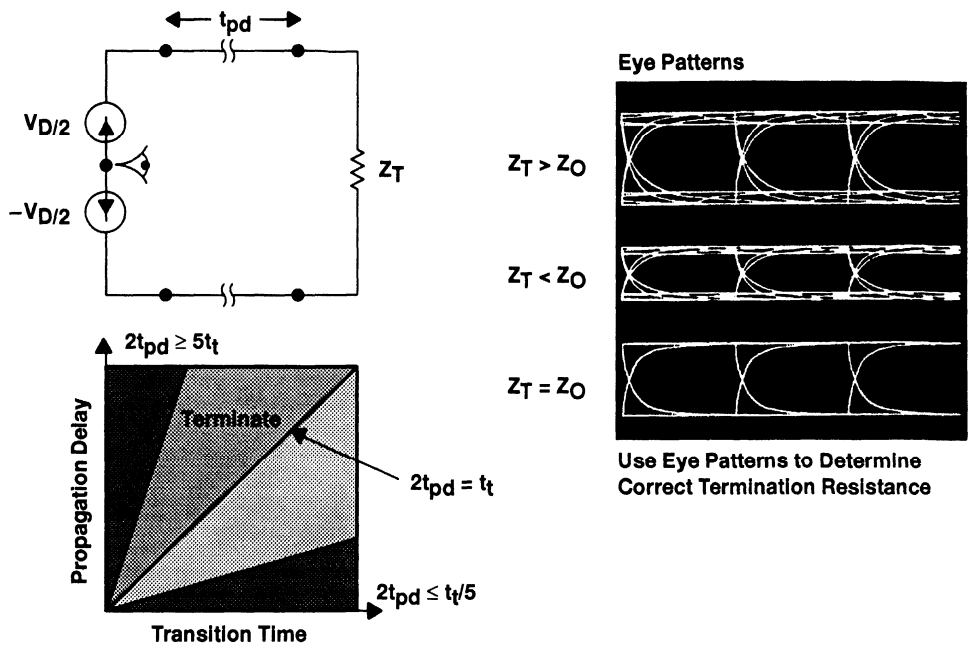


Figure 1–9. To Terminate or Not to Terminate?

1.5.2 Transmission Line Considerations and Effects

When the cable is operating like a transmission line, extra loads in the form of transmitters and receivers can be added, providing that they do not cause too great a shunting effect on the line. These extra loads, if they are evenly distributed along the line, can be treated as an extra distributed capacitance along the line adding to the effect of the line capacitance and inductance. This extra load decreases the line impedance and reduces the speed of the signal along the line.

In the case of the lumped-parameter model, the line represents a pure fixed load to the transmitter device. For example, the capacitance of the line is modelled as a fixed value that effectively limits the output voltage slew rate of the transmitter, assuming it can supply a finite amount of current to the line.

1.5.3 Transmission Line Reflections

Consider a driver circuit driving the line. When the driver output voltage changes state, the driver appears to see the effective characteristic impedance of the line, Z_O. This causes the voltage at the output of the driver circuit to be reduced as a result of the potential divider action formed by Z_O and the driver circuit output impedance, Z_D.

At any point along the line the ideal source impedance appears as Z_O and the ideal load impedance also appears as Z_O. This gives the impression that the line is being driven by a voltage source of twice the magnitude of the line voltage.

When the signal reaches the receiving end of the line it meets a terminating impedance equal to the impedance (Z_O) of the line that it is already travelling on. It interprets this as a continuation of the line. The voltage on the line is not altered and the current flowing along the line flows through the termination resistor and back to the driver via either ground or the other line in the system. Operation of the circuit as just described would result in optimum data transmission efficiency with little or no signal reflections. However, circuit operation in the real world is not always so perfect.

If the termination impedance is dissimilar to the characteristic impedance of the line itself, the voltage at the termination point is altered. The voltage at the termination point is dependent of the relative size of the

termination impedance to the line impedance. If the termination impedance is higher than the line impedance, the line voltage increases causing a positive voltage reflection of the signal. When the termination impedance is lower than the line impedance, the line voltage decreases leading to a negative reflection. The same effect occurs at the driver output terminals due to impedance mismatches between driver and line.

Reflections at each end of the line eventually settle and leave a constant dc voltage on the line. The value of this voltage is equal to the ideal open circuit output voltage multiplied by the termination impedance divided by the sum of the driver output impedance and termination impedance.

Reflections as described can cause problems when driving lines at high frequencies. False receiver triggering can occur and repeated signal reflections causes signal wave distortion.

1.6 Noise Influences

There are two main classifications of transmission schemes, single ended or differential. Each are affected by noise influences in differing ways – the next two sections describe each transmission scheme paying particular attention to the affects of noise. Figure 1–10 details both types of transmission scheme.

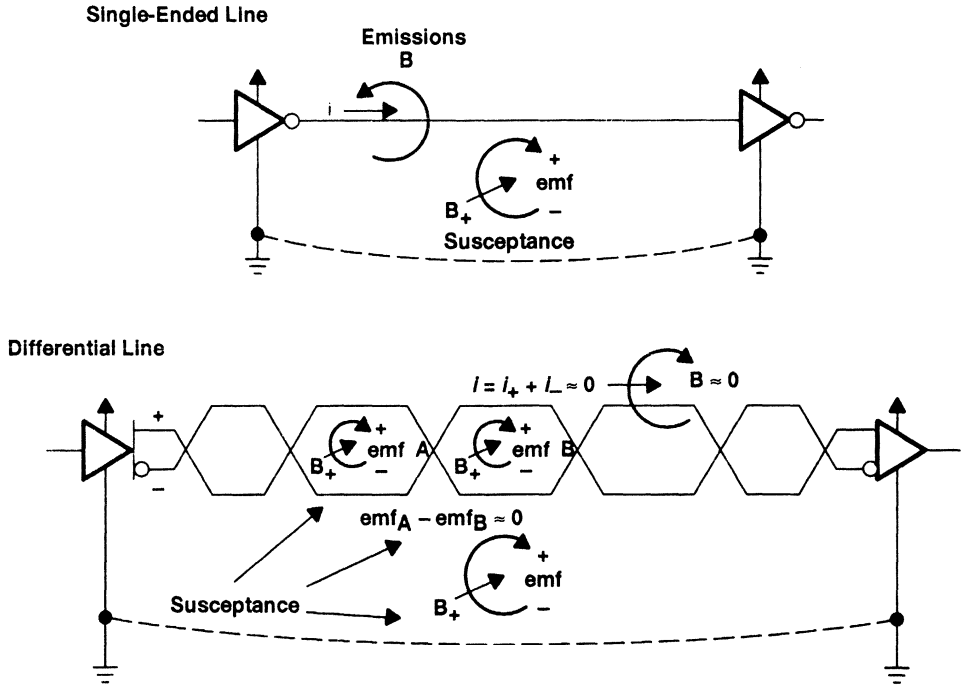


Figure 1–10. Noise Influences

1.6.1 Single-Ended Line Considerations

Single-ended data transmission systems consist of a signal line on which data is sent down, and a ground line through which the current returns. A direct result of this is that the ground line forms part of the transmission line, which can be of benefit in some circumstances but not in others.

One of the major benefits, and most obvious, is that a single-ended system is the lowest cost solution in terms of cabling costs. In general terms it requires only half the cable of a differential system. It is also relatively simple to install and operate.

The main disadvantage of the single-ended solution is its noise couping. Because the ground wire forms part of the system, any transient voltage or shifts in voltage potential can be induced (from nearby

high-frequency logic or high-current power circuits), leading to signal degradation ultimately leading to false receiver triggering. For example, a shift in the ground potential at the receiver end of the system can lead to an apparent change in the input switching threshold of the receiver device, thus increasing susceptibility to noise.

Crosstalk is also a major concern especially at high frequencies. Crosstalk is generated from both capacitive and inductive coupling. Capacitive coupling tends to be more severe at higher signal frequencies as capacitive reactance decreases. The impedance and termination of the coupled line determines whether the electric or the magnetic coupling is dominant. If the impedance of the line is high the capacitive pickup is large. Alternatively, if the line impedance is low, the series impedance as seen by the induced voltage is low, allowing large induced currents to flow.

These problems normally limit the distance and speed of reliable operation for a single-ended link.

Crosstalk can be reduced by:

- Limiting the slew rate of signals so they do not cause crosstalk to be induced onto other lines
- Limiting the line length
- Shielding the signal conductor

While the common-mode noise could be reduced by:

- Isolating the signal ground from power conductors (e.g., keep signal grounds separated as far as possible from power grounds).
- Ground wires should be as low an impedance as possible.
- Using star ground system configurations.

Some of these techniques are used in systems such as RS-232 e.g., maximum slew rate of the RS-232 is defined as 30 V/μs while Futurebus+, an emerging high-speed backplane standard, uses trapezoidal waveforms to limit crosstalk.

1.6.2 Differential Line Considerations

A differential communication system involves the use of two signal-carrying wires between transmitter and receiver, such that the signal current flows in opposite directions in each wire. The net effect of this is the receiver is only concerned with the difference in voltage between the two wires. The absolute value of the dc common-mode voltage of the two wires is not important. In practice, transmitters and receivers have a finite common-mode voltage range in which they can operate.

The use of a differential communications interface allows transmission at higher data rates over longer distances to be done. This is because the effects of external noise sources and cross differential lines appear as an extra common-mode voltage that the receiver is insensitive to. The difference between the signal levels on the two lines, therefore, remain the same. By the same argument, a change in the local ground potential at one end of the line appears as just another change in the common-mode voltage level of the signals. The differential output to the line also provides a doubling of the driver's single-ended output signal. Twisted-pair cable is commonly used for differential communications since its twisted nature tends to cause cancellation of the magnetic fields generated by the current flowing through each wire, thus reducing the effective inductance of the pair.

The main disadvantage of a differential system lies in the fact that two signal wires are required for each communication link. This increases system cost but provides superior performance when data is transmitted at high rates over long distances.

The RS-485 and RS-422 standards both use differential-type transmission.

1.7 Network Topology

In addition to considering signal attenuation, the effects of noise, signal distortion and correct line termination, we must also consider the way in which stations are connected to the line. Furthermore, the position of the line termination resistor and device positioning must be considered. There are two basic methods of connection (see Figure 1–11);

- The star connection
- The daisy chain connection

Considering the star connection, the transition edge from the driver can be loaded by a group of separate transmission lines rather than one. Each transmission-line boundary causes a change in impedance resulting in reflections.

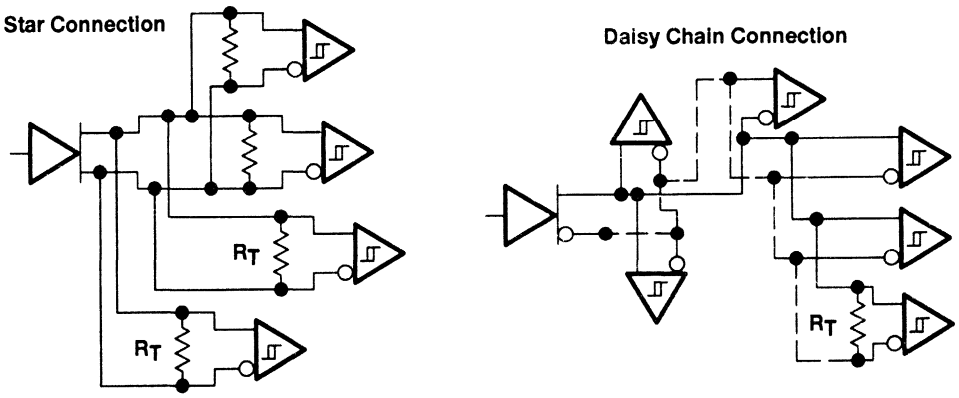


Figure 1–11. Network Topology

Another situation to avoid is the termination of multiple stations, since this could excessively load the driver. Termination at the extreme ends for the RS-485 (half duplex) and far end only for the RS-422 is recommended and is accounted for in each standard. Normally stubs (taps of the main line) should be kept as short as possible so not to appear as transmission lines themselves.

The recommended method is to use the daisy chain, a configuration where the transmission line continues from one receiver to the next and only the last receiver on the chain is terminated. This means that the transmission line and, hence, the driver sees one continuous transmission line with only one termination resistor. Each tap-off is in effect a stub, but in this case they are not all grouped together and are kept very short to reduce their effect.

Figure 1–12 further confirms the need to keep stub lengths short and the use of correct termination techniques by comparing the effect on signal quality for the daisy chain and star method of connection.

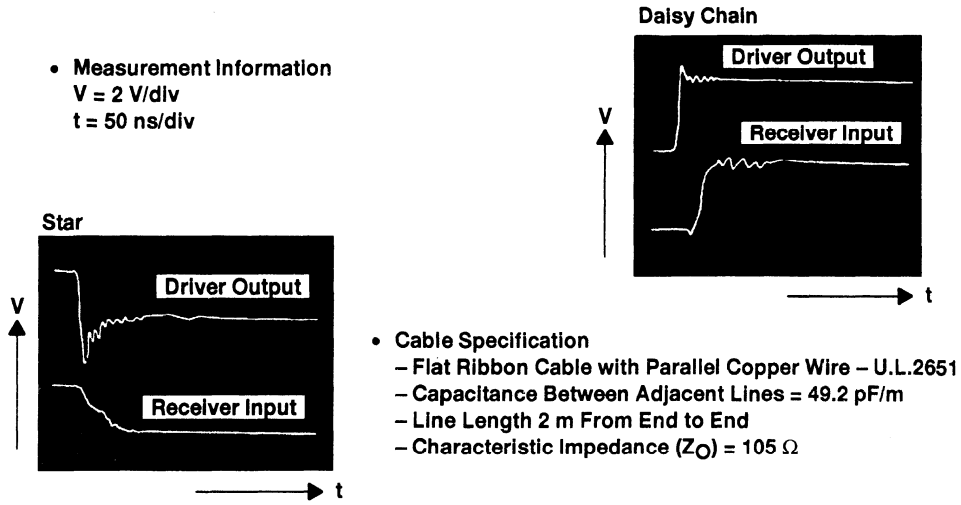


Figure 1–12. Star Versus Daisy-Chain Topology

In both instances exactly the same application scenario is used as is the same cable specification. The cable used is a flat ribbon cable with parallel copper wire conforming to U.L. Specification 2651. Connections are made as shown in Figure 1–12 and the total cable length from source to destination is 2 m.

1.7.1 How Short is Short?

It has been described earlier that a pair of cables act as a transmission line if the round trip propagation delay, t_{pd}, is more than 5 × the transition times of the driver, t_t. The converse is true if the line is not to operate as a transmission line but as a lumped parameter model. This forms the basis of the stub length calculation given in the following paragraphs.

The rule of thumb states that the transition time of the pulse sent down the line should take ten times the amount of +
time taken for the pulse to propagate to the end of the stub. As a result, any reflections are incorporated into the transition edge.

From this basis, the length of a stub is calculated using the cable and driver parameters.

The pulse speed down the line, U, equals the reciprocal of the product of the line impedance and line capacitance, both of which are normally specified for the cables used. The propagation delay down the stub should be at the most one tenth of the transition time of the pulse. These facts can be brought together to give the length of the stub, L_S, as;

$$L_S = \frac{t_{t(D)}}{10}$$

Using the SN75ALS180 and its transition time of 13 ns, a cable with a characteristic impedance of 78 Ω and line capacitance of 65 pF/m:

Using:

$$Z_O = \sqrt{\frac{L_O}{C_O}}$$, as an approximation of the equation shown in subsection 1.3.1.

In practical situations $j\omega L >> R$ and $j\omega C >> G$, therefore R and G can be assumed to be negligible although the R component must be considered for long line lengths.

And:

$$V_P = \frac{1}{\sqrt{L_O C_O}}$$ as an approximation of the phase velocity equation in 1.3.1,

Substitution gives:

$$V_P = \frac{1}{Z_O C_O}$$

Using the values given earlier:

$$V_P = \frac{1}{78 \times 65 \times 10^{-12}} = 198 \times 10^6 ms^{-1}$$

Now, using the rule of thumb described earlier:

$$t_{pd} = \frac{t_{tD}}{10} \text{ and } L_s = t_{pd} V_P$$

Gives $t_{pd} = \frac{13 \times 10^{-9}}{10}$ and; therefore, $L_S = 1.3 \times 10^{-9} \times 198 \times 10^6 = 257$ mm = 10 inches

This means the length of each stub should be no more than 256 mm. Under this length the stub can be considered as a lumped load and does not cause any unwanted reflections. The main effect of each stub in this case is a slight increase in the capacitance loading of the line.

2 Interface Circuits for ANSI EIA/TIA-232-E

2.1 General Information

This section on ANSI Electronic Industries Association/Telecommunication Industry Association EIA/TIA-232-E and ITU V.28 (generally referred to as RS-232), discusses the electrical aspects of the standard, i.e., the physical layer. However, the reader should note the products under discussion in this section are application specific to the 9-pin DB9 Personal Computer Data Terminal Equipment (DTE) serial interface, which is effectively a subset of the full RS-232 standard. As a semiconductor manufacturer, TI finds that the majority of RS-232 applications are moving to this interface. Due to the nature of the signals, (i.e., five receive and three transmit lines,) the older established RS-232 products no longer provide an optimum solution. This interface is now driving the need for single-chip RS-232 solutions. Additional features such as single-supply operation, increased ESD protection, and power-down modes have moved from the desirable features to the essential features of today's interface. In the later half of this section we discuss the DB9 interface and TI's products designed specifically for this application.

Looking at the DB9 interface one step back into the digital system, there is in most cases a universal asynchronous receiver/transmitter (UART) or asynchronous communication element (ACE). The ACE provides the parallel to serial conversion and the necessary start/stop bits, parity-bit generation, and checking for error-free data transmission. TI manufactures a number of ACEs, such as the TL16C552. This integrates two serial ports with FIFO buffers together with a PC parallel port.

2.2 EIA/TIA-232-E Industry Standard for Data Transmission

The EIA introduced the RS-232 standard in 1962 in an attempt to standardize the interface between (DTE) and Data Communication Equipment (DCE). The DTE comprises the data source, data sink, or both. The DCE provides the functions to establish, maintain and terminate a connection, and to code/decode the signals between the DTE and the data channel. Although emphasis was then placed on interfacing between a modem unit and data terminal equipment, other applications were quick to adopt the RS-232 standard. The growing use of the personal computer (PC) quickly ensured that RS-232 became the industry standard for all low-cost serial interfaces between the DTE and peripheral. The mouse, plotter, printer, scanner, digitizer, and tracker-ball, in addition to the external modems and test equipment, are all examples of peripherals that connect to an RS-232 port (see Figure 2–1). Using a common standard allows widespread compatibility plus a reliable method for interconnecting a PC to peripheral functions.

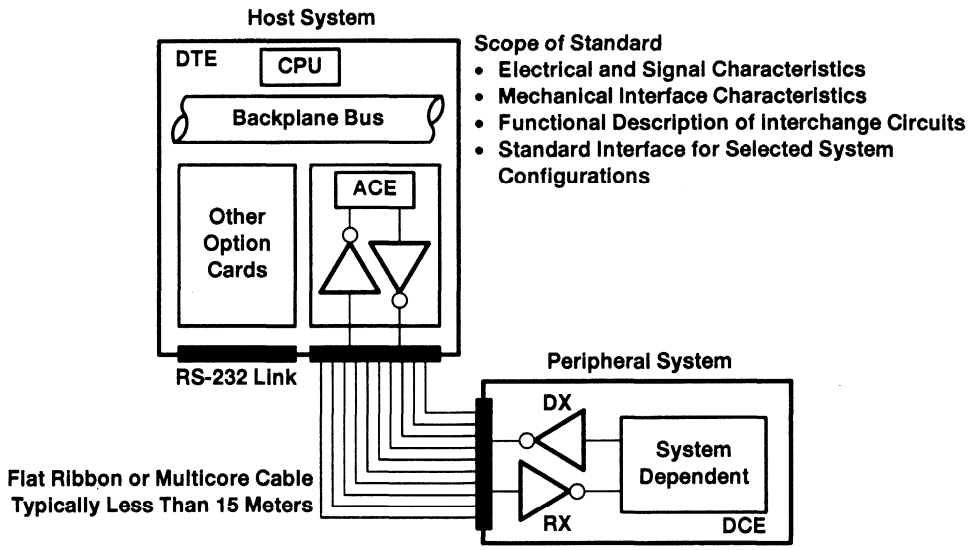


Figure 2–1. EIA/TIA-232-E Industry Standard for Data Transmission

The EIA RS-232-C standard, revised in 1969, was superseded by EIA-232-D (1986), and recently has been once again superseded by EIA/TIA-232-E, which brings it in line with ITU V.24, and V.28 and ISO IS2110. The latest revision includes an update on the rise time to unit interval ratio and reverses the changes made by the D revision (see Figure 2–2). Although an older standard with problems like high-noise susceptibility, low data rates and very limited transmission length, RS-232 fulfills a vital need as a low-cost communication system. Consequently, new products are being developed at a faster rate than ever.

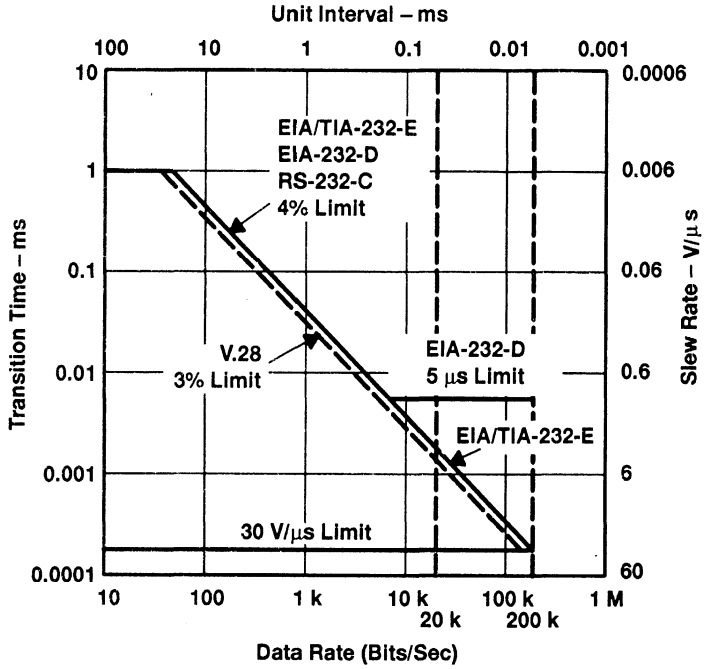


Figure 2–2. RS-232 Transition Time vs Data Rate

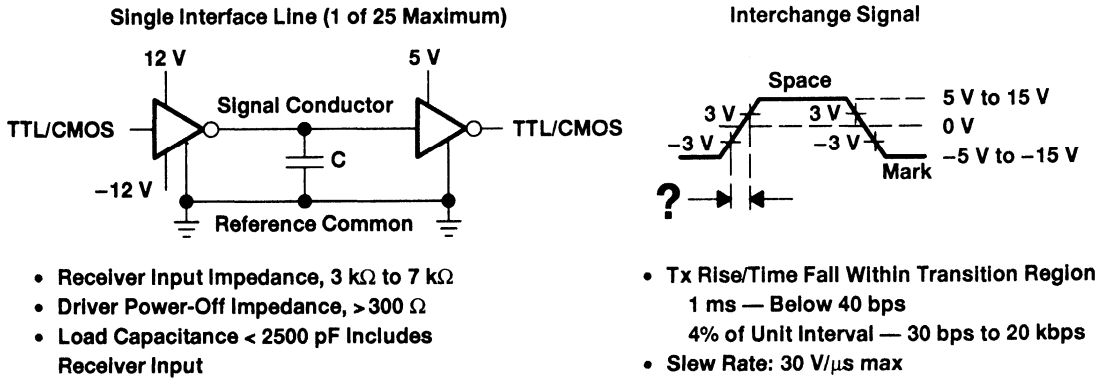
2.3 EIA/TIA-232-E Specification

The standard sets out to ensure:

- Compatible voltage and signal levels
- Common pin wiring configurations
- Minimum amount of control information between the DTE and DCE

It accomplishes these features by incorporating the following areas in the standard:

Electrical and Signal Characteristics – Electrical and signal characteristics of the transmitted data in terms of signal voltage levels, impedances, and rates of change (see Figure 2–3).



- **Receiver Input Impedance, 3 kΩ to 7 kΩ**
- **Driver Power-Off Impedance, >300 Ω**
- **Load Capacitance < 2500 pF Includes Receiver Input**

- **Tx Rise/Time Fall Within Transition Region**
  1 ms — Below 40 bps
  4% of Unit Interval — 30 bps to 20 kbps
- **Slew Rate: 30 V/μs max**

Figure 2–3. EIA/TIA-232-E Electrical Specification

Mechanical Interface Characteristics – Mechanical interface characteristics defined as a 25-pin D connector with dimensions and pin assignments specified in the standard. Although the standard only specifies a 25-pin D-type connector, most laptop and desktop PCs today use a 9-pin DB9S connector (see section 2.3.3). The reader should note the DCE equipment connector is male for the connector housing and female for the connection pins. Likewise, the DTE connector is a female housing with male connection pins.

Handshake Information – A functional description of the interchange circuit enables a fully interlocked handshake exchange of data between equipment at opposite ends of the communication channel. However, V.24 defines many more signal functions than RS-232, but those that are common are compatible. Twenty-two of the twenty-five connector pins have designated functions, although few if any practical implementations use all of them. The most commonly used signals are also shown in subsection 2.3.3.

It is worth noting that for applications that use the 25-pin D-type connector there is often a problem in communication due to different handshaking signals being employed by each system.

2.3.1 EIA/TIA-232-E Electrical Specification

All RS-232 circuits carry voltage signals with the voltage at the connector pins not to exceed ±25 V. Any pin must be able to withstand short circuit to any other pin without sustaining permanent damage. Each line should have a minimum load of 3 kΩ and maximum load of 7 kΩ, which is usually part of the receiver circuit. A logic 0 is represented by a driven voltage between 5 V and 15 V and a logic 1 of between −5 V and −15 V. At the receiving end a voltage between 3 V and 15 V represents a 0 and a voltage of between −3 V and −15 V represents a 1. Voltages between ±3 V are undefined and lie in the transition region. This effectively gives a 2-V minimum noise margin at the receiver.

The maximum cable length was originally defined in RS-232-C as 15 meters; however, this has been revised in EIA-232-D and EIA/TIA-232-E and is now more correctly specified as a maximum capacitive load of 2500 pF. This equates to around 15 to 20 meters of line length depending on cable capacitance.

As mentioned in an earlier section, RS-232 specifies a maximum slew rate of the signal at the output of the driver to be 30 V/μs. This limitation is concerned with the problem of crosstalk between conductors in a multiconductor cable. The faster the transition edge is, the greater the amount of crosstalk. This restriction together with the fact that the drivers and receivers use a common signal ground and the associated noise introduced by the ground current severely limits the maximum data throughput.

For this reason the RS-232 standard specifies a maximum data rate of 20 kbps. The standard also specifies the relationship between unit interval and rise time through the transition region (3 V to −3 V) or t_t. This is the main difference between the D and the E revision. This is shown more clearly in Figure 2–2. EIA-232-D, with a data rate of up to 8 kbps, specifies the relationship between transition time and unit interval or bit time, t_b, to be 4% of the maximum data rate. Above 8 kbps, the transition time is relaxed to a 5-μs maximum independent of the data rate. Both the C and the E revision specify the ratio of t_t/t_b to be 4% all the way up

to 20 kbps. One can extrapolate this further using the 4% figure. With the maximum slew rate of 30 V/ms, the maximum achievable data rate is 200 kbps; however practically this is limited to around 120 kbps. A number of software programs operate at transfer rates of 116 kbps. Furthermore, over longer line lengths, the maximum drive current of the line driver becomes the dominant feature affecting data rate displacing the 30 V/μs slew rate. As the line length increases the load capacitance also increases requiring more current to maintain the same transition time. The curves shown in Figure 2–4 indicate the drive current required to maintain the 4% relationship at different data rates. In today's low-power systems, this level of output current is not sustainable at above approximately 20 kbps. In practice the line length is usually limited to around three meters for the higher data rates. Most drivers can handle the higher transmission rates over this line length without seriously compromising supply current.

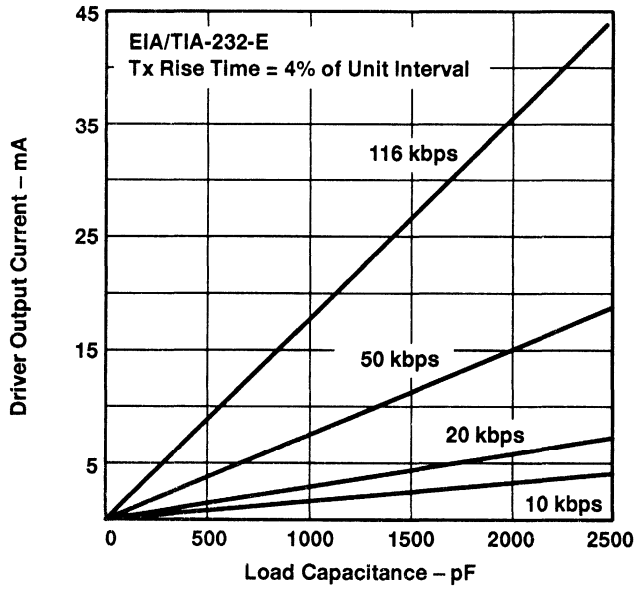


Figure 2–4. EIA/TIA-232-E Driver Output Current vs. C_L

The curves shown in Figure 2–4 were generated using the following equation, which is an approximate equation relating transition time t_t, line capacitance C_1, receiver input impedance R_i, driver short circuit current I_O, and the initial and final line voltage (–3 V and 3 V) of the transition region, V_i and V_f respectively,

$$t_t = R_i \times C_1 \times \ln\left[\frac{|R_i \times I_O| + |V_f|}{|R_i \times I_O| + |V_i|}\right]$$

Turning this equation around with respect to C_1 and cancelling R_i, V_i, and V_f we get:

$$C_1 = \frac{1}{3} \times \frac{t_t}{\ln\left[\frac{I_O + 1}{I_O - 1}\right]}$$

The voltage levels, V_f and V_i, used in this equation are the extremes of the transition region. Assuming a typical driver short-circuit current of 20 mA and a receiver input resistance of 5 kΩ, the typical time taken to pass through the transition region would be:

$$t_t = 300 \times C_1 \text{ seconds.}$$

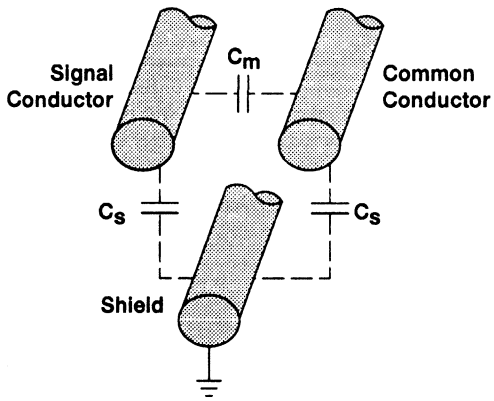
This equation can be manipulated further to gain a relationship of unit interval with line length in terms of load capacitance and short circuit driver current. The equation in Figure 2–5 assumes conformance to the 4% rule.

2.3.2 Calculating Maximum Line Length

So far we have discussed line length in terms of load capacitance. For practical purposes we must not consider turning this value for load capacitance into true line length. The standard states a maximum line capacitance of 2500 pF. The input capacitance for a receiver of 20 pF leaves 2480 pF as the maximum line capacitance.

We must next consider the type of cable to be used. Standard RS-232 cable as supplied by a number of manufacturers has a mutual capacitance of approximately 100 pF per meter. In addition to this we must add the stray capacitance. Stray capacitance varies considerably depending on whether the line is shielded.

For shielded cable the stray capacitance it is typically double the mutual capacitance. As can be seen from Figure 2–5, for shielded cable the maximum line length is 20 meters, for unshielded cable it is over 40 meters.



Line Length Calculation

Maximum Capacitance	= 2500 pF
Receiver I/P Capacitance	< 20 pF
Maximum Line Capacitance	= 2480 pF
Total Line Capacitance/m	$C_C = C_M + C_S$
Mutual Capacitance of Cable/m	$C_M \approx 100$ pF
Stray Capacitance/m	$C_S \approx 200$ pF
Maximum Line Length	$= \frac{2480}{C_C}$
Standard Cable C_M	= 24 pF/m
Max Line Length Shielded	= 10 Meters

Data Rate Calculation

$$\text{Unit Interval} = 1/3 \frac{0.04}{C_C \ln\left(\frac{I_O + 1}{I_O - 1}\right)}$$

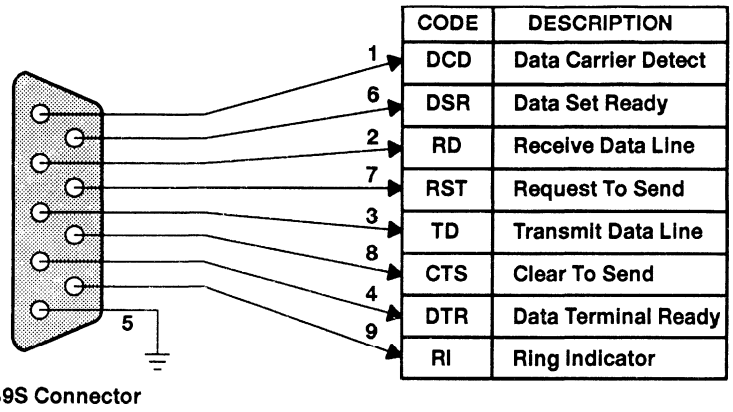
I_O = Short Circuit Current of Driver

Figure 2–5. Calculating Line Length and Data Rate

2.3.3 The DB9S Connector

As mentioned earlier today's notebook, labtop, and many desktop PCs with their quest for reduced size, no longer use the standard 25-pin D-type connector detailed in the standard but have substituted it for a 9-pin D-type. This is commonly known as the DB9S connector. Like the 25-pin, the DCE connector is a male outer casing with female connection pins, and the DTE is a female outer casing with male connecting pins.

As the interface is now made up on only nine pins the handshaking lines have been reduced accordingly but still are sufficient for most applications. Figure 2–6 shows the pins assignments for the interconnect cable into the DTE connector. An explanation of the function of each signal is given in Figure 2–6.



CODE	DESCRIPTION
DCD	Data Carrier Detect
DSR	Data Set Ready
RD	Receive Data Line
RST	Request To Send
TD	Transmit Data Line
CTS	Clear To Send
DTR	Data Terminal Ready
RI	Ring Indicator

Figure 2–6. RS-232 DB9S Interface

Data Carrier Detect (DCD) – Received Line Signal Detector – The On condition on this signal line as sent by the DCE informs the DTE that it is receiving a carrier signal that meets its criteria from the remote DCE. In modems this circuit is held on as long as it is receiving a signal that can be recognized as a carrier. On half duplex channels, DCD is held off when RTS is in the On condition.

Data Set Ready (DSR) – This is a signal turned on by the DCE to indicate to the DTE that it is connected to the line.

Receive Data Line (RD) – The signals on the RD line are in serial form. When the DCD signal is in the Off condition the RD line must be held in the Mark state.

Request to Sent (RTS) – The signal is turned on by the DTE to indicate it is now ready to transmit data. The DCE must then prepare to receive data. In half duplex operation, it also inhibits the receive mode. After some delay the DCE turns the CTS line on to inform the DTE it is ready to receive data. Once communication is over and no more data is transmitted by the DTE, RTS is then turned from on to off by the DTE. After a brief time delay to ensure that all data has been received that was transmitted, the DCE turns CTS off.

Transmit Data Line (TD) – The signals on this circuit are transmitted serially from DTE to DCE. When no data is being transmitted the signal line is held in the Mark state. For data to be transmitted, DSR, DTR, RTS and CTS must all be in the Mark state.

Clear to Send (CTS) – This signal is turned on by the DCE to indicate to the DTE that it is ready to receive data. CTS is turned on in response to the simultaneous On condition of the RTS, DSR and DTR signals.

Data Terminal Ready (DTR) – This signal in conjunction with DSR indicates equipment readiness. DTR is turned on by the DTE to indicate to the DCE it is ready to receive or transmit data. DTE must be in the On condition before the DCE can turn on the DSR. When the DTR is turned off by the DTE, the DCE is removed from the communication channel following the completion of transmission.

Ring Indicator (RI) – The ring indicator is turned on by the DCE while ringing is being received and is a term left over from the use of the standard in telephone line modem applications. This is primarily used in auto-answer systems.

Signal Ground (pin 5) – This is the ground that provides the common ground reference for all the interchange circuits and is separate from the protective ground. The protective ground is electrically bonded to the equipment frame and is usually directly connected to the external ground. Any static discharges are then routed directly to ground without affecting the signal lines.

While all these pins are assigned, once again not all equipment uses every pin. Consider the mouse that can use as few as four lines (Signal ground, RI, TD and RD). Most equipment utilizes a minimum of RTS, DTR, TD, RD, CTS and DSR.

Also of note is the usage of the DTE interface. The majority of equipment uses this interface and makes use of the null modem as a means of communication between DTEs. The null modem makes use of feeding back the RTS signal to the CTS line on each interface. Figure 2–7 details the connections for implementing a full null modem for the DB9S connector.

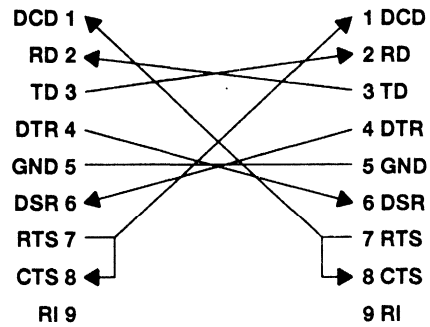


Figure 2–7. RS-232 Null Modem

2.4 SN75C185: Optimized PC Interface

If we study the DB9S DTE interface further we see there are three transmit lines and five receive lines. This is an awkward combination for the standard RS-232 IC configurations in use today. Consider the ubiquitous SN75188 and SN75189 quadruple drivers and receivers. To implement this interface would require three ICs, one '188 and two '189s. Equal combinations of drivers such as the triple driver/receiver of the SN75C1406 still require two chips to implement the interface.

For this reason TI has developed the SN75C185. By providing the exact combinations of driving and receiving elements, along with the necessary passive components, a highly-optimized solution can be provided – the SN75C185 is just that. The SN75C185 integrates three drivers and five receivers and includes the necessary capacitors for driver slew-rate limit (30 V/μs) and receiver filter implementation, all in a single 20-terminal package.

The designer's dilemma is eased further by the use of a flow-through pinout architecture (see Figure 2–8). By aligning one side of the SN75C185 with the pins of the DB9S connector and the other side to industry standard ACEs or UARTs, printed circuit board (PCB) layout can be greatly simplified.

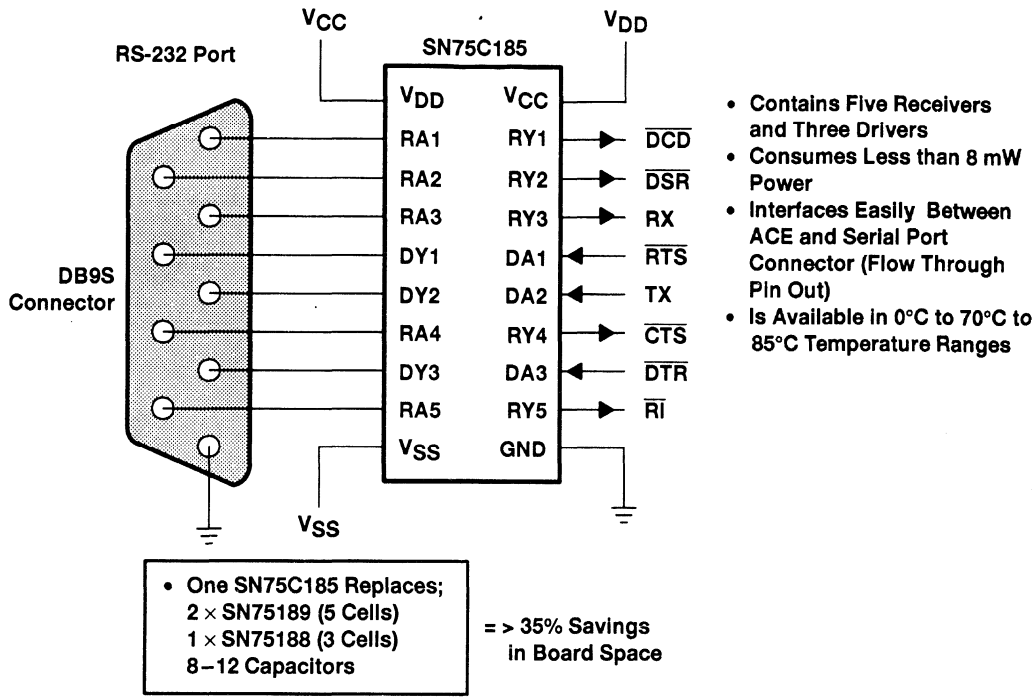


Figure 2–8. The SN75C185 Used As An Optimized PC Interface

Since its introduction in 1989, the footprint of the SN75C185 has become an industry standard. This provides for multiple sources and various semiconductor processes for addressing different design requirements. TI and others have released cost-reduced versions at the expense of power and external components. The single-chip interface concept is also being applied to the peripheral (or DCE) end of the cable as well.

2.4.1 SN75C185 Power Considerations

System power consumption is often considered very late in the design cycle. Of even more concern is that the power consumption of the interface circuitry, being the least attractive circuit to design, is often totally overlooked. The consequences of this can be catastrophic especially when using devices in confined spaces. These areas normally have very poor air circulation causing the ambient temperature of the whole system to increase.

These types of problems are particularly difficult to diagnose because failure can often be intermittent as devices pass into and out of thermal shutdown.

For these reasons, low quiescent-power devices are becoming a necessity for modern applications. As digital technologies advance, their power consumption decreases, making the interface circuits the limiting factor as far as system power consumption is concerned.

2.4.2 Interface Power Consumption Calculations

Before the availability of the SN75C185 common implementations of RS-232 required one quad-driver package and two quadruple receiver packages; in the driver chip, one device is redundant and in the receiver chips, three devices are redundant. These devices would, however, still be taking their quiescent current and wasting power. In order to provide the interface signals, three integrated circuits were required while only two-thirds of the capability was being used. The calculations that follow demonstrate this difference.

When comparing the 'C185 solution to that provided by the SN75188 and SN75189 devices, the power saving is enormous (see Figure 2–9).

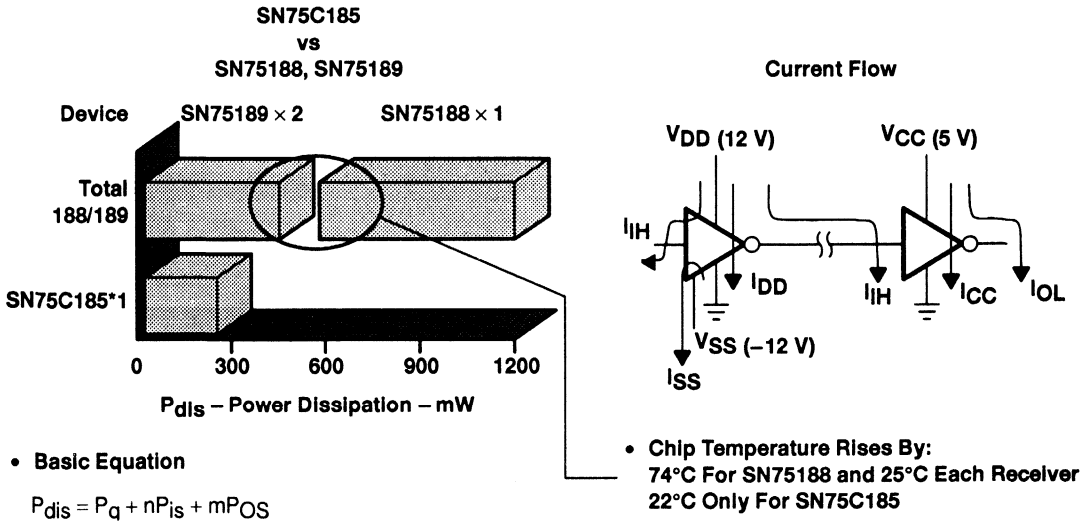


Figure 2–9. Power Supply Considerations

Both implementations require three supply voltages, a 5V and ±12V supplies. The power dissipated, P_{dis}, within each device is the quiescent power of the device, P_q, plus the power dissipated in the input stage, P_{is}, and the power dissipated in the output stage, P_{OS}, (when it is driving the line).

Hence,

$$P_{dis} = P_q + nP_{is} + mP_{OS}$$

Where n is the number the active input stages and m is the number of active output states.

SN75188/SN75189 Combination – Using the SN75188 for the driver, the quiescent power consumption would be 576 mW [(I_{DD} × 12 V) + I_{SS} × 12 V]. In addition to this the power dissipated in the input stage, P_{isd}:

$$P_{isd} = V_{DD} * I_{IL} = 12\ V * 1.6\ mA = 19.2\ mW/driver.$$

This is multiplied by 4 to take into account all four drivers, putting the fourth driver into a defined state so as to reduce any noise problems that could be introduced by leaving the input floating.

The power dissipated in the output stage, P_{OS}, is:

$$P_{OS} = \left(V_{DD} - V_{OH}\right) * \frac{V_{OH}}{R_L} = (12\ V - 9\ V) * \frac{9\ V}{3\ k\Omega} = 9\ mW/driver$$

This number is multiplied by 3 to take into account the three drivers active on the interface line. The sum gives a total power dissipation of:

$$P_{dis} = 576 \text{ mW} + 4 \text{ V} \times 19.2 \text{ mW/driver} + 3 \text{ V} \times 9 \text{ mW/driver} = 680 \text{ mW}.$$

The junction temperature of a DIP device would then have risen by 75°C.

Using the SN75189 receivers, a quiescent power of 130 mW would be dissipated by each package. The power dissipated in the output stage has a similar equation to that of the driver.

$$P_{os} = V_{OL} \times I_{OL} = 0.45 \text{ V} \times 10 \text{ mA/receiver} = 4.5 \text{ mW/receiver}$$

This power dissipated is multiplied by 5 to take into account the five receivers being used. The input stage can also dissipate some power.

$$P_{is} = \frac{(V_{OH})^2}{R_L} = \frac{9^2}{3} = 27 \text{ mW/receiver}$$

Assuming three receivers in one SN75189 and two receivers in the other are being used, the power dissipated for the first receiver is:

$$P_{dis} = 130 + 3 \times 27 + 3 \times 4.5 = 206 \text{ mW}.$$

The power dissipated in the second receiver is:

$$P_{dis} = 130 + 2 \times 27 + 2 \times 4.5 = 183 \text{ mW}.$$

This raises the temperature of the first and second receiver by 25°C and 23°C respectively.

The total power dissipated by the SN75188/189 combination is the sum of these three powers, which equals 1.1 W.

Using the SN75C185 – The power dissipation of the SN75C185 can be calculated in a similar manner. The quiescent-power consumption of the SN75C185 is equal to:

$$P_q = V_{DD} \times I_{DD} + V_{SS} \times I_{SS} + V_{CC} \times I_{CC}$$

$$= 12 \text{ V} \times 200 \text{ µA} + -12 \text{ V} \times 200 \text{ µA} + 5 \text{ V} \times 750 \text{ µA}$$

$$= 8.55 \text{ mW}$$

The power dissipated in the input stage of the driver, P_{is}, is:

$$P_{is} = V_{DD} \times I_{IL} = 12 \text{ V} \times 1 \text{ µA} = 12 \text{ µW}$$

This is multiplied by three to take into account all of the drivers.

The power dissipated in the output state of the driver, P_{os}, is:

$$P_{os} = (V_{DD} - V_{OH}) \times \frac{V_{OH}}{R_L} = (12 - 10) \times \frac{10}{3} = 6.67 \text{ mW}.$$

This number is multiplied by 3 to take into account the three drivers that are driving the interface line, resulting in a power dissipation of 20 mW.

The power dissipated in the output stage of the receiver, P_{os}, has a similar equation to that of the driver, so:

$$P_{os} = V_{OL} \times I_{OL} = 0.4\ V \times 3.2\ mA = 1.28\ mW$$

This value is multiplied by 5 giving a total 6.4 mW of power dissipated in the receiver's output stages.

The power dissipated in the input stage, P_{is}, equals:

$$P_{is} = \frac{(V_{OH})^2}{R_L} = \frac{10^2}{3} = 33.3\ mW/receiver$$

This power dissipation also requires multiplying by 5, which gives a total input power dissipation of 167 mW.

Then by summing all the power contributors, the total power dissipation is derived and is giving by;

$$P_{dis} = P_q + 3P_{is} + 3P_{os} + 5P_{is} + 5P_{os}$$

$$= 8.55 + 3 \times 12 \times 10 - 3 + 3 \times 6.67 + 5 \times 33.3 + 5 \times 1.28$$

$$= 201\ mW.$$

The total power dissipated by the SN75C185 is 201mW

This represents a tremendous power saving, especially when considering that the line is still being driven. The temperature rise within the SN75C185 would only be 22°C, enabling it to operate more reliably and with higher ambient temperatures.

2.4.3 On-Chip Slew-Rate Limiting

The EIA-232-E standard specifies a maximum slew rate through the transition region of 30 V/μs. Relating this to capacitance and current, only 100 μA of output current into 30 pF load capacitance is needed to exceed the slew-rate limit. All devices are capable of supplying more that 5 mA. Therefore, if the slew rate limit is not to be exceeded, the switching speed of the driver's output stage needs to be reduced. An established solution is to place loading capacitors on the output of the driver. The value of the loading capacitor required depends upon the line length, but it is generally in the order of 330 pF. The effect of this capacitor causes the output transistors to saturate, causing it to short circuit current limit, thus preventing fast switching edges.

There are some major problems with this established process; one being the variance in current at which the output short-circuits as well as the line length. For example, a device capable of sourcing 10 mA needs a total capacitance of 330 pF placed on its output to meet the 30 V/μs slew rate limit. Placing this value across a device capable of sourcing 4 mA has its slew rate limited to less that 12 V/μs.

Another problem encountered is the increase in power dissipation through the output stage. The output voltage of the driver is normally close to one supply rail, so when it tries to switch to the other, the active transistor has most of the supply voltages across it. The extra external capacitor holds the driver's voltage close to the supply voltage causing the output transistor to source a large amount of current. The combination of the large source current and large voltage causes it to dissipate large amounts of power. Operating at these prolonged bursts of high current ultimately increases the chip temperature, which can affect the long-term life of the device. Bipolar technologies are normally much better able to withstand such effects.

A better solution, and the one employed by the drivers in SN75C185, is to place the slew-rate limiting within the chip itself. Using similar techniques to those employed for slew-rate-limited operational amplifiers, the slew rate of line drivers can also be limited. Using the Miller capacitance multiplying effect, the slew rate of the driver can be slowed down. The biasing current to the output transistors is unaffected by this technique and are more than sufficient to drive the 3 kΩ load as offered by the receiver.

2.4.4 Internal Noise Filtering

The EIA-232-E standard states a maximum line cable capacitance of 2500 pF, which corresponds to an approximate line length of 20 meters. As the interface line gets longer, it becomes more susceptible to noise pick up from the surrounding environment.

For operation at high data rates, the use of the differential line might be the best solution. If however, a low-cost and simple single-ended solution is required, then standard RS-232 devices can be modified to give noise protection. This is achieved by slowing down the response of the receiver's input. The maximum data rate specified in the standard is 20 kbps, corresponding to a minimum pulse period of 100 μs. Therefore, in normal applications, most devices are far faster than specification requires.

To slow down older bipolar receivers such as SN75189s, a capacitor needs to be placed on each of its response control terminals. This means an additional four capacitors per device, which can be awkward and costly. The effect of this response control capacitor is to set up a low-pass filter on the receiver's input. In order to provide long pulse rejection, the capacitor needs to be quite large. Furthermore, the filter response is asymmetric, affording protection against positive noise voltage spikes only, negative spikes are unaffected, and tends to attenuate rather than reject short noise pulses.

Receivers in the SN75C185 integrate on-chip filtering that reject fast transient noise pulses. The on-chip filters are more precise than filters implemented using external passive components. These filters are totally symmetrical, offering protection against both positive and negative noise pulses, and have the ability to reject, rather that attenuate, short noise pulses. To approach the level of filtering offered by the 'C185 receivers, the standard '188-type receivers require much larger capacitors but still falls well short of filtering requirements.

3 Interface Circuits for RS-485,

3.1 The Need for Balanced Transmission Line Standards

This section focuses on industry's most widely used balanced transmission line standard, the EIA RS-485 (referred to hereafter as RS-485). After reviewing key aspects of the RS-485 standard, you are introduced to the practicalities of implementing a differential transmission scheme based on a factory automation example. Finally, new additions to Texas Instruments EIA product line are discussed along with their application, where appropriate.

Data transmission between computer system components and peripherals over long distances and under high-noise conditions usually proves to be very difficult, if not impossible, with single-ended drivers and receivers. Recommended EIA standards for balanced digital voltage interfacing provide the design engineer with a universal solution for long-line system requirements.

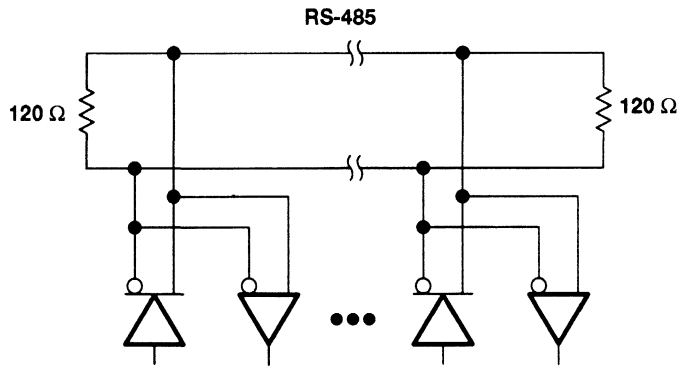
RS-485 is a balanced (differential) digital transmission line interface developed to incorporate and improve upon the advantages of the current-loop interface and improve on the RS-232 limitations. The advantages are:

- Data rate – 10 Mbps and beyond
- Longer line length – up to 1.2 km
- Differential transmission – less noise emissions

3.1.1 Application Areas

The RS-485 allows bidirectional multipoint party-line communication and can effectively be used for mini-LAN applications, such as data transmission between a central computer and remote intelligent stations. For example, a typical application could be RS-485 lines between point of sales terminals and a central computer for automatic stock debiting.

As a result of its versatility an increasing number of standard's committees are embracing the RS-485 standard as the physical layer specification of their communications standard. Examples include the ANSI (American National Standards Institute) Small Computer Systems Interface (SCSI) that is featured in Section 4, the Profibus standard, and the DIA Measurement Bus.



- **Up to 32 Unit Loads (typ)**
- **Half Duplex Communication**
- **Protocol not Included in Specification**

KEY PARAMETERS	SPECIFICATION LIMITS
Maximum common-mode voltage	−7 V to 12 V
Receiver input resistance	12 kΩ minimum
Receiver sensitivity	±200 mV
Driver load	60 Ω
Driver output short-circuit limit	150 mA to GND 250 mA to −7 V to 12 V

Figure 3–1. RS-485 Specification Highlights

3.1.2 RS-485

The balanced transmission line standard RS-485 was developed in 1983 to interface a host computer's data, timing, or control lines to its peripherals. The standard specifies the physical layer only. Protocols, timing, serial or parallel data, and connector choice are all left to be defined by the designer.

RS-485 was originaliy defined as an upgrade to and a more flexible version of RS-422. Where RS-422 facilitates simplex communication only, RS-485 allows for multiple drivers and receivers on a single line facilitating half-duplex communication. Like RS-422 the maximum line length is not specified but based on 24-AWG cable, it is nominally around 1.2 km. Maximum data rate is unlimited and is set by the ratio of rise time to bit time, similar to RS-232. In many cases it is the length of the cable that limits the data rate more that the drivers due to transmission line effects and noise (see Section 1).

The differences between RS-485 and RS-422 lie primarily in the driver features that allow reliable multipoint communications.

3.2 Process-Control Design Example

To fully understand the considerations of designing an RS-485 system it is advantageous to take a specific design example. In this case we consider a factory automation system with a host controller and several out-stations. Each out-station is capable of transmitting as well as receiving data.

The system has the following features and a general system specification is shown in Figure 3–2.

- Furthest out-station is 500 m from the host controller
- We require up to 31 out-stations on the line. With the host controller this totals 32 stations in total.
- System data rate is 500 kilobits per second.
- Only one cable is used for data transmission operating in half-duplex mode.

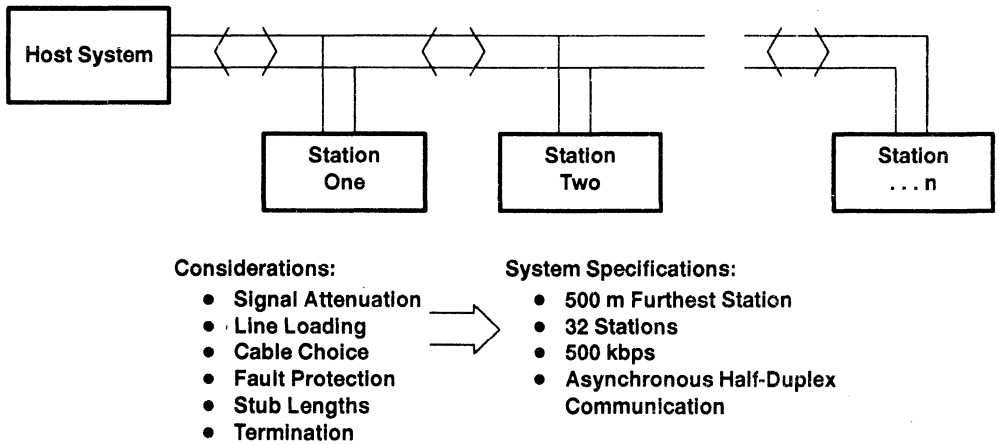


Figure 3–2. Process Control Design Example

3.3 Line Loading

RS-485 takes into account the need for line termination and the subsequent loading on the transmission line. The decision on whether to terminate the line or not is system dependent and is affected by the choice of the maximum line length and data rate.

Line Termination – As we discussed in Section 1, the test for whether a transmission line is to be considered as a distributed parameter model or a lumped parameter model is dependent upon the relationship of signal transition time, t_t, at the receiving end and the propagation time, t_{pd}, of the signal down the cable. The threshold between the two types of transmission line is given by the following equation:

$$2t_{pd} = t_t$$

If we build a margin of error into this equation a better test is to determine the relation of twice the transition time to 5 times the propagation delay:

If the relationship $2t_{pd} \geq 5t_t$ is true, then the transmission line must be treated as a distributed parameter model and terminated accordingly.

If the opposite is true than,

$$2t_{pd} \geq \frac{t_t}{5} \text{ is true and}$$

the transmission line can be treated as a lumped parameter model and termination is not necessary.

To transmit data at the design goal of 500 kbps and comply with RS-485, the input transition time can be no more than 0.3 times the unit interval (ui). This establishes an upper limit on the transition time of:

$$t_t \leq 0.3 \times \text{ui}$$

$$t_t \leq 0.3\left(\frac{1}{500 \times 10^3}\right)$$

$$t_t \leq 60 \times 10^{-9} \text{ s}$$

If we could obtain a cable with a phase velocity equal to that of the speed of light in a vacuum, the propagation delay of the cable would be 3.33 ns/m multiplied by 500 m or 1,665 ns. Using the criteria for determining that we have a transmission line:

$$2t_{pd} \geq \frac{t_t}{5}$$

$$3,333 \geq 12$$

With the slowest possible signal transition and the fastest phase velocity, we have a transmission line. Using real-world components would only substantiate the fact that our 500 m half-duplex transmission line must be terminated at both ends.

The Unit Load Concept – The maximum number of drivers and receivers that can be placed on a single RS-485 communication bus depends upon their loading characteristics relative to the definition of a unit load (UL). The RS-485 standard recommends a maximum of 32 ULs per line.

One UL (at worst case) is defined as a load allowing 1 mA of current under a maximum common-mode voltage stress of 12 V or 0.8 mA at –7 V. ULs may consist of drivers and/or receivers and fail-safe resistors but does not include the ac termination resistors.

The example in Figure 3–3 shows a UL calculation for the SN75ALS176B. Since this device is internally connected as a transceiver (i.e., driver output and receiver input connected to the same bus) it is difficult to obtain separate driver leakage and receiver input currents. For this calculation reference is made to the receiver input resistance, 12 kΩ, giving a transceiver current of 1 mA. This can be taken to represent 1 UL, which allows up to 32 devices to be connected to the line.

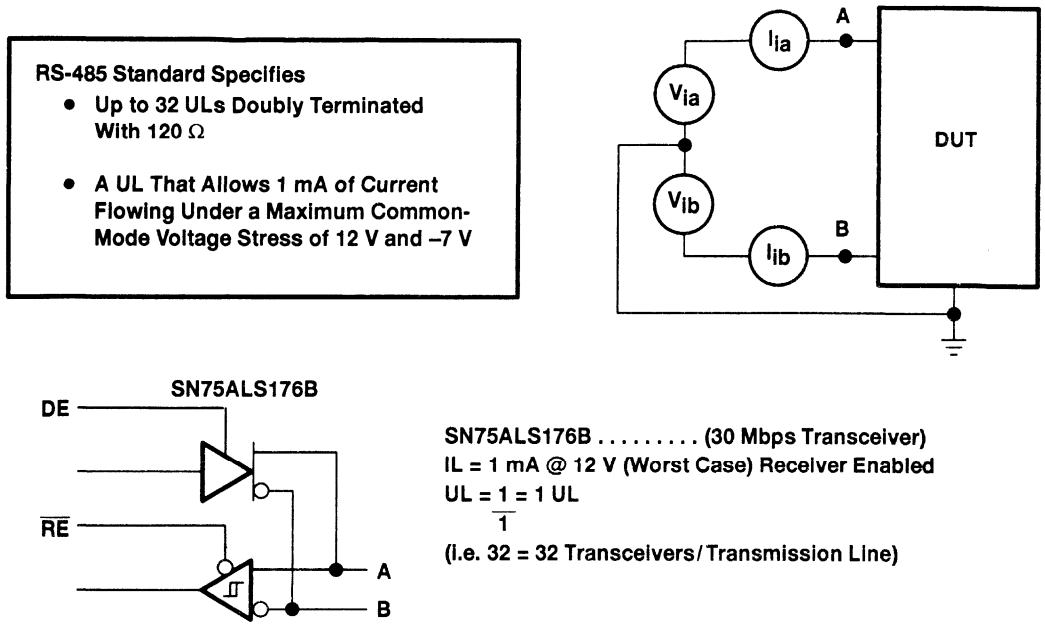


Figure 3–3. The Unit Load Concept

Obviously it may be possible to connect more devices than the number given in the RS-485 recommendation, but this is at the designer's risk.

3.3.1 Signal Attenuation

Section 1.3 discusses attenuation in more detail but a rule of thumb for allowable attenuation is –6 dBV. Attenuation figures are usually supplied by cable manufacturers. The curve in Figure 3–4 shows the attenuation change versus frequency for 24-AWG cable. For 500 meters of cable and using 6-dBV, the maximum attenuation that can be tolerated is 0.35 dBV/30 meters. In this case, the 500 kbps data-rate frequency components of the signal up to 10 Mbps is still detectable at the receiver. This effect coupled with the variation of signal velocity with frequency (termed dispersion) results in distortion of the pulse at the receiving end of the line.

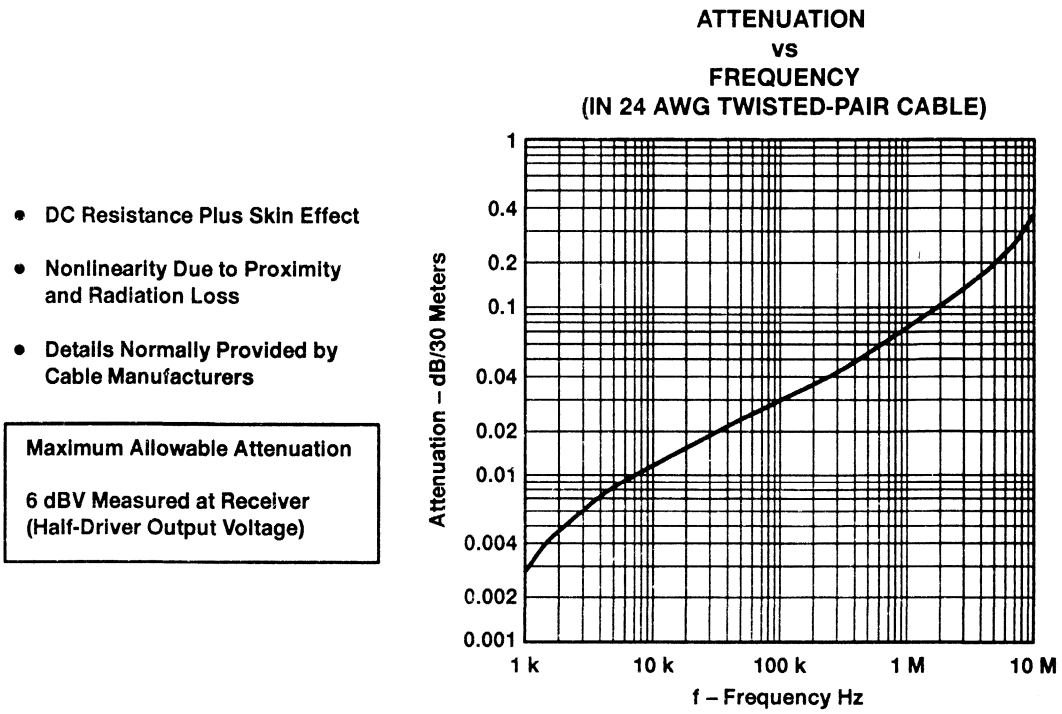


Figure 3–4. Signal Attenuation

The simplest way to determine the affects of random noise, jitter, attenuation, and dispersion is with the use of eye patterns. For information on how to set up eye patterns, refer to Section 1.4 of this document. Figure 3–5 shows the distortion of the signal at the receiving end of 500 meters of 20 AWG twisted-pair cable at different data rates. Using the system constraint of 500 kbps, we see the distortion is limited to the rounding of the signal pulse. When the data rate is increased further, the affects of jitter then become noticeable. In this case, at 1 Mbps, we begin to observe 5% jitter. At 3.5 Mbps we start to loose the signal completely and the quality of transmission is severely degraded. The maximum allowable jitter in a system should be limited to 5%. The causes of jitter are discussed in more detail in subsection 1.4.2.

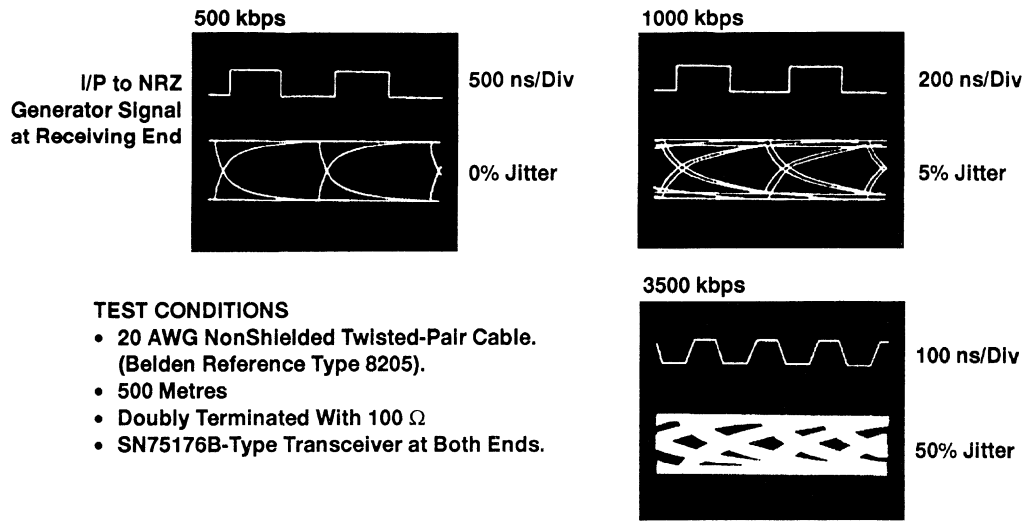
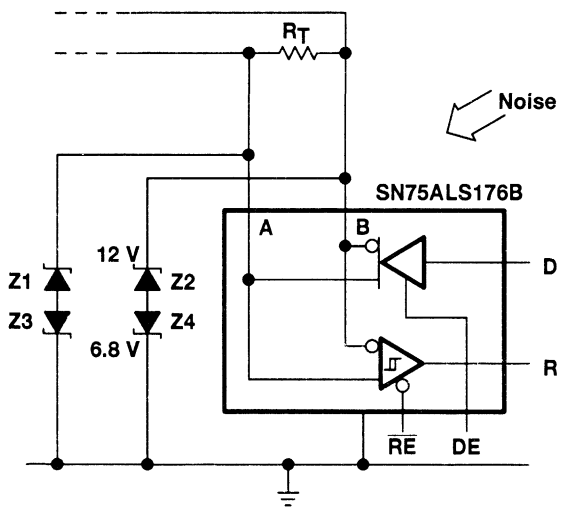


Figure 3–5. RS-485 Signal Distortion vs Data Rate

3.3.2 Fault Protection and Fail-Safe Operation

Fault Protection – Factory control applications generally require protection against excessive noise voltages. The noise immunity afforded by the differential-transmission scheme, and in particular the wide common-mode voltage range of RS-485 may be insufficient. Protection can be accomplished in a number of ways. The most effective being through galvanic isolation, which we discuss later. Galvanic isolation provides good system-level protection but requiring a higher cost. A less expensive solution can be accomplished by the use of protection diodes but with a lower level of protection.

Figure 3–6 shows how external diodes offer transient spike protection for the SN75ALS176 RS-485 transceiver.



$R_T = R_O = 120\ \Omega$
Z1 = Z2 = BZX 85 Rated at 12 V
Z3 = Z4 – BZX 85 Rated at 6.8 V

Figure 3–6. Input Protection for Noisy Environments

R_T is the usual termination resistance and is equivalent in value to the characteristic impedance of the line.

Z1 and Z2 are chosen to protect the input from positive noise voltage spikes greater than 12 V while Z3 and Z4 protect the device from negative-going spikes greater than –6.8 V. The peak voltage at the peak current rating of Z1 and Z2 should be less than the absolute maximum ratings of the device.

Fail Safe Operation – The feature of fail-safe protection is also a requirement in many RS-485 applications; however, its usefulness needs to be considered and understood at an application level.

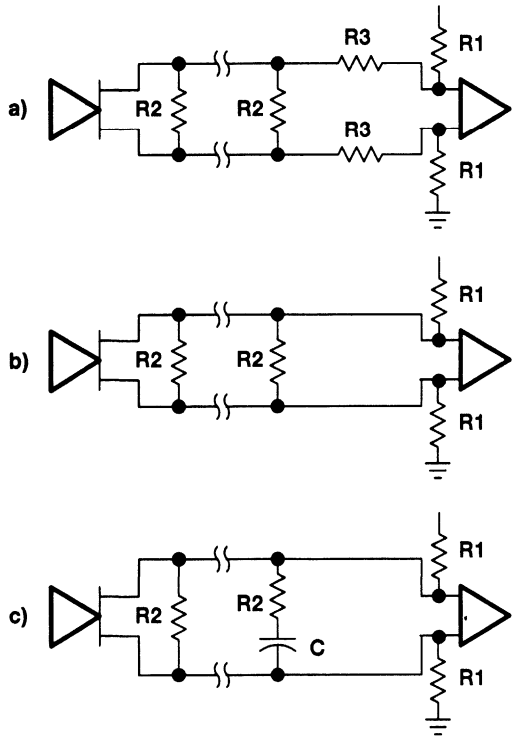
The Need For Fail-Safe Protection – In any party-line interface system with multiple driver/receivers, there are long periods of time when the driving devices are inactive. This state is known as line idle and occurs when the drivers place their outputs into a high-impedance state. During line idle, the voltage along the line is left floating (i.e., indeterminate – neither logic-high nor logic-low state). As a result, the receiver can be falsely triggered into either a logic-high or logic-low state, depending upon the presence of noise and the last polarity of the floating lines. This is obviously undesirable as the circuitry following the receiver could interpret this as valid information. It becomes desirable to detect such a situation and place the receiver outputs into a known and predetermined state. The name given to methods that ensure this condition is called fail safe. An additional feature that a fail safe should provide is to protect the receiver from shorted line conditions, which can again cause erroneous processing of data.

There are several ways to implement a fail safe, including a hard-wired fail safe using line bias resistors or with protocols. Protocols, although complicated to implement, are the preferred method. However, since most system designers, hardware designers in this case, prefer to implement such functions in hardware, a hard-wired fail safe is most often implemented.

A hard-wired fail safe should provide a defined voltage across the receiver's input regardless of whether the signal pair is shorted together or is left open circuited. The fail safe should also be incorporated into the line termination, if present, when at the extremes of the line.

Internal Fail Safe – Manufacturers have gone part way to facilitating fail-safe design by including some form of open-line fail-safe circuitry within the integrated circuits. The extra circuitry is quite often just a large pullup resistor on the noninverting receiver input and a large pulldown resistor on the inverting input of the receiver. These resistors are normally in the range of 100 kΩ and, when used in conjunction with line termination resistors (typically 50 Ω to 100 Ω) to form a potential divider, only a few millivolts are generated differentially. As a result, this voltage (receiver threshold voltage) is insufficient to assume the receiver state. To use these internal resistors effectively means no line termination resistors can be used, which reduces the allowed reliable data rate significantly.

External Fail-Safe Open-Line and Terminated Conditions – A more reliable way of offering open-line fail safe is to use external pullup and pulldown resistors at one, and only one point on the bus (see Figure 3–7). There are two basic ways of doing this; one way is to polarize the line with the pullup/pulldown resistors and use these resistors to match the line impedance. Another way is to use large polarizing resistors while using an extra resistor to terminate the line. The first idea has one advantage in that it provides a low-impedance path to ac ground, so that any common-mode currents induced on the line have a low-impedance path to ground. However, a problem can be encountered with this method because the driver output now has to drive much lower common-mode impedances. If the driver output current capability is marginal, the device could go into output short-circuit current limit. The second way, although requiring an extra resistor, does not load the driver's output to such an excess.



	Ω	Open	Idle	Short	u.l.	A, dBV
R1 =	2500					
R3 =	110	Y	Y	Y	5.6	−0.5
R2 =	120					
R1 =	27000					
R3 =	1000	Y	Y	Y	1.5	−1
R2 =	120					

	Ω	Open	Idle	Short	u.l.	A, dBV
R1 =	620					
R2 =	120	Y	Y	N	20.5	0

	Ω	Open	Idle	Short	u.l.	A, dBV
R1 =	1200					
R3 =	0	Y	Y	N	11.1	0
R2 =	120					
C =	0.1 μF					

Figure 3–7. External RS-485 Fail Safe for Open- and Terminated-Line Conditions

Placing external pullup and pulldown resistors, R1, on the noninverting and inverting inputs of the receiver produce an open-circuit fail safe. Terminating the transmission line with its characteristic impedance, Z_O, with R2 produces a potential divider between 2R1 and R2. The voltage formed across the line, V_{ODZ}, equals

$$V_{ODZ} = V_{CC} \times \frac{\frac{R2}{2}}{2R_1 + R2}$$

Devices meeting the RS-485 receiver threshold voltage specifications require V_{ID} to be greater than 200 mV. From this the relationship of R1 to R2 can be derived:

$$R1 = R2 \times \frac{1}{4} \times \frac{V_{CC} - V_{ODZ}}{V_{ODZ}}$$

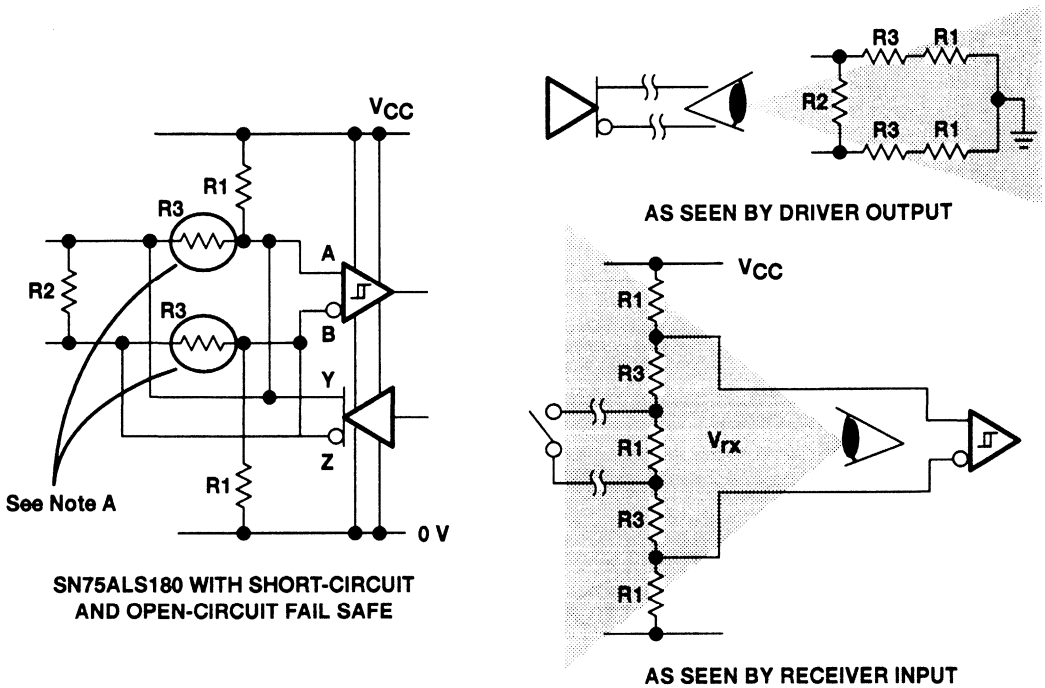
With V_{CC} = 5V, V_{ODZ} = 200 mV and Z_O = R2 = 100 Ω, yields R1 = 0.6 kΩ.

Biasing the receiver in this way only provides open-line fail safe, it does not provide shorted-line fail safe. However, when using transceivers like the SN75ALS176, it is impossible to provide shorted-line fail safe configuration since the driver and receiver share the same IC terminals. For devices like the SN75ALS176 this open-line configuration is the only hard-wired fail safe available.

This termination uses 20 of the allowed 32 unit loads, leaving 12 available for transceiver connections, see Figure 3-7 (b.

External Fail Safe With Shorted-Line Conditions – To implement protection from the shorted-line condition, more resistors are required. When the line is shorted the transmission line's impedance goes to zero and the termination resistors are also shorted. Putting extra resistors in series with the input to the receiver can provide shorted-line fail-safe protection.

The extra resistors, R3 in Figure 3–7, can only be added when using devices with separate driver outputs and receiver inputs. Internally wired transceivers cannot be used for shorted-line fail safe. If this form of protection is required then a device such as the SN75ALS180, with it separate driver outputs and receiver inputs, should be used. If a transceiver type device is used then the extra R3 resistors would cause extra attenuation of the output signal. The 'ALS180 has its driver outputs fed directly to the line, then bypassing the R3 resistors.



NOTE A: Cannot implement short-circuit fail safe with SN75176 type transceiver.

Figure 3–8. Short-/Open-Circuit Fail Safe

Calculating The Resistor Values – If the line becomes shorted, R2 is removed from the circuit leaving a voltage across the receiver inputs of:

$$V_{ID} = V_{CC} \times \frac{2R3}{R1 + 2R3}$$

For RS-485 applications the standard specifies the maximum input voltage threshold (V_{IT}) to be greater than 200 mV. So, a known state can be assumed when $V_{ID} > V_{IT}$ or $V_{ID} > 200$ mV. This condition becomes the first design constraint.

$$1)\ V_{CC} \times \frac{2R3}{R1 + 2R3} > 200\ mV$$

When the line goes into a high impedance state, the receiver sees the two R3s in series with R2 plus the two R1s pulling up and down on either input. The receiver input voltage is now:

$$V_{ID} = V_{CC} \times \frac{R2 + 2R3}{2R1 + R2 + 2R3}$$

Relating this new V_{ID} to the minimum specified in the standard, V_{IT}, gives the second design constraint:

$$2)\ V_{CC} \times \frac{R2 + 2R3}{2R1 + R2 + 2R3} > 200\ mV$$

The transmission line sees an effective line termination resistance of R2 in parallel with twice the sum of R1 and R3. This should match the transmission line's characteristic impedance, Z_O, and therefore provides a third constraint of:

$$3)\ Z_O = 2R2 \times \frac{R1 + R3}{2R1 + R2 + 2R3}$$

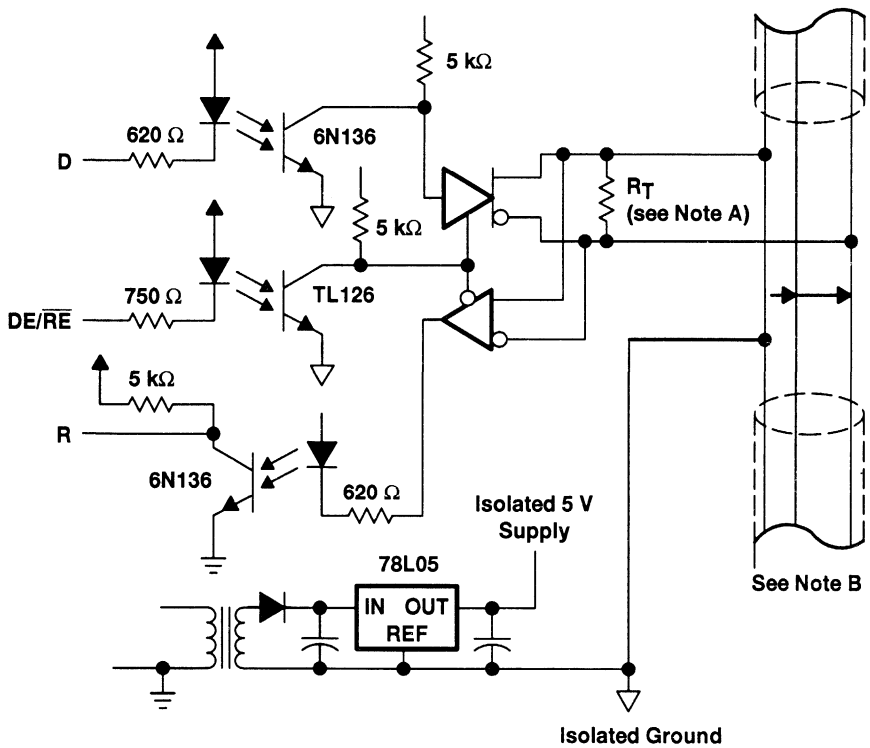
The fourth and final constraint comes from the signal attenuation that the fail-safe circuit causes.

3.3.3 Galvanic Isolation

Computer and industrial serial interfacing are areas where noise can seriously affect the integrity of data transfer. A proven route to improved noise performance for any interface system is galvanic isolation.

Such isolation in data communication systems is achieved without direct galvanic connection or wires between drivers and receivers. Magnetic linkage from transformers provide the power for the system, and optical linkage provides the data connection. Galvanic isolation removes the ground loop currents from data lines; and, hence, the impressed noise voltage that affects the signal are also eliminated. Common-mode noise effects can be completely removed and many forms of radiated noise can be reduced to negligible limits using this technique.

For example consider the case of a process control system where the interface node, shown in Figure 3–9, connects between a data logger and host computer via a RS-485 link.



NOTES: A: The line matching resistor, R_T, is used only at the ends of the cable. Terminated fail-safe circuitry may also be included at one point on the bus.

B. Shield should be terminated to each chassis ground and earth ground at one point only. the third-wire ground should be earth grounded at one point only.

Figure 3–9. Process Control SN75LBC176

When an adjacent electric motor starts up, a momentary difference in ground potentials at the data logger and at the computer may occur due to a surge in current. If no isolation scheme is employed for the data communication path, data may be lost during the surge interval and, in the worst case, damage to the computer could occur.

Circuit Description – The schematic shown in Figure 3–9 forms a one node interface for a distributed controlling, regulation, and supervision (DSCRS) system. Such a scheme could be used in a process control application. Transmission takes place via a two-wire bus, formed by a twisted-pair and ground wire with an overall shield connected in a ring circuit. Low power is useful in this type of application since many remote outstations are either battery operated or require battery backup capability and the size of the isolation transformer can be kept small. The bus driver used is the SN75LBC176. It was chosen for its low power consumption.

Galvanic isolation is provided by means of three optocouplers/optoisolators. The 6N136 is chosen for its high data rate capability, t_p = 75 ns (max), and its high voltage isolation.

The 6N136 is designed for use in high-speed digital interfacing applications that require high—voltage isolation between the input and the output. Its use is highly recommended in extremely high-ground-noise and induced-noise environments.

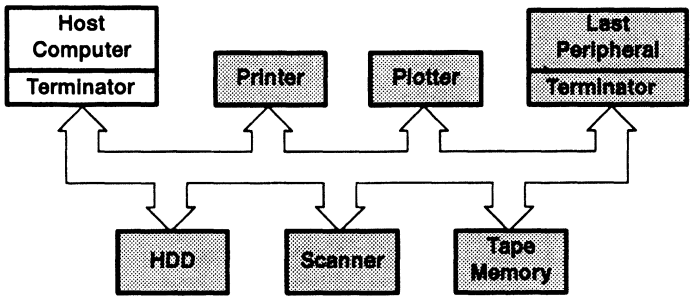
The 6N136 consists of a GaAsP light-emitting diode and integrated light detector, compose of a photo diode, a high-gain amplifier and a Shottky-clamped open-collector output transistor. An input diode forward current of 5 mA switches the output transistor low, providing an on state drive current of 13 mA (eight 1.6 mA TTL loads). A TTL input is provided for applications that require output transistor gating.

Housed in a single 8-terminal dual-inline-plastic package, the 6N136 is characterized for operation over the temperature range of 0°C to 70°C. The internal Faraday shield provides a common-mode transient immunity of 1000 Vμs.

4 Interface Circuits for SCSI

4.1 SCSI Overview

Small Computer Systems Interface (SCSI) details the ANSI specification for a peripheral bus and command set. The specifications defines a high-performance peripheral interface that distributes data independently of its host, helping to free up the host for more user-oriented commands. Already there are a large number of disk drives, notebook PCs and CD-ROM drives incorporating a SCSI port (see Figure 4–1).



- **Multipoint Half-Duplex Transmission**
- **18 (8-Bit Data) or 27 (16-Bit Data) I/O Lines**
- **Single-Ended and Differential (RS-485) Interface**
- **25-Meter Line Length for Differential SCSI**
- **Up to 10 Million Data Transfers Per Second**

Figure 4–1. Typical SCSI Peripheral Bus Layout

Basic SCSI is an 8-bit parallel I/O bus with a parity checking line and nine control/handshake lines making 18 lines total. More recently, in order to increase the data throughput, the data bus has been increased to 16 bits with two parity bits while maintaining the nine control lines, making a total of 27 lines. This is referred to as Wide SCSI.

4.1.1 SCSI Physical Layer

There are two electrical specifications referred to in the SCSI standard — single ended and differential.

It is beyond the scope of this section to discuss the complete SCSI standard, we shall concern ourselves here with the physical layer only. For more information on the standard you are encouraged to refer to the numerous publications on SCSI.

Single-Ended Interface – The single-ended driver and receiver configuration utilizes TTL logic levels and is primarily intended for applications with a cabinet, the maximum line length being limited to 6 meters and the data rate is normally limited to 5 million transfers per second (Mxfers/s), although careful system design can create a maximum transfer rate up to 10 Mxfers/s.

Differential Interface – The differential driver and receiver configuration uses the EIA RS-485 standard and is primarily concerned with transmitting data between cabinets, on heavily loaded buses, or in high-reliability systems with a maximum line length of 25 meters and data rates up to 10 Mxfers/s.

4.2 Single-Ended SCSI

4.2.1 Termination of Single-Ended Bus

Termination of the single-ended SCSI bus is becoming increasingly important as designers strive for faster system speeds. If error-free data rates of 10 Mbps over a 6-meter bus are to be achieved then signal integrity must be preserved. Termination reduces unfavorable transmission line effects such as reflections and distortion that can degrade system performance as signal speeds increase. Proper termination of bidirectional buses, such as SCSI, require terminators at each end of the cable.

4.2.2 Signal Transitions

The potential for high rates depends upon quick, clean transitions between low and high signal levels. The range of SCSI signals is shown in Figure 4–2. A low to high transition or deassertion of a signal is initiated by an open collector driver switching off and causing an instantaneous voltage step to travel down the line.

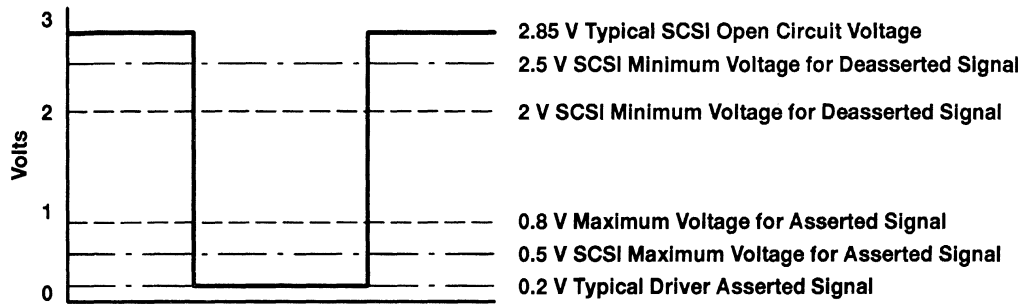


Figure 4–2. SCSI Bus Signal Range

The size of the first step on deassertion depends upon the amount of current in the line (I_L), the characteristic line impedance seen by the signal (Z_O), and the driver low-level output voltage (V_{OL}), and can be calculated as follows:

$$V_S = V_{OL} + Z_O I_L$$

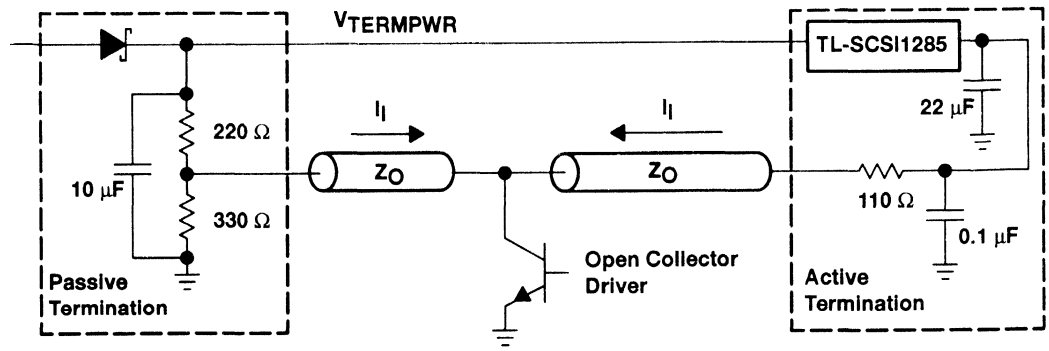
To achieve the maximum data rate the first step needs to exceed the receiver threshold voltage in a single transition. Although the 110 Ω impedance of a typical SCSI ribbon cable suggests that this requires only limited line-current capability, the impedance seen by a signal is always less than half the specified cable value. Extra capacitance due to peripheral connections to the bus, transmission line effects, and the position of the signal source can all combine to reduce the effective impedance to 30Ω or less.

To make up for this low impedance, it is the terminator's job to source as much current as possible during deassertion. This role is restricted by the SCSI specification, however, which limits each terminator to supplying a maximum of 24 mA to prevent the line current from exceeding the 48 mA current sink limit of the open collector drivers.

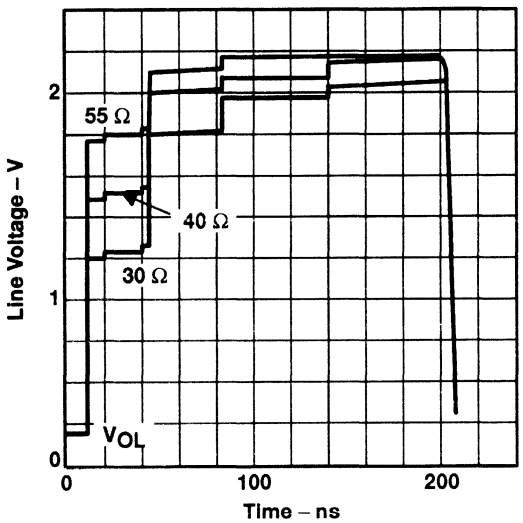
The role of the SCSI terminator is not confined to low-to-high signal transitions. Once a signal has been deasserted the terminator is required to bias the bus lines to the correct open circuit voltage level and thereby provide maximum noise margins.

4.2.3 Passive and Active SCSI Termination

SCSI termination has traditionally been carried out using passive termination networks. As illustrated in Figure 4–3 these consist of two resistors for each signal line; a 220 Ω pullup resistor connected to the termination power source (TERMPWR), and the 330 Ω pulldown resistor connected to ground. A Shottky diode is needed by all termination schemes to protect the power source from reverse currents.



High Data Rates Require Fast Transition From V_{OL} To >2 V



First Step Voltage Is $V_S = V_{OL} + Z_O I_I$

Line Impedance Varies With:
- **Cable Impedance**
- **Line Loading**

Line Current Depends Upon Termination Scheme <48 mA

Figure 4–3. Single-Ended SCSI Termination

This type of termination at each cable end typically results in a maximum line current of around 34 mA. Assuming the terminator is on a heavily loaded bus, signified by an impedance of approximately 32 Ω, the equation in Figure 4–3 gives a first step value of 1.76 V – well short of the desired 2-V level.

In additional to this limited current capability and the power consumption penalty imposed by the resistor dividers, passive terminators also suffer from an unregulated line bias voltage. As a result the line voltage fluctuates with variations in the load current and TERMPWR leading to smaller noise margins and reduced data rates.

The most common alternative to passive termination replaces the resistive network with a voltage regulator in series with a single 110-Ω resistor for each line (see Figure 4–3). This method, known as Active, Boulay, or alternative 2 termination, was developed to overcome two of the main shortcomings of passive termination.

The 110 Ω resistors increase the typical line current available on deassertion to 42 mA, which, from a transmission line viewpoint, is equivalent to a 35% increase in load impedance. The line current and the high-level noise margins are also more stable since TERMPWR is no longer used to set the bias voltage directly. Instead it is used to form the input to the voltage regulator, which then provides a regulated bias voltage (see Figure 4–4).

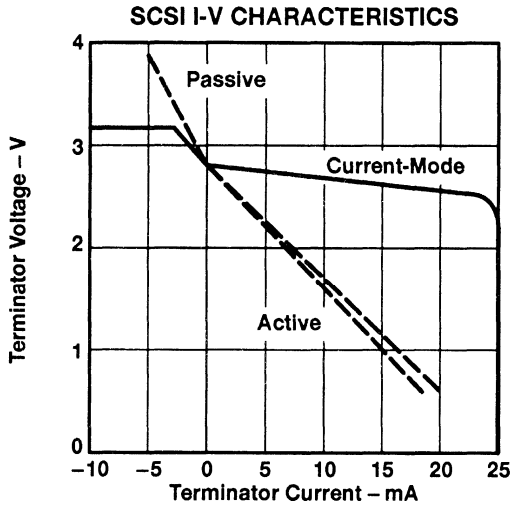
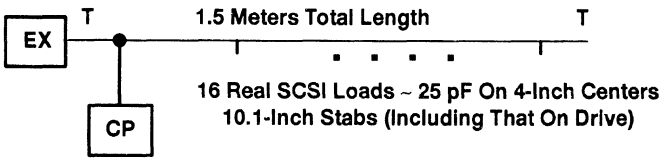


Figure 4–4. Current-Source Termination

4.2.4 Current-Source Termination Using the SN75LBC968

There are numerous analog problems associated with driving the single-ended SCSI bus and single-ended parallel buses in general. The SN75LBC968 addresses most of them. This devices exhibits the analog performance to maximize first-step assertion levels in wired-OR lines and minimize radiated emissions, crosstalk, and radiated emission susceptibility.



SCSI Data Only, Active Negation All Lines
Four Inches Between Exciter and Comparator

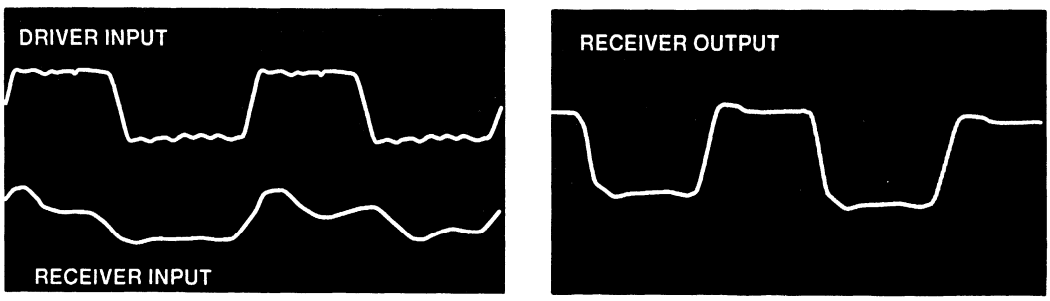


Figure 4–5. High First-Level Step Comparisons

The fundamental cause of the low first-step level is added loading of the bus with distributed capacitance from the attached devices. The '968 addresses this by offering a lower capacitance to the bus of only 13.5 pF and nearly one-half of the maximum allowed by standard. The current-mode termination of the SN75LBC968 supplies a constant current to the line when the bus voltage falls below 2.5 V. This makes the termination current (and the next low-to-high voltage step) independent of the low-level (asserted) bus voltage, unlike voltage-mode terminators. The constant current supplied by the '968 provides 16% more minimum current than Boulay termination and 33% more than passive termination. This extra current translates directly to first-step noise margin. The line drivers of the SN75LBC968 have a feature that was introduced in the SCSI standards to address the first-step problem and is called active negation. This active negation is a controlled amount of output current from the driver during the transition from assertion to negation and is now required on the highest speed versions of SCSI.

As we know, there is a capacitance between parallel conductors that is a function of the dielectric, distance, and conductor shape. We also know that the magnitude of the current through a capacitor is the product of e, ω, and C, where e is the voltage across the capacitance, C is the capacitance, and ω is the angular frequency ($2\pi f$) of the signal. In a parallel data bus, the current through this coupling capacitance generates a noise voltage in adjacent signal lines and, if large enough, can cause erroneous interpretation of the signal logic state. This is crosstalk and is a major limitation to the ultimate data transfer rates of single-ended parallel buses.

Since there is usually little that can be done with C or e, the SN75LBC968 driver circuit reduces the amount of crosstalk by limiting ω. The highest frequency in a binary signal is present in the transition between logic states. By necessity, three to five times the fundamental switching frequency is required to adequately define the instance between states. However, energy at higher frequencies is not needed for data transmission and can only lead to more emissions and crosstalk.

Since all single-ended SCSI drivers may not be as analog friendly as the '968s, the receiver of this device has a noise filter and a large amount of input hysteresis to reject all but the wanted signals. The noise filter rejects voltage spikes less than 5 ns while the 600 mV of hysteresis rejects lower frequency noise with magnitudes below this level. These features not only help reject crosstalk-induced noise, but make the bus less susceptible to noise from sources outside the bus as well.

Nine current-mode terminators have been integrated with nine-lines drivers and receivers that provides a common multiple to the byte-parity-arranged SCSI bus. With the nine control lines, an 8-bit SCSI bus can be implemented with two transceivers, a 16-bit bus with three, a 32-bit bus with five, and so on. The other features of this device, such as 3-V logic compatible inputs, power-up/-down glitch protection, and shrink small-outline packaging with flow-through architecture, make this an excellent solution to driving high-speed parallel data buses with single-ended signals

4.2.5 Power Considerations

As well as enabling increased date rates, termination also increases the power consumption of a SCSI system. As SCSI has found increased usage in portable or battery powered systems, this has become more important. Exactly how much more power is needed depends upon the method of termination, but this is not quite as obvious as it may first seem.

During data-on periods, the power dissipation of each of SCSI termination method is very similar. For an 8-bit bus with all the data lines asserted, the power dissipation in the termination is approximately 1 W.

During data-off periods the position significantly changes. The resistor dividers of a passive terminator still draws around 750 mW of power. Both the SN75LBC968 and Boulay terminators, however, require a total quiescent current of less then 10 mA, providing a 30× saving in power consumption.

4.3 Differential SCSI

4.3.1 SN75LBC976DL: Two-Chip Differential SCSI

Much debate has taken place on differential versus single-ended SCSI for data rates above 5 million transfers per second (Mxfers/s). It is clear, however, that for data rates approaching 10 Mxfers/s and at line lengths in excess of a few meters, differential SCSI is essential.

As we discussed earlier, the standard 8-bit interface is made up of eight data lines, one parity bit, and nine control lines, making 18 channels in total. The only differential transceivers capable of transmitting at a 10 Mxfers/s data rate have utilized the low-power schottky (LS) and advanced low-power schottky (ALS) technologies. Using these technologies and considering the 18 transceivers for each interface, the power consumption is quite considerable, 2.4 W with all drivers disabled. Turn the drivers on and the power consumption rises to nearly 4 W.

From a designer's viewpoint, 2.4 W is a considerable amount of heat to remove from a system. This is evident in the case of compact hard disk drives where equipment size is a limiting a element. A further factor is board area, using one discrete transceiver foe each channel (i.e., eighteen 8-pin SO packages) is unacceptable for many applications.

From a semiconductor designer's view point, integrating a number of transceivers is of course possible however, the limiting factor once again is power dissipation. The SN75LBC976 is designed to overcome both the problems of power dissipation and integration (see Figure 4–6). The device incorporates on a single IC, nine RS-485 configurable transceivers, each capable of transmitting at 10 Mxfers/s. This is made possible using LinBiCMOS™ technology. With all drivers disabled, the quiescent power consumption of the 'LBC976 is a mere 1.5 mW, with all drivers enabled the quiescent consumption rises to 45 mW, a considerable saving over LS and ALS parts. The package size has also been reduced to a minimum using the 0.635 mm pitch 56-pin shrink small-outline package (SSOP) which reduces board area significantly compared with alternate packages such as plastic leaded chip carrier (PLCC). The reader should note that irrespective of the device power, there is still the relatively high line current. The SSOP package has been thermally enhanced to handle this level of power dissipation. We will cover this point later as we look at the thermal characteristics of the package.

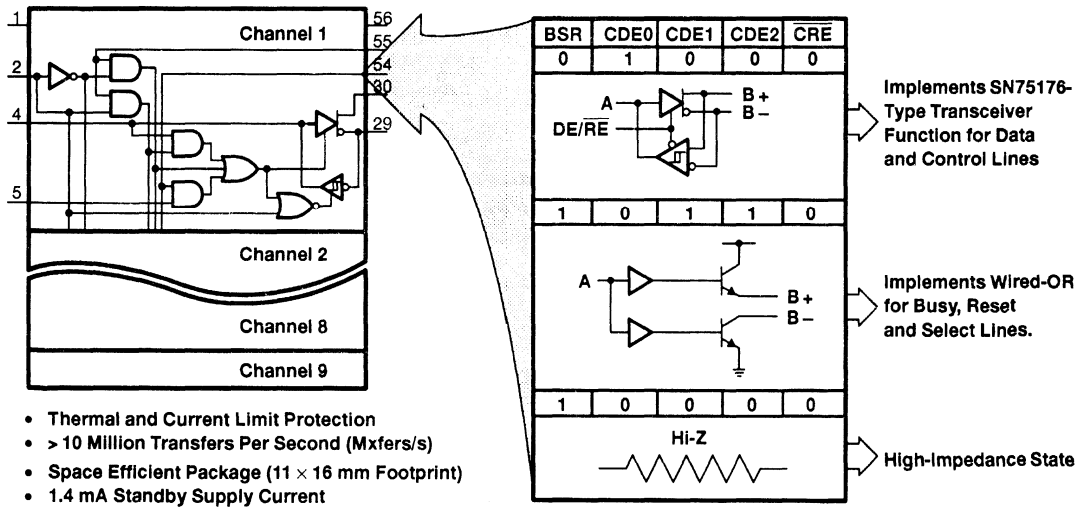


Figure 4–6. The SN75LBC976 Used In A Two-Chip Differential SCSI

LinBiCMOS is a trademark of Texas Instruments Incorporated.

The SN75LBC976 is fully configurable for connection to any type of SCSI system arrangement. The nine channels can be arranged into seven possible channel functions using the BSR, CDE0, CDE1, CDE2, $\overline{CRE}$ control terminals.

The 7 channel configurations are:

- Transparent permanently enabled receiver
- Transparent permanently enabled driver
- Bidirectional transceiver with direction control
- Driver with enable control
- Open-ended driver for wired-OR control lines
- Driver with ORed data and enable lines
- Permanent high-impedance state

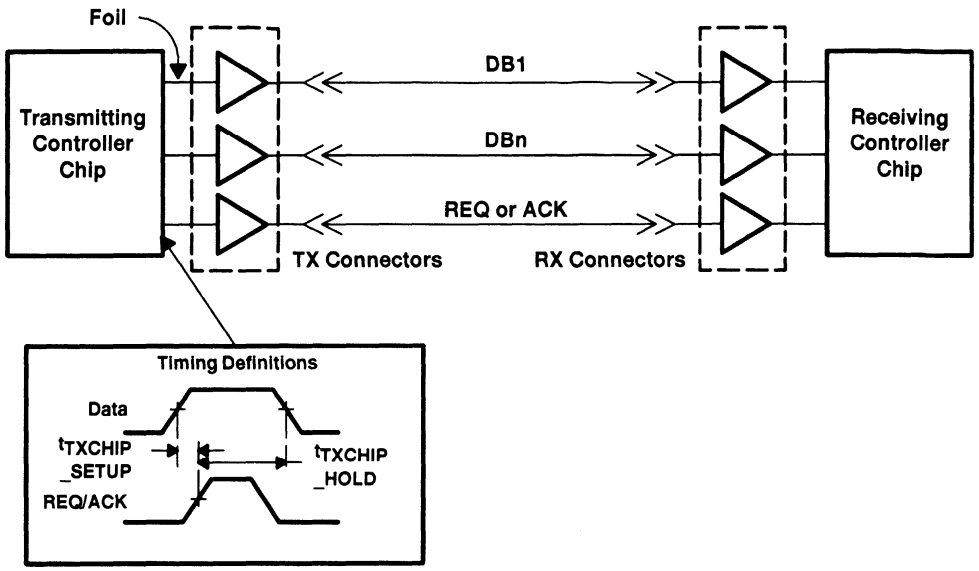
4.3.2 SCSI Skew Considerations

SCSI, as we have discussed, is a parallel data bus. This is also the case with the intelligent peripheral interface (IPI). IPI is similar to SCSI in that it is a high-speed peripheral bus with the same high-speed differential interface requirements. Being parallel, both standards transfer data over the cable more than one bit at a time. SCSI and IPI allow 8-bit (one byte) or a 16-bit (one word) data width and transfers as often as once every 100 ns or 10 million transfers per second.

Since the logical state of any one bit can change every 100 ns, this defines a period during which the logical state should be valid across the bus. This is the unit interval (UI). The voltage transitions that define the start and end of the UI can propagate along the bus at different velocities due to the physical differences along each electrical path. So the original UI at the start of the electrical path is different at the destination.

Time variation of the defining voltage transitions is typically called skew. The limit for skew, designated $t_{sk(lim)}$, is the fastest propagation delay minus the slowest propagation delay along any part of the bus. This, in effect, reduces the UI by $t_{sk(lim)}$ establishing a minimum unit interval, UI_{min}, that can be transmitted with a particular data bus.

The proposed SCSI-3 standard for fast transfers (10 Mxfers/s), defines UI_{min} in terms of setup and hold times at the SCSI connector for interoperability with any other SCSI device. At the time this document is being written the requirements are as shown in Figure 4–7.



SCSI-3 Standard Requirements:

- $t_{TXCHIP\_SETUP} - t_{SK\_DRVR} - t_{SK\_FOIL} = t_{TXCONNECTOR\_SETUP} \geq 23$ ns
- $t_{TXCHIP\_HOLD} - t_{SK\_DRVR} - t_{SK\_FOIL} = t_{TXCONNECTOR\_HOLD} \geq 33$ ns
- $t_{RXCONNECTOR\_SETUP} = t_{RXCHIP\_SETUP} - t_{SK\_RCVR} - t_{SK\_FOIL} \geq 15$ ns
- $t_{RXCONNECTOR\_HOLD} = t_{RXCHIP\_SETUP} - t_{SK\_RCVR} - t_{SK\_FOIL} \geq 25$ ns

Figure 4–7. SCSI-3 Fast Transfer Skew Budget

The budget behind the connector is left to the designer and depends upon the SCSI controller, transceivers, and layout being used. Table 4–1 shows some skew budget examples with various controller chips that comply with the requirements at the SCSI connector. The recommended column is data for the worst case number for SCSI controllers surveyed by the SCSI SPI working group and budgets 8 ns for the external driver and 9 ns for the external receiver. This is the origin of the $t_{sk(lim)}$ specifications in the SN75LBC976 data sheet

Table 4–1. Transceiver Skew Budgets for Various SCSI Controllers

PARAMETER	RECOMMENDED BUDGET	VENDOR A	VENDOR B	VENDOR C	UNITS
min Tx_controller_setup =	32	30	35	35	ns
min Tx_controller_hold =	42	42	45	45	ns
min Rx_controller_setup =	5	0	5	0	ns
min Rx_controller_hol =	15	20	15	10	ns
t_{sk_etch} =	1	1	1	1	ns
max t_{sk_dvr} =	8	6	11	11	ns
max t_{sk_rvc} =	9	4	9	14	ns

The time it takes one transceiver of the 'LBC976 to change logic states is called the propagation delay time. For a driver this is designated as $t_{d(D)}$ and a receiver this is designated t_{pd} and does not differentiate whether the logical transition is from high-to-low or low-to-high level. The $t_{sk(lim)}$, as specified in the data sheet and the recommendation of the SCSI standard are assured by measuring the propagation delay time of each channel of each 'LBC976 and accepting only those devices within the specified $t_{sk(lim)}$ range. To keep the production costs of the 'LBC976 reasonable, these tests are done at 25°C and at 70°C ambient temperatures at a V_{CC} of 5 V.

Admittedly, the die temperatures and supply voltage are all the same (or nearly the same) during TI's production testing and not necessarily the same would be seen in actual use. However, the sensitivity of the propagation delay times to these factors is the same and is repeatable from device to device. In other words, as long as the operating environment of all of the SCSI interface channels is similar, the change in propagation delay times from the data sheet conditions are the same. This maintains the $t_{sk(lim)}$ specification even though the actual propagation delay times may change.

It is nearly impossible to predict the instantaneous die temperatures of these devices in actual use. Due to the nondeterministic nature of the state of any one channel and the averaging affect of nine channels and of the package thermal time constant, the die temperature must be considered using the mean power dissipation. It is also reasonable to assume that mean power dissipation of separate devices on the same printed circuit board to be close to each other and the temperature of the air around them does not have a large gradient between them. Even if there is an air temperature gradient of 45°C, there would be only about a 2-ns difference in the driver propagation delay times and little or no difference in the receiver propagation delay times. If such a temperature gradient actually existed across a board, it is likely that skew budgets are not going to be the problem with the equipment.

4.3.3 SN75LBC976 Channel Power Dissipation Considerations

Channel Power Dissipation – To understand the SN75LBC976 power dissipation when connected to a SCSI bus and the subsequent heat-sinking requirements, we need to develop a realistic model for the power consumption under working conditions. We must consider the power dissipation within the silicon. There are three primary sources — the dc quiescent power, the ac or switching power, and the dc or resistive losses in the output drivers.

The current necessary to bias the circuits of a single enabled 'LBC976 differential driver is typically 0.53 mA and a maximum of 1.1 mA. A single enabled receiver circuit requires 3.22 mA typically and 5 mA maximum. The typical values have been measured on 94 SN75LBC976DLs from three different wafer lots. The maximums have been verified over temperature on the same samples.

It follows that the driver quiescent power consumption, P_{DCC} is:

$$P_{DCC} = I_{CC} \times V_{CC}$$

$$= 0.53 \text{ mA} \times 5 \text{ V} = 2.65 \text{ mW/channel average}$$

$$= 1.11 \text{ mA} \times 5.25 \text{ V} = 5.83 \text{ mW/channel maximum}$$

And the receiver quiescent power, P_{RCC} is:

$$P_{RCC} = I_{CC} \times V_{CC}$$

$$= 3.22 \text{ mA} \times 5 \text{ V} = 16.10 \text{ mW/channel average}$$

$$= 5 \text{ mA} \times 5.25 \text{ V} = 26.25 \text{ mW/channel maximum}$$

The average I_{CC} of a representative sampling of the SN75LBC976 has been measured to be 9.77 mA for nine unloaded drivers switching at 5 MHz (10 Mbps), a 50% duty cycle, and with V_{CC} = 5 V. Nine receivers at the same frequency and duty cycle and unloaded outputs consumed 36 mA average. Since both measurements include P_{DCC} or P_{RCC}, they are subtracted below:

Driver switching losses, P_{DAC}, at 5 MHz:

$$P_{DAC} + P_{DCC(average)} = \left(I_{CC(average)}/9\right) \times V_{CC}$$

$$P_{DAC} = \left(I_{CC(average)}/9\right) \times V_{CC} - P_{DCC(average)}$$

$$= (97.7/9) \times 5 - 2.65$$

$$= 51.6 \text{ mW/channel}$$

Receiver switching losses, P_{RAC}, at 5 MHz:

$$P_{RAC} + P_{RCC(average)} = \left(I_{CC(average)}/9\right) \times V_{CC}$$

$$P_{DAC} = \left(I_{CC(average)}/9\right) \times V_{CC} - P_{RCC(average)}$$

$$= (36 \text{ mA}/9) \times 5 \text{ V} - 16.10$$

$$= 3.9 \text{ mW/channel}$$

The output stage losses vary with the magnitude of the output voltages or the output transistor saturation voltages and with the load conditions. The following is based upon the solution of the equivalent circuit of a differential SCSI bus and no further proof is included in this analysis.

For the differential driver, the worst case condition is with a driver asserting the line with SCSI bus termination and a differential output voltage of about 2 V. Under these conditions there would be 144 mW dissipated in the output transistors when asserted and 71 mW when negated. The average output voltage of the SN75LBC976 driver is 2 V. As such, the average power dissipated in the output transistors is also a worst case condition.

Driver output dc losses with the line asserted, P_{DOH}, is given by:

$$P_{DOH} = 144 \text{ mW/Channel}$$

Driver output dc losses with the line negated:

$$P_{DOL} = 71 \text{ mW/Channel}$$

The receiver output stage is rated for sinking 8 mA at a maximum low-level output voltage of 0.8 V.

Receiver output dc losses, P_{RO}, is given by:

$$P_{RO} = 8 \text{ mA} \times 0.8 \text{ V} = 6.4 \text{ mW/Channel maximum}$$

Since $P_{DCC} + P_{DAC} + P_{DO} >> P_{RCC} + P_{RAC} + P_{RO}$, the worst case power dissipation in a data channel occurs when the driver is enabled and transmitting data. This case is used to analyze the device power dissipation.

Device Power Dissipation – Assuming the probability that any one bit on the bus is asserted is equal to the probability of any one bit on the bus being negated, the state of the output is nondeterministic, and the thermal time constant of the device is long with respect to the data transfer period, the die temperature is determined by the mean power dissipation. In the driver output, this is the mean of the asserted and negative values:

Mean device output dc losses:

$$P_{DO(DEV)} = (P_{DOH} + P_{DOL})/2 \times 9 \text{ channels}$$

$$= (144 \text{ mW/Ch} + 71 \text{ mW/Ch})/2 \times 9 \text{ channels}$$

$$= 967.5 \text{ mW}$$

From the assumptions above and the probability that the driver output changes state on the next cycle is equal to the probability that it does not, the mean power dissipated due to driver switching is one-half P_{DAC}, which was measured with the switching loss occurring every cycle.

Mean device switching losses:

$$P_{DAC(DEV)} = P_{DAC}/2 \times 9 \text{ channels}$$

$$= (51.6 \text{ mW/ch})/2 \times 9 \text{ channels}$$

$$= 232.2 \text{ mW}$$

Total device quiescent power:

$$P_{DCC(DEV)} = P_{DCC(average)} \times 9 \text{ channels}$$

$$= 2.65 \text{ mW/Ch} \times 9 \text{ channels}$$

$$= 23.85 \text{ mW}$$

The total mean power dissipated in nine enable drivers transmitting over a SCSI bus for several package thermal time constants is then:

$$P_{D(DEV)} = P_{DO(DEV)} + P_{DAC(DEV)} + P_{DCC(DEV)}$$

$$= 967.5 \text{ mW} + 232.2 \text{ mW} + 23.85 \text{ mW}$$

$$= 1223.6 \text{ mW}$$

4.3.4 Junction Temperature and Layout Considerations

Measurements of the thermally enhanced 56-pin SSOP package and lead frame (see Figure 4–8) used on the SN75LBC976DL were performed on a 130 mm × 98 mm six-layer printer circuit board with the ground and heat-sinking terminals connected to a second layer ground plane through the first via interconnect. The ground plane was 0.254 mm below the surface of the board and was a 1-oz. copper layer. The two tests resulted in junction temperature rise above ambient temperatures of 52.9 and 46.6°C/W with zero air flow.

The mean junction temperature rise above ambient when all drivers are enabled and transmitting data over the SCSI bus for several package thermal time constants can then be calculated using the following.

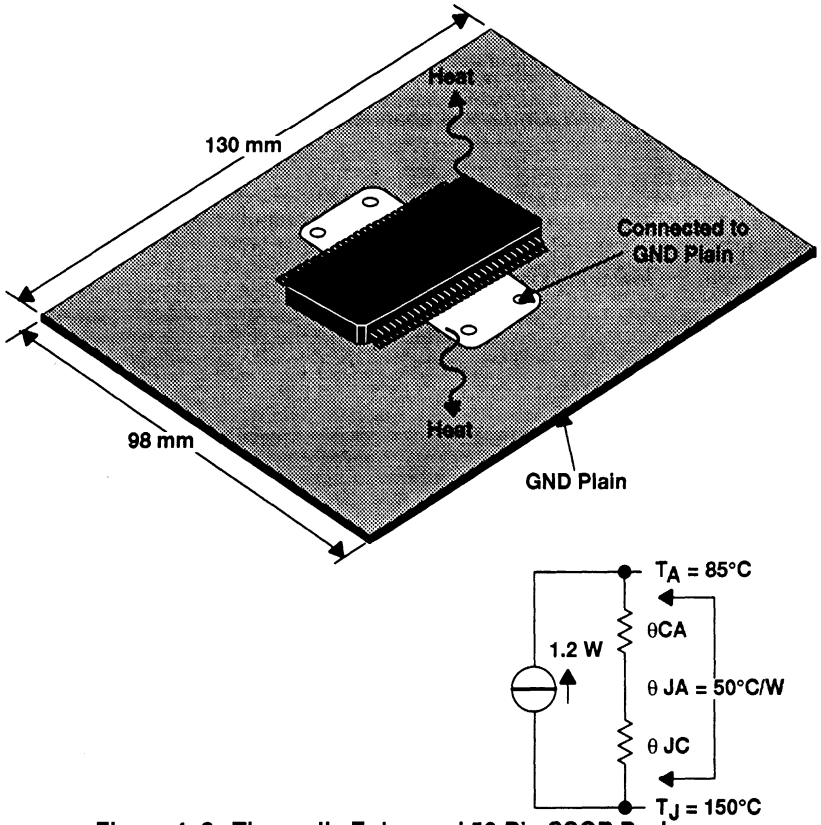


Figure 4–8. Thermally Enhanced 56-Pin SSOP Package

Junction temperature rise above ambient:

$$T_J - T_A = \theta_{JA} \times P_{D(DEV)}$$

$$= (52.9°C/W + 46.6°C/W)/2 \times 1233.6\ mW \times 1\ W/1000\ mW$$

$$= 60.8°C$$

Most designs require two junction temperature conditions to be met. The junction operation temperature should not exceed 150°C under worst case operating conditions and the average operating junction temperature should be no more than 110°C.

Since the worst case condition of all nine channels transmitting data was used for analysis, the maximum ambient air temperature (T_A) with no air flow should be:

$$T_{A(max)} = 150°C - 60.8°C = 89.2°C$$

When evaluation the average operating junction temperature the effects of transmit/receive duty cycle communication port activity must be taken into account.

4.4 Driving the Wired-OR SCSI LInes with the SN75LBC976

The control lines of the SCSI bus have three Wired-OR lines, they are busy (BSY), reset (RST), and select (SEL). These lines are wired-OR in that the line drivers connected to these lines drive in one direction only (assertion) and are 3-stated (high impedance) when negated. This allows numerous drivers to be active at the same time without affecting the logic state of the line and requires that all drivers be released or off before the logical state can change. When 3-stated, the bus termination network passively negates the signal.

The technique used for wired-OR operation with differential transceivers is to input the signal into the driver enable terminal and connect the driver input to a fixed logic level input. When the input signal to the driver enable is active (high), the driver becomes enabled and the outputs drive the SCSI bus to the state of the driver input. When the input signal at the driver enable goes low, the driver turns off and allows the bus termination to negate the signal on the bus after all other drivers on the bus are also shut off.

Many communications controllers used for differential SCSI have separate inputs and outputs for these signals. When used with the SN75176-type RS-485 transceiver, these controller I/Os can be directly connected to separate driver enable inputs or receiver outputs. The SN75LBC976 device does not have a separate driver input and receiver input, these are tied together internally to save terminals.

Controllers with separate I/Os can still be used with the 'LBC976 using the connections shown in Figure 4–9. The controller output goes high and enables the driver and disables the receiver. Upon disabling the receiver, the external pullup or pulldown resistor drives terminal A of the 'LBC976 to the correct level for bus assertion and the driver asserts the SCSI signal line. When the controller output goes low, the driver disables and allows the termination to negate the bus signal. After a short delay, the receiver outputs are enabled and reflect the logical sate of the bus signal.

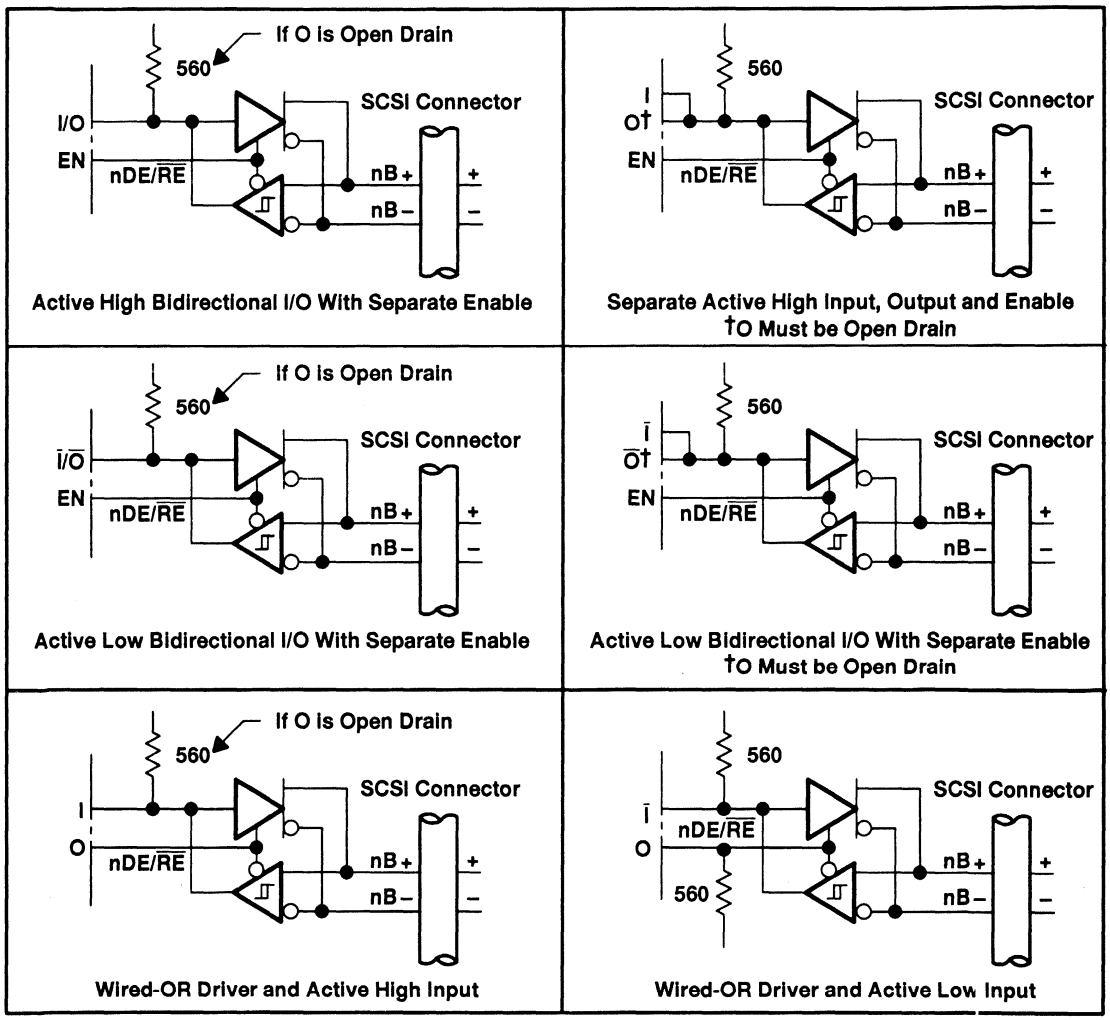


Figure 4–9. Typical SCSI Transceiver Connections

5 Summary and Further Information

5.1 EIA Standards

For details and a copy of the Catalog of EIA & Jedec Standards & Engineering Publications and for copies of EIA standards contact the Electronic Industries Association

EIA Standard Sales Office
2001 Pennsylvania Avenue, N.W.
Washington, D.C. 20006
United States
Telephone Number + 1 (202) 457–4966

5.2 References

The following books were invaluable in producing this section:

1. *Digital, Analog, and Data Communication*, – William Sinnema and Tom McGovern – Prentice-Hall International – ISBN 0-835-91313-9.
2. *Data Transmission*, – D. Tugal and O. Tugal – McGraw Hill

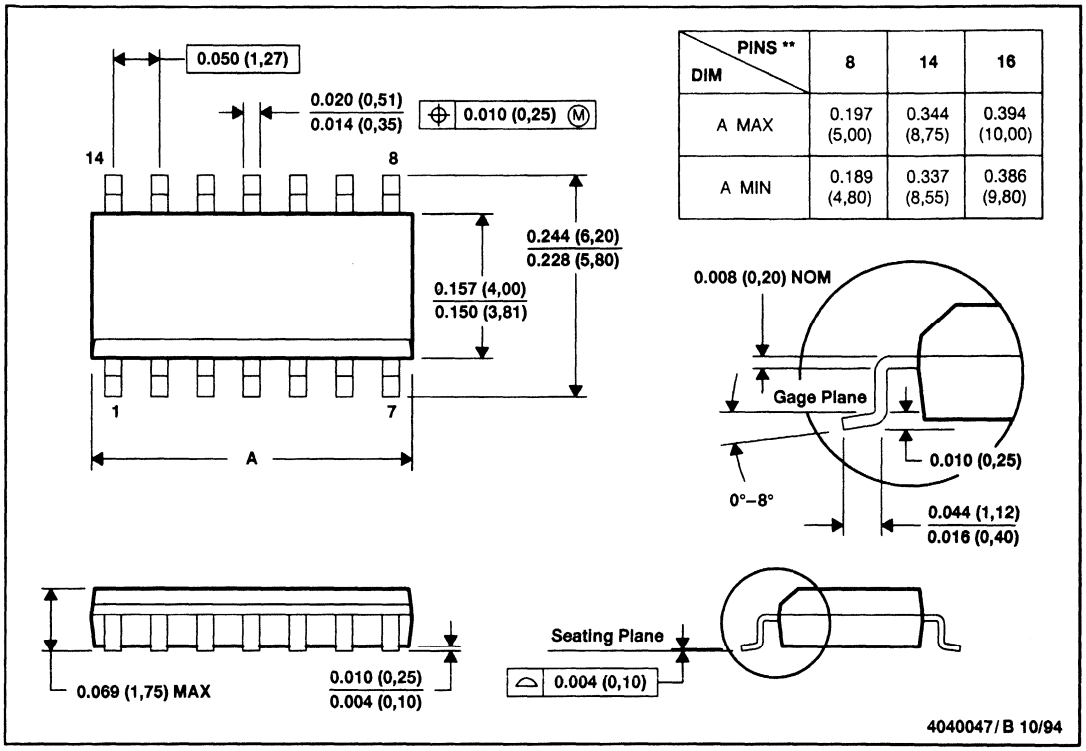
5 Mechanical Data

AUGUST 1995

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Four center pins are connected to die mount pad
E. Falls within JEDEC MS-012

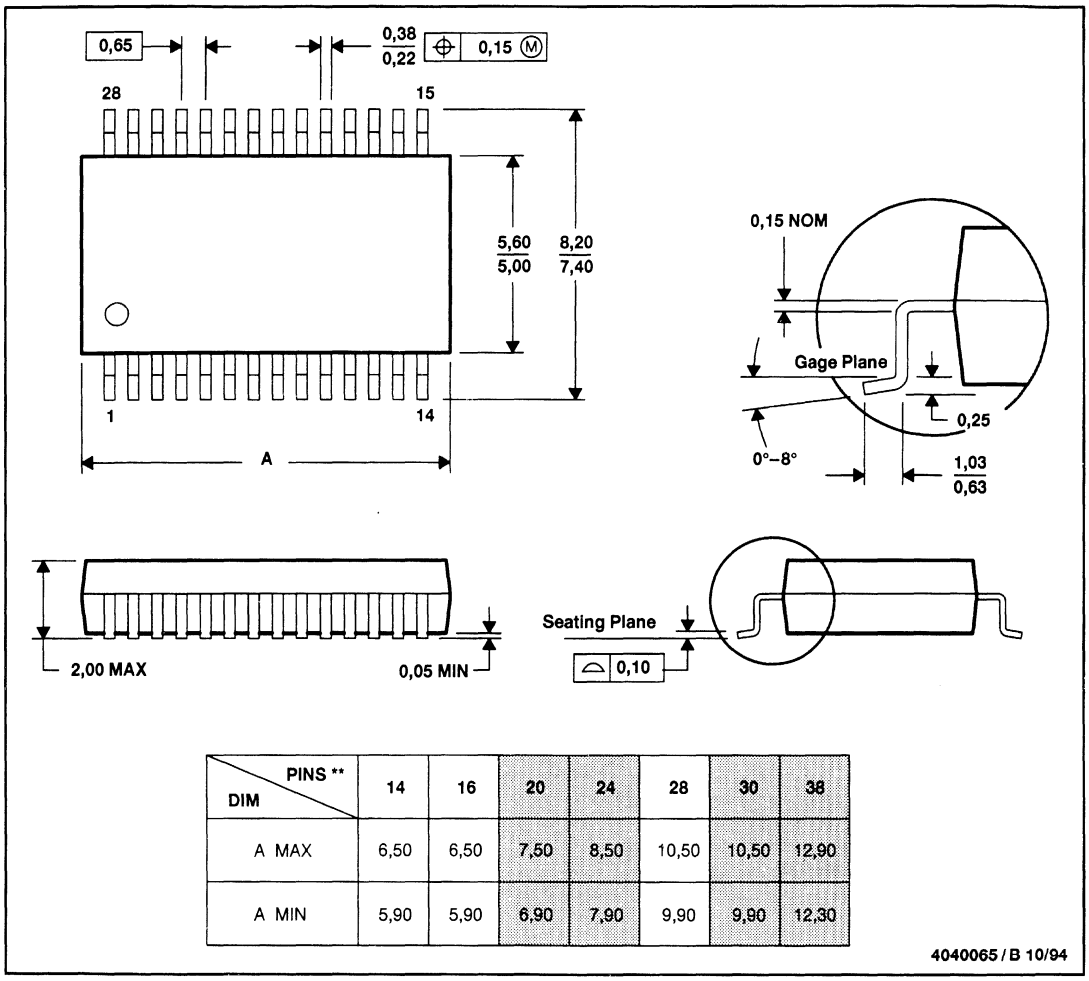
MECHANICAL DATA

AUGUST 1995

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

28 PIN SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

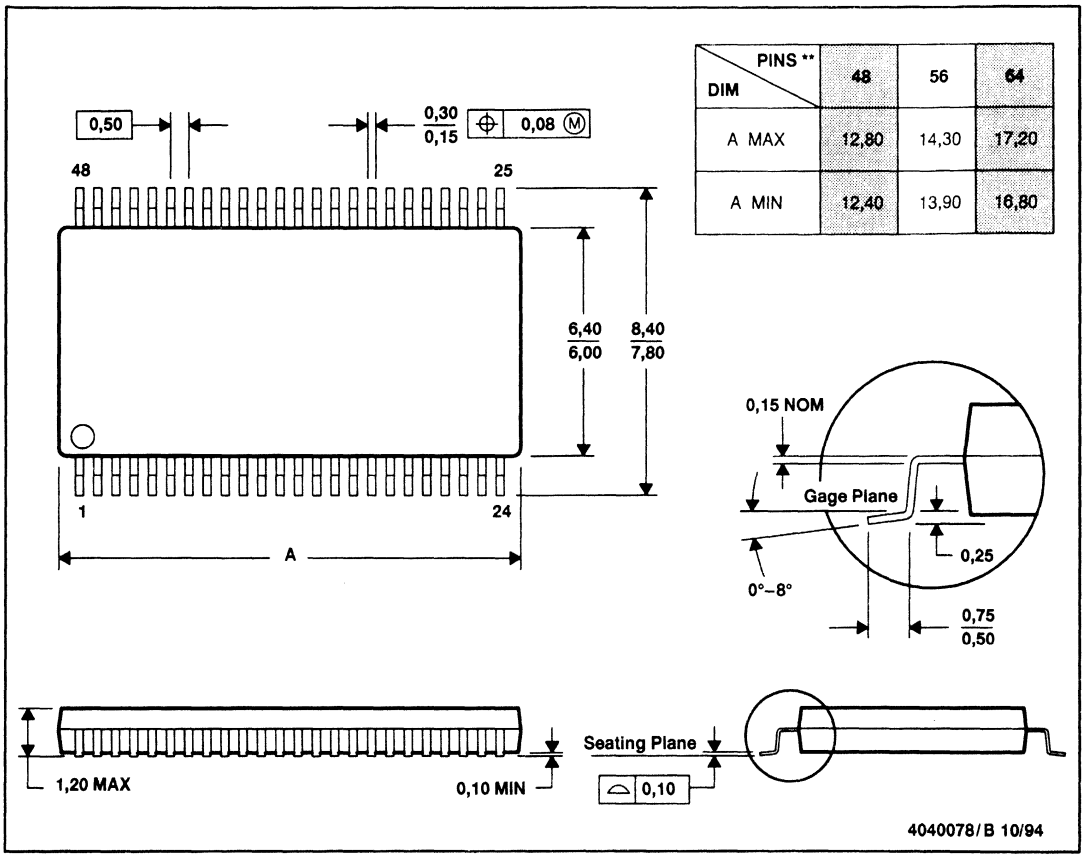
4040065 / B 10/94

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

AUGUST 1995

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PIN SHOWN



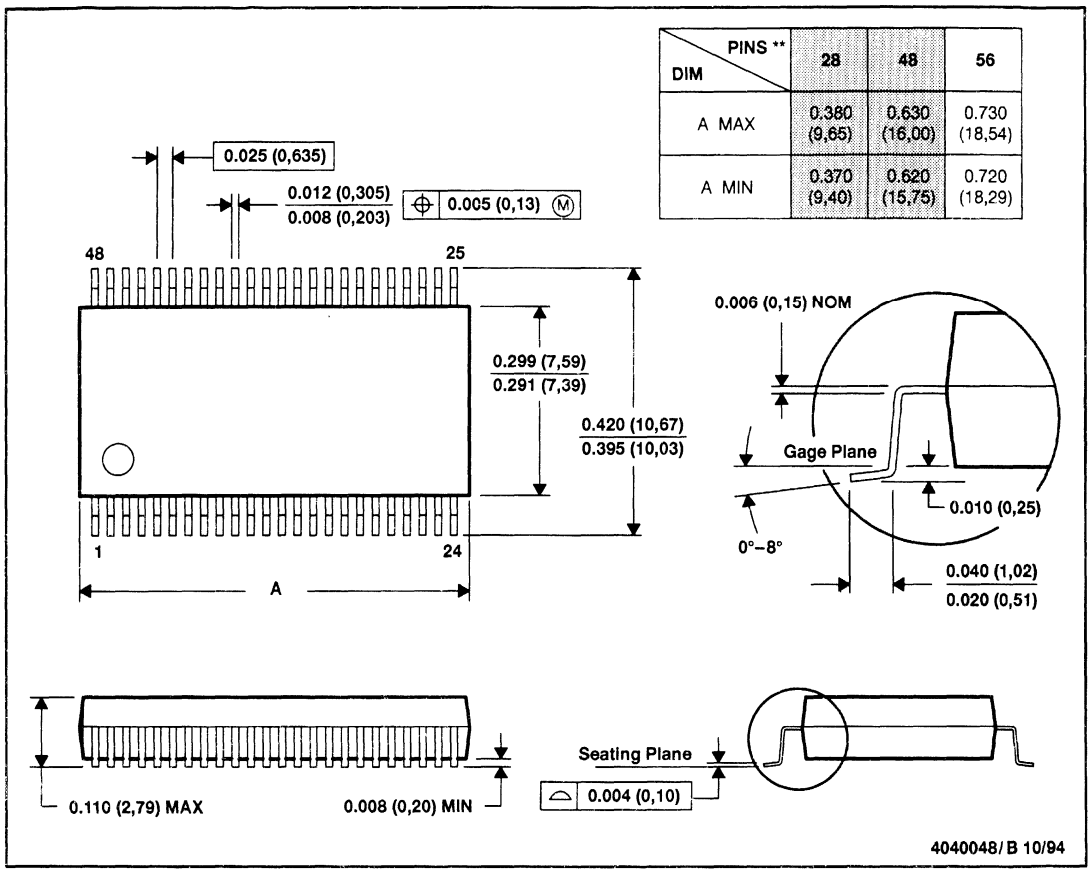
DIM \ PINS **	48	56	64
A MAX	12,80	14,30	17,20
A MIN	12,40	13,90	16,80

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

AUGUST 1995

DL (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PIN SHOWN



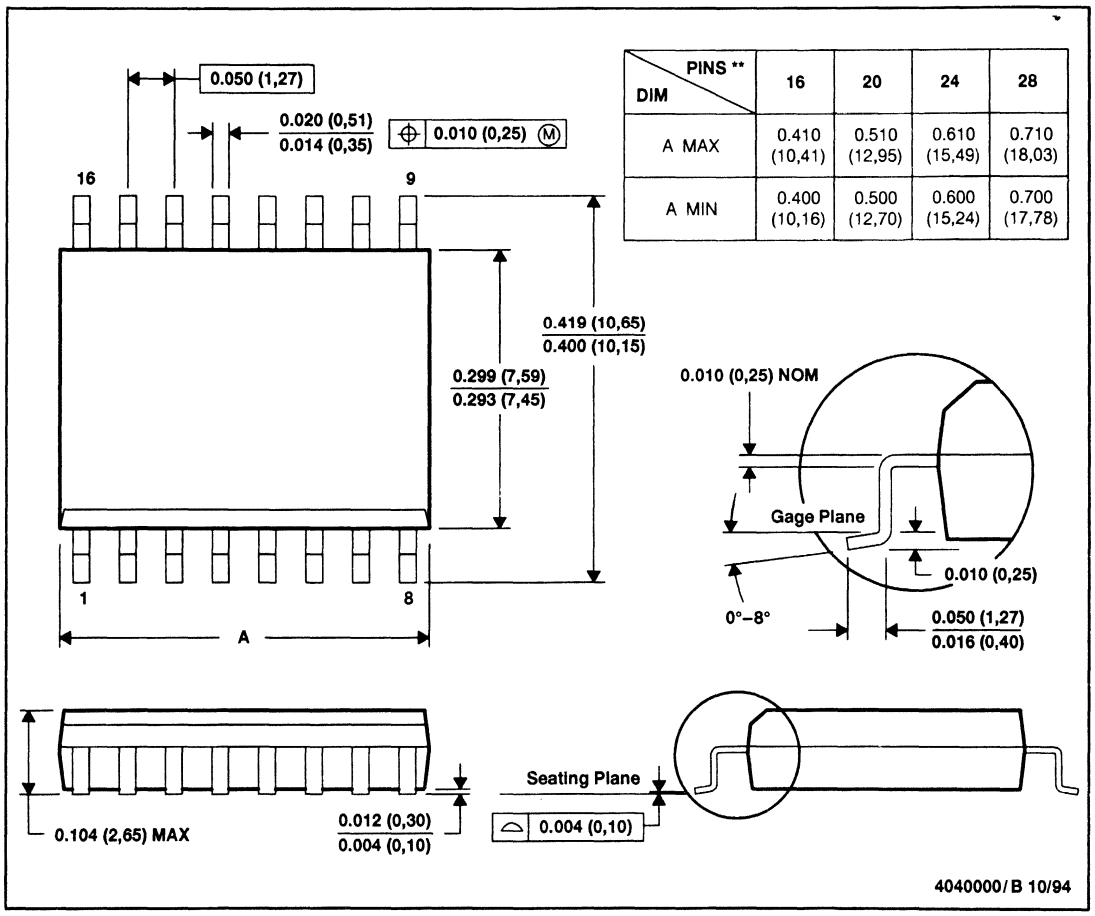
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

AUGUST 1995

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PIN SHOWN



DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

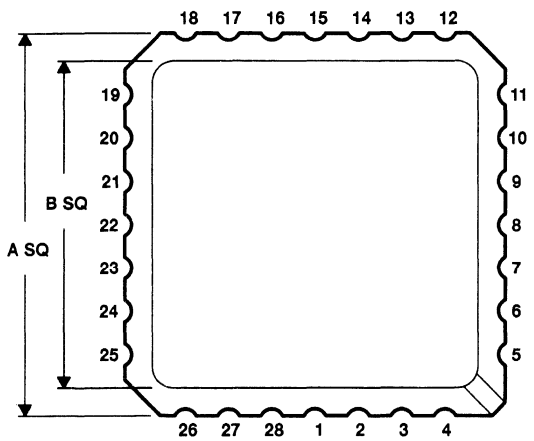
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

AUGUST 1995

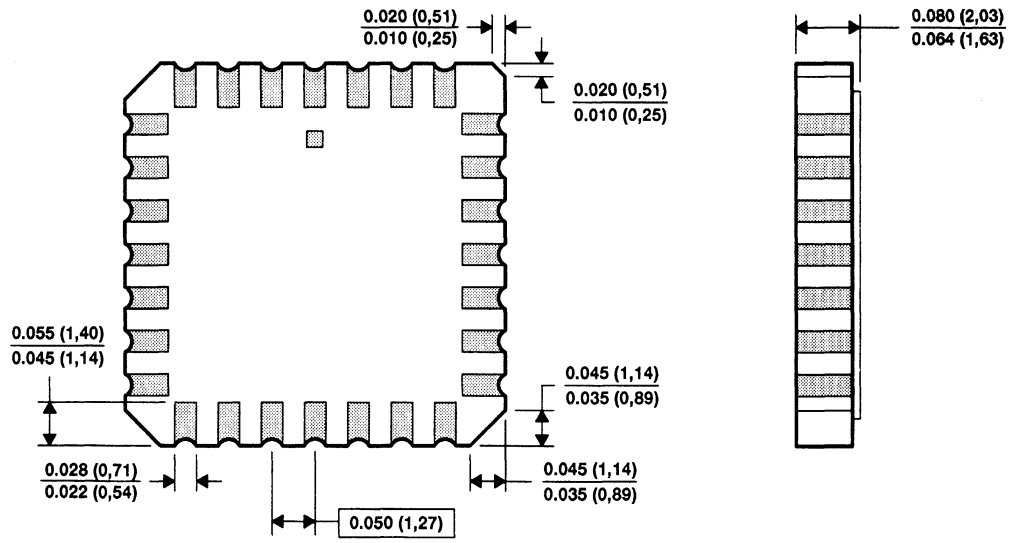
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.422 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.730 (18,78)	0.761 (19,32)	0.485 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



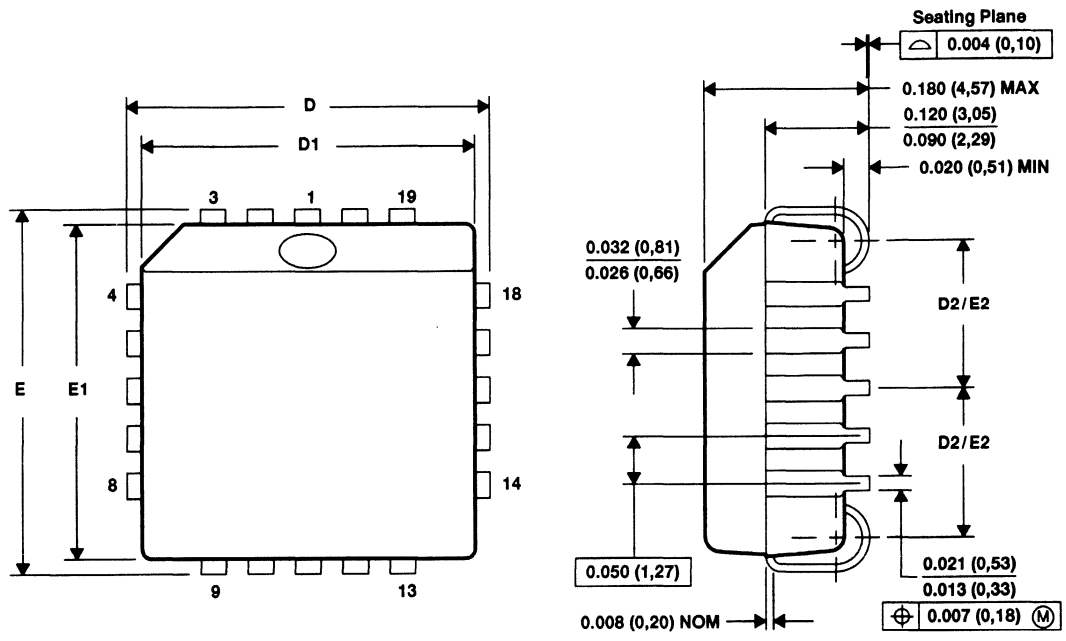
4040140/B 10/94

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

AUGUST 1995

FN (S-PQCC-J)** **PLASTIC J-LEADED CHIP CARRIER**

20 PIN SHOWN



NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 10/94

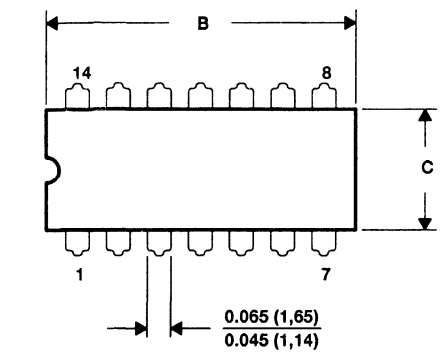
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

AUGUST 1995

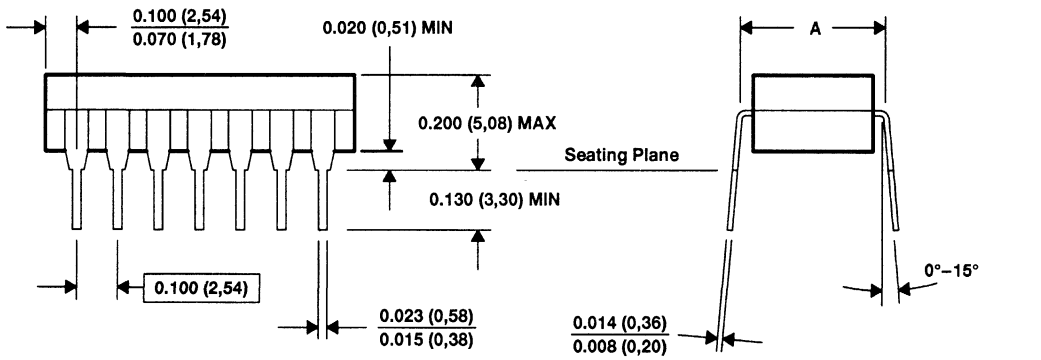
J (R-GDIP-T**)

CERAMIC DUAL-IN-LINE PACKAGE

14 PIN SHOWN



DIM \ PINS **	14	16	18	20	22
A MAX	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)	0.410 (10,41)
A MIN	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)	0.390 (9,91)
B MAX	0.785 (19,94)	0.785 (19,94)	0.910 (23,10)	0.975 (24,77)	1.100 (28,00)
B MIN	0.755 (19,18)	0.755 (19,18)	—	0.930 (23,62)	—
C MAX	0.280 (7,11)	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)	0.388 (9,65)
C MIN	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)	—



4040083/B 10/94

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only
E. Falls within MIL-STD-1835 GDIP1-T14, GDIP1-T16, GDIP1-T18, GDIP1-T20, and GDIP1-T22

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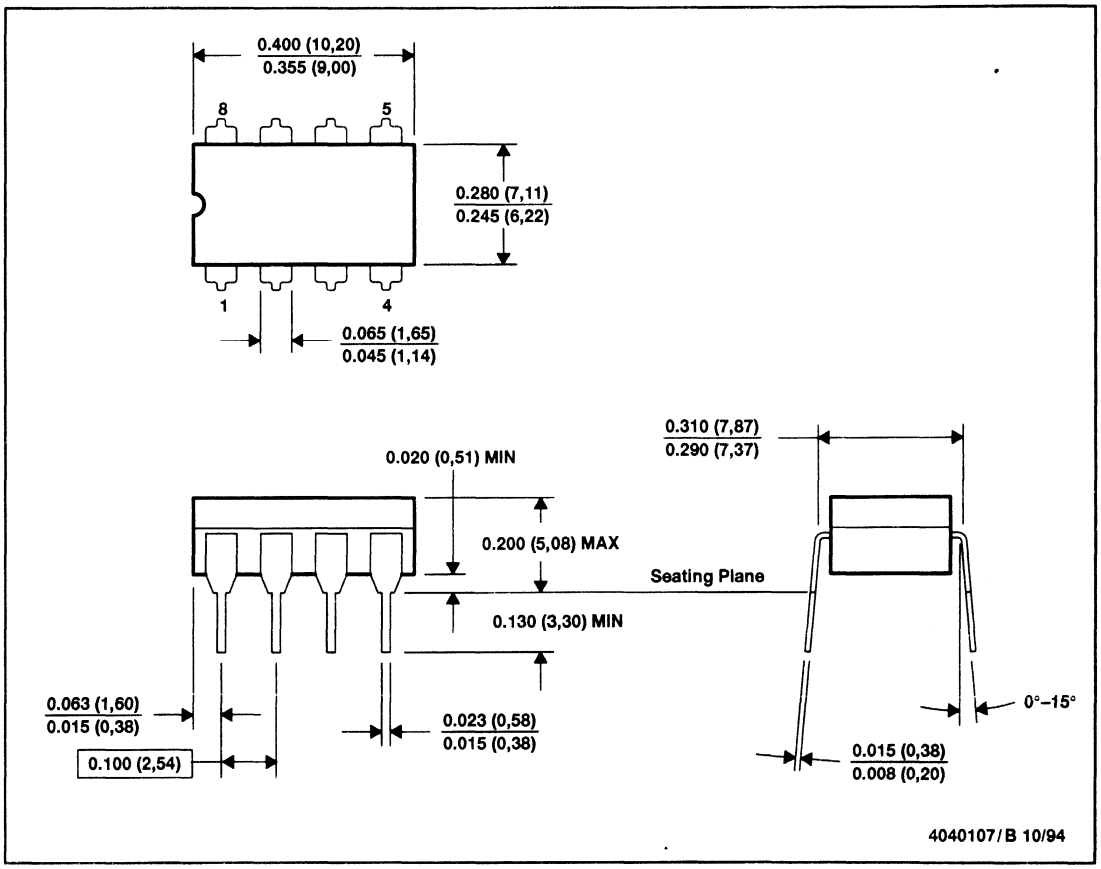
AUGUST 1995

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only
E. Falls within MIL-STD-1835 GDIP1-T8

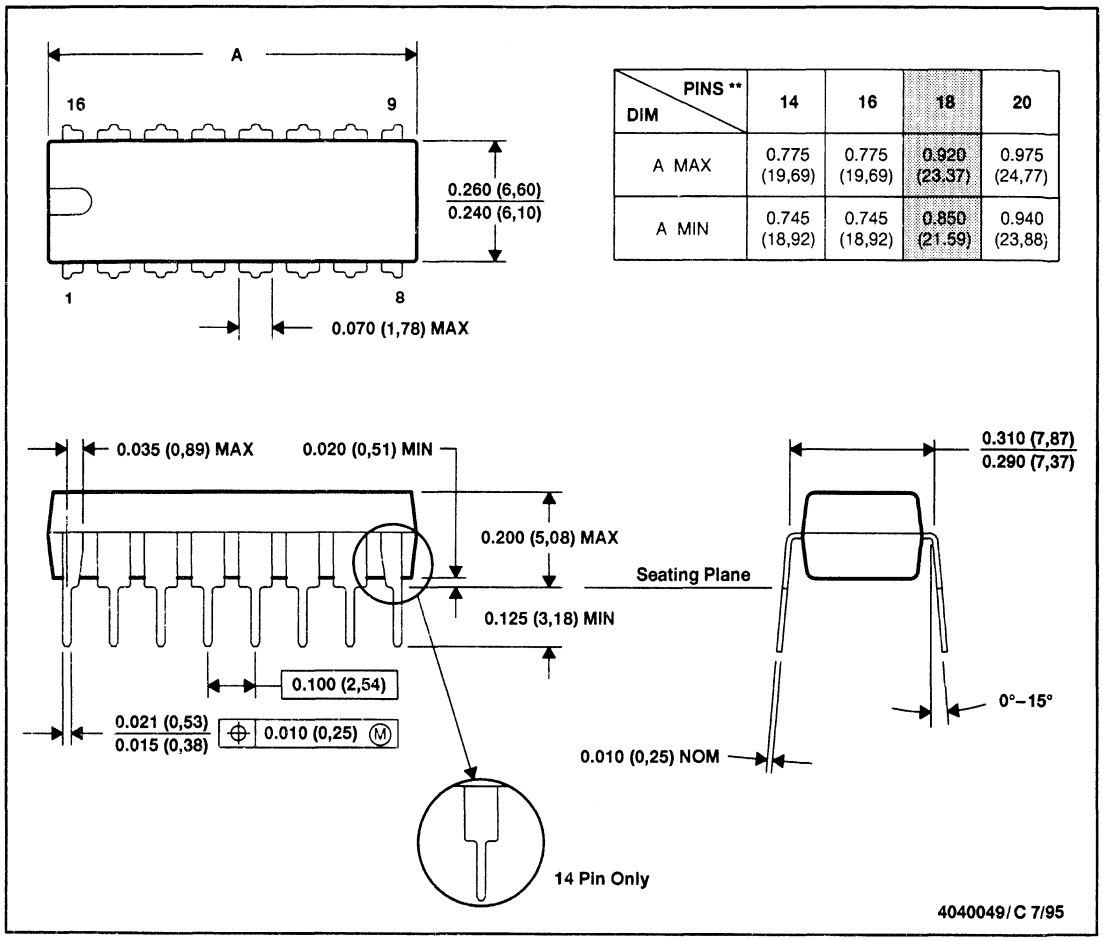
MECHANICAL DATA

AUGUST 1995

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PIN SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23.37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21.59)	0.940 (23,88)

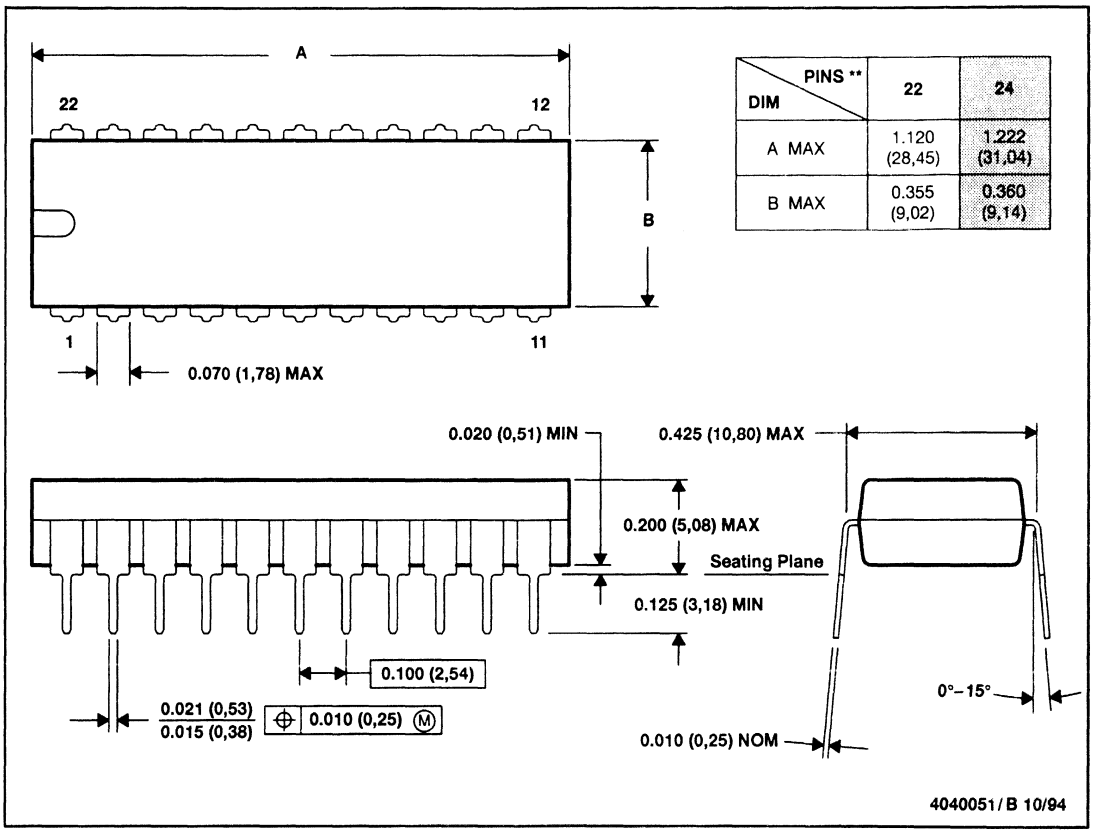
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001)

AUGUST 1995

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

22 PIN SHOWN



DIM \ PINS **	22	24
A MAX	1.120 (28,45)	1.222 (31,04)
B MAX	0.355 (9,02)	0.360 (9,14)

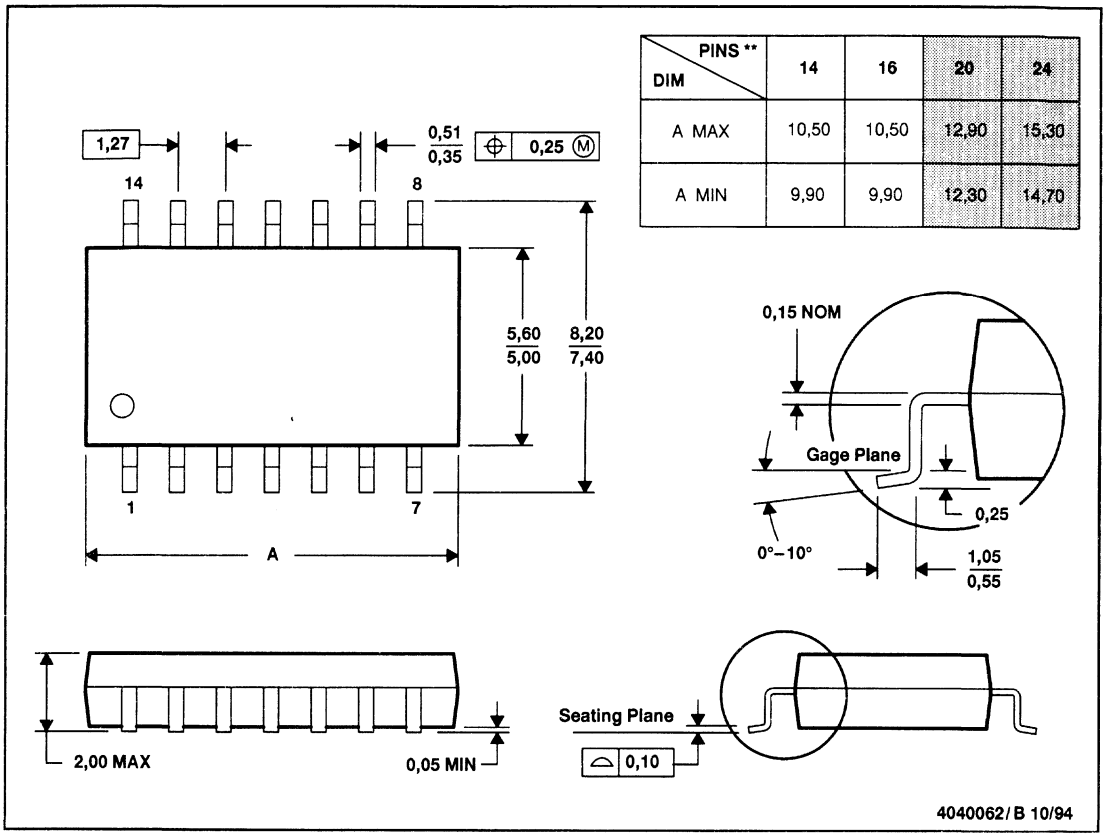
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-010

MECHANICAL DATA

AUGUST 1995

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

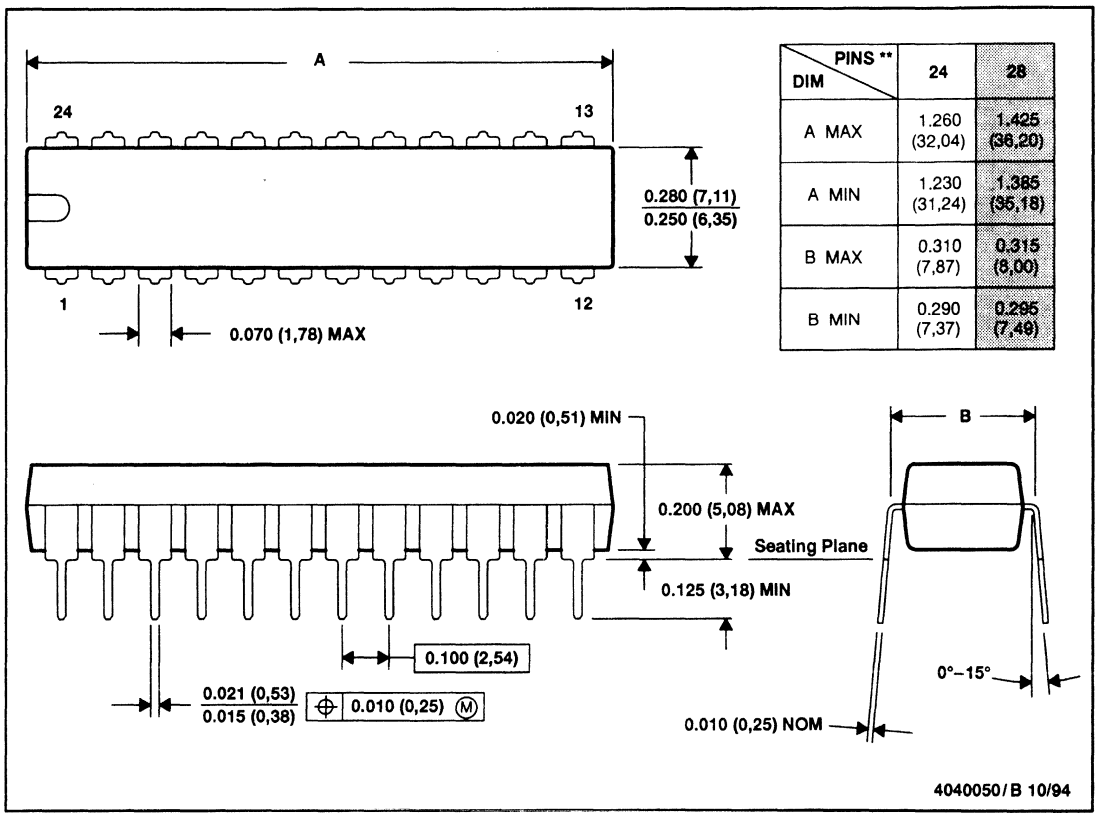
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

AUGUST 1995

NT (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

24 PIN SHOWN



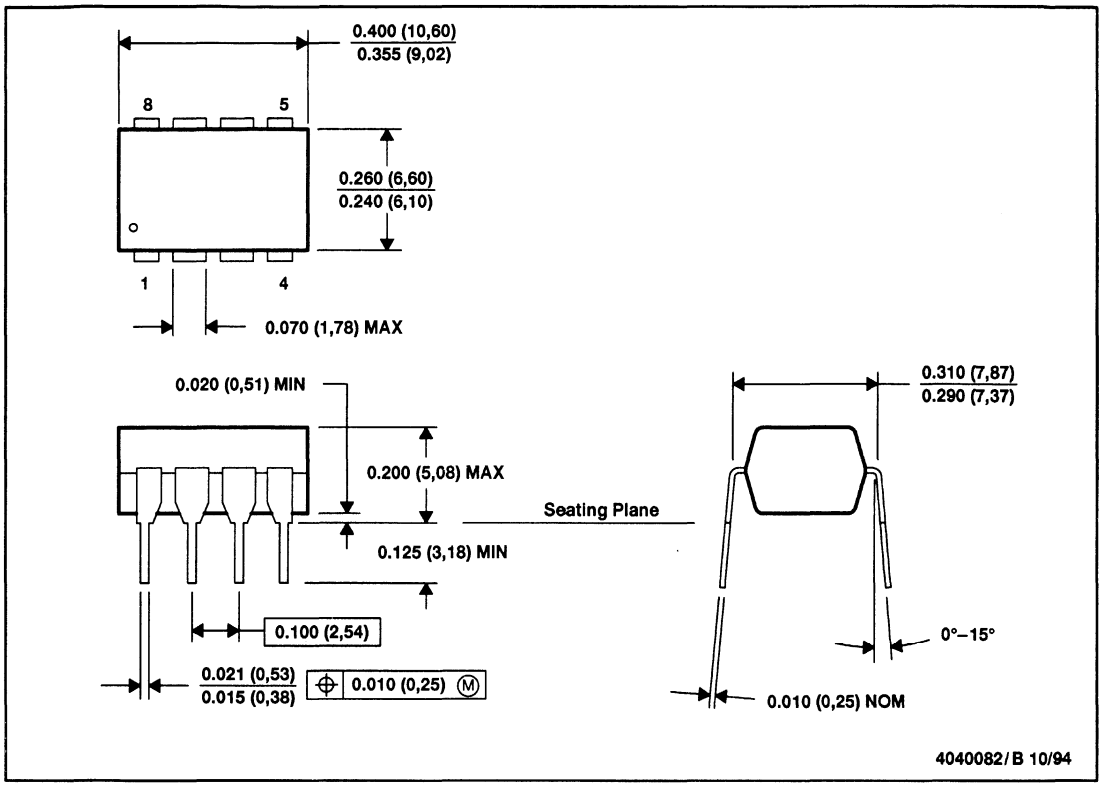
DIM \ PINS **	24	28
A MAX	1.260 (32,04)	1.425 (36,20)
A MIN	1.230 (31,24)	1.385 (35,18)
B MAX	0.310 (7,87)	0.315 (8,00)
B MIN	0.290 (7,37)	0.295 (7,49)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

MECHANICAL DATA

AUGUST 1995

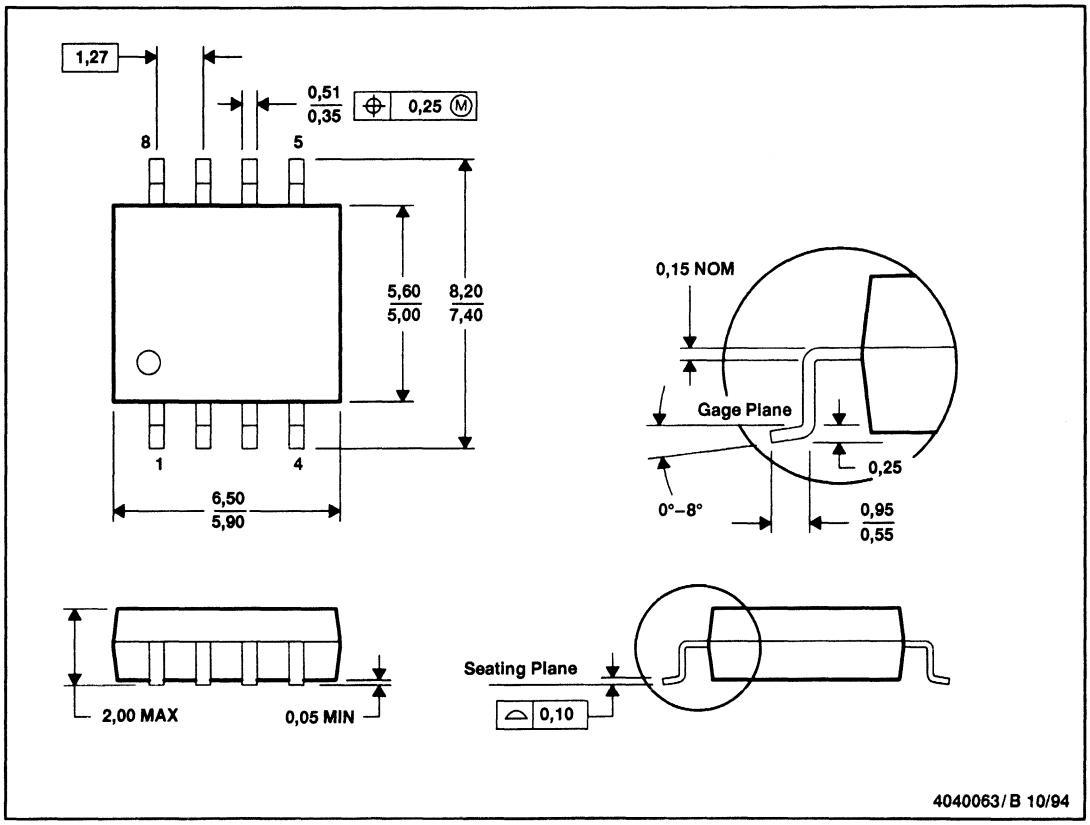
P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

AUGUST 1995

PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**

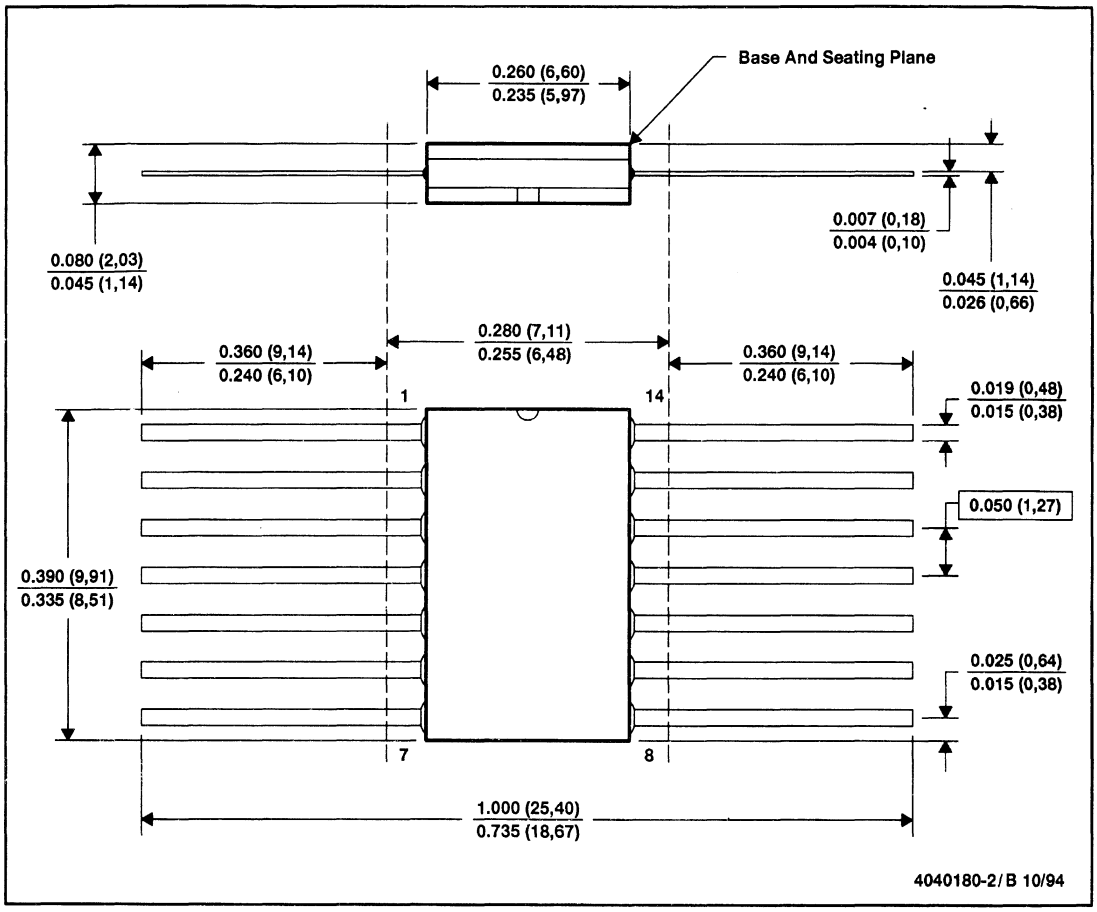


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MECHANICAL DATA

AUGUST 1995

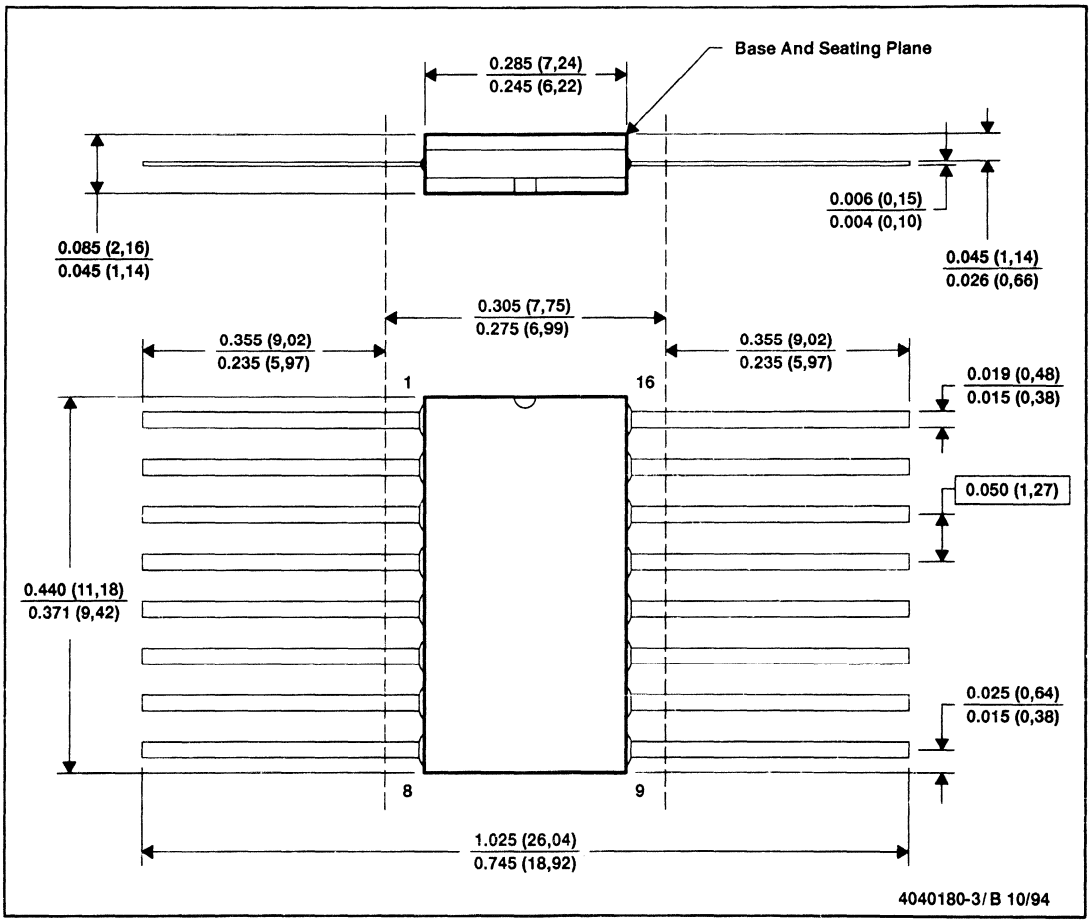
W (R-GDFP-F14) **CERAMIC DUAL FLATPACK**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only
E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

AUGUST 1995

W (R-GDFP-F16) **CERAMIC DUAL FLATPACK**

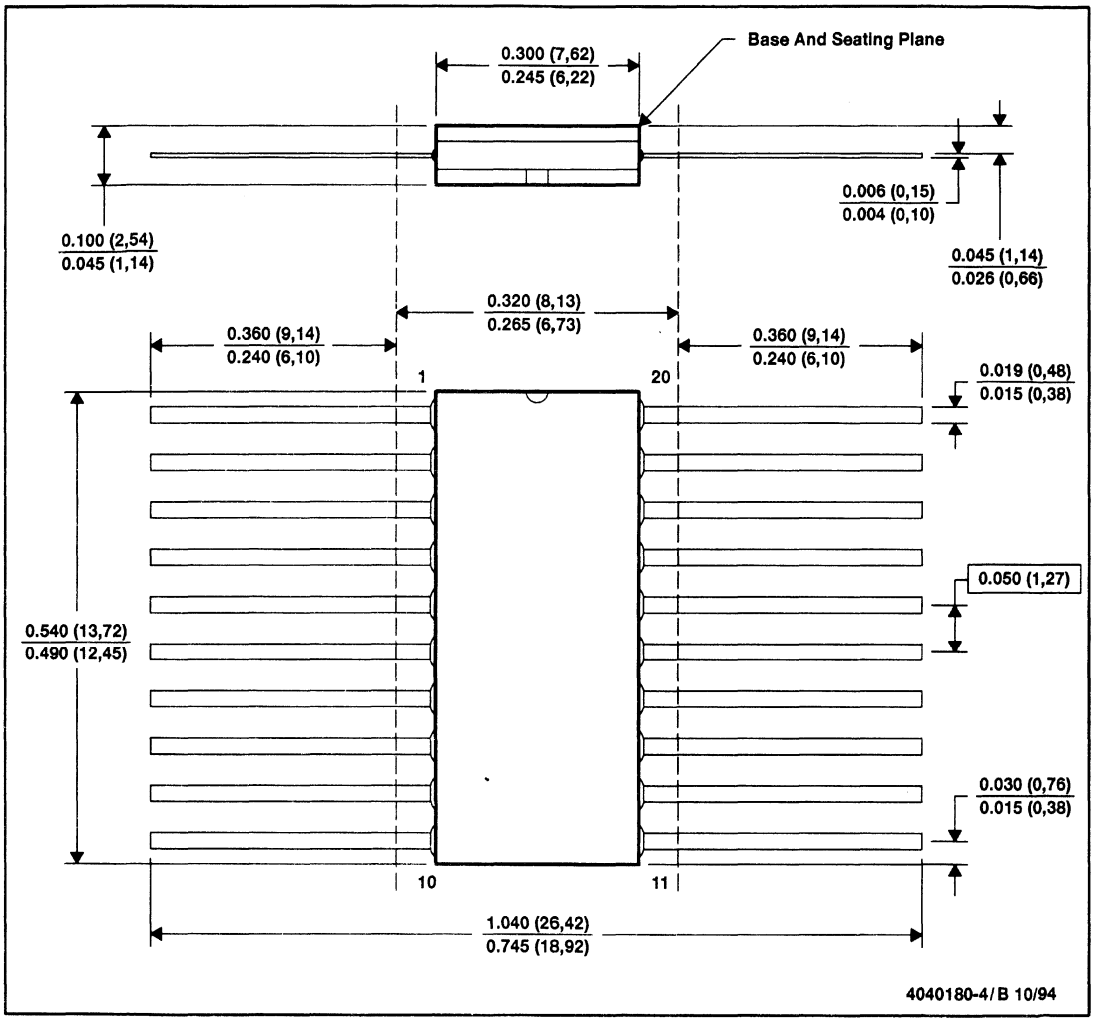


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only
E. Falls within MIL-STD-1835 GDFP1-F16 and JEDEC MO-092AC

MECHANICAL DATA

AUGUST 1995

W (R-GDFP-F20) **CERAMIC DUAL FLATPACK**



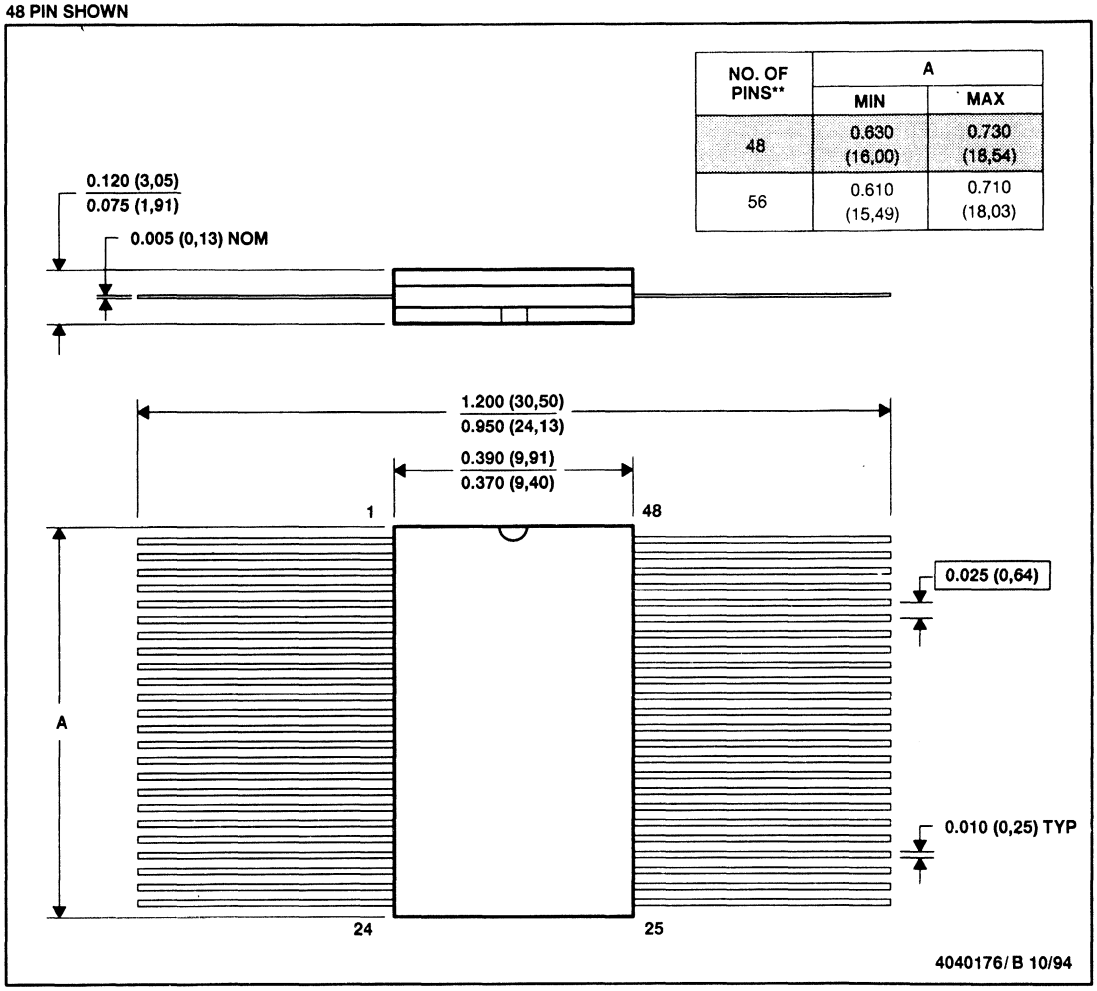
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only
E. Falls within MIL-STD-1835 GDFP2-F20

AUGUST 1995

WD (R-GDFP-F**)

CERAMIC DUAL FLATPACK

48 PIN SHOWN



NO. OF PINS**	A	
	MIN	MAX
48	0.630 (16,00)	0.730 (18,54)
56	0.610 (15,49)	0.710 (18,03)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for pin identification only
E. Falls within MIL-STD-1835: GDFP1-F48 and JEDEC MO-146AA
GDFP1-F56 and JEDEC MO-146AB

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